ISBN : 978-93-85100-14-7

ICTIMES - 2017

Proceedings of

International Conference on Latest Trends in Electronics and Communication (ICLTEC)

Under the Auspices of ***International Conference on trends in Information, Management, Engineering and Sciences (ICTIMES)***

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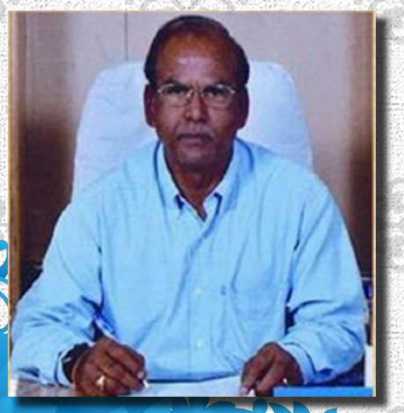

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VIDEO ENHANCEMENT USING CONTRAST LIMITED ADAPTIVE HISTOGRAM EQUALIZATION

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Abstract: With the continuous rise of Internet-based multimedia services, such as video sharing websites, web radios and IP-based telephony, multimedia communications are getting more and more popularity and demand. From the service provider's perspective, there is an increasing need to providing high-quality content; at the same time, from the network provider's view, the requirement is to design networks that can effectively support these services with adequate quality-of-service. Histogram Equalization is a contrast enhancement technique in the image processing which uses the histogram of image. There are several extensions of histogram equalization has been proposed to overcome the brightness preservation. Contrast enhancement using brightness preserving bi-histogram equalization (BBHE) and Dualistic sub image histogram equalization (DSIHE) which divides the image histogram into two parts based on the input mean and median respectively then equalizes each sub histogram independently. Measure video quality by peak signal to noise ratio (PSNR).The purpose of image enhancement is to increase image visibility and details. Enhanced image provide clear image to eyes or assist feature extraction processing in computer vision system.This paper focuses on enhancing the quality of low-grade video of surveillance cameras.

Key Words: Histogram Equalization, Contrast Enhancement , Image, MSE, PSNR

I. INTRODUCTION

Video enhancement is one of the most important and difficult components in video research. The aim of video enhancement is to improve the visual appearance of the video, or to provide a "better"transform representation for future automated video processing, such as analysis, detection, segmentation, recognition, surveillance, traffic, criminal justice systems. In this paper, we present an overview of video enhancement processing and analysis algorithms used in these applications.

Video enhancement problem can be formulated as follows: given an input low quality video and the output high quality video for specific applications. How can we make video more clearer or subjectively better digital video has become an integral part of everyday life. It is well-known that video enhancement as an active topic in computer vision has received much attention in recent years. The aim is to improve the visual appearance of the

video, or to provide a "better"transform representation for future automated video processing, such as analysis, detection, segmentation, and recognition. Moreover, it helps analyses background information that is essential to understand object behavior without requiring expensive human visual inspection [6]. There are numerous applications where digital video is acquired, processed and used, such as surveillance, general identity verification, traffic, criminal justice systems, civilian or military video processing .

II.BRIGHTNESS PRESERVING BI HISTOGRAM EQUALIZATION

The Brightness preserving bi histogram equalization firstly decomposes an input image into two sub images XL and XU based on the mean Xm of the input image. One of the sub image is set of samples less than or equal to the mean whereas the other one is the set of samples greater than the mean. Then the BBHE equalizes the sub images independently based on their respective histograms with the constraint that the samples in the formal set are mapped into the range from the minimum gray level to the input mean and the samples in the latter set are mapped into the range from the mean t the maximum gray level. Means one of the sub images is equalized over the range up to the mean and the other sub image is equalized over the range. From the mean based on the respective histograms .Thus, the resulting equalized sub images are bounded by each other around the input mean, which has an effect of preserving mean brightness.

$$X=X_L U X_U \quad (1)$$

$$\text{Where, } X_L = \{X(i,j) \mid X(i,j) \le X_m \ \forall\ X(i,j) \in X\} \quad (2)$$

$$\text{And } X_U = \{X(i,j) \mid X(i,j) > X_m \ \forall\ X(i,j) \in X\} \quad (3)$$

The histograms created from X_L and X_U are denoted as h_L and h_U respectively

Local maximum values of $h_L(x)$ *and* $h_U(x)$ are found by applying differential operation to $h_L(x)$ *and* $h_U(x)$ as shown in equation (4) and (5);

$$h'_L(x) = h_L(x) - h_L(x-1), \quad \text{for} 1 \le x \le J \quad (4)$$

$$h'_U(x) = h_U(x) - h_U(x-1), \quad \text{for} 1 \le x \le J \quad (5)$$

A sub-congregation *{hL(xi)}* or histogram local maximum values *hL(xi)*, are found by using the equations (6) and (7);

$$|h'_L(x))| < \min\{|h'_L(x-1))|, |h'_L(x+1))|\} \quad (6)$$

$$h'_L(x-1) > 0,\ h'_L(x+1) < 0 \quad (7)$$

Where, $0 \le x \le J$, $1 \le i \le N_{Lmax}$ and N_{Lmax} is the number of local maximum values. Mean $h_{Lk,}$ is derived from sub-congregation $\{ h_L(x_i) | k \le i \le N_{Lmax}\}$.

Then, the evaluated $h_{Lk,}$ is the plateau threshold value(i.e. T_L) for first sub-histogram and same procedure isfollowed for another sub-histogram and finds T_U. Thethreshold values of sub-histograms h_L and h_U are T_L and T_U respectively.

The sub-histograms are modified using threshold operation as shown in equation (8) and (9). The modified histogram $h_{mod}\ (x)$ with the threshold valueis,

$$h_{Lmod}(x) = \begin{cases} h_L(x), & \text{for} h_L(x) \le T_L \\ T_{L,} & \text{otherwise} \end{cases} \quad (8)$$

$$h_{Umod}(x) = \begin{cases} h_U(x), & \text{for} h_U(x) \le T_U \\ T_{U,} & \text{otherwise} \end{cases} \quad (9)$$

Probability Density Functions (PDF's) are found from $h_{Lmod}\ (x)$ *and* $h_{Umod}\ (x)$ and then cumulative density functions (CDF)[9].

III CONTRAST LIMITED ADAPTIVE HISTOGRAM EQUALIZATION (CLAHE)

Adaptive histogram equalization is a computer image processing technique used to improve contrast in images. It differs from ordinary histogram equalization in the respect that the adaptive method computes several histograms, each corresponding to a distinct section of the image, and

uses them to redistribute the lightness values of the image. Ordinary histogram equalization simply uses a single histogram for an entire image.

Consequently, adaptive histogram equalization is considered an image enhancement technique capable of improving an image's local contrast, bringing out more detail in the image.

However, it also can produce significant noise. A generalization of adaptive histogram equalization called contrast limited adaptive histogram equalization, also known as CLAHE, was developed to address the problem of noise amplification. CLAHE operates on small regions in the image, called tiles, rather than the entire image. Each tile's contrast is enhanced, so that the histogram of the output region approximately matches the histogram specified by the 'Distribution' parameter. The neighboring tiles are then combined using bilinear interpolation to eliminate artificially induced boundaries. The contrast, especially in homogeneous areas, can be limited to avoid amplifying any noise that might be present in the image.

Contrast Limited AHE (CLAHE) differs from ordinary adaptive histogram equalization in its contrast limiting. This feature can also be applied to global histogram equalization, giving rise to contrast limited histogram equalization (CLHE), which is rarely used in practice. In the case of CLAHE, the contrast limiting procedure has to be applied for each neighborhood from which a transformation function is derived. CLAHE was developed to prevent the over amplification of noise that adaptive histogram equalization can give rise to.

This is achieved by limiting the contrast enhancement of AHE. The contrast amplification in the vicinity of a given pixel value is given by the slope of the transformation function. This is proportional to the slope of the neighborhood cumulative distribution function (CDF) and therefore to the value of the histogram at that pixel value. CLAHE limits the amplification by clipping the histogram at a predefined value before computing the CDF. This limits the slope of the CDF and therefore of the transformation function. The value at which the histogram is clipped, the so-called clip limit, depends on the normalization of the histogram and thereby on the size of the neighborhood region. Common values limit the resulting amplification to between 3 and 4 times the histogram mean value.

IV. QUALITY ASSESSMENT

It used by many researchers. PSNR is the ratio between the maximum possible power of a signal and the power of corrupting noise that affects the fidelity of its representation. It is defined via the Mean Squared Error (MSE) between an original frame o and the distorted framed as following

$$\text{MSE} = \frac{1}{M.N}\sum_{m=1}^{M}\sum_{n=1}^{N} | o(\text{m},\text{n}) - d(m,n) | \quad (10)$$

Where each frame has M × N pixels, and o(m, n) and d(m, n) are the luminance pixels in position (m, n) in the frame. Then, PSNR is the logarithmic ratio between the maximum value of a signal and the background noise (MSE). If the maximum luminance value in the frame is L (when the pixels are represented using 8 bits per sample, L = 255) then

$$\text{PSNR} = 10 \log \frac{255^2}{MSE} \quad (11)$$

It can be noticed that PSNR can be computed only once the image is reconstructed at the receiver, hence, it may not be appropriate to use in real-time mechanisms. This is one disadvantage of such metric. The other would be the reliability to derive MOS from this metric. However, according to [5] there exist heuristic mappings of PSNR to MOS as shown in Table 1.

Table 1.PSNR and MOS

.

PSNR(dB)	MOS
> 37	5(Excellent)
31-37	4(Good)
25-31	3(Fair)
20-25	2(Poor)
< 20	1(Bad)

V.VIDEO ENCHANCEMENT

Video enhancement problem can be formulated as follows: given an input low quality video and the output high quality video for specific applications. How can we make video more clearer or subjectively better. Digital video has become an integral part of everyday life. It is well-known that video Enhancement as an active topic in computer vision has received much attention in recent years. The aim is to improve the visual appearance of the video, or to provide a "better" transform representation for future automated video processing, such as analysis, detection, segmentation, and recognition. Moreover, it helps analyses background information that is essential to understand object behavior without requiring expensive human visual inspection [6]. There are numerous applications where digital video is acquired, processed and used, such as surveillance, general identity verification, traffic, criminal justice systems, civilian or military video processing .

In this paper, if enhanced video embed high quality background information, the existing techniques of video enhancement can be classified into two broad categories: Self-enhancement and frame-based fusion enhancement. Traditional methods of video enhancement are to enhance the low quality video itself. It doesn't embed any high quality background information. Such as contrast enhancement method, HDR-based video enhancement, compressed-based video enhancement, and wavelet-based transform video enhancement. These approaches are uniformly called self-enhancement of low quality video. It don't enough luminous of low quality video. The reason is that in the dark video, some areas are so dark that all the information is already lost in those regions. No matter how much illumination enhancement you apply, it will not be able to bring back lost information. Frame-based fusion enhancement refers to low quality video, which fuse illumination information in different time video. The approach is that it is by extracting high quality background information to embed low quality video. How would one combine information from two (or more) background images in a meaningful way? How would one pick high-quality background parts while keeping all the low-quality important information. To these problems, the previous researchers have abundant research. Fig.1 shows the more detail categories of video enhancement

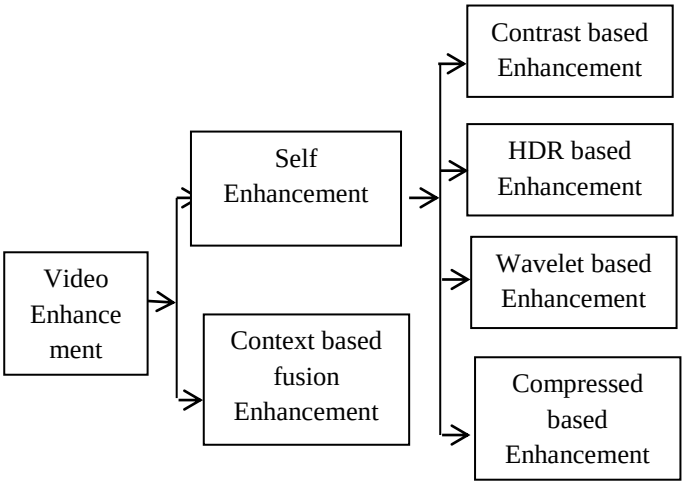

Figure 1: Blok diagram of Video Enhancement

In the frame work show that initially video is first convert into frames and each frame is enhanced by using adaptive histogram equalization process with fusion and red channel processing concept. At the end finally enhanced video we get.

This method is considered a local operator since the operation only affects pixel values in an image individually on a pixel-by-pixel basis and each pixel is mapped in the same way. The global are independent of local spatial context. It performs the same operation on each pixel and don't work well when illumination varies locally. The simplest tone reproduction is a linear mapping which scales

the radiances to the range between 0 and 255. The logarithm of the radiances is taken and linearly scaled to [0, 255].

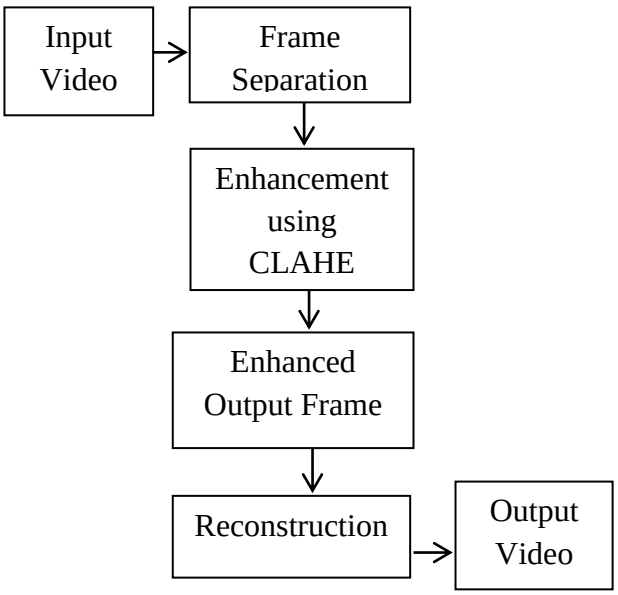

Figure2:Flow diagram of Video Enhancement using CLAHE.

Some regions of a video catch human visual attention at first glance more than other regions, and the regions are considered more salient method.

A Framework Overview

Global contrast enhancement is required to reveal hidden details in dark and bright regions. In addition to enhancing regions with extremely high or low luminance, proposed technique is also significantly stretches the contrast in mid-tone regions, which most other curve-based global .Saliency values can be regarded as complex local information indicating the degree of human interest in each pixel in a video. Saliency maps are most frequently used to extract useful objects in the preprocessing of surveillance systems or recognition problems [10].

VI. EXPERIMENT RESULTS

In this paper we are using MATLAB Software .MATLAB has evolved over a period of years with input from many users. In university environments, it is the standard instructional tool for introductory and advanced courses in mathematics, engineering, and science. In industry, MATLAB is the tool of choice for high-productivity research, development, and analysis.MATLAB features a family of application-specific solutions called toolboxes. Very important to most users of MATLAB, toolboxes allow you to learn and apply specialized technology. Toolboxes are comprehensive collections of MATLAB functions (M-files) that extend the MATLAB environment to solve particular classes of problems. Areas in which toolboxes are available include signal processing, control systems, neural networks, fuzzy logic, wavelets, simulation, and many others.

To enhance the better quality of a video the tone adjustment technique is used here. In addition, noise estimation is taken into account to quantify the artifacts of noise generation during contrast enhancement process. The Video sequence is separated into frames to yield a single high quality image.Fig 3 is shows the paper proposed technique front panel and it implement using MATLAB 7.11 Version its show the GUI of the paper.

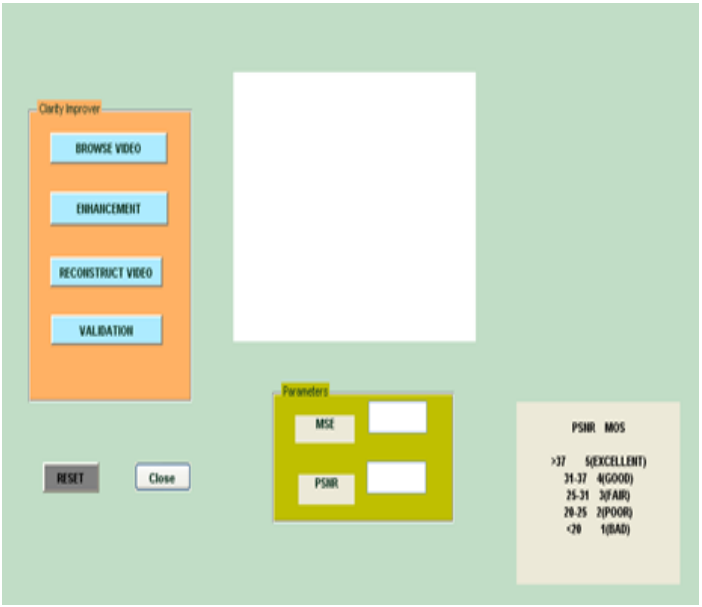

Figure 3:.GUI of Video enhancement Technique

GUI is consists of four Push Bottons they are Browse Video, Enhancement, Reconstruction and Validation.

When Browse Video button is pressed below window display and selected video is played.

Figure4: Video Browse push button window

When Enhancement push button is pressed this below window appears. Enhancement process is started first separating frame and enhancement is done.

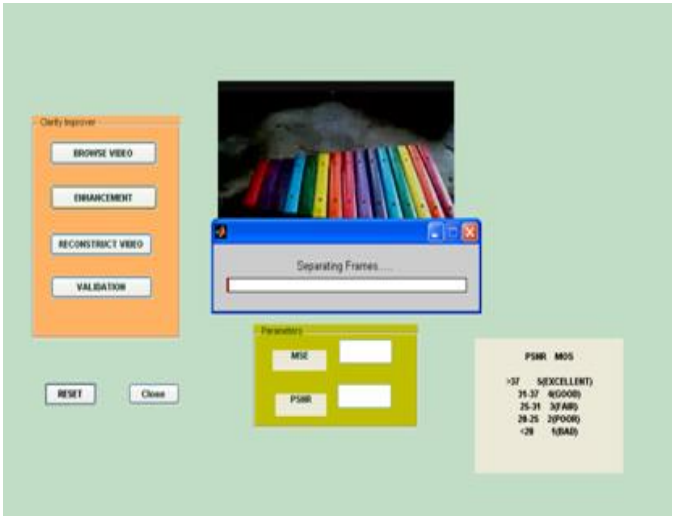

Figure5: separating frames window

After separating enhancement is done my using AHE with fusion and red channel processing

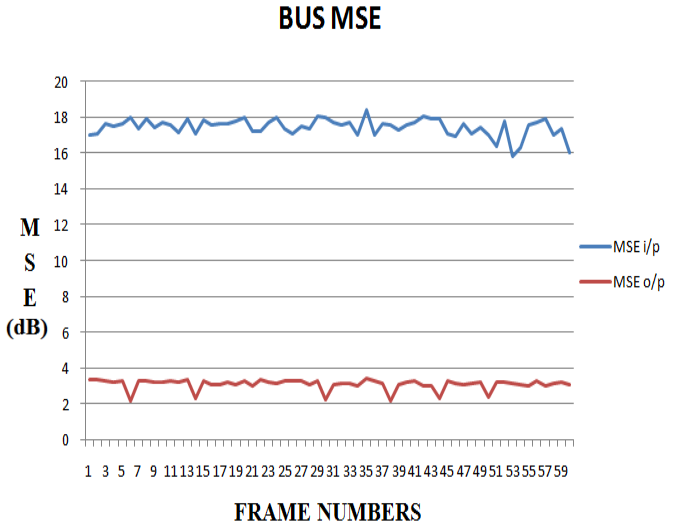

Figure 6:Graph of MSE of BUS video

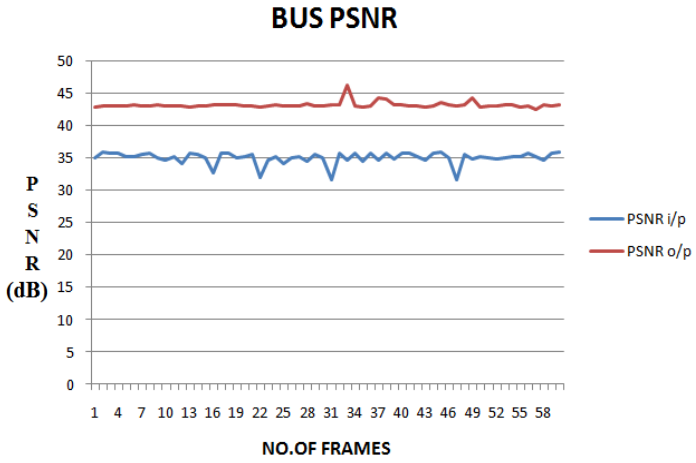

Figure 7:Graph of PSNR of BUS video

Figure 8: enhancing frames window

After enhancing again enhanced video is played so that enhancement can be observed.

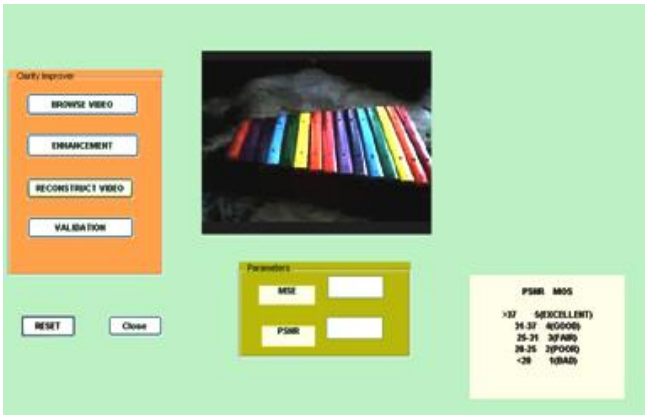

Figure9: Enhanced video is playing window

After enhancing for the purpose of video quality estimation calculating PSNR of video.

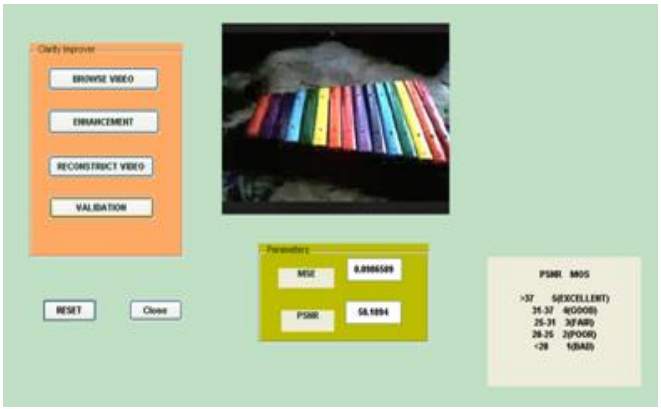

Figure 10: MSE & PSNR calculation window

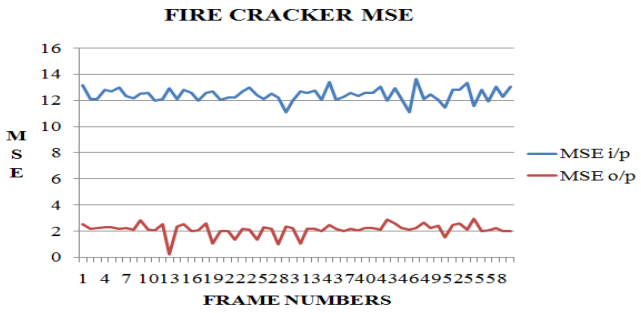

Figure 11: Graphof MSE of FIRE CRAKER video

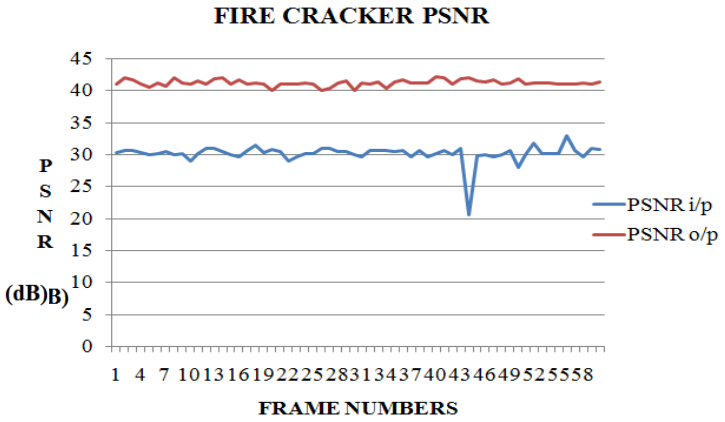

Figure 12:Graph ofPSNR of FIRE CRAKER video

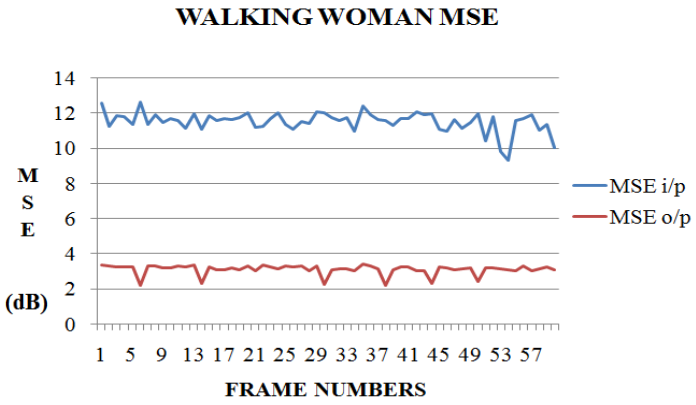

Figure 13:GraphofMSE of WALKING WOMAN video

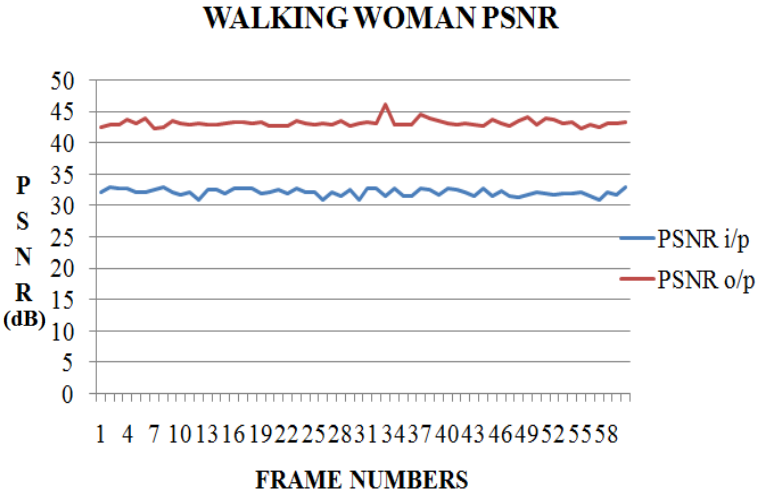

Figure 14: GraphofPSNR of WALKING WOMAN video

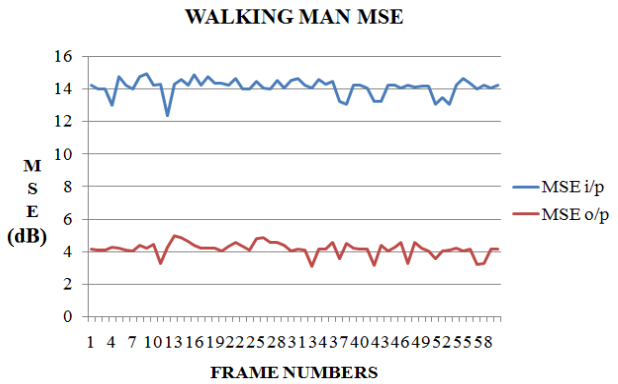

Figure 15:Graph ofMSE of WALKING MAN video

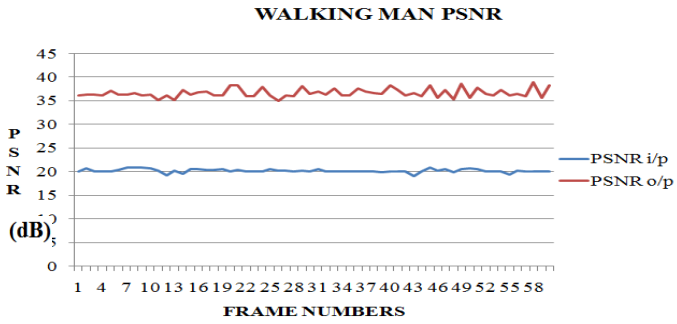

Figure 16:GraphofPSNR of WALKING WOMAN video

VII. CONCLUSION

It is observed from the above table 3 the difference in PSNR for Bus video input and output is 8.12 which is a satisfactory result. MSE difference between input and output is 14.16 which is a satisfactory result. It is observed from the above table3 the difference in PSNR for Fire Cracker video input and output is 11.02dB which is a satisfactory result. MSE difference between input and output is 10.29 which is a satisfactory result. It is observed from the above table3 the difference in PSNR for Walking Woman video input and output is 11.04dB which is a satisfactory result. MSE difference between input and output is 8.54 which is a satisfactory result. It is observed from the above table3 the difference in PSNR for Walking man video input and output is 16.45dB which is a satisfactory result. MSE difference between input and output is 9.98which is a satisfactory result. This proposed video enhancement framework consisting of Contrast Limited Adaptive Histogram Equalization. This work showed that achieves greater performance using luminance component. To evaluate the enhancement performance, the PSNR value was used to measure the quality of enhancement. This technique will also prove that enhancing the quality of low-grade video surveillance cameras.

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Table 2: Average PSNR and MSE values of different types of I/P & O/P videos for 60 frames of each

S. No	Video Name	format	Frame rate (f/sec)	Duration (sec)	I/P Video PSNR(dB)	O/P Video PSNR(dB)	I/P Video MSE	O/P Video MSE
1	Bus	.avi	15	4	35.01	43.13	17.46	3.10
2	Fire cracker	.avi	15	4	30.16	41.18	12.43	2.14
3	Walking woman	.avi	15	4	32.11	43.15	11.52	3.10
4	Walking man	.avi	15	4	20.24	36.69	14.14	4.16

BIOGRAPHY

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Optimized Multi-Wavelet Based Image Compression Model for Medical Applications

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Abstract: **Medical image compression has become more important in the medical field, because many hospitals use compression store for routine tracking and follow-up. No compression occupies a lot of memory by which there is a heavy hardware complexity. In order to achieve a memory constraint problems, this paper proposed a new image compression model based on multiwavelet transform and a hybrid Huffman encoder. The proposed approach accomplishes the multi wavelet transform to obtain finer resolution level by which the redundant information reduces more effectively. Further the proposed model also accomplished a feature selection process based on the spectral properties of image. Then the obtained spectral features are processed for encoding through a hybrid Huffman encoder. Various test samples are used for performance evaluation under various scenarios such as varying noise variance and varying bit rate.**

Keywords: *Medical image compression, Multiwavelet, Power spectral density, Huffman encode, PSNR, CR.*

I. INTRODUCTION

Recently, the compression of medical images has gained a lot of research interest to achieve a reduced storage and bandwidth requirements in systems like PCAs (Picture Archival and Communication Systems) and telecommunications. Medical image processing and compression have become important to medical field. Nowadays, many hospitals around the world use compression to store routinely-made patient images for follow-up and tracking the patient state. Basically image compression techniques can be classified into two categories: lossless and lossy compression techniques. Lossless techniques are applied when data are critical and loss of information is not acceptable. Since the medical imagery carries mot important information, the design of a medical image compression technique should be very careful. Even a less information loss results in a large degradation in the quality of image by which the image directs to a wrong diagnosis. Hence the medical images subjects to lossless compression only. There are various medical image compression techniques. In the area of image coding for medical application [1], multi bit rate [2] applications are emerging. Conventional coding approaches are limited to their application due to network diversity issues. Since the medical images carry most important and huge information, encoding them at very low bit rate will results in the information loss and also gives the low quality medical image reconstruction. If this was viewed through the effect of channel, it will become worse due to the effect of narrow bandwidth. Several approaches are proposed in earlier for encoding the MRI image data before transmission. However, these approaches obtained better results at high bit rates and shown poor results in the case of low bit rates. This problem can be overcome by encoding the Images in such a way that there will be in compatibility for the encoded bits with lower bit rate.

Hierarchical coding is one of the coding techniques which perform image coding in a hierarchical fashion by considering the importance of pixels at every stage. In hierarchical coding, the image is initially processed for decomposition through Discrete Wavelet transform (DWT). DWT decomposes the image into subbands (LL, LH, HL and HH). Then the obtained sub bands are processed for further coding. For the encoding of obtained wavelet bands, various encoding approaches were proposed in past. These coding approaches are lossy or lossless compression approach as per the developed methods. In these approaches more dominantly used approaches are Huffman coding and arithmetic coding approach. As Huffman coding are lower in computational complexity as compared to arithmetic coding mostly Huffman coding are seen in JPEG coding architecture. Huffman coding is entropy based coding technique where the data bits are compressed based on the frequency of occurrence of the unique words. It is often observed that this coding approach allocated higher code bit length than the original code word for lower frequency data bits. This result in decompression and result in higher bit counts. Additionally the decoding states required to decompress the data increases resulting in slower operational speed. To overcome the problems at all phases of image compression system, this work proposed a new image compression system based on spectral characteristics of image. A simple block diagram of the proposed image compression system is shown in figure.1.

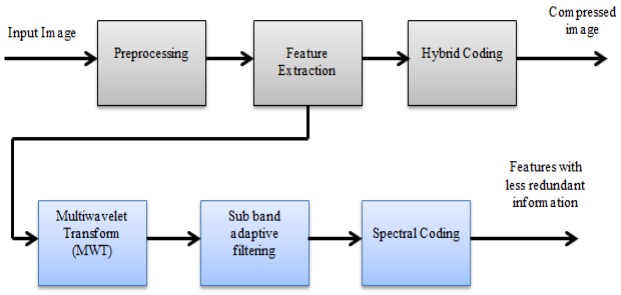


Figure.1 Overall proposed system model

Initially, the image was subjected to multiwavelet transform and then the obtained wavelet bands are subjected to further band coefficient selection process to reduce the additional computational overhead occurred with processing of all wavelet bands. Here the sub band adaptive filtering is accomplished to achieve the bands with less in number. Further the obtained bands are spectral coded based on the correlations between. Then the obtained features are processed for encoding process. To achieve a higher compression and faster decoding time in this work an hybrid coding approach of variable and fixed length coding scheme is to be developed for the improvement of speed and compression ratio for digital image compression.

Rest of the paper is organized as follows: section II illustrates the literature survey. Section III describes the multiwavelet band selection model based on adaptive band filter (ABF). Section IV describes the spectral selective band process. Section V describes the details of proposed hybrid Huffman encoder. Section VI illustrates the experimental results and finally the conclusions are given in section VII.

II. LITERATURE SURVEY

Recently, in the field of medical image compression, the wavelet transform has been developed as a cutting edge technology. Wavelet-based coding [3], [4], [5], [6] methods provide an improved picture quality at high compression ratios. To achieve the better compression performance, the wavelet filters should have the property of symmetry, orthogonality, higher approximation order and short support. Due to the constraints in the implementation, scalar wavelets can't satisfy all these enhanced properties. Compared with scalar wavelets, Multiwavelets [7], [8], [11] have several advantages and are generated by only a finite set of functions. One of the main advantage with multiwavelet, it can possess symmetry and orthogonality simultaneously [9], [10], whereas the scalar DWT can't possess these two properties simultaneously. These two properties of multiwavelet made it to offer the increased performance and also high degree of freedom compared with scalar wavelets, in image processing applications. Zero-tree/block coding [12], [13], [14], [15] clusters the subband/wavelet coefficients by considering their nature of energies both in space and frequency. These coders apply the hierarchical set partitioning method with respect to a threshold to split the significant coefficients in the bit plane coding pass, while preserving the insignificant coefficients. This procedure creates a symbol by coding large region of zero pixels. This method provides an effective method to represent a group of zeros of subband/wavelet coefficients compactly. The high efficiency in the compression can be achieved through the context modeling [16], [17], [18]. In this type of coders, an arithmetic coding based on the context was applied on the individual pixel of DWT bit planes. In the context modeling, the strong correlations between the coefficients of same band and also with the other bands are utilized effectively for encoding. Though, there is simplicity in the context modeling [13], [14], [15] the limited context information is insufficient to predict the current node's status. Some carefully designed context modeling algorithms [17], [18] outperformed the zero-tree/block coders in performance with respect to PSNR. However, the computational complexity is observed to be very high, because, there is a need to scan the entire subbnads at least once to complete the encoding of full bitplane.

III. BAND SELECTIVE-MULTI WAVELET TECHNIQUE

Here the selective multi-multiwavelet coding is applied over the image to obtain the bands which are more informative instead of all bands. Generally as the band decomposition increases, the probability of redundancy among different bands increases. This redundancy of information increases the processing overhead, and intern makes the system slower. Hence it is required to have an adaptive band selection process for extracting the actual informative band from the processed bands. With reference to band selection process proposed in [19], in this work the process of adaptive band selection is developed for multi wavelet coefficients.

In this process the analysis bank decomposes the image I into K subbands, each produced by a branch $H_z(k)$ of the analysis bank. After decimation and expansion by a factor N, the full band signal is reconstructed from the subbands in the synthesis bank by filtering with filters $G_k(z)$ followed by summation. The analysis filters $H_k(n)$ are derived from the real value of a lowpass FIR filter p[n] of even length L_p. For the estimation of signal using such filtration cost optimization approach is used where the subband are processed adaptively termed as subband adaptive filter (SAF) [19].The SAF operation is based on the LMS-type adaptive filter. The convergence of such filter is based on the optimization of this LMS function, wherein weight functions are used to optimize the mean error. To converge the cost function faster in [20] a Normalized SAF (NSAF) is proposed. In [20], the convergence speed is increased by increasing the number of subband filters while maintaining the same level of steady-state error. However, it suffers from huge complexity when used in adapting an extremely long unknown system. To overcome this problem in [21] a dynamic selection based NSAF (DS-NSAF) scheme is proposed. This approach sorts out a subset of the subband filters contributing to convergence performance and utilizes those in updating the adaptive filter weight. This approach dynamically selects the subband filters so as to fulfill the largest decrease of the successive mean square deviations (MSDs) at every iteration. This approach reduces the computational complexity of the conventional SAF with critical sampling while maintaining its selection performance. The operational approach for the conventional DS-SAF approach [20] is as outlined.

In a SAF system the desired band d(n) that originates from an its lowering band is defined by,

$$d(n) = u(n)W^o + v(n) \quad (1)$$

where $w^0$is an unknown column vector to be identified with an adaptive filter, *v(i)* corresponds to a variance σ_v^2 for each band, and *u(n)* denotes a row input vector with length M defined as;

$$u(n) = [u(n)\ u(n-1)\ \ldots\ u(n-M+1)] \quad (2)$$

In the process of adaptive selection, the Normalized SAF (NSAF) [21] approach was proposed. A basic architecture for such coding is as shown in figure 2.

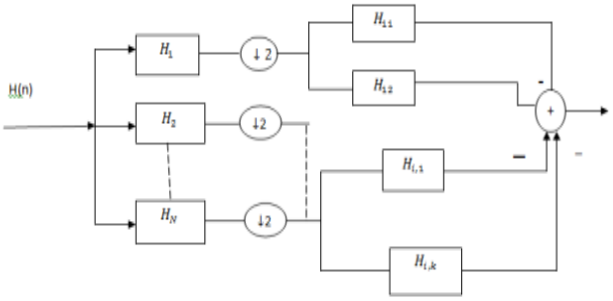


Figure 2. NSAF filter architecture [20]

In this approach the image sample is partitioned into N subbands by the analysis filters $H_0(z)$, … $H_{n-1}(z)$. The resulting subband signals are then critically decimated to a lower sampling rate relative to their demanded bandwidth. The original signal d(n) is decimated to k signals and the decimated filter output at each subband is defined as;

$y_{i,D}(k) = u_i(k)w(k)$, (3)

Where, $u_i(k)$ is a 1 x M row such that,

$u_i(k) = [u_i(kN), u_i(kN-1), \ldots\ldots, u_i(kN-M+1)]$ and

$w(k) = [w_0(k),\ w_1(k), \ldots\ldots, w_{M-1}(k)]^T$ denotes the estimated weight value and the decimated band error is then defined by,

$e_{i,D}(k) = d_{i,D}(k) - y_{i,D}(k) = d_{i,D}(k) - u_i(k)w(k)$ (4)

Where $d_{i,D}(k) = d_i(kN)$ is the reference information at each band. In the process of NSAF the weight optimization is defined as,

$$w(k+1) = w(k) + \mu \sum_{i=0}^{N-1} \frac{u_i^T(k)}{\|u_i(k)\|^2} e_{i,D}(k) \quad (5)$$

Where μ is the step size.

This weight is used to optimize the band selection process where in it takes a large computation to converge for the optimization. To overcome this issue in [20] a MSD based weight optimization is proposed. In this DS-NSAF approach the largest decrease of the MSDs between successive iterations is used.

Hence the weight error vector is then defined as, $\tilde{w}(k) = w^o - w(k)$. The weight optimization is then defined as,

$$\tilde{w}(k+1) = \tilde{w}(k) - \mu \sum_{i=0}^{N-1} \frac{u_i^T(k)}{\|u_i(k)\|^2} e_{i,D}(k) \quad (6)$$

Using this weight vector and taking the expectation a MSD is computed which satisfies the absolute expectation as,

$$E\|\tilde{w}(k+1)\|^2 = E\|\tilde{w}(k)\|^2 + \mu^2 E\left[\sum_{i=0}^{N-1} \frac{e_{i,d}^2(k)}{\|u_i(k)\|^2}\right] - 2\mu E\left[\sum_{i=0}^{N-1} \frac{u_i(k)\tilde{w}(k)e_{i,D}(k)}{\|u_i(k)\|^2}\right] \quad (7)$$

$$\triangleq E\|\tilde{w}(k)\|^2$$

Where

$$\Delta = \mu \sum_{i=0}^{N-1} \left(2E\left[\frac{u_i(k)\tilde{w}(k)e_{i,D}(k)}{\|u_i(k)\|^2}\right] - \mu E\left[\frac{e_{i,d}^2(k)}{\|u_i(k)\|^2}\right]\right) \quad (8)$$

Defines the difference of MSDs between two successive bands. With bands having minimum MSD is then chosen to have a selective band for processing rather to all decomposed bands. This band selection process reduces the processing coefficient with minimum deviation due to the selecting criterion of minimum MSD value.

IV. SPECTRAL FEATURES SELECTION

The compression is to be applied on the regions wherein the image is not affected for its visual quality. To achieve a better embedding operation in this work we have applied directional filters which predict the variations in every direction, i.e. the direction in which the coefficient are least variant, is selected for embedding. The region of such distribution is best suitable for embedding as the energy distribution in such region is very low in a particular direction. Hence directional filters based embedding is best suited for compression in spectral domain. To achieve the objective in this work, a spectral selection approach for coefficient selection is developed based on the power spectral density (PSD).

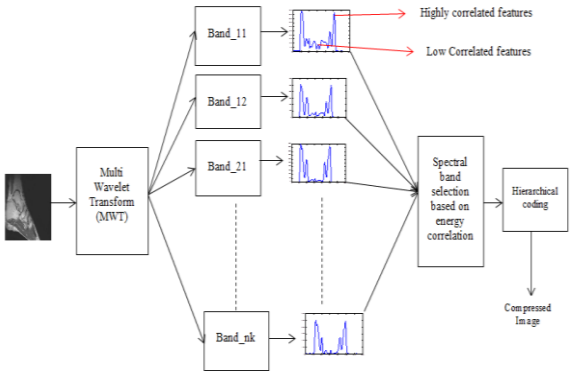


Fig.3 Spectral Feature Selection from the selected bands

For the selection of the selective coefficient of the selected spectrum, a coefficient selection algorithm is proposed. The developed approach is termed as "Spectral selective coding" (SSC). The process of selective coding is as outlined; For the selected Normalized band 'BN_i' obtained from the decomposition approach, a decision of coefficient selection is made based on spectral magnitude. This approach of coefficient selection, results in selection of coefficients, at lower frequency level without effecting higher resolutions coefficients. To compute the spectral magnitude of the band coefficient a power spectral densities (PSD) is computed. PSD is defined as a density operator which defines the variation of power over different content frequencies, in a given signal x(t).

The Power spectral density (PSD) for the given matrix 'x' varying with 't' is defined as,

$$P = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} B(t)^2\ dt \quad (9)$$

Where $B(t)$is the band obtained through the multiwavelet decomposition and P is the power spectral density over a time period t. Taking the selected band 'B_{Ni}' as reference, a PSD for each coefficient, 'PB_i' is computed. The PSD coefficients for the normalized band matrix of dimension m x n is defined by,

$PB_{i,j} = PSD\ (B_{Ni,j})$, for i = 1 to m and j = 1 to n (10)

The PSD per coefficient is defined as,

$$PB_{i,j} = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} B_{Ni,j}(t)^2 \, dt \quad (11)$$

Where, i,j are the corresponding row and column, which are read over a time period of 't'. 't' is the time taken to read the whole set of 'B_{Ni}' matrix.

For the obtained power spectral densities of all bands, a correlation factor is measured successively. The correlation is measured for all bands with respect to all bands. i.e., intra bands and inter bands (multi wavelet bands from LL band and the remaining LH, HL and HH bands). The sub bands which having less correlation is selected for further encoding. The bands which have minimum correlation can reduce the redundant information more precisely and also ensures less computational complexity.

V. ENTROPY DRIVEN BIT CODING

Two statistical methods of data compression namely Huffman and Hybrid Huffman coding are used here for the compression/ Decompression of medical image. Further analyses on the two methods are carried out with reference to the speed of encoding and decoding, the memory used for the storage of these test sets. The system consists of an encoder block and a decoder block for the compression and decompression of the image considered. Further encoding is processed over the selected features as discussed in section IV. Initially they are transformed into binary format. Ten they are processed for the encoding through the proposed entropy driven coding.

There is a tradeoff in selecting the code between the amount of compression that is achieved and the complexity of the decoder. Moreover, if the clock frequency of the tester is f_T and the clock frequency of the scan chain is f_{sys} (system clock frequency) then the ratio of the system clock frequency and the tester clock frequency $f_{sys}=f_T$ limits the minimum size of a codeword. The compression/decompression scheme described in this paper is based on hybrid Huffman coding. In statistical coding, variable length code words are used to represent fixed-length blocks of bits in a data set. The most popular Huffman code gives the optimum compression for a test set divided into a particular fixed-length block size, it generally requires a very large decoder. A Huffman code for a fixed-length block size of b bits requires a finite state machine (FSM) decoder with 2_{b-1} states. Thus, the size of the decoder for a Huffman code grows exponentially as the block size is increased.

During the time that the contents of the serializer are being shifted into the scan chain, the tester is shifting bits into the decoder. When the decoder receives a complete codeword, it needs to output the corresponding block of b bits into the serializer. If the codeword is too short, then the serializer may not have been emptied yet which would cause a problem for the decoder. So, in order to ensure that the serializer is always empty when the decoder finishes decoding a codeword, the minimum size of a codeword L_{min} must be no smaller than the ratio of the tester and scan-clock rates times the size of each block,

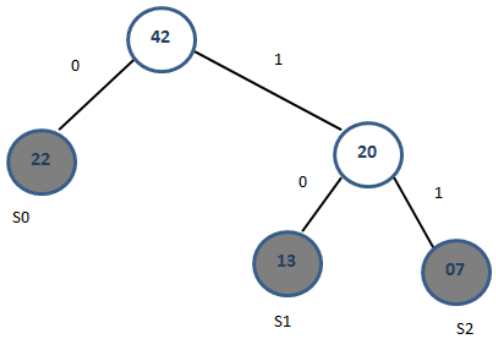


Fig.4 Huffman tree for the three highest frequency symbols

$$L_{min} \geq b \, \frac{f_r}{f_{sys}} \quad (12)$$

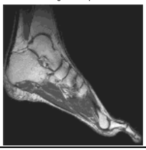
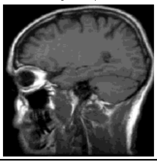
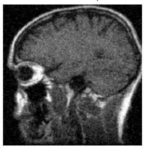
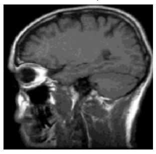
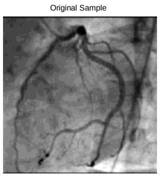
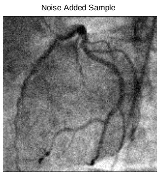
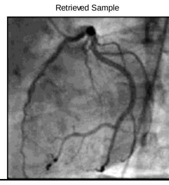
For example, if the block size is 8 and the scan-clock rate is twice the tester clock rate, then the minimum size of a code word is 4. Note that if it is not possible to have the scan clock rate be faster, then the tester clock rate, then an alternative solution (as previously described) is to make the scan clock rate be twice as fast as the "effective clock rate" as seen by the decoder by simply having the tester channel feed two scan chains so that the rate that the decoder receives data from the tester is half as fast as the rate at which data can be shifted into the scan chain. Using a Huffman code would provide the maximum compression; however, it would require a complex decoder and may not satisfy the constraint on the minimum size of a codeword. Therefore, some alternative statistical code must be selected. The approach taken here involves using a selective coding approach for which a very simple decoder can be constructed. Consider the case where the test set is divided into fixed-length blocks of b bits. There will be 2^b Code words. The first bit of each codeword will be used to indicate whether the following bits are coded or not. If the first bit of the codeword is a 0, then the next b bits are not coded and can simply be passed through the decoder as is (hence, the complete codeword has b + 1 bits).

VI. SIMULATION RESULTS

The performance evaluation of proposed compression model is described in this section. Various types of medical images like MRI, CT, X-RAY are taken as test samples. For every case of test sample, the proposed model accomplishes compression and decompression and the performance was evaluated through some performance metrics such as Peak Signal to Noise Ratio (PSNR), Mean Square Error (MSE), Computation Time (CT), Processing Overhead and the Compression Rate (CR). The test Sample considered for simulation are represented in figure.5. Matlab software was used to implement the proposed compression model. The obtained results under Gaussian noise variance of 0.01 are shown in the following table.

Figure.5 test samples

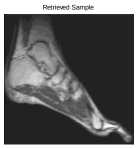
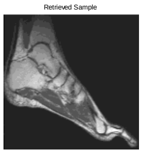
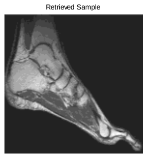
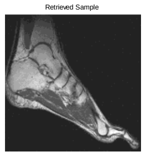
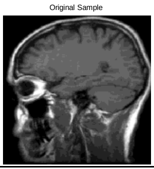
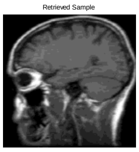
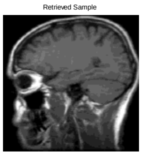
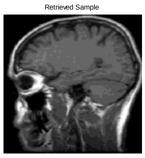
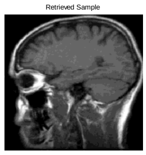
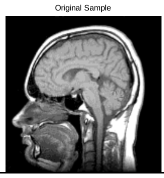
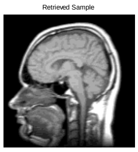
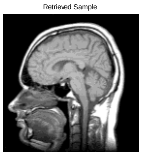
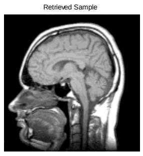
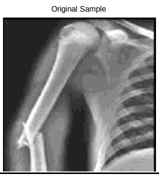
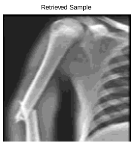
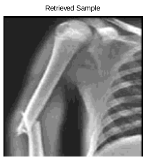
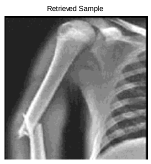
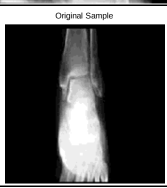
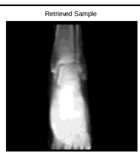
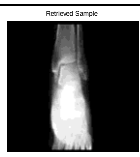
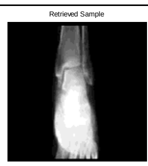
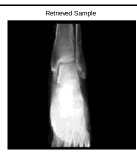
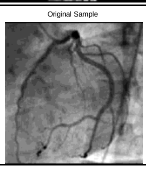
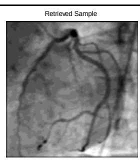
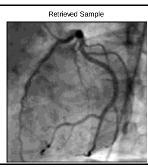
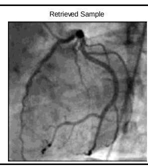
Table.1 Observed results for the test samples under noise variance

Original sample	Noise Added Sample	Retrieved Sample
Original Sample 	Noise Added Sample 	Retrieved Sample 
Original Sample 	Noise Added Sample 	Retrieved Sample 
Original Sample 	Noise Added Sample 	Retrieved Sample 
Original Sample 	Noise Added Sample 	Retrieved Sample 
Original Sample 	Noise Added Sample 	Retrieved Sample 
Original Sample 	Noise Added Sample 	Retrieved Sample 
Original Sample 	Noise Added Sample 	Retrieved Sample 
Original Sample 	Noise Added Sample 	Retrieved Sample 

The compression performance also depends on the bit rate, i.e bit per pixels. As the bit per pixels increases, the quality of image retrieved at decoder increases. Thus the proposed approach

with higher bit rate has better performance. However as the bit rate increases, the computational time increases. The obtained results under various bit rates are shown in table.2, below.

Table.2 Observed results for test sample under Various Bit rates

Original sample	Retrieved Sample at			
	BPP=0.2	BPP=0.4	BPP=0.6	BPP=0.8
				
				
				
				
				
				
				
				

To evaluate the quality assessment for the processed data the quality metric of peak signal to noise ratio (PSNR), mean square error (MSE) and spatial similarity index measure (SSIM) is used, tested over different noise density and coding factor. PSNR is most commonly used as a measure of quality of image test sample .Peak signal-to-noise ratio is defined as a ratio between the maximum possible power of a signal and the power of corrupting noise that affects the fidelity of its representation. PSNR is usually expressed in terms of the logarithmic decibel scale.

$$PSNR(dB) = 10log_{10}\left(\frac{I_{peak}^2}{MSE}\right) \quad (13)$$

Where I_{peak} is the peak values of the input video. Peak signal to noise ratio is used to evaluate the quality of data after retrieval process. The Mean squared error (MSE) of an estimator is one of the way to quantify the amount by which an estimator differs from the true value of the quantity being estimated. As a loss function, MSE is called squared error loss. MSE measures the average of the square of the error. The error is the amount by which the estimator differs from the quantity to be estimated defined by,

$$MSE = \frac{1}{MXN}\sum(f - \hat{f})^2 \quad (14)$$

Where f is the original image and $\hat{f}$ is the retrieved image. The SSIM, similarity factor establishes the similarity of pixel intensities between the ground truth test sample and the decoded data, given as,

Along with these metrics the performance of Proposed compression model is measured through some more performance evaluation parameters such Compression Rate (CR), Encoding Time (ET), Decoding Time (DT) and Total Time (TT). The obtained performance metrics under different cases of noise variances are shown in the table.3.

Table.3 Performance Metrics under various noise variances

Sample	Noise variance = 0.01					Noise variance = 0.03				
	CR	ET	DT	TT	PSNR	CR	ET	DT	TT	PSNR
S1	2.8854	6.8845	2.5466	9.4391	56.2341	2.5471	6.7412	2.4485	9.1897	54.1432
S2	2.7451	6.2358	2.8563	9.0921	57.2145	2.3369	6.3325	2.6685	9.0011	55.5421
S3	2.3678	7.1258	3.4178	10.2736	58.1234	2.1242	7.0028	3.1472	10.1523	56.4235
S4	3.2214	7.2235	3.3387	10.5622	56.0014	2.9987	7.1247	3.2014	10.3261	53.3385
S5	2.9965	6.3385	2.8741	9.2126	58.8742	2.5574	6.2358	2.5813	8.8171	56.8752
S6	3.0028	6.8564	2.5671	9.4235	57.0067	2.8541	6.8654	2.4478	9.3132	55.3145
S7	2.8512	5.3874	2.0035	7.3909	55.8954	2.6635	5.7438	2.1038	7.8476	53.6632
S8	3.1458	6.2285	2.8562	9.0847	56.3217	3.0008	6.2547	2.7968	9.0515	52.8547

Table.4 Performance Metrics under various Bit Rates (Bit Per Pixels (BPP))

Sample	BPP = 0.2					BPP = 0.5				
	CR	ET	DT	TT	PSNR	CR	ET	DT	TT	PSNR
S1	3.2254	6.3312	3.0245	9.3557	58.2278	3.5568	6.7845	3.2254	10.009	59.3314
S2	3.4578	6.8745	3.1247	9.9992	59.6978	3.8741	6.9986	3.3369	10.335	59.8975
S3	3.2689	6.3598	3.6985	10.058	58.4478	3.5328	6.6632	3.8654	10.528	59.1278
S4	3.4589	7.0021	3.2457	10.247	57.4586	3.8657	7.3247	3.4475	10.772	58.9687
S5	3.0058	6.4589	3.8852	10.344	56.3242	3.4412	6.5879	3.9687	10.556	58.2201
S6	3.2568	7.2231	3.4752	10.698	56.3324	3.4568	7.3320	3.7542	11.086	58.1453
S7	3.7742	5.9986	3.5471	9.5457	58.2475	3.9964	6.3254	3.7145	10.039	59.2274
S8	3.6539	5.9863	3.1287	9.1152	57.3328	3.7249	6.2289	3.2278	9.9538	59.0028

Table.5 comparitive analysis between the proposed and standard JPEG compression

Metric	S1		S2		S3		S4	
	JPEG	Proposed	JPEG	Proposed	JPEG	Proposed	JPEG	Proposed
CR	2.0156	2.9956	1.2031	1.9985	1.6719	2.5685	2.3358	3.0417
ET	5.2188	6.3245	4.6406	6.4523	5.2520	6.8885	6.8957	7.1458
DT	9.4063	4.2250	7.2188	4.8795	9.7656	7.2147	9.8886	4.8874
TT	14.625	10.5465	11.8594	11.3498	15.0153	14.1302	16.7843	12.0332
PSNR	39.8869	45.8635	42.5901	48.5278	39.5556	44.7898	39.7456	46.3289

From the table.5, it can be observed that the all performance metrics for the proposed copression model is optimal compared with standard JPEG, expect encoding time. since the proposed approach accomplishes the multiwavelet transform for featureextraction, the time talen for encoding is high. The proposed approach is based on the multiwavelet transform wheres as the JPEG is based on the Discrete wavelet transform. The proposed approach selects the bands followed by feature form the selected bands in an iteratiuve fashion. This phase consumes more time. thus the encoding time for the proposed approahc is obsreved as high compared to JPEG. Except encoding the remaining paramatere such as compression ratio, docidn gtime, total time and PSNR of proposed approach is observed as optimal compared with JPEG. The repestive compraision plots for compression ratio, total time and PSNR are represneted in figure.6, figure.7 and figure.8 respectively.

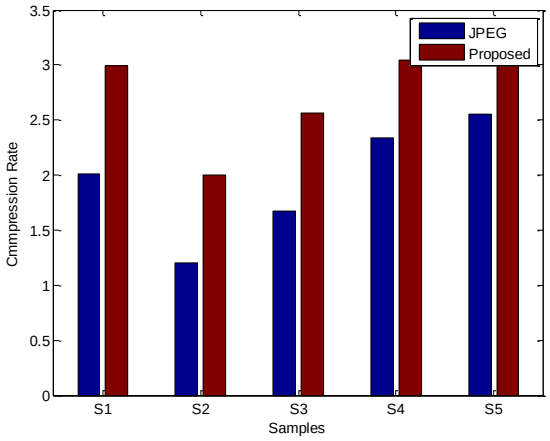


Figure.6 Compression rate comparision

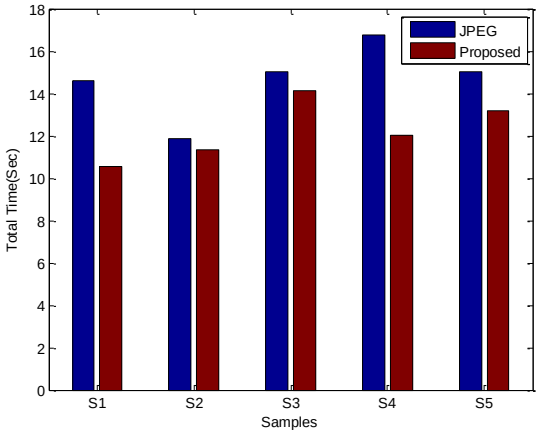


Figure.7 Total time taken in seconds comparision

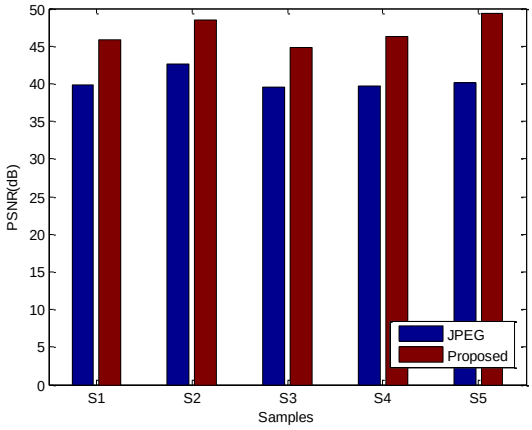


Figure.8 PSNR comparision

From the above figures, it can be observed that the proposed approach has high compression ratio, lower total time an dhigher PSNR. It can also be observed that the proposed approach works effectively even under noise contamination. Thus the proposed compression model achives an optimal performance for medical image compression.

VII. CONCLUSION

This paper proposed a new image comprssion model based multiwavelt transform and the hybrid huffmal coder. The multiwavelet transform helps in searching the more and more finer resolution levels in which the image wont be effected during the compression. For the obtaine multiwavelet bands, a feature selection process is applied to further reduce the redundant information based on the spectral properties. Further the obtained features are processed for encoding through the proposed hybrid hufmann encoder. The simulation results illustraes the performance of proposed approach and outperforms the conventional approach both visually and numerically.

VIII. REFERENCES

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A Framework for Underwater Image Enhancement and Object Detection

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Abstract— **The underwater images are distorted due to absorption and scattering of light. The enhancement techniques used to improve the quality of underwater images are based on the level of noise introduced and also the water quality. Underwater image enhancement is necessary extract the desired or suspicious objects under the sea. This paper describes an improved image enhancement for the underwater images in YCbCr space and canny edge detection for underwater images. The edge detection is done for each Y, Cb and Cr components separately and are combined to get more accurate edge detected underwater image. The morphological process is also applied to obtain the thin edges and the identified objects parameter like area, length, width, etc are also calculated. The obtained results of the proposed method improve the accuracy of object detection.**

Keywords— ***underwater images, color segmentation, histogram, number of edges.***

I. INTRODUCTION

The quality of underwater images plays a pivotal role in scientific missions such as monitoring sea life, taking census of populations, and assessing geological or biological environments. Capturing images underwater is challenging, mostly due to haze caused by light that is reflected from a surface and is deflected and scattered by water particles, and color change due to varying degrees of light attenuation for different wavelengths. Light scattering and color change result in contrast loss and color deviation in images acquired underwater. Several methods have been introduced for underwater image enhancement and detection. The underwater image processing differs from normal image processing due to noise and poor illumination [1], [2]. Conventional techniques use blind color equalization for enhancing the underwater images. Images enhanced using these techniques are not giving promising results for edge detection, feature extraction and analysis. In particular, blue and green colors are dominant in underwater images. The colors like red and yellow almost disappear with increasing depth. So, efficient image enhancement and edge detection is required for underwater analysis.

In the RGB model the color components are not separated. This makes it unsuitable for enhancing images. Meanwhile YCbCr model separates the input image into three components and gives more flexibility in modifying images. In this paper, the algorithm enhances the brightness, visibility and contrast of underwater images. The enhanced image is subjected to edge detection. The proposed technique uses YCbCr model for processing. Enhancing the luminance component in this model automatically enhances the brightness of the image without disturbing Cb and Cr components.

Object detection in underwater image is difficult since the object edges are affected by light reflection near water surface. Also in deep water, the boundary of the object is not detected accurately due to dark color of the object and poor illumination. The enhanced images produce an improved edge detection results. In this paper section II describes the literature survey and section III describes the proposed work. Section IV and V explains the results with evaluation measurements and session VI concludes the paper.

II. EXISTING WORK

Edge detection is most widely used in image processing and analysis of the underwater images such as feature description image segmentation, pattern recognition, etc. The classic edge detection methods require pre-processing for efficient underwater images. So pre-processing is a key factor for obtaining efficient feature extraction. In [3], underwater image processing for object detection is described. In that paper, first the RGB image is converted into blue image and then LOG operator is used for edge detection. The advantages of the LOG operator over the other operators are the edge smoothening by Gaussian function and the rational invariance by laplacian portion. A disadvantage of the operator is the large size of the kernels.

In [4], enhancement of underwater images using CLAHE Algorithm is explained. RGB color space is converted into L*a*b color space and CLAHE algorithm is applied to L only. Yuejiao et la [5] used K-means algorithm for underwater image edge detection and classification.

Banerjee [6] proposed a real time underwater image enhancement technique for imaging with AUV150 images. In that paper [6], sequence of linear, non-linear filters and adaptive contrast correction in the RGB and YCbCr color space is used to enhance the underwater images. This multi-step image enhancement algorithm RyPro is suitable for real time-applications.

In [7], an automated approach for fish detection was proposed. The shape information of the fish is incorporated into the level sets through PCA method.

PSO algorithm is used to enhance color image. In this [8], first RGB values are adjusted using PSO and enhancement using PSO was done in HSV color space. These techniques are time consuming and have more computational complexity. The proposed method is simple and more suitable for real-time applications such as fish monitoring and suspicious object detection in underwater.

III. PROPOSED WORK

The proposed method consists of two steps which involves pre-processing of the acquired image followed by the edge detection.

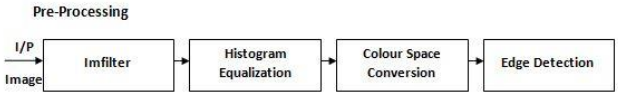


Fig.1 Pre Processing Block Diagram

The pre-processing consists of the following steps.

i) Imfilter
ii) Histogram Equalization
iii) Colour Space Conversion
iv) Edge Detection

Imfilter is used for multidimensional image filtering. It filters the multi-dimensional array using multi-dimensions filters. The array can be a non-sparse numeric array of any class and dimension. The resultant array is of same class and size of the input array.

Histogram Equalization is the process of automatically adjusting intensity values. It involves transforming the intensity values so that the histogram of the output image approximately matches a specified histogram. The transformation helps in enhancing the contract of the image. It can be achieved by converting an RGB image to an YCbCr image and enhancing the intensity.

Color Space Conversion is a process of converting the RGB color space into its equivalent components and colorimetric values depending upon the application we are using. Here we are using YcbCr color space. YcbCr color space is widely used in digital video. Since the image is acquired by a camera, we are using this Color space. The video obtained from the camera is split into several frames and every tenth frame is taken for the image processing. In this format, the luminance information is stored as a single component (Y) while the chrominance components are stored in two color difference components (Cb and Cr). However, performing histogram equalization on R, G and B components independently will not enhance the image.

Edge Detection is an image processing technique used to find the boundaries of an object inside the image. It works by detecting discontinuities in brightness. Edge detection is used in image segmentation and data extraction. Common edge detection algorithms include Sobel, Canny, Perwitt, Roberts and fuzzy logic methods. Most of the information about an object in an image is defined by the edges.

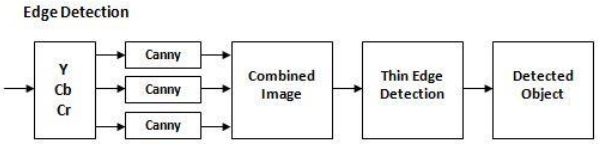


Fig. 2 Edge Detection Block Diagram

Here we are using the canny operator for detecting the edges of the given image because of its better performance in noisy environments. *Canny edge detection* is a technique to extract useful structural information from different vision objects and dramatically reduce the amount of data to be processed. It has been widely applied in various computer vision systems.

The general criteria for edge detection include:

1. Detection of edge with low error rate, which means that the detection should accurately catch as many edges shown in the image as possible
2. The edge point detected from the operator should accurately localize on the centre of the edge.
3. A given edge in the image should only be marked once, and where possible, image noise should not create false edges.

Among the edge detection methods developed so far, canny edge detection algorithm is one of the most strictly defined methods that provide good and reliable detection. Owing to its optimality to meet with the three criteria for edge detection and the simplicity of process for implementation, it became one of the most popular algorithms for edge detection.

Algorithm:

1. Convert the RGB color space image into YCbCr color space image.

2. Histogram equalization is applied in the obtained YCbCr image which enhances the contrast of the image.
3. Now, the enhanced image is split into its respective Y, Cb and Cr components.
4. Canny edge detection is applied to each of the Y, Cb and Cr component images.
5. All the three edge detected image are now combined to form a single YCbCr edge detected image.
6. The obtained YCbCr edge detected image is dilated inorder to obtain the thin edge.
7. Now, the boundary of the thin edge image is traced.
8. Finally, the boundary line indicates the detected object.

IV. Results and Comparison

The proposed algorithm has been implemented using MATLAB. This implemented method is tested on various underwater images. The figure shows the original and enhanced image and its respective histograms.

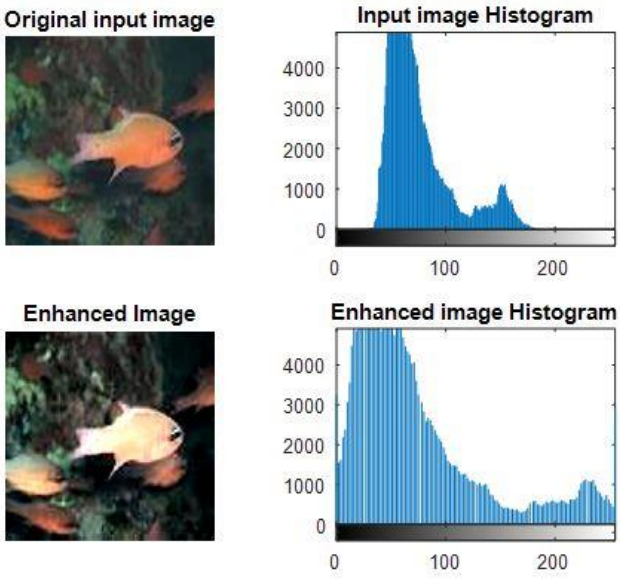


Fig. 3 Input and enhanced image with histogram

The figure shows the Y, Cb and Cr image after histogram equalization.

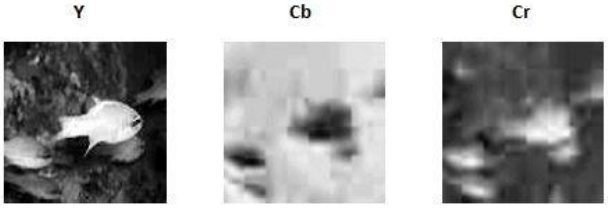


Fig. 4 Y, Cb and Cr Components

The figure shows the edge detected image of Y, Cb and Cr components and the combined edge detected YCbCr image.

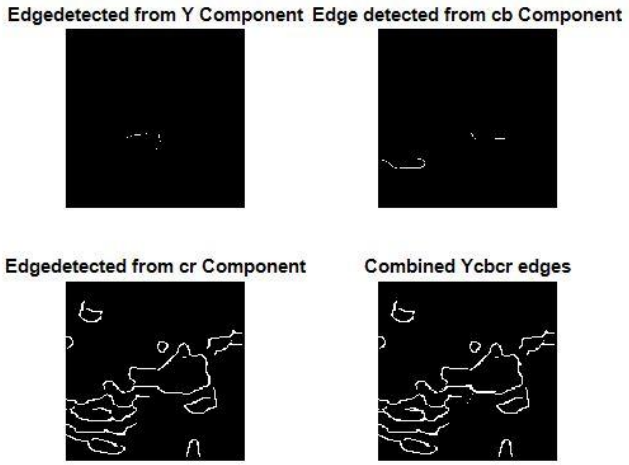


Fig. 5 Edges of Y, Cb, Cr Components and Combined Edges

The figure shows the dilated image of the combined YCbCr image, thin edge detected image, boundary tracing and object detected image.

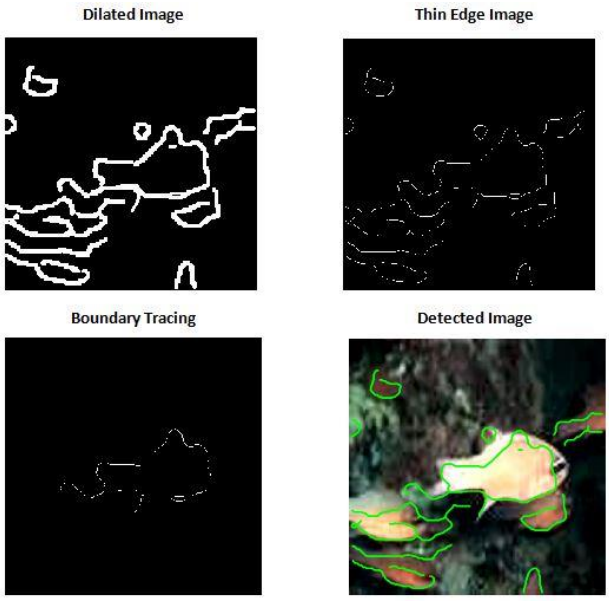
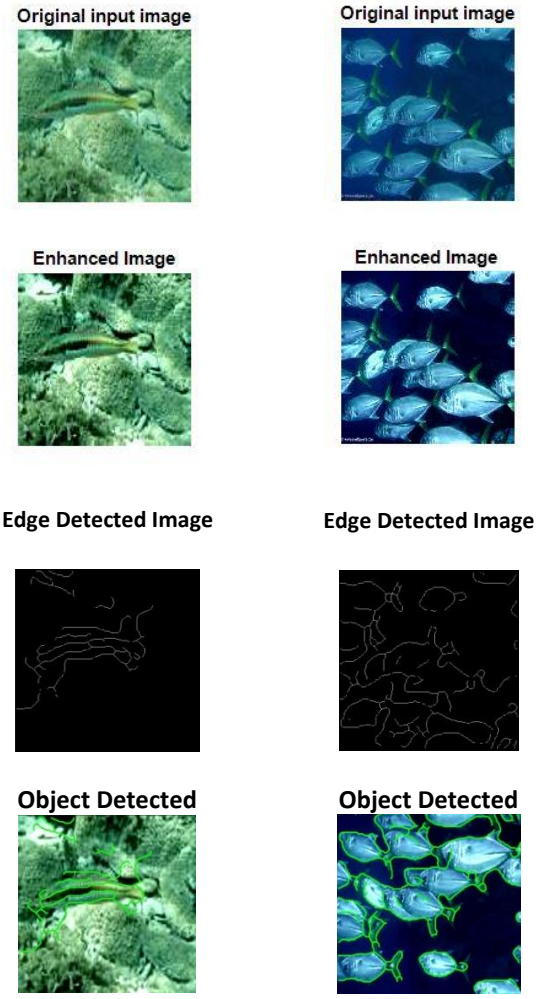


Fig. 6 Image after dilation with boundary tracing

The following figure shows the image enhancement and detection of two underwater images.



The performance of the algorithm is tested using underwater fish images. The detected object (fish) size (area) and width are measured and tabulated in table 1. And also the detected object index number is also given. The index number denotes the maximum size of the connect component in the image.

TABLE I: Detected Object Width and Area

Input	Detected Object Size		Index number
	Area	Width	
Image 1	745	443	7
Image 2	1141	384	14
Image 3	1810	499	2

V. CONCLUSION

Underwater image enhancement and edge detection has been discussed in this paper. The object extracted using this method, produces better results than canny edge detection without enhancement. In this method, edge detection is applied separately for Y, Cb and Cr components. The proposed technique has clear potential to identify fish population from the video sequences taken from noisy underwater environment. It is also useful for earth remote sensing images. In future, restoration models can be used to improve the accuracy of detected object.

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A LOW FREQUENCY NOISE CANCELLATION VLSI CIRCUIT DESIGN USING LMS ADAPTIVE FILTER FOR IN-EAR HEADPHONES.

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Abstract – The noising of audio signal is key challenge problem in Audio Signal Processing. Since noise is random process and varying every instant of time, noise is estimated at every instant to cancel from the original signal. There are many schemes for noise cancellation but most effective scheme to accomplish noise cancellation is to use feed forward filtered-x least mean square. Active Noise Cancellation (ANC) is achieved by introducing "anti noise" wave through an appropriate array of secondary sources. The FxLMS algorithm implemented in Mat lab using Xilinx system generator to achieve noise control.. These factors are used to demonstrate the efficiency of the algorithm used. Then it is implemented in VLSI platform through Verilog coding using Xilinx

I. INTRODUCTION

Conventional active noise cancelling (ANC)head phones often perform well in reducing the low-frequency noise and isolating the high-frequency noise by earmuffs passively. The existing ANC systems often use high-speed digital signal processors to cancel out disturbing noise, which results in high power consumption for a commercial ANC headphone. The contribution of this paper can be classified into: 1) proper filter length selection; 2) low-power storage mechanism for convolution operation; and 3) high-through put pipelining architecture. The existing active noise cancelling (ANC) systems use delayed LMS adaptive filter. These ANC systems require high computational complexity, power intensive hardware, and significant processing time for measuring noise signal, and then calculating and synthesizing proper anti noise signals to cancel out the noise signals in real time

In this paper, a dedicated feed forward ANC circuit implementation based on the well-known FxLMS adaptive algorithm for high fidelity in-ear headphones is developed. . By selecting a proper filter length, 62.7% of the computation complexity of convolution filter can be saved without sacrificing any ANC performance. In addition, a dedicated storage mechanism called one-update circular buffer is proposed to keep the switching activity low to save power. Finally, a three-stage pipelining multiply accumulator (MAC) architecture is used to increase the data throughput.

II SURVEY OF EXISTING METHODS

S. M. Kuo etal explained that Active noise control (ANC) is achieved by introducing a cancelling "anti noise" wave through an appropriate array of secondary sources. These secondary sources are interconnected through an electronic system using a specific signal processing algorithm for the particular cancellation scheme

I. Panahi, etal, explained the Active noise cancellation (ANC) applications for headphones are strongly influenced by practical constraints. Most previous works developing algorithms for ANC headphones are based on simplified simulations only and neglect practical limitations.

L. Wu, X. Qiu,etal mentioned in the adaptive feedback active noise control system based on the internal model control (IMC) structure, the reference signal is regenerated by synthesizing the error signal and the secondary signal filtered with the estimation of the secondary path, hence more computation load and extra programming are required

III EXISTING MODEL: DELAYED LMS ADAPTIVE FILTER

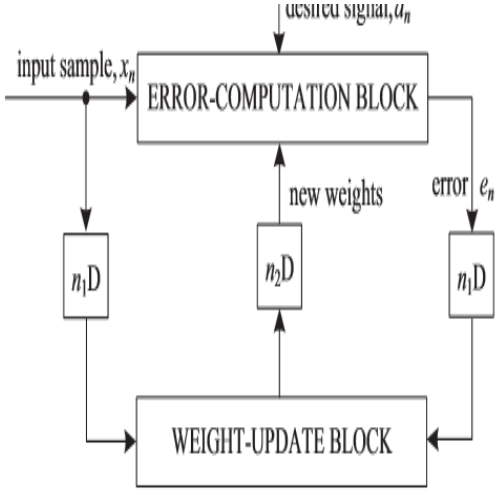

Fig 1:Modified delayed LMS adaptive filter

In the design based on pipelined with *m* pipeline stages, the error *en* will produced after *m* adaptation delay cycles.So the algorithm therefore uses the *en−m*

. The DLMS adaptive filter weight-update equation is represented by

$$\mathbf{w}_{n+1} = \mathbf{w}_n + \mu \cdot e_{n-m} \cdot \mathbf{x}_{n-m}.$$

The DLMS adaptive filter block diagram is shown in Fig. 1, where the adaptation delay of *m* cycles amounts to the delay introduced by the full adaptive filter structure and the structure consisting of finite impulse response (FIR) filtering and the weight-update process.

The weight-update equation of the modified DLMS algorithm is given by

$$\mathbf{w}_{n+1} = \mathbf{w}_n + \mu \cdot e_{n-n_1} \cdot \mathbf{x}_{n-n_1}$$

where

$$e_{n-n_1} = d_{n-n_1} - y_{n-n_1}$$

and

$$y_n = \mathbf{w}_{n-n_2}^T \cdot \mathbf{x}_n.$$

The modified DLMS algorithm decouples computations of the error-computation block and the weight-update block . It permitted us to perform optimal pipelining by feed forward cut-set retiming to minimize the number of pipeline stages and adaptation delay.

IV PROPOSED MODEL: ADAPTIVE FEED FORWARD FILTERED-X LEAST MEAN SQUARE FX LMS FILTER

A feed forward ANC control system uses an input microphone close to the noise source to pick up the noise signal x(n) before it is sensed by the listener. Accordingly, the ANC controller can produce an anti noise signal y(n)processing equal amplitude but opposite phase of x(n). Such anti noise signal is used to drive the cancelling-loud speaker to generate a cancelling sound that attenuates the primary acoustic noise in the ANC system. Fig. 1 shows the application of the feed forward Fx LMS adaptive algorithm in ANC system

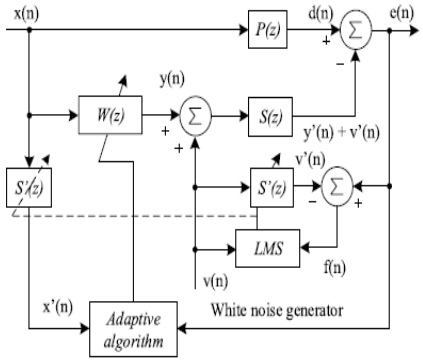

Fig2: Feed forward Fx LMS filter

P(z) and S(z), respectively, denote the primary-path and the secondary-path models**.** W(z) indicates the filter weights of the ANC controller to adaptively generate the required anti noise signal according to the time-variant noise source. and e(n) is the error signal generated by acoustically combining the primary noise d(n)and the adaptive filter output y(n).

The output y(n) of an adaptive filter at time n is given by y(n) = w(n)x(n) Where w(n) = [w0(n)w1(n) . . .wL−1(n)]T is the L × 1 filter coefficient vector and x(n) =[x(n)x(n − 1) . . . x(n − L + 1)]T is the L × 1 reference signal vector. The FxLMS algorithm updates the weighting coefficients of the adaptive filter in a way as w(n + 1) = w(n) + μ1x(n) ∗ h(n)e(n) where μ1 is the step size of the algorithm that determines the stability and convergence speed of the algorithm h(n) is the impulse response of S(z) and **e(n) = d(n) − y(n).**

The input vector x(n) is filtered by S(z) before updating the weighting vector. However, in practical applications, S(z) is unknown and must be estimated by S(z). Therefore, the resulting FxLMS algorithm can be represented by wl (n+1) = wl (n) + μ1x(n − l)e(n), l = 0, 1, 2, . . . , L − 1where x(n) =m(n)x(n − m), m = 0, 1, 2, . . . , M −1 , estimated version of the reference input x(n) after passing through the secondary path

Usually, the standard transversal filter used in the ANC controller .A standard adaptation algorithms proposed for the transversal filters e.g. Least Mean Square (LMS) or Recursive Least Square (RLS) cannot be used for the automatic adjustment of ANC controllers

FxLMS is a gradient based algorithm used for the identification of an unknown system (e.g. a desired ANC controller) at the presence of a secondary path. The performance of an FxLMS-based ANC system is limited by a number of related factors that must be addressed in the appropriate order. The absolute maximum level of performance is limited first by the characteristics of the physical plant to be controlled, including the secondary path impulse response and the acoustic noise bandwidth.

This means that no matter how good is the electronic control system, the FxLMS will not function properly if the secondary path has a long impulse response and/or the acoustic noise has a wide bandwidth

V. RESULTS

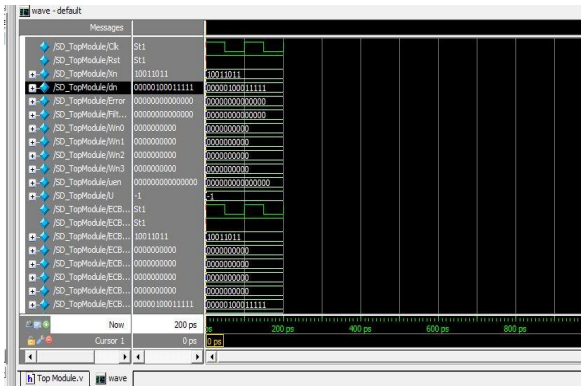

Fig.3 output for first 2 clocks

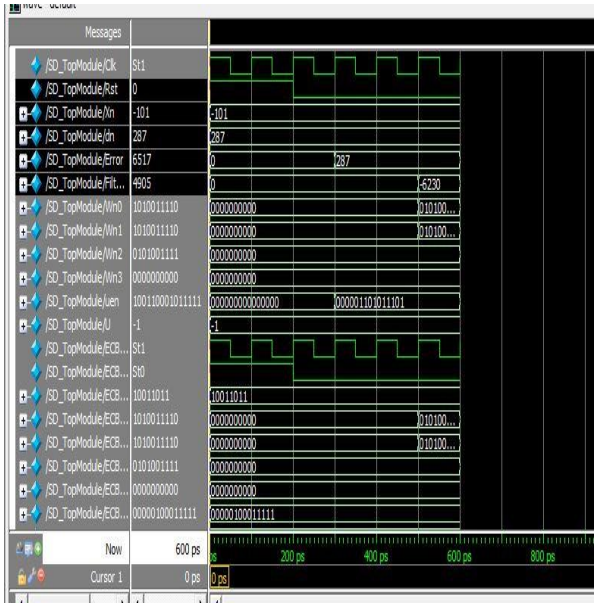

Fig 4 : Final Output and input with noise

Table I Comparison with Existing works

SL. No	Parameters	Existing methods	Proposed method
1	Power consumption	high	low
2	Power storage	high	low
3	Algorithm	Delayed LMS Algorithm	Fast LMS Algorithm
4	cost for Headphones	high	low
5	Size and weight of Headphone	large : Because of additional use of Battery	Small
6	Mathematical complexity	less in Secondary path	less in Secondary path

From the table, it is clear that power consumption is low compare to the previous works and the headphones cost is also low

VI. CONCLUSIONS

In this paper, an area-/power-efficient feed forward Fx LMS ANC circuit has been developed for in-ear head phones. The proposed design has been successfully implemented by using TSMC 90-nm CMOS technology. To verify the validity of the proposed design, a series of physical measurements has been executed in an anechoic chamber. Furthermore, the measurement results were compared with that of other state-of-the-art works. The experimental results show that the proposed high-performance/low-power ANC circuit design can reduce disturbing noise of various frequency bands very well, and outperform the existing works. The proposed design can attenuate 15 dB in physical measurement for the broad band pink noise between 50 and 1500 Hz when operated at 20-MHz clock frequency at the cost of 84.2 k gates and a power consumption of 6.59 mW only.

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Path Loss calculation in WBAN at CM3 Channel by using Printed Dipole Antenna

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Abstract—A wireless body area network(WBAN) is a recent trend in medical field where wearable devices which can measure signals such as heart beat and pulse rate are connected in a wireless network. New technologies of wireless sensor networks were enabled with the rapid growth in physiological sensors, low power integrated circuits and wireless communication. The major challenge it faces is path loss during transmission of the signal. By calculating this path loss, one can not only use it to find the accuracy of the received signal but also try to reduce it. Dipole antennas are used to analyse the path loss in CM3 channel of wireless body area network at 900MHz. This analysis helps to select the best way to propagate the signal in Wireless Body Area Network.

Keywords: WBAN; LOS; NLOS; Path loss.

1. Introduction

A multiple body parameters-computing device which can be worn on or kept inside human bodies is called the wireless body area network (WBAN). A mobile hub which acquires the data from the user and transmits it to a remote database is required. A smart phone in a pocket or bag serves the purpose. A Body Area Network consists of a mobile or any other electronic device in a pocket or pouch which is attached to the waist. This device acts like a data hub receiving the body parameter signals from the patient and transmitting them to a remote database [2]. Communication is the transmission of information from one place to another without help of wires, cables, or any such conductors. The distance of transmission can be anywhere between a few meters to thousands of kilometers [4]. Path loss can be defined as the attenuation suffered by a signal travelling along a line between a transmitter and a receiver [8]. The causes of path loss include physical phenomena such as reflection of signal by striking any obstacle, refraction through a medium and diffraction at the edges of a body. The natural expansion of the radio wave front in free space causes the propagation losses. A tabular form including different scenarios along with their descriptions and frequency bands which are used in IEEE 802.15.6 device's operation are given in below.

Table I Different channel models in WBAN

SCENERIO	DESCRIPTION	FREQUENCY BAND	CHANNEL MODELS
S1	Implant to Implant	402-405MHz	CM1
S2	Implant to Body surface	402-405MHz	CM2
S3	Implant to external	402-405MHz	CM2
S4	Body surface to body surface(LOS)	13.5,50,400, 600,900MHz 2.4,3.1-10.6GHz	CM3
S5	Body surface to body surface(NLOS)	13.5,50,400, 600,900MHz 2.4,3.1-10.6GHz	CM3
S6	Body surface to external(LOS)	900MHz 2.4,3.1-10.6GHz	CM4
S7	Body surface to external(NLOS)	900MHz 2.4,3.1-10.6GHz	CM4

2. Literature Survey

The natural expansion of the radio wave front in free space causes the propagation losses. The path loss constitutes of these propagation losses. [1]. Body area networks have its applications mainly in the medical field. These applications include electronic sensors which monitor patients for different health conditions. A system that can act as a Data Book in the field of diagnosis and treatment of ailments is also proposed [2]. This technology can also blood pressure (BP) and other patient vital signs. Research on BANs can be gone back to 1961 with work from Mackay [3] on radio telemetry inside the Body. T G Zimmerman initially gave the wireless body area networks in the editorial from 1996[4]. A homogeneous loss medium having an insulated dipole antenna is tested for path loss models in paper [5]. And the effect of permittivity and conductivity on the path loss is studied. Path loss models become widely acceptable and applicable if extraction of the propagation channel properties is possible for body-centric systems [6]. The possible thickness of the tissues in an adult and a child at various regions of the body is studied in [7].

3. Experimental Setup and Measurements

The dipole antennas are used for calculating the loss between transmitter and receiver in WBAN. N9320B Spectrum Analyzer and N9310A RF Signal Generator manufactured by Agilent Technologies are used and the analysis is carried out by different antennas like dipole antenna. The RF signal generator is used to generate a signal with desired frequency and power. The spectrum analyzer is used to display the signal with the specifications like power in dB and frequency in the range of 100Hz to 3GHz. Initially two antennas of same kind are taken. One is connected to the RF Signal generator using a connector. Other one is connected to the Spectrum Analyzer with the connector. Both the antennas are adjusted in such a way that they are in Line of Sight (LOS). It is observed that when the distance between the antennas is increased the loss is gradually increased. The below figure 1 shows the experimental setup of spectrum analyzer and RF signal generator.

Figure 1 Experimental setup

The below figure 2 shows the waveform on the spectrum analyzer with a frequency of 900MHz.Similarly, dipole antenna antenna is tested using the analyzers.

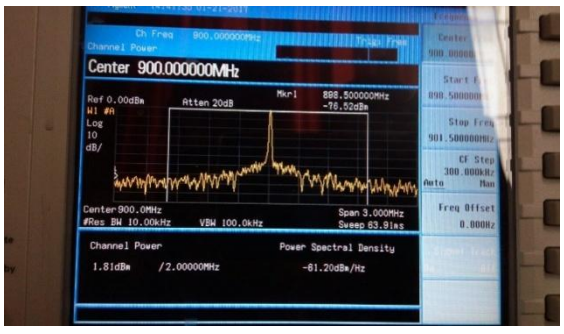

Figure 2. Waveform in spectrum analyzer

Now the position of the antenna is changed to Non-Line of Sight (NLOS). The transmitting antenna is placed in the shirt pocket, the receiving antenna is placed in the pant pocket as shown in figure 3 and path loss is calculated.

Figure 3. Chest (Heart) to pocket

The below table I shows the transmitted and received powers by using Dipole antenna at 900MHz frequency.

Table I. Measurement by dipole antenna at 900MHz

MEASUREMENT BY DIPOLE ANTENNA AT 900MHZ			
Frequency	**Transmitted Power**	**Received Power**	**Position**
900MHz	10	3.96	LOS
900MHz	-10	-16.88	
900MHz	-27	-37.67	

4. Conclusion

Wireless Body Area Network is a budding technology which offers a numerous advantage and ample of applications to many patients and to the society as well in one way or the other. Applications of WBAN include Medical health care Sports and fitness monitoring; Military and Security.In the whole process of finding the path loss dipole antenna gave a good result compared to Yagi antenna, patch antenna and other antennas. Among the propagation models such as okumura model, Hata model, free space path loss model and other models, it is found that a log distance propagation model proved to be the model with the lowest path loss. Analysing different antennas for selecting the best antenna is achieved using experimentation. This paper shows the experimental measured path loss at CM3 channel of WBAN at 900 MHz in LOS condition at different palces of the body.

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Consistent Data Delivery in Mobile Adhoc Networks

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Abstract- **Mobile adhoc Networks (MANETs) technologies have been gradually impacting almost all spheres of our lives. Recently, the Mobile adhoc Networks (MANETs) are gaining increased attention for generating extensive wireless communication. Routing protocols for ad hoc wireless networks must be able to perform efficient and effective mobility management. Most existing ad hoc routing protocols are susceptible to node mobility, especially for large-scale networks. Also in Mobile adhoc network, the node mobility and the location update interval are main factors leading to packet forwarding failure due to the receiver moving from one position to another. Focused this concern Spot based Opportunistic Routing Protocol (SOR) has been proposed to face issues of the high node mobility. This proposed scheme is designed for the dynamic nature of MANETs associated with various constraints. SOR routing protocol which takes advantage of find an effective routing which is used to transmit information from source to destination across the whole network topology. End of the results shows that SOR achieves excellent performance even under high node mobility with acceptable overhead.**

Keywords — MANETs, SOR, Mobility, Data Delivery, Location Update Interval.

I. INTRODUCTION

Realizing the necessity of open standards in this emerging area of computer communication, a working group within the Internet Engineering Task Force (IETF), termed the name Mobile ad hoc networks (MANETs) working group was formed to standardize the routing protocols and functional specifications of the Mobile adhoc networks. Mobile adhoc networks routing functionality is to mainly support for the self-organizing mobile networking infrastructure. Even though ad hoc networks are expected to work in the absence of any fixed infrastructure. Mobile Ad hoc networks are defined as the category of wireless networks that utilize multi-hop radio relaying and are capable of operating without the support of any fixed infrastructure. MANETs are self-organizing networks and they have been made up of mobile nodes, which are using their neighbors as a mean of communication with other nodes in the network.

Existing routing protocols in ad-hoc networks utilize the single route that is built for source and destination node pair. Due to node mobility, node failures and the dynamic characteristics of the radio channel, links in a route may become temporarily unavailable, making the route invalid.

The overhead of finding alternative routes mounts along with additional packet delivery delay. Mobile Adhoc networks change their topology, expressed by the node connectivity over time, as the nodes change their position in space. [1] Mobile ad hoc networks are characterized by dynamic topology due to node mobility, limited channel bandwidth and limited battery power of nodes.

The key challenge here is to be able to route with low overheads even in dynamic conditions [2]. Adhoc mobile networks are very dynamic, self-organizing, self-healing distributed networks which support data networking without an infrastructure. [4] Mobile Ad hoc Networks consists of a set of wireless mobile nodes communicating to each other without any centralized control or fixed network infrastructure and can be deployed quickly [5]. Adhoc mobile networks are very dynamic, self-organizing, and self-healing distributed networks which support data networking without an infrastructure. Due to lack of trusted nodes, Mobile adhoc networks require specialized authenticated protocol [6]. Mobile Adhoc Network is an autonomous system consisting of a set of mobile hosts that are free to move without the need for a wired backbone or a fixed base station. [7] Mobile Adhoc Networks having self-organizing and self-configuring network without the need of any centralized base station and physical connections of mobile devices. Mobile ad-hoc network has no fixed topology due to mobility of nodes, interference, path loss and multipath propagation. Mobile Ad hoc Networks is a robust infrastructure less wireless network having mobile nodes. A MANETs can be created either by mobile nodes or by both static and dynamic mobile nodes. A mobile node has arbitrarily associated with each other forming uniformed topologies. They serve up as both routers and hosts. [8] A Mobile Adhoc Network (MANETs) is a collection of autonomous wireless mobile nodes forming frequently changing network topology. Which nodes can communicate with each other through wireless links that needs efficient this is enough for into dynamic routing protocols [9].

To summarize, this paper is organized as follows. Section II provides details of the various classifications of Routing protocols, Section III Existing MANETs Routing Protocol, Section IV Literature Survey, V. Proposed System, and the conclusion of the paper in Section VI.

II. CLASSIFICATION ON ROUTING PROTOCOLS

The routing protocols in Mobile adhoc networks can be broadly classified into four categories. They are

- Routing information update mechanism
- Use of temporal information for routing
- Routing topology
- Utilization of specific resources

A. *Based on the Routing Information Update Mechanism*

Ad hoc wireless network routing protocols can be classified into three major categories as follows based on the routing information update mechanism.

- Proactive or table-driven routing protocols
- Reactive or on-demand routing protocols
- Hybrid routing protocols

B. *Based on the Use of Temporal Information for Routing*

This classification of routing protocols is based on the use of temporal information used for routing. Since ad hoc wireless networks are highly dynamic and path breaks are much more frequent than in wired networks, the use of temporal information regarding the lifetime of the wireless links and the lifetime of the paths selected assumes significance. The protocols that fall under this category can be listed as follows.

- Routing protocols using past temporal information
- Routing protocols that use future temporal information

C. *Based on the Routing Topology*

Routing topology being used in the Internet is hierarchical in order to reduce the state information maintained at the core routers. Ad hoc wireless networks, due to their relatively smaller number of nodes, can make use of either a flat topology or a hierarchical topology for routing.

- Flat topology routing protocols
- Hierarchical topology routing protocols

D. *Based on the Utilization of Specific Resources:*

Based on the Utilization of specific resources in MANETs has been classified in the following ways. They are listed below.

- *Power-aware routing*
- *Geographical information assisted routing*

III. EXISTING MANET'S ROUTING PROTOCOLS

Reactive or On-Demand Routing protocols execute the path finding process and exchange routing information only when a path is required by a node to communicate with a destination. Ad hoc on-demand distance vector (AODV) and dynamic source routing (DSR) are well-known examples of Reactive routing protocols. This section explores some of the existing on-demand routing protocols in detail.

- Dynamic source routing protocol (DSR)
- Ad hoc on-demand distance vector (AODV)
- Location-aided routing protocol (LAR)

A. *Dynamic Source Routing Protocol*

Dynamic source routing protocol (DSR) is an on-demand protocol designed to restrict the bandwidth consumed by control packets in ad hoc wireless networks by eliminating the periodic table-update messages required in the table-driven approach. The major difference between this and the other on demand routing protocols is that it is beacon-less and hence does not require periodic hellopacket (beacon) transmissions, which are used by a node to inform its neighbors of its presence. The basic approach of this protocol (and all other on-demand routing protocols) during the route construction phase is to establish a route by flooding RouteRequest packets in the network. The destination node, on receiving a RouteRequest packet, responds by sending a RouteReply packet back to the source, which carries the route traversed by the RouteRequest packet received.

Consider a source node that does not have a route to the destination. When it has data packets to be sent to that destination, it initiates a RouteRequest packet. This RouteRequest is flooded throughout the network. Each node, upon receiving a RouteRequest packet, rebroadcasts the packet to its neighbors if it has not forwarded already or if the node is not the destination node, provided the packet's time to live (TTL) counter has not exceeded.

Each RouteRequest carries a sequence number generated by the source node and the path it has traversed. A node, upon receiving a RouteRequestpacket, checks the sequence number on the packet before forwarding it. The packet is forwarded only if it is not a duplicate RouteRequest. The sequence number on the packet is used to prevent loop formations and to avoid multiple transmissions of the same RouteRequest by an intermediate node that receives it through multiple paths. Thus, all nodes except the destination forward a RouteRequest packet during the route construction phase. A destination node, after receiving the first RouteRequestpacket, replies to the source node through the reverse path the RouteRequest packet had traversed. This protocol uses Route cachethat stores all possible information extracted from the source route contained in a data packet. Also which is used at the time of routing construction phase.

Advantages

DSR protocol uses the reactive approach which eliminates the need to periodically flood the network with table update messages. This on-demand routing approach route is established only when it is required and hence the need to find routes to all other nodes in the network as required. The intermediate nodes also utilize the route cache information efficiently to reduce the control overhead.

Disadvantages

Drawbacks of DSR protocol is that the route maintenance mechanism does not locally repair a broken link. Even though this protocol performs well in static and low-mobility environments, the performance degrades rapidly with increasing mobility. Also, considerable routing overhead is involved due to the source-routing mechanism employed in DSR. This routing overhead is directly proportional to the path length.

B. *Adhoc On-Demand Distance-Vector Routing Protocol*

Ad hoc on-demand distance vector (AODV) routing protocol uses an on demand approach for finding routes, that is, a route is established only when it is required by a source node for transmitting data packets. It employs destination sequence numbers to identify the most recent path. In AODV, the source node and the intermediate nodes store the next-hop information corresponding to each flow for data packet transmission.

In an on demand routing protocol, the source node floods the RouteRequest packet in the network when a route is not available for the desired destination. It may obtain multiple routes to different destinations from a single RouteRequest. The major difference between AODV and other on-demand routing protocols is that it uses a destination sequence number (DestSeqNum) to determine an up-to-date path to the destination. A node updates its path information only if the DestSeqNum of the current packet received is greater than the last DestSeqNum stored at the node.

A RouteRequest carries the source identifier (SrcID), the destination identifier (DestID), the source sequence number (SrcSeqNum), the destination sequence number (DestSeqNum), the broadcast identifier (BcastID), and the time to live (TTL) field. DestSeqNum indicates the freshness of the route that is accepted by the source. When an intermediate node receives a RouteRequest, it either forwards it or prepares a RouteReply if it has a valid route to the destination. The validity of a route at the intermediate node is determined by comparing the sequence number at the intermediate node with the destination sequence number in the RouteRequest packet. If a RouteRequest is received multiple times, which is indicated by the BcastID-SrcID pair, the duplicate copies are discarded. All intermediate nodes having valid routes to the destination, or the destination node itself, are allowed to send RouteReply packets to the source. Every intermediate node, while forwarding a RouteRequest, enters the previous node address and it's BcastID. A timer is used to delete this entry in case a RouteReply is not received before the timer expires. This helps in storing an active path at the intermediate node as AODV does not employ source routing of data packets. When a node receives a RouteReply packet, information about the previous node from which the packet was received is also stored in order to forward the data packet to this next node as the next hop toward the destination.

Advantages

The main advantage of this protocol is that routes are established on demand and destination sequence numbers are used to find the latest route to the destination. The connection setup delay is less.

Disadvantages

One of the disadvantage of AODV protocol is that intermediate nodes can lead to inconsistent routes if the source sequence number is very old and the intermediate nodes have a higher but not the latest destination sequence number, thereby having stale entries and also multiple *RouteReply* packets in response to a single *RouteRequest* packet can lead to heavy control overhead.

C. Location-aided routing protocol (LAR)

LAR reduces the control overhead by limiting the search area for finding a path. The efficient use of geographical position information, reduced control overhead, and increased utilization of bandwidth are the major advantages of this Location-aided routing protocol. The applicability of this protocol depends heavily on the availability of GPS infrastructure or similar sources of location information. Hence, this protocol cannot be used in situations where there is no access to such information.

IV. LITERATURE SURVEY

A. *A performance Comparison of Multi-hop Wireless ad hoc network Routing Protocols [1]*

Traditional routing algorithms prove to be inefficient in such a changing environment. Ad-hoc routing protocols such as dynamic source routing (DSR), ad-hoc on-demand distance vector routing (AODV) and destination-sequence distance vector (DSDV) have been proposed to solve the multi hop routing problem in ad-hoc networks. Performance studies of these routing protocols have assumed constant bit rate (CBR) traffic. Real-time multimedia traffic generated by video-on demand and teleconferencing services are mostly variable bit rate (VBR) traffic. Most of this multimedia traffic is encoded using the MPEG standard. When video traffic is transferred over MANETs a series of performance issues arise. This paper presents a performance comparison of three ad-hoc routing protocols - DSR, AODV and DSDV when streaming MPEG4 traffic. Simulation studies show that DSDV performs better than AODV and DSR. However all three protocols fail to provide good performance in large, highly mobile network environments.

B. *A Survey on Position-based Routing in Mobile ad hoc networks [2]*

A survey on position-based routing in mobile ad hoc networks paper presents an overview of ad hoc routing protocols that make forwarding decisions based on the geographical position of a packet's destination. Other than the destination's position, each node need know only its own position and the position of its one-hop neighbors in order to forward packets. Since it is not necessary to maintain explicit routes, position-based routing does scale well even if the network is highly dynamic. The main prerequisite for position-based routing is that a sender can obtain the current position of the destination.

C. *A framework for reliable routing in mobile ad hoc networks [21]*

Mobile ad hoc networks consist of nodes that are often vulnerable to failure. As such, it is important to provide redundancy in terms of providing multiple node-disjoint paths from a source to a destination. This papers propose a modified version of the popular AODV protocol that allows us to discover multiple node-disjoint paths from a source to a destination.

From that can conclude that it is necessary to place for call reliable nodes in the network for efficient operations. The proposed method of a deployment strategy that determines the positions and the trajectories of these reliable nodes such that achieve a framework for reliably routing information.

D. *Survey on Opportunistic Routing in Multihop Wireless Networks [10]*

The study of Opportunistic routing is based on the use of broadcast transmissions to expand the potential forwarders that can assist in the retransmission of the data packets. The receptors need to be coordinated in order to avoid duplicated transmissions. This is could be achieved by ordering the forwarding nodes and in the position-based packet forwarding strategies. This proposed Opportunistic routing protocols differ in the criterion to order the receptors and the way of the receptors coordinate. This paper presents a survey of the most significant opportunistic routing protocols for multihop wireless networks.

E. *ExOR: Opportunistic MultiHop Routing for Wireless Networks [6]*

This paper describes ExOR, an integrated routing and MAC protocol that increases the throughput of large unicast transfers in multi-hop wireless networks. ExOR chooses each hop of a packet's route after the transmission for that hop, so that the choice can react which intermediate nodes actually received the transmission. This deferred choice gives each transmission multiple opportunities to make progress. As a result ExOR can use long radio links with high loss rates, which would be avoided by traditional routing. ExOR increases a connection's throughput while using no more network capacity than traditional routing. ExOR's design faces the following challenges. The nodes that receive each packet must agree on their identities and choose one forwarder. The agreement protocol must have low overhead, but must also be robust enough that it rarely forwards a packet zero times or more than once. Finally, ExOR must choose the forwarder with the lowest remaining cost to the ultimate destination. For pairs between which traditional routing uses one or two hops, ExOR's robust acknowledgments prevent unnecessary retransmissions, increasing throughput by nearly 35%. For more distant pairs, ExOR takes advantage of the choice of forwarders to provide throughput gains of a factor of two to four.

V. PROPOSED SYSTEM

The design process of Spot based Opportunistic Routing Protocol (SOR) is based on geographic routing and opportunistic forwarding. The nodes are assumed to be aware of their own locations and the positions of their direct neighbors. In SOR Routing Protocol choosing the candidates and assigning priority among nodes for the forwarding candidates plays a major role while designing this routing protocol. Actually candidate means the node assigned as next hop which is selected among all nodes in the direction of forwarding region. The forwarding area has been determined by sender and the next hop node.

A. *SOR Protocol Design*

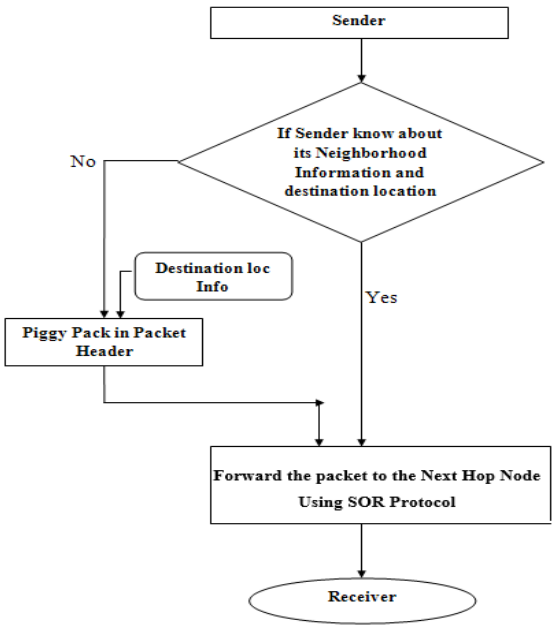

Figure 1 – SOR Protocol Designing Process flow

Spot based Opportunistic Routing Protocol (SOR) Designing process flow is shown in Figure 1. It takes the responsibility to solve the problems in the candidate selection and gives the priority to forwarding candidates. Also only the nodes located in the direction of forwarding region may get the chance to be backup nodes. Focused this concern an SOR Protocol has been designed in the following ways.

- Location Information adding in Packet header
- Candidate node selection
- Distance calculation between Each Node
- Priority assigning for the forwarding candidates
- Collects the Neighbor node List details
- Receiver details

From the above module details lists Candidate selection process has been primarily taken while designing SOR Protocol.

B. *Candidate Selection Process in SOR protocol*

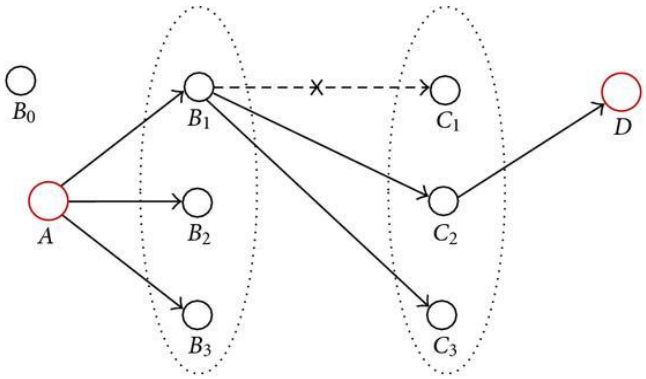

Figure 2: Candidate Selection process in SOR Protocol

Candidate selection process in Spot based Opportunistic Routing Protocol (SOR) is shown in the above Figure 2. Actual determination of the forwarding area is done by the sender and the next hop node. The node located in the forwarding area satisfies the following conditions. First one is that it might be present in the positive progress towards the destination. Next one important condition is that its distance to the next hop node should not exceed half of the transmission range of a wireless node. Based on that in above figure 2 the nodes from the A to D positive progress may take from the nodes B1, C1 and C2.Likewise the candidate process has been done by the SOR Routing Protocol.

VI. CONCLUSION

This paper addresses the problem of reliable data delivery in highly dynamic mobile ad hoc networks. Constantly changing network topology makes conventional ad hoc routing protocols incapable of providing satisfactory performance. In the face of frequent link break due to node mobility, substantial data packets would either get lost, or experience long latency before restoration of connectivity. The efficacy of the involvement of forwarding candidates against node mobility, as well as the overhead due to opportunistic forwarding is analysed. Through implementation, confirm the effectiveness and efficiency of SOR high packet delivery ratio may achieve while the delay and duplication are the lowest.

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Denoising of Image Corrupted by Random Valued Impulse Noise using Homogeneous Amount Based Filter

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Abstract **- In Image processing, Impulse noise is one kind of common noise which damages digital image quality heavily. In this paper, a new two-stage filter for the removal of random-valued impulse noise is presented. The new filter identifies noise candidates by analyzing the amount of similar pixels in intensity value, and then reconstructs them by the total variation inpainting method. The experimental results are reported which show the efficiency of our method in removing random-valued impulse noise. Further, our filter can be used for image restoration from images damaged by the superimposed artifacts**.

Index terms **– Homogeneous amount, Image denoising, Impulse noise, Two-stage scheme.**

1. INTRODUCTION

Similar to other digital signal, digital images are sometime could be corrupted by noise. Noise is an error mainly occurred during image acquisition and transmission. There are several ways that noise can be occurred in an image. For e.g. If the image is acquired directly in a digital format, the mechanism for gathering the data (such as a CCD detector) can introduce noise. Transmission of electronic data can introduce noise. Some noises are Gaussian noise, Rayleigh noise, Gamma noise, Exponential noise, Impulsive noise and so on.

Impulse noise is one kind of common noises which damages digital image quality heavily. There are many nonlinear filters have been proposed for suppressing impulse noise. In general, impulse noise appears as a sprinkle of bright or dark spots on the image, and normally these spots have relatively high contrast towards their surrounding areas. Therefore, even at low corruption level, impulse noise can significantly degrade the appearance and quality of the image.

Impulse noise is often introduced into frames of videos during acquisition and transmission. Based on noise Values, it can be classified as easier to remove salt and pepper noise and more difficult random valued impulse noise. This paper focus on removing the latter. Several filtering methods have been proposed for the removal of impulse noise from colour images using different approaches. When noise levels are high, many filters are not satisfactory in the removal of random-valued impulse noise.

In this paper, a new two-stage filter the homogeneous amount based (HAB) filter for the removal of random-valued impulse noise from highly corrupted images is proposed. In the noise detection stage, the noisy pixels are distinguished in an unrestricted field of view by analyzing the amount of similar pixels in brightness. In the noise cancellation stage, the detected impulses are reconstructed by an image inpainting method—the total variation inpainting (TVI) model.

2. RELATED WORK

There is often a trade-off made between noise removal and preservation of fine, low-contrast and edge detail that may have characteristics similar to noise. The number of filters used for removing noise from gray scale and color images. They are classified into several categories depending on specific for Gaussian noise removal but often distort edges and have poor performance against impulsive noise.

Chan RH et al.,[1]proposed a two-phase scheme for removing salt-and-pepper impulse noise. In the first phase, an adaptive median filter is used to identify pixels which are likely to be contaminated by noise (noise candidates). In the second phase, the image is restored using a specialized regularization method that applies only to those selected noise candidates. In terms of edge preservation and noise suppression, the restored images show a significant improvement compared to other methods. The median filter has good denoising power and computational efficiency, but MED always treats pixels without discrimination and results in blurring details and edges.

Tao Chen et al.,[2]described a methodology for removing the Random Valued Impulse Noise by designing a novel adaptive median filter that employs the switching scheme

based on the impulse detection mechanism. The objective is to utilize the center-weighted median (CWM) filters that have varied center weights to define a more general operator, which realizes the impulse detection by using the differences defined between the outputs of CWM filters and the current pixel of concern.

Tao Chen et al.,[3]designed a novel nonlinear filter, called tri-state median (TSM) filter, for preserving image details while effectively suppressing impulse noise. It incorporates the standard median (SM) filter and the center weighted median (CWM) filter into a noise detection framework to determine whether a pixel is corrupted, before applying filtering unconditionally.

Chen T, Wu H, proposed the adaptive center-weighted median (ACWM) filter [4] ,which can efficiently remove random-valued impulse noise by using the differences between the current pixel and the outputs of CWM with varied center weights.

Aizenberg I, Butakoff C designed a filter, the differential rank impulse detector (DRID) [5], to identify impulse more efficient. It incorporates the signal intensities and the ranks of signal values. Recently, the two-stage methods have been widely investigated and popularly used for removing impulse noise. The basic idea of the two-stage scheme is that the noise candidates in an image are firstly determined using a detector, and then the detected noises are reconstructed by a filter method.

3. SYSTEM MODEL

Image restoration is the operation of taking a corrupted/noisy image and estimating the clean original image. Corruption may come in many forms such as motion blur, noise, and camera misfocus. Removal of noise is an important step in the image restoration process, and remains a challenging problem in spite of the sophistication of recent research. The goal of restoration method is to preserve the underlying structure in the image, while removing noise.

Optimal noise removal should delete the visible noise as cleanly as possible and maintain the detail information and natural appearance to obtain a natural-looking image. In order to remove the impulse noise cleanly from input images without blurring the edge, the proposed system is divided into two stages and new two-stage filter the homogeneous amount based (HAB) filter for the removal of random-valued impulse noise is proposed.

1. Noise Detection
2. Noise Cancellation.

A. Noise Detection

Presented algorithm does the restoration in two stages and the idea here is to create a data chain using homogenous level of each pixels. The data chain can be created using direct search method.

B. Notion for detecting the Homogeneous pixels

The homogeneous amount of a pixel provides a measure of how many similar pixels are connected to the current pixel in the entire image scope. We use the homogeneous amount to recognize corrupted pixels based on the two assumptions:

1) A noise pixel takes a gray value substantially larger than or less than those of its neighbors.
2) A noise-free image should be locally smoothly varying and is separated by edges.

C. Block Diagram

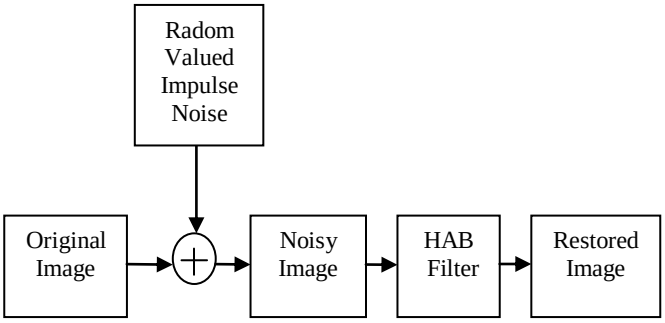

FIG 3.1 Block Diagram of proposed method

Figure 3.1 shows the block diagram of the proposed method. In the block diagram, the original image is added with the random valued impulse noise. The noisy image undergoes the Homogeneous amount based filter, to recover the original image. The recovered image is then compared with the original image for performance calculation.

D. Algorithm Steps

(1) We create a data chain whose head is p, and let Chain (p) denote the data chain.

(2) We begin the direct search at p: If a pixel, say $q \in N^0(p)$, has the same homogeneity level as p, then add the checked pixel q to Chain(p), and set q as the current considering pixel, repeat this step; if the pixel q does not exist in $N^0(p)$, then stop the direct search.

(3) For each pixel in Chain (p), we check whether there still has unchecked homogeneous pixel in its neighborhood. If there is no such pixel, then stop searching; otherwise, do the direct search at that pixel. We repeat the step until there is no unchecked homogeneous pixel for each pixel in Chain (p).

(4) When finishing step (1) to (3), we can obtain the homogeneous amount of p from Chain (p) since D_T (p) = Chain (p).

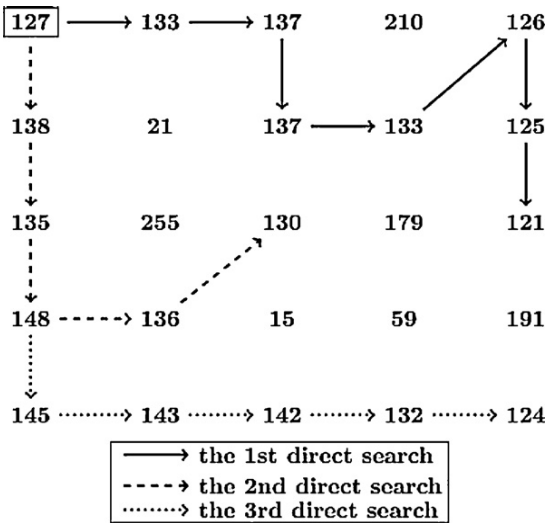

FIG 3.2 Demonstrating how to obtain the maximal homogeneity set with T = 20 at the boxed location.

E. Noise Cancellation

We employ an image inpainting method to reconstruct the corrupted pixels. The total variation inpainting (TVI) model is one of efficient methods to fill the missing block with surrounding information propagation. We use the TVI method to restore the corrupted pixels by the fact that the TVI model is simple but provides a good reconstruction for noise blotches. TVI method was proposed as

$$\frac{\partial u(x, y; t)}{\partial t} = \operatorname{div}\frac{\nabla u}{|\nabla u|} + \lambda_D (u-u_0)$$

where u(x, y ; t) is evolving image at t time, and the constant λ_D is a indicator function of the inpainting domain D($\subset \Omega$). Therefore, inside the inpainting domain, the model employs a simple anisotropic diffusion process:

$$\frac{\partial u(x, y; t)}{\partial t} = \operatorname{div}\frac{\nabla u}{|\nabla u|}$$

Since we use the TVI model to reconstruct the domain D which the noise candidates occupy, here we set λ_D as zero for simplification. Then we rewrite the TVI model as

$$\frac{\partial u(x, y; t)}{\partial t} = \delta(x, y)\ \operatorname{div}\frac{\nabla u}{|\nabla u|},\ (x, y) \in \Omega$$

Where δ (x,y) = 1 (x,y) ∈ D; 0 otherwise.

4. IMPLEMENTATION RESULTS

In this section, the performance of the Proposed Method based on Homogeneous Amount based filtering, is analyzed. Experimental results are carried out using standard images in MATLAB R2011a. Impulse noise is introduced into the image using "impulsenoise" function.

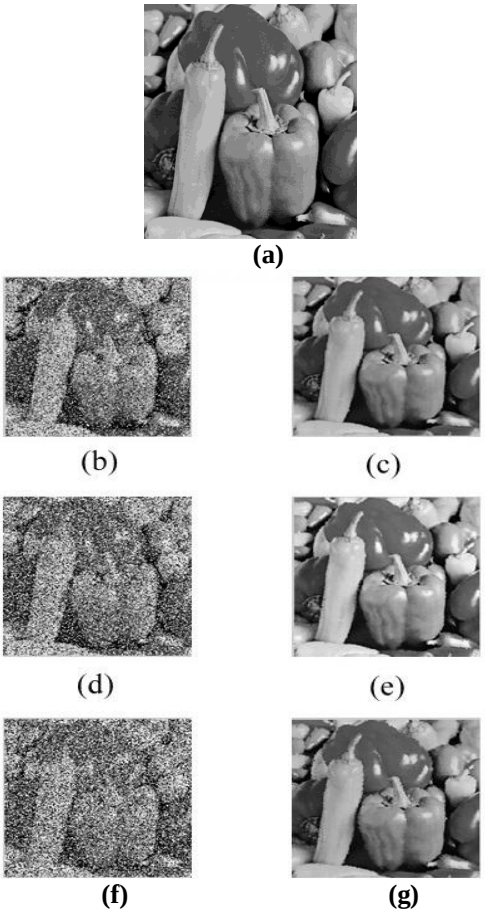

FIG 4.1 Results of restoring noisy Peppers image corrupted by 30%, 40%, 50% RVIN. (a) Noise-free image (512 ×512 in pixels) (b) 30% Noisy image (c)Restored image of 30% noise (d) 40% Noisy image (e)Restored image of 40% noise (f) 50% Noisy image (g)Restored image of 50% noise.

In FIG 4.1, the standard Peppers image is taken as original image is shown in FIG 4.1(a).The noise free image is corrupted with 30%, 40%,50% random valued impulse noise is shown in FIG 4.1(b),(d) and (g) respectively. Then the noisy image is filtered using Homogeneous amount based filter and the restored results for noise percent of 30%, 40%, 50% are shown in FIG 4.1 (c),(e) and (f) respectively.

Table 1 Comparisons of restoration results in PSNR (dB).

Noise Level	**MED (5x5)**	**PSM**	**DWM**	**DBM**	**HAB**
20%	30.98	32.44	35.23	37.03	38.17
40%	26.39	30.10	30.24	34.67	36.48
50%	24.65	29.38	28.98	31.12	32.71

The Table 1 shows the restored results for the seven different filters in peak signal to noise ratio (PSNR). In the HAB filter, we use T=14 for all cases of noise level, the iterations N = 100, N = 100 and N = 200 for 20%, 40% and 50% noise level, respectively. The filtered image of the HAB filter is better than those of the median-type filters, and is competitive to that of the Luo filter

5. CONCLUSION

The above results have shown that the proposed method using Homogeneous Amount Based (HAB) filter outperforms the existing methods such as Median filter, Center weighted median filter, Tristate median filter, Adaptive center-weighted median, Differential rank impulse detector, Genetic programming filter, Luo filter.

The proposed algorithm thus achieves better denoising performance and edge preservation capability. The filtered results of our filter also look very natural. One can see that the HAB filter can detect not only the small impulses but also the large “impulses”.

As a future extension, along with RVIN, super imposed artifacts are introduced in the image and then applied for filtering process. In addition, the time complexity of the proposed algorithm can be reduced for better performance.

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NOVEL ENERGY EFFICIENT CARRY SKIP ADDER BASED ON DUAL MODE LOGIC DESIGN

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ABSTRACT- ***The recently proposed dual mode logic (DML) gates family enables a very high level of energy-delay optimization flexibility at the gate level. In this paper, this flexibility is utilized to improve energy efficiency and performance of combinatorial circuits by manipulating their critical and noncritical paths. An approach that locates the design's critical paths and operates these paths in the boosted performance mode is proposed. The noncritical paths are operated in the low energy DML mode, which does not affect the performance of the design, but allows significant energy consumption reduction. The proposed approach is analyzed on a 128 bit carry skip adder.***

Keywords: ***Dual Mode Logic, energy efficiency, high performance, critical paths, energy-delay optimization.***

I. INTRODUCTION

The DML logic gates family was proposed in order to provide a very high level of energy-delay (E-D) optimization flexibility. DML allows an on-the fly change between two operational modes at the gate level: static mode and dynamic mode. In the static mode, DML gates consume very low energy, with some performance degradation, as compared to standard CMOS gates. Alternatively, dynamic DML gates operation obtains very high performance at the expense of increased energy dissipation. A DML basic gate is based on a static logic family gate, e.g., a conventional CMOS gate, and an additional transistor. While DML gates have very simple and intuitive structure, they require an unconventional sizing scheme to achieve the desired behavior .Performance of most digital circuits and systems is determined by the delay of critical paths (CP). Even though standard synthesis tools attempt to design logic blocks without CP (*i*:*e*: equalized path delay), the slack from the targeted *Clk* (Clock) frequency always exists and should be repaired by designers.

Many methods have been proposed to address these slacks. These methods include adaptive voltage scaling with a CP emulator circuit, multi oxide thickness driven threshold-voltages, multi-channel lengths for energy reduction in the non-CPs and performance boost in the CPs. *Meijer et al.* and *Liu et al.* applied a body bias on a non-CP to improve energy consumption and increase performance of the CPs, respectively. While the aforementioned methods solve the critical path slack problem, in most cases they also result in a significant increase of energy consumption. In addition to these gate level approaches higher-level approaches were presented such as multi-mode logics, parameterized logic. In this paper, we issue both the gate and higher architectural levels. This paper proposes to meet the delay requirements of CPs along with lowering the over-all energy consumption of the design by utilizing the powerful modularity of DML. We propose and analyze a new approach, which locates the design's CPs and utilizes the on-the-fly

modularity of DML to operate these paths in the boosted (dynamic) performance mode. The non-critical paths are operated in the low energy static DML mode, which does not affect the performance of the design. Since in most cases the majority of gates in the design are not on the CPs, the increase in energy consumption of the critical paths will be negligible in comparison to the general circuit consumption. Moreover, DML static gates dissipate less power than their CMOS counterparts, resulting in reduced power dissipation of the whole design .The proposed approaches have been analyzed on a 16 bit Carry Skip Adder (CSA) benchmark. Simulations carried out in a standard 180nm CMOS process.

II. DML BASICS

A. DML OVERVIEW

A basic DML gate architecture is composed of an un-clocked static gate, *e*:*g*: CMOS, and an additional transistor *M1*,whose gate is connected to a global clock signal. In this paper we focus on DML gates where the static gate implementation is based on conventional CMOS. A DML gate implementation can be one of two: ``*Type A*'' and ``*Type B*'', as shown in Figure 1(a-b) and Figure 1(c-d), accordingly. In the static DML mode of operation (Static mode), the M1 transistor is cut-off by applying the high *Clk* signal for ``*Type A*'' and low *Clk_bar* for ``*Type B*'' topology. Therefore, the gates of both topologies operate similarly to the static logic gate, CMOS in this case. For a dynamic operation of the gate (Dynamic mode), the *Clk* is enabled for toggling, providing two separate phases: pre-charge and evaluation. During the pre-charge phase, the output is charged to *VDD* in ``*Type A*'' gates and discharged to *GND* in ``*Type B*'' gates. During evaluation, the output is evaluated according to the values at the gate inputs, in a similar fashion to NORA/np- CMOS implementations. It was shown that DML gates have presented a very robust operation in both static and dynamic modes under process variations (PVT) and at low supply voltages. Dynamic mode robustness is mainly achieved by the intrinsic active restorer (pull-up in ``*Type A*'' and pull-down in ``*Type B*''). This restorer also allows sustaining glitches, charge leakage and charge sharing. Unique sizing of the DML gate transistors is the key factor for achieving low energy consumption in the static DML mode (in which the topology of the gate is identical to the static gate). This sizing is also responsible for reduction of all capacitances of the gate. In a similar way, the unique transistor sizing enables evaluation through a low resistive network achieving fast operation in the dynamic mode. An intuitive visualization of the tradeoff inherently related to DML is shown in Figure 1(e). Energy efficiency is achieved in the static DML mode at the expense of slower operation (Low Energy and Low Performance, left scales). However, the dynamic mode is characterized by high performance, albeit with increased energy consumption (High Energy and High Performance, right scales). These tradeoffs allow a very high level of flexibility at the system level, as will be shown

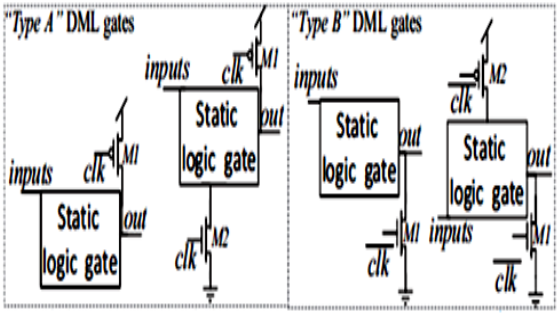


Fig 1 : (a) (b) (c) (d)

in Section III. Figure 1(f) and Figure 1(g) show the sizing of CMOS based DML gates in ``*Type A*" and ``*Type B*", respectively. These are optimized for dynamic operation. Figure 1(h) shows the conventional sizing of a standard CMOS gate where, *WMIN* is a minimal transistor width, β is the PUN to PDN inherent up-sizing factor and *f* is the gate's general up-sizing factor. As can be seen, the in and out capacitances of DML gates are significantly reduced, as compared to CMOS gates, due to the

utilization of minimal width transistors in the pull-of``*Type A''* or pull-down of ``*Type B''* networks

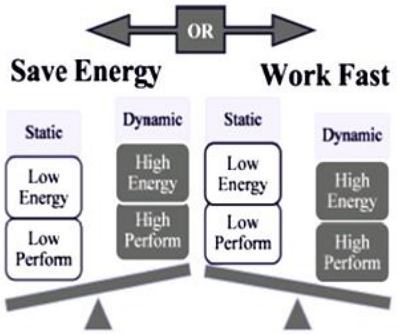


Fig 1: (e)

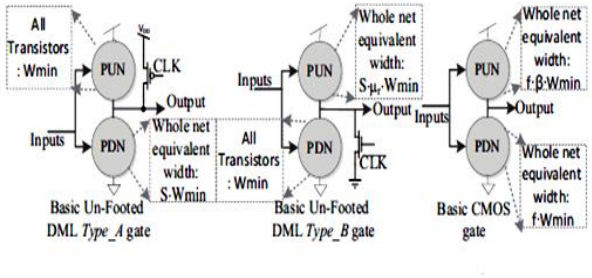


Fig 1: (f) (g) (h)

. The size of the pre-charge transistor is kept equal *S_WMIN* in order to maintain a fast pre-charge period, despite the output load upsized gate, where *S* is the evaluation network upsizing factor. Figure 1(b) and Figure 1(d) show the footed ``*Type A*" and the headed ``*Type B*" DML gates, respectively. It allows successful pre-charge for a cascaded topology of standard Static gates Synchronous devices to a DML logic. Many aspects of DML gates sizing, as well as preferred set of gates for ``*Type A*" and ``*Type B*" topologies, have been analyzed and discussed. Optimization for network up-sizing parameters for load driving was conducted using the Logical Effort (LE) method [3]. The DML key achievement is that while presenting very high performance in the dynamic mode by the proposed sizing, the same topology also enables improved energy efficiency in static mode, as compared to a conventional CMOS.

B. STATIC DML AS A SEMI-ENERGY OPTIMAL CMOS

Design space of a CMOS gate is mainly influenced by *VTH* ,transistor width, *VDD*, channel length, oxide thickness and body voltage. The influence of those parameters on E-D plain-optimization is being explored. For the CMOS family, the symmetry of the gate (*i*:*e*: equal rise and fall times) is highly important. This is due to the fact that in a combinational system there is always some uncertainty regarding the transition type. As a result, the pull-up network (PUN) of CMOS gates, which is constructed by low mobility PMOS devices, is sized up by the β parameter. When optimizing a CMOS gate's energy at the expense of its performance, the transistor's width is the main parameter used for reducing the energy consumption. This is due to several facts:(1) Switching energy is proportionate to the load and quadratic dependent on *VDD*. Under energy optimization, the symmetry of the gates' performance does not constitute a constraint so the transistor's width can be reduced, as well as β This significantly lowers the load capacitances. (2) With circuit's *VDD* lowering and technology scaling, leakage energy has become one of the key factors for static power dissipation. The leakage energy is caused by the numerous leakage currents of a device.

The main leakage currents are the sub-threshold and gate leakage currents. These currents are linearly dependent on the transistor's width And under energy optimization they are considerably reduced. CMOS based DML operated in static mode with transistor sizes optimized for the dynamic mode is *de facto* a semi-energy-optimal CMOS structure with an additional negligible output capacitance for the *Clk* transistors (transistors M1 and M2). Static DML is still highly robust due to its complementary nature and withstands aggressive voltage scaling. This methodology can also be referred to as a stand-alone technique for reducing the energy consumption of digital circuits. The E-D tradeoff

space under this approach is very wide and in this paper the discussion is limited only to transistors sizing, as shown in Figure 1(f) and Figure 1(g) for DML gates.

III. CP-DML APPROACHES FOR ENERGY EFFICIENCY AND HIGH PERFORMANCE

This section elaborates the proposed design approaches for energy efficient and high performance design of combinatorial systems. Sub-Section A presents an approach which utilizes DML gates in the dynamic mode on the CPs in order to improve their delays. Sub-Section B elaborates various aspects of energy reduction of all non-CP portions of the design.

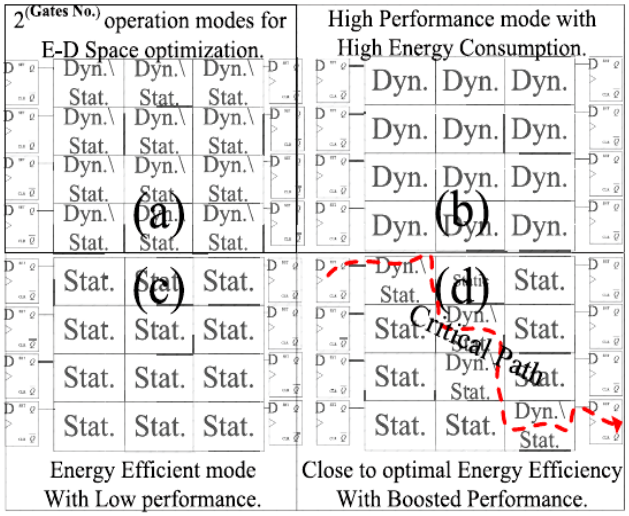


FIGURE 2. (a) DML design optional operation modes (b) DML design degenerated to the dynamic mode (c) DML design degenerated to the static mode (d) DML design where only the CP's are dynamically operated while the rest of the design operate in the low energy static mode. Where, Dyn. And Stat. stands for Dynamic and Static respectively

Theoretically, a general DML design can be controlled (input signal-driven control or external signal-driven control) to operate each gate in one of two modes: Static and Dynamic. This means that a general design can be operated in 2(*Gates Number*) different options, each one leading to a different operating point on the E-D space of the design. Figure 2(a) visualizes this modularity. The degenerated approaches for operating all the gates in one of the two modes, similar to a sole gate, are shown in Figures 2(b) and 2(c). Switching between these two modes leads to the distinct tradeoff, meaning that the design optimized either to achieve maximum performance or minimum energy consumption.

A.SOLVING CPs TIMING VIOLATIONS

As discussed in Section I, the CPs of a design are automatically identified using standard design flow tools. By replacing only these paths with DML gates and applying the dynamic mode on these paths, their delay can be reduced. The rest of the design is implemented using standard CMOS static logic. Of course, special design constraints should be enforced in all the intersections between a static path and a dynamic one. In some of these cases, a footer and header should be applied. Figure 2(d) presents a design in which the CPs were located and *only those paths* were given the option to toggle between dynamic and static mode, according to the system requirements. If the system design can withstand slower operation, the CP logic will operate in static mode. If the system is required to meet the defined *Clk* period for all cycles, the CPs will operate in the dynamic mode. Such application can be a smart phone that operates with two frequencies: slow one for power save/ hibernating mode and a fast one for video streaming. To emphasize, low complexity systems will normally bear only one frequency for operation and therefore the CPs will constantly operate in the dynamic

mode. Normally, the amount of gates on the CP is small as compared to the total amount of gates in the design. Therefore, in most cases, the inherent dynamic-operation energy of these CPs will lead to a non-significant increase in total energy consumption of the design.

B. SOLVING THE CPs TIMING VIOLATION WHILE REDUCING THE TOTAL ENERGY CONSUMPTION

As described in the previous Sub-Section, the CPs are mapped and operated in the dynamic DML mode. In Sub-Section A,the rest of the circuit was assumed to keep a standard CMOS logic gates topology. Therefore, the design was proposed to solve the CPs' timing constraints at the expense of a small degradation in energy consumption, as compared to a complete CMOS design. In this Sub-Section, all portions of the design, which are not a part of the CPs, will be mapped to static mode DML gates (similar to semi-energy optimized CMOS gates, described in section II). In most designs, these non-CPs are not time constrained and therefore the asymmetry behavior of their transitions and consequently their performance degradation will withstand the *Clk* period. The use of the static DML mode for the mass majority of gates in the design will lead to a signi ficant reduction in the total dynamic and static energy consumption. Figure 3 visualizes this approach.

IV. MODULAR BENCHMARK

This section, presents the chosen benchmarks. As depicted in Section III we will discuss three designs:

1) A CPs accelerator, as described in Sub-Section III(A), which has 2 operation modes:

_ ``DML Carry Path-Dynamic"- The DML CPs are activated in the dynamic mode.

_ ``DML Carry Path-Static"- The DML CPs are activated in the static mode.

In both of these modes the rest of the non-CPs portions of the system are designed with standard CMOS.

2) A CPs accelerator with low energy consuming non-CPs, as described in Sub-Section III(B), which has 2 operation modes:

_ ``DML Carry Path-Dynamic.With low energy non-CPs-tatic" - The DML CPs are activated in the dynamic mode, while the rest of the system operates in the DML static mode.

_ ``DML Carry Path- Static. With low energy non-CPs- Static" - The DML CPs are activated in the DML static mode, similar to the rest of the system.

3) CMOS equivalent design.

A Carry Skip Adder (CSA, also called carry bypass adder),was chosen as a benchmark to demonstrate and evaluate the proposed concept. The CP of the CSA increases as a function of the number of inputs, making it possible to examine the E-D trends as a function of the CPs lengths. It is important to note that the proposed methods can apply over any combinatorial circuits and a CSA was chosen only due to its modularity and simplicity.

A. CMOS CSA DESIGN

A conventional CSA is composed of a set of Ripple Carry Adder (RCA) blocks. They essentially utilize the carry propagation in order to skip the carry from one RCA to the next RCA block. It is possible to predict the propagation of the carry by a simple XOR gate. Such prediction mechanism can substantially reduce the delay. The CP in CSA occurs when the carry ripples at the first block, and then skips the rest of the blocks and then ripples again at the last block.This is the longest possible route in the CSA. *Lehman et al.*have researched CSAs with non-uniform sized distributed RCA blocks [20]. *Majerski* has presented a multi-level of carry-skip propagation architecture. *Guyot et al.* and *Oklobdzija et al.* proposed algorithms for choosing optimized block sizes. In this paper, a simple CMOS CSA design with a fixed size of 4-bits blocks was designed, as shown in Figure 4. Clearly, the methods presented in this paper can be generalized to any CSA block size constant or variable and for multi or single level carry path. A general single-bit Full Adder (FA) equations are:

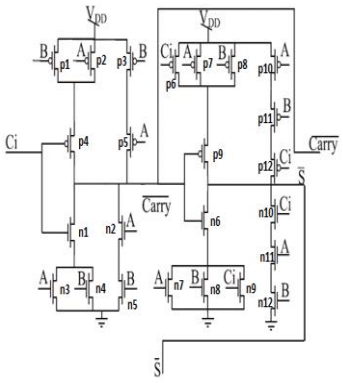


Figure 3. Full Adder

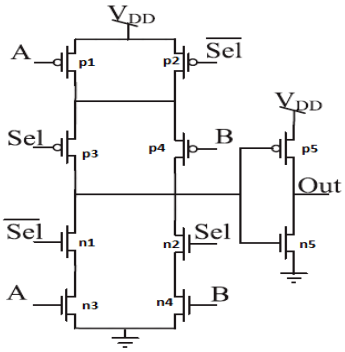


Figure 4. Multiplexer

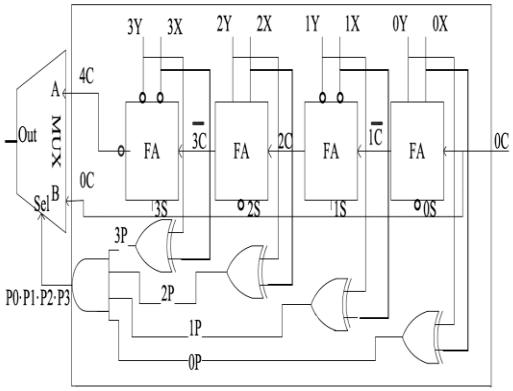


Figure 5**.** Ripple Carry Adder Block

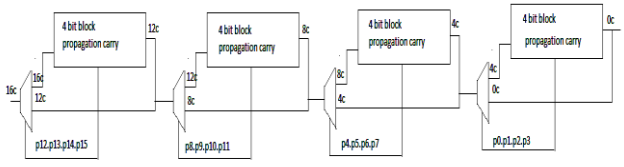


Figure 6. Carry Skip Adder Block

B. DML CRITICAL PATH DESIGN

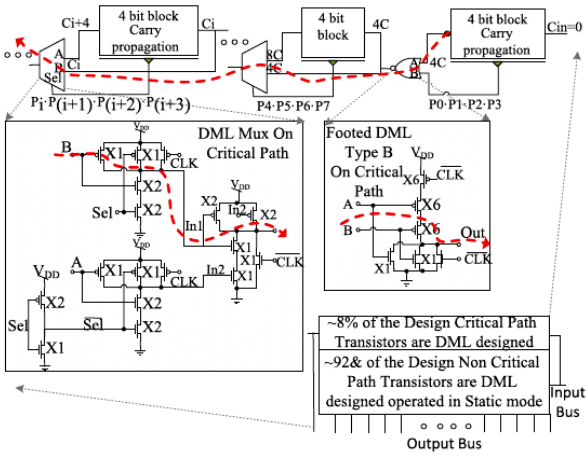


Figure **7.** DML Critical Path Design

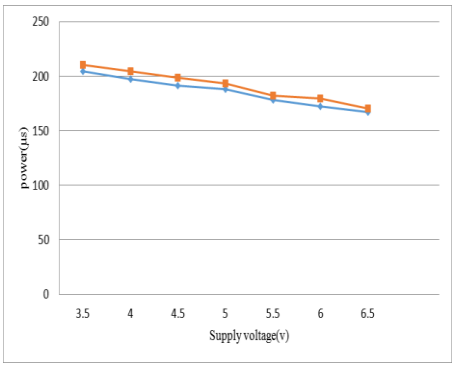
Selected CSA

Figure 7 shows the DML implementation of the CSA's CP.The CP _ows through the _rst NOR (assuming that the carry in of the whole design is 0) and through all the MUXs of the design. The gate level implementation of the CP can be constructed with various topologies of DML: DML NOR gates are most efficiently implemented in the ``*Type A*'' topologies and NAND gates in ``*Type B*'',. The Boolean logic does not allow an ef_cient implementation of a MUX with a NOR following a NAND or vice-versa, which is the preferred topology for DML logic design.Therefore, in the chosen topology, the CP is composed only of NANDs (where one of them is implemented using efficient ``*Type B*'' and the other one has a less optimal ``*Type A*'' structure). The last inverter in each RCA block is a headed ``*Type B*'' inverter, which maintains correct Pre-Charge phase for the CP. The sizes of the transistors in terms of minimal transistor width are shown in Figure 7. In the design, implemented in such way, only 8% of transistors will (optionally) operate dynamically, while the remaining 92% of the transistors are kept at the low energy static mode. This modular design keeps the same complexity and the same dynamic-to-static-gates ratio, as a function of the input vector's length, *N* [bits].

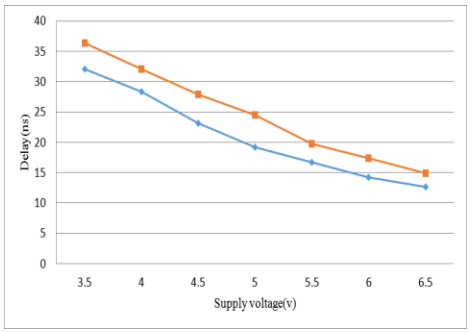
V. SIMULATION RESULTS

The modular benchmarks circuits, described in the previous section were simulated in a standard 180nm CMOS process, using the Mentor Graphics. Implementations of these methods on the benchmark CSAs were mainly examined over the E-D plain and as a function of the operating voltage and the CP's length. Note, the naming convention for the different designs and operating modes is elaborated in the preface of Section III. All energy and delay measurements are per-operation.

POWER COMPARISON AT DIFFERENT APPLIED VOLTAGE



DELAY COMPARISON AT DIFFERENT APPLIED VOLTAGE



VI. CONCLUSION

CP timing violation and energy minimization are important issues in all digital circuits. The invaluable possibilities, inherent to design with DML gates, leverage the flexibility of the design to meet CP timing along with reducing the total energy consumed by the circuit, as shown in this paper. Until now, meeting the CP timing was closely related to a rise in the consumed energy by conventional methods. In this work this paradigm is contradicted - both timing and low energy consumption requirements are met. We showed that the performance of the 180nm CSA benchmark circuit was improved by X2, while also achieving reduction of energy consumption of X2.5. Since the CSA circuit is not optimal for DML implementations, it is expected that these improvements will be even more significant for other designs.

VII. REFERENCES

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Bio-Electronic Approach for Various Adders Circuit Design

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***Abstract*— The DNA molecule is indubitably the most powerful medium known for DNA's ability to code, store information as a means of data storage. But till now, DNA molecule has found little use in computing applications. For initiating computing application with DNA molecule, it requires to design DNA transistors which can be utilized to design basic gates to implement Boolean logic. Interestingly some recent researches have shown that it's very much possible to design a three terminal transistor like device architecture by controlling the flow of RNA polymerase along DNA with specific integrases. Along with that, very recently, fundamental experimental designs for realizing various basic Boolean logic functions have been demonstrated successfully with DNA molecule. Till now the experimental design was in multi strand fashion. Present work adopted, modified and extended such DNA logic gate concept to execute design, simulation and performance analysis of various adder circuits in a single strand fashion. Adders are one of the most widely digital components in the digital integrated circuit design and necessary part of Digital Signal Processing. In this work the design of various adders such as Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder and Carry Select Adder are discussed and are compared on the basis of their performance parameters such as delay and the calculation of error percentage.**

Keywords*— DNA, RNA, Transistors, Logic Gates, Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Skip Adder, Carry Select Adder.

I. INTRODUCTION

The world of electronics starts with a material called "semiconductor" which can be induced to conduct or stop the flow of electrons or holes. Si has been the dominant electronics material since the latter half of the 20th century. It must be clear that the successful development of Si devices took years and decades. In conventional electronic circuits transistors are implemented to process, store and transfer signal or data with the flow of electrons or holes. Where as two or more transistors together form a logic gate, which allows a computer to manage mathematical operations. From the beginning to till date, the main aim of the electronics industry is to produce more powerful chips. In that process, designers have scale transistors in size to produce smaller, faster, power efficient chip at lower price [1]. The net result of this transistor scaling action is because the transistor to reach the physical, technical and economic limits. And also that has produced small, faster chips, beyond a certain limit, the number of silicon atoms in the insulating layer of a transistor is no longer sufficient to prevent the leakage of electron that causes the circuit to shorten [1]. In order to overcome these limitations the scientists and technologists are looking for new materials, innovative structures and revolutionary ideas to realize reliable transistor like action in such tiny space [2]. Most novel materials available today are at the first step, where researchers are trying to understand their properties and characteristics of transistors fabricated using them.

Presently throughout the world several groups of scientists, researches and technologists are trying to store, retrieve and process signals using bio-chemical reactions with newer biological materials [3-5]. In such context, with research it has been proven that, the blueprint for life DNA, can also become the templates for making a new generation of transistors, logic gates and subsequent computer chips [6]. In last decade lots of research articles have been reported on experimental realization of transistor like action and logic operation with DNAs [7-9]. Recently, Drew Endy et. al. at Stanford University in California have designed a transistor like device that controls the movement of an enzyme called RNA polymerase along a strand of DNA with bacteriophage serine integrases [10]. They have also experimentally created logic gates that allow both information storage and logical operations with multiple transcriptors [10]. Such remarkable break through can be utilized to realize biochip and subsequent biological computers which can be used to study and reprogram the living systems, monitor environments and improve cellular therapeutics [9-10]. Till now most of the research activities related to DNA logic gate realization are concentrated into intense experimental activities. But, along with such experimental ventures theoretical simulation is also important to understand the operation and functionality of higher order circuits with such DNA based logic gates. Arithmetic unit are the essential blocks of digital systems such as Digital Signal Processor, microprocessors, micro controllers and other data processing units. In many arithmetic applications and other kinds of applications, adders are not only used in the arithmetic logic unit but also used in other parts of processors. In general, addition is a process which involves two numbers which are added and carry will be generated. All complex adder architectures constructed from its basic building blocks such as Half Adder (HA), Multiplexer circuit and Full Adder(FA). Under the present work, based on DNA logic gates, the design, simulation and performance

analysis of various adder circuits has been logically realized with MATLAB Simulink and also the performance parameters of various adders are compared. The input and summed output for the DNA logic based adder circuits has been simulated and verified with timing diagrams. Such simulation work will not only justify the applicability of such DNA logic gates in complex circuit realization, it will also lead a step forward towards practical implementation of Bio-computers. Same time extension of present research with the development of proper mathematical model of DNA transistor will initiate the development of circuit simulator with DNA logic gates.

II. DNA GATE LOGICAL MODELING

The RNA polymerase is an enzyme that also known as DNA dependent RNA polymerase and it produces primary transcript RNA chains using DNA genes as templates, a process called transcription [11].This produced primary transcript RNA can be reconfigured with a transistor like three terminal device model which can be named as transcriptor[10] The RNA synthesis follows after the attachment of RNA polymerase to a specific site, "promoter", on the template DNA strand and the synthesis process continues until a termination sequence ("terminator") is reached [12]. The flow of RNA polymerase along DNA strands between input and output induces an current called transcriptional current. The gate like control will be realized with independent chemical control signals (defined as "integrase") which will regulate the flow of RNA polymerase to realize Boolean logic operation fig. 1 [10].

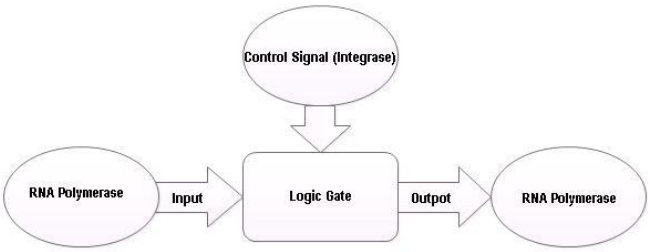

Fig. 1. Schematic for equivalent logic representation

As shown in the fig. 2, the logic element will use asymmetric transcription terminators as reversible check valves. A transcription terminator will be accommodating two opposing DNA recombination sites named as Transcription Elements (TEs, represented with dark green and dark blue solid triangles) which will normally disrupt RNA polymerase flow. The input integrase which is recombinases (genetic recombination enzymes) will catalyze unidirectional inversion of DNA within opposing recombination sites [10]. This will modify TEs (represented with partially dark green-blue and partially dark blue-green solid triangles) and invert of the transcription terminator to provide of DNA recombination sites and will allow RNA polymerase flow. Every opposing recombination sites (TEs) will be recognized by independent integrases which will provide independent control over the orientation or presence of one or more terminators.

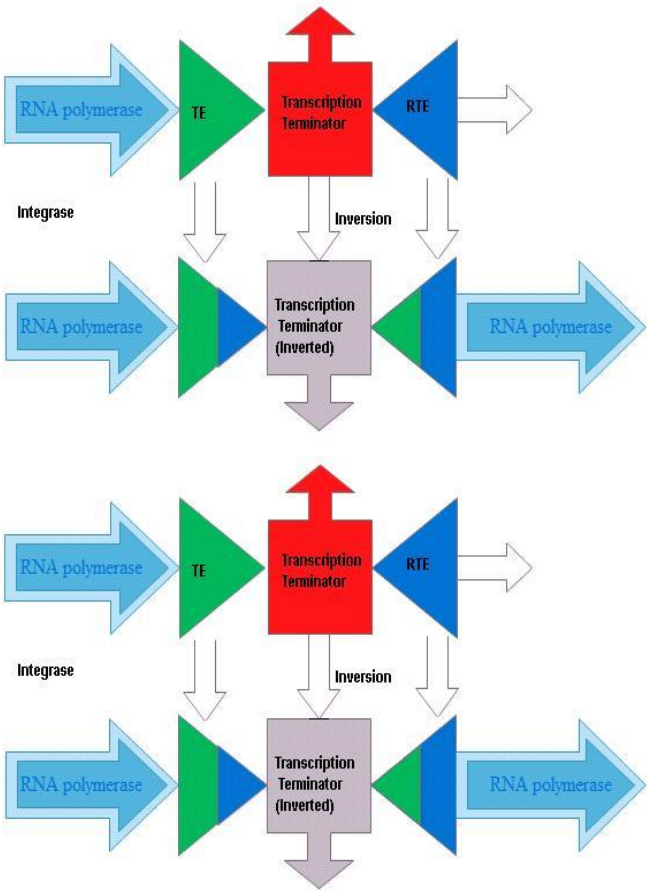

Fig. 2. Logic control of RNA polymerase flow with integrase. Symbols: TE: Transcription Elements, RTE: Recombination sites for TE

Under the present work, various adder circuits built with basic unit devices (Full adders, Half adders, NAND and AND logic gates), has been designed [13].

So to realize a Adder circuit with DNA logic, the DNA NAND gate has to be designed first. Since NAND gate is a universal gate, it can be used for realizing all the basic gates such as AND, OR and NOT. Then with help of NAND gate the half adder[13] and full adder circuits can be designed.

A. Implementing NAND Logic

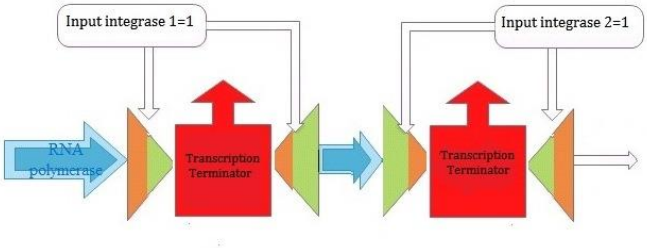

Fig.3. Schematic for logical representation of NAND showing blocked transcription with presence of both the integrases.

A transcriptor NAND logic element requires two asymmetric transcription terminators with two pairs of

opposing recombination sites (Transcription Elements) associated with each transcription terminator, as shown in Fig. 3. The transcription current will not flow when both the integrases are present but the transcription current will flow if at least one integrase is present or no integrase is present as shown in fig 4.

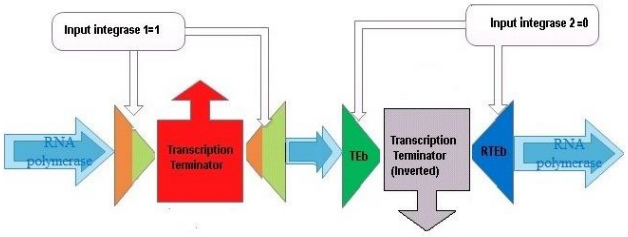

Fig.4. Schematic for logical representation of NAND showing the flow of transcription current with presence of integrase 1 and absence of integrase 2.

B. *Implementing OR Logic*

A transcriptor OR logic element requires only one asymmetric transcription terminator with two pairs of opposing recombination sites (Transcription Elements) associated with transcription terminator. The transcription current will flow if any one of the integrases will present but no transcription current flow when only both the integrase is absent as shown in fig 5.

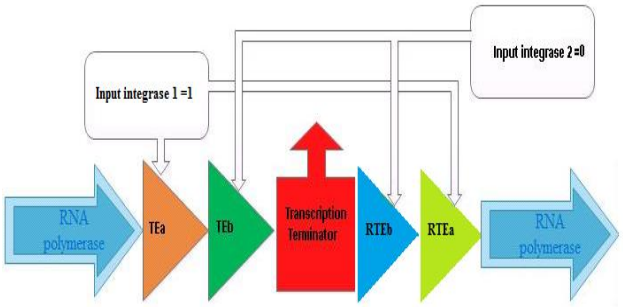

Fig. 5. Schematic for logical DNA OR showing transcription continuation with presence of integrase 1 (=1).

With further extension of this concept, other Boolean logics like AND, OR, NOR, NOT can be also implemented with DNA logic [9-10].

III. ADDERS

The design of various adders such as Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSlA) are discussed below.

A. *Ripple Carry Adder*

Ripple carry adder is a basic adder which works on basic addition principle. The Simulink model of RCA is shown below.

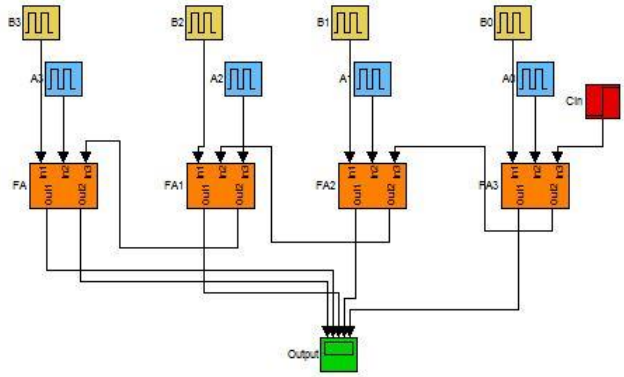

Fig.6. Simulink block diagram of Ripple carry adder (RCA) circuit.

RCA contains series structure of full adders (FA), where each full adder is used to add two bits along with carry bit. The carry generated from each full adder is given to next full adder and so on. Hence, the carry is propagated in a serial manner.

B. *Carry Look Ahead Adder*

Carry look ahead design is based on the principle of looking at lower adder bits of argument and addend if higher orders carry generated. The Simulink model of CLA circuit is shown below.

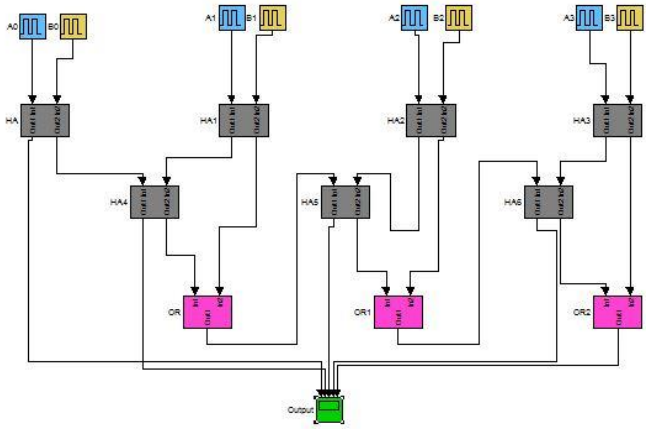

Fig.7. Simulink block diagram of Carry look ahead adder (CLA) circuit.

C. *Carry Save Adder*

In carry save adder (CSA) the carry is not propagated through the stages. Instead, carry is stored in present stage, and updated as attend value in next stage. The Simulink model of CSA is shown below.

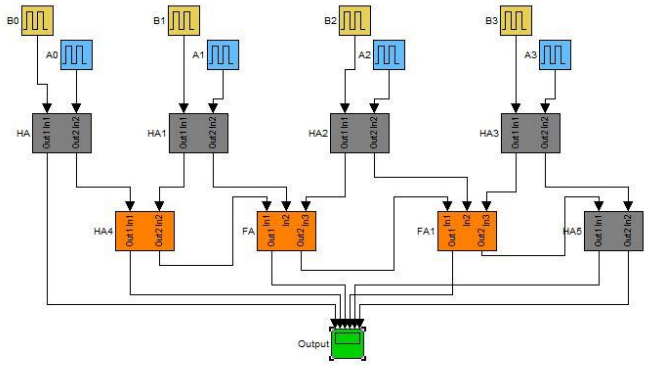

Fig.8. Simulink block diagram of Carry save adder (CSA) circuit.

D. Carry Select Adder

Carry select adder (CSlA) circuit architecture consists of independent generation of sum and carry i.e Cin=1 and Cin=0 are executed parallelly. Depending upon Cin , the external multiplexers select the carry to be propagated to next stage. Further, based on the carry input, the sum will be selected. The Simulink model of CSlA is shown below.

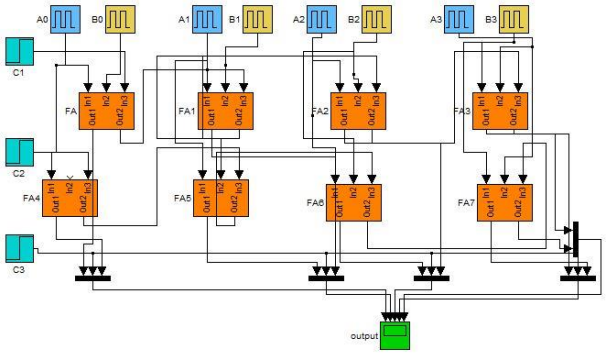

Fig.9. Simulink block diagram of Carry select adder (CSlA) circuit.

IV. Results and Comparison

Under the present work, the various types of adder circuits has been logically design and implemented with MATLAB Simulink and the timing diagram for input and output has been successfully simulated. The Simulink block diagram of the respective adder circuits has been presented in the early section. Were the RNA polymerase has been considered as one of the input signal inside each full adder block and two integrase a, b of 4 bit binary will from the logic inputs for the adder circuits.

To implement the various adder circuits in Simulink user defined function block has been selected from library and every block is fitted with logical function to replicate transcriptor and transcription elements. Whereas the pulse source of variable widths have been considered for replicating integrase a, b and a unit step function has been selected to replicate RNA polymerase input inside the full adder and half adder block.

Where in the above Simulink model pink color block represent the OR logic, grey block for half adder logic, orange block for full adder logic, black color block for multiplexer logic. The top side represents the input section. Cyan color block for input carry logic, light blue for integrase a (a0,a1,a2 and a3) and yellow for integrase b (b0,b1,b2 and b3).

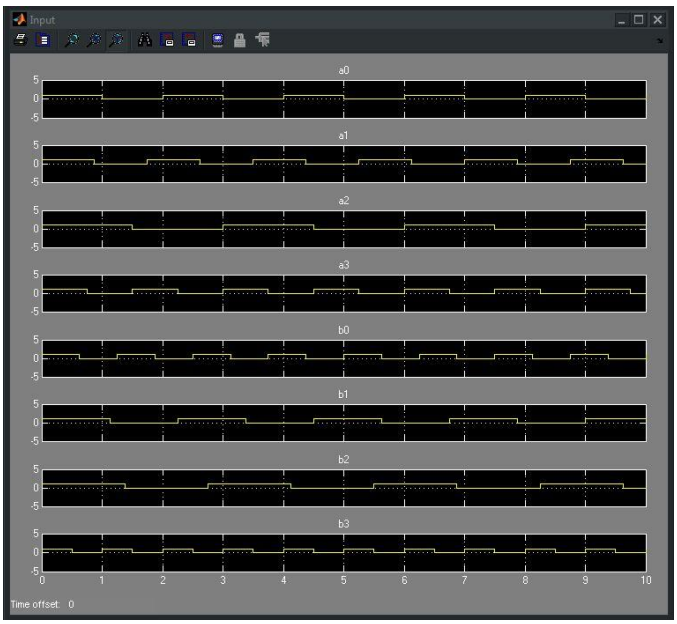

Fig. 10. With time the integrase a0,a1,a2,a3,b0,b1,b2,b3 and RNA given as top to bottom.

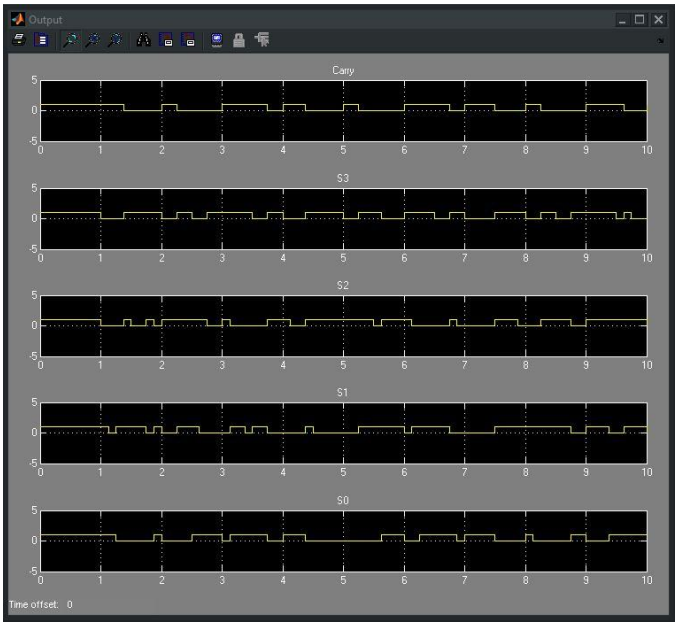

Fig. 11. With time the carry,s3,s2,s1 and s0 sum output are shown from top to bottom.

The performances of adder topologies are discussed for robustness against delay and error percentage. They are

selected for this work since they have been commonly used in many applications. Addition is a crucial operation for any high speed digital systems, digital signal processing or control systems. Therefore appropriate choice of adder topologies is an essential importance in the design of VLSI integrated circuits for high speed and high performance CMOS circuits.

TABLE I

Time unit	Integrase a (a3 a2 a1 a0)	Integrase b (b3 b2 b1 b0)	Output sum (carry s3 s2 s1 s0)
2	1001	1011	10100
4	1011	1111	11010

Fig.12. Truth table for 4 bit adder circuit

TABLE II

Time unit	Integrase a (a3 a2 a1 a0)	Integrase b (b3 b2 b1 b0)	output (c s3 s2 s1 s0)	Adders	Time unit	Sum (error in %)				
						C	S3	S2	S1	S0
2	0→1, 0→0 0→0,1→1	0→1, 0→1 0→0, 0→1	10100	RAC	2	15	-	7	15	-
					4	15	7	15	7	-
				CLA	2	15	-	10	15	15
					4	15	7	15	10	15
4	0→1, 1→1 0→0, 1→1	0→1,0→1 1→1,0→1	11010	CSA	2	10	-	7	15	15
					4	10	-	-	10	15
				CSLA	2	15	-	15	-	-
					4	15	15	-	15	-

Fig. 13. Error percentage table for various adder circuits

TABLE III

Sl no.	Type of adders	OR	HA	FA	MUX	Delay
1	RCA			4		6hr
2	CLA	3	7			5hr 45min
3	CSA		5	3		8hr 15min
4	CSla			8	5	12hr

Fig.14. Delay table for various adder circuits.

The summed output of the simulated adder circuits has been also verified with truth table (Table I). A single cell may produce discontinuous responses to small changes in control signals which can be corrected with Population Measurements with n-number of cells. A digitization error rate can be defined as the combined probability of producing false high or low outputs in response to intermediate control signal changes. Based on the experimental analysis presented by Jerome Bonnet et.al.; the approximated digitization error percentage for AND gate is 10% for 1→0 and 0→1 input change, 8% for 0→1 and 0→1 input change etc[10]. Whereas for Half adder the approximated digitization error percentage for sum is 7% for 1→0 and 0→1 input change, 15% for 0→1 and 0→1 input change etc[13]. Based on those experimental results, the digitization error percentages have been calculated for the full adder and multiplexer design and finally calculated the error percentage for the proposed various adder circuit design presented in Table. II.

Based on the experimental analysis presented by Jerome Bonnet et.al; they also assayed recombination response times, finding that 15-min control-signal pulses were sufficient to activate integrase-mediated switching. So the each and every gates present in the circuit require 15 min for their switching. For the half adder the switching time is 15.Whereas in the full adder and the multiplexer the time required is about 45 min. From the delay given in Table III, it is observed that the maximum propagation delay requires for Carry select adder and next come for the Carry skip adder. The least propagation delay is for Carry look ahead adder and gate count also shown in the Table III.

V. CONCLUSION

Under the present work the DNA logic gate design concepts has been theoretically investigated in detail. The logical design concepts of NAND gate have been implemented with proper understanding and explanations. Finally 4 bit various adder circuits has been logically designed with DNA based NAND gate, Half adder, Full adder and multiplexer circuit with MATLAB Simulink model. The timing diagrams for the added output, logic inputs and RNA input signal are simulated. The digitization error in percentage has also been approximated and presented for different input combinations for adder circuit. And also compared the propagation delay for various adder circuits is calculated and presented for possible paths between the inputs to the output. Such block level design of DNA based adder circuits will provide valuable understanding about the DNA based logic circuit design. Not only that such block level design can be added with proper mathematical model of DNA transistor which will initiate the development of future bioelectronics circuit simulators.

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Genetic Algorithm based Fractional Order PID Control for Temperature Control Plant

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Abstract:

With the continuous innovation and to control the temperature produced by appliances to help the energy consumption. The energy demand and control motor temperature, speed, positions along with the congested transmission systems, fractional order PID[1] is suggested as the best solution So many methods are involved to control temperature but sometimes they fail because of increased temperature. Temperature sensors are used many appliances but due to this failure sometimes accidents happen. To overcome this issue we introduced fractional order PID controller to control the temperature [2] before attending the cutoff level. To design the fractional order PID controller [1] using a genetic algorithm to get better value for the fractional orders of the corresponding systems.

Key words: FOPID, GA Tuning, Temperature control system

INTRODUCITON

The FO-PID [1] control has a fractional integral and a differential elements in which these orders are non-integral. Generally, as the physical plant has a fractional characteristic, it is expected that the fractional controller will be effective for actual plants. There are some advantages of fractional control scheme, it was reported that PI$^{\alpha}$D control system has a robust characteristics for the input saturation.

Implementation of FOPID [1] finite order approximation is required, fractional elements have infinite order. There have been various researches for approximation of fractional elements by the finite order filter. The SMP (short memory principle) method is effective in terms of implementation and approximation accuracy. The SMP method gives the discrete approximation of the fractional element and provides the better approximation accuracy than other digital methods. The binomial coefficients at the beginning were reduced as time advances. The integral and differential are approximated using the data during recent interval. The output error remains in steady state as the FOPID approximated by SMP. To eliminate the steady state error, divide the fractional integral into traditional integral s^{-1} , it is called distributed implementation.

1. The implementation method of fractional order integration, which has the integration characteristics in low frequency is examined.
2. Approximation accuracy using SMP is evaluated.

TYPES OF FRACTIONAL ORDER CONTROLLER:-

Historically there are four major types of fractional order controllers [1],

- CRONE Controller.
- Tilted Proportional and Integral(TID) Controller.
- Fractional Order PID (FOPID) Controller.
- Fractional Order Lead-Lag Compensator.

REASON FOR SELECTING FOPID:-

Most of the physical plant has a fractional characteristic, it's expected that the fractional controller will be effective for actual plants.

BLOCK DIAGRAM:-

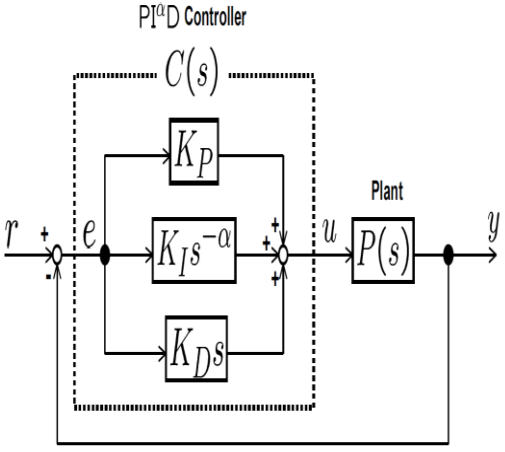


Fig. 1 BLOCK DIAGRAM OF PI$^{\alpha}$D CONTROLLER

PI$^{\alpha}$D controller one of the FOPID controllers with fractional integrator. In case α=1, the Controller is equivalent to the traditional PID controller. Advantages of the fractional Control scheme, it was reported that PI$^{\alpha}$D control system has robust characteristics for the saturation of the input.

Fractional order PID controller output is

$C_f(s) = K_p + K_i/s^{\lambda} + K_d s^{\mu}$

The FOPID [1]controller needs to design five parameters, K_p, K_I, K_d, λ, μ. The order λ and μ are not necessary to be integers , they will be any real numbers.

- Selecting λ=1, μ=1, a classical PID can be obtained.
- Selecting λ=1, μ=0, a PI^{λ} can be obtained.
- Selecting λ=0, μ=1, a PD^{μ} can be obtained.
- Selecting λ=0, μ=0, a gain can be obtained.

The $PI^{\lambda}D^{\mu}$-controller is more flexible and gives an opportunity to better adjust the dynamical properties of a fractional-order control system.

system transfer function [2]

P(s) = ((1)/(14994s^1.98+6009.5s^0.97+1.69)

FOPID α- APPROXIMATION TECHNIQUE:

A commonly used Three definition of the fractional calculus is the Riemann-Liouville definition[7],

$$aD_t^{\alpha} f(t) = \frac{1}{\tau(m-\alpha)}\left(\frac{d}{dt}\right)^m \left(\int_0^{\tau} \frac{f(\tau)}{(t-\tau)^{(1-(m-\alpha))}} d\tau\right)$$

$$ {}_aD_t^{\alpha} f(t) = \frac{1}{\Gamma(m-\alpha)}\left(\frac{\mathrm{d}}{\mathrm{d}t}\right)^m \left(\int_a \frac{f(\tau)}{(t-\tau)^{1-(m-\alpha)}} \mathrm{d}\tau \right.$$

An alternative definition, based on the concept of fractional differentiation, is the Grunwald-Letnikov definition given by [7],

$$ {}_aD_t^{\alpha} f(t) = \lim_{h\to 0} \frac{1}{\Gamma(\alpha)h^{\alpha}} \sum_{k=0}^{(t-\alpha)/h} \frac{\Gamma(\alpha+k)}{\Gamma(k+1)} f(t-kh)$$

Caputo fractional derivatives,

$$ {}_aD_t^{\alpha} f(t) = \frac{1}{\Gamma(n-\alpha)} \int_a^t \frac{f^{(n)}(\tau)}{(t-\tau)^{\alpha-n+1}} d\tau, \quad \text{for } n-1 < \alpha <$$

Most frequently referred definition, grunwald-letnikov definition. $S^{-\alpha}$ denotes the fractional integration operator.The operator means the integral in case that α< 0 and the differential in case that α > 0.

Oldham and Spanier (1974) [6]

$$\frac{d^q f(\beta x)}{dx^q} = \beta^q \frac{d^q f(\beta x)}{d(\beta x)^q}$$

K.S. Miller and B. Ross (1993**)** [6]**.**

$$D^{\alpha} f(t) = D^{\alpha_1} D^{\alpha_2} \ldots D^{\alpha_n} f(t)$$

$$\alpha = \alpha_1 + \alpha_2 + \ldots + \alpha_n$$

$$\alpha_i < 1$$

Kolwankar and Gangal (1994) [6].

$$\mathbf{D}^q f(y) = \lim_{x\to y} \frac{d^q\left(f(x) - f(y)\right)}{d(x-y)^q}$$

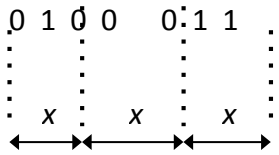
GENETIC ALGORITHMS (GA):

Most real world optimization problems involve complexities like discrete, continuous or mixed variables, multiple conflicting objectives, non-linearity, discontinuity and non-convex region. The search space (design space) may be so large that global optimum cannot be found in a reasonable time. The existing linear or nonlinear methods may not be efficient or computationally inexpensive for solving such problems. Various stochastic search methods like simulated annealing, evolutionary algorithms (EA) or hill climbing can be used in such situations. EAs have the advantage of being applicable to any combination of complexities (multi-objective, non-linearity etc) and also can be combined with any existing local search or other methods. Various techniques which make use of EA approach are Genetic Algorithms (GA), evolutionary programming, evolution strategy, learning classifier system etc. All these EA techniques operate mainly on a population search basis. In this lecture Genetic Algorithms, the most popular EA technique, is explained.

Concept

EAs start from a *population* of possible solutions (*called individuals*) and move towards the optimal one by applying the principle of Darwinian evolution theory i.e., *survival of the fittest*. Objects forming possible solution sets to the original problem is called *phenotype* and the encoding (representation) of the individuals in the EA is called *genotype*. The mapping of phenotype to genotype differs in each EA technique. In GA which is the most popular EA, the variables are represented as strings of numbers (normally binary). If each design variable is given a string of length '*l*', and there are *n* such variables, then the

design vector will have a total string length of *'nl'*.



An individual consists a genotype and a fitness function. *Fitness* represents the quality of the solution (normally called *fitness function*). It forms the basis for selecting the individuals and thereby facilitates improvements.A flowchart indicating the steps of a simple genetic algorithm is shown below.

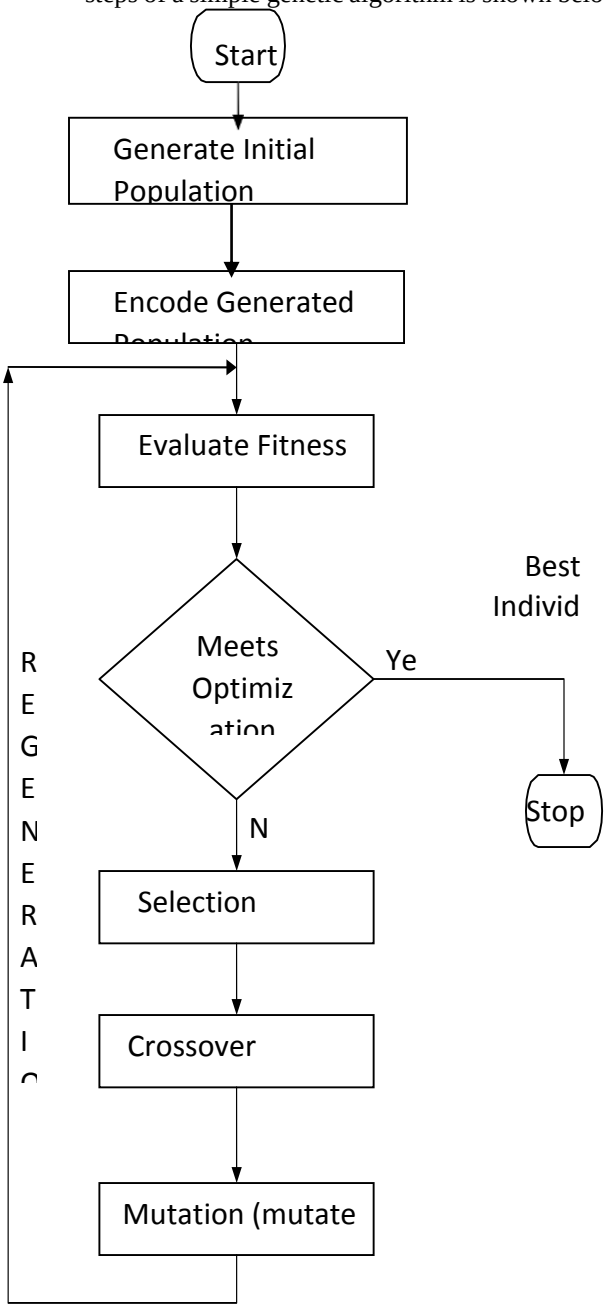


Fig 2 Flow chart for GA tuning algorithm

The pseudo code for a simple EA is given below

```
i = 0
initialize population p0
Evaluate initial population
While (! Terminate condition)
{
        i = i+1
        Perform competitive selection
        Create
        population
        P_i from P_i-1
        by
        recombinati
        on and
        mutation
        Evaluate
        population
        P_i
}
```

The initial population is usually generated randomly in all EAs. The termination condition may be a desired fitness function, maximum number of generations etc. In selection, individuals with better fitness functions from generation '*i*' are taken to generate individuals of '*i+1*'th generation. New population (*offspring*) is created by applying *recombination* and *mutation* to the selected individuals (*parents*). Recombination creates one or two new individuals by swaping (crossing over) the genome of a *parent* with another. Recombined individual is then *mutated* by changing a single element (genome) to create a new individual.

Finally, the new population is evaluated and the process is repeated. Each step is described in more detail below.

Parent Selection

After fitness function evaluation, individuals are distinguished based on their quality. According to Darwin's evolution theory the best ones should survive and create new offspring for the next generation. There are many methods to select the best chromosomes, for example roulette wheel selection, Boltzman selection, tournament selection, rank selection, steady state selection and others. Two of these are briefly described, namely, roulette wheel selection and rank selection:

Roulette Wheel Selection:

Parents are selected according to their fitness i.e., each individual is selected with a probability proportional to its fitness value. In other words, depending on the percentage contribution to the total population fitness, string is selected for mating to form the next generation. This way, weak solutions are eliminated and strong solutions survive to form the next generation. For example, consider a population containing four strings shown in the table below. Each string is formed by concatenating four substrings which represents variables a,b,c and d. Length of each string is taken as four bits. The first column represents the possible solution in binary form. The second column gives the fitness values of the decoded strings. The third column gives the percentage contribution of each string to the total fitness of the population. Then by "Roulette Wheel" method, the probability of candidate 1 being selected as a parent of the next generation is 28.09%. Similarly, the probability that the candidates 2, 3, 4 will be chosen for the next generation are 19.59, 12.89 and 39.43 respectively. These probabilities are represented on a pie chart, and then four numbers are randomly generated between 1 and 100. Then, the likeliness that the numbers generated would fall in the region of candidate 2 might be once, whereas for candidate 4 it might be twice and candidate 1 more than once and for candidate 3 it may not fall at all. Thus, the strings are chosen to form the parents of the next generation.

Rank Selection:

The previous type of selection may have problems when the fitnesses differ very much. For example, if the best chromosome fitness is 90% of the entire roulette wheel then the other chromosomes will have very few chances to be selected. Rank selection first ranks the population and then every chromosome receives fitness from this ranking. The worst will have fitness 1, second worst 2 etc. and the best will have fitness N (number of chromosomes in population). By this, all the chromosomes will have a chance to be selected. But this method can lead to slower convergence, because the best chromosomes may not differ much from the others.

Crossover

Selection alone cannot introduce any new individuals into the population, i.e., it cannot find new points in the search space. These are generated by genetically-inspired operators, of which the most well known are *crossover* and *mutation*.

Crossover can be of either one-point or two-point scheme. In one point crossover, selected pair of strings is cut at some random position and their segments are swapped to form new pair of strings. In two-point scheme, there will be two break points in the strings that are randomly chosen. At the break-point, the segments of the two strings are swapped so that

new set of strings are formed. For example, let us consider two 8-bit strings given by '10011101' and '10101011'.

Then according to one-point crossover, if a random crossover point is chosen after 3 bits from left and segments are cut as shown below:

100 | 11101

101 | 01011

Crossover is not usually applied to all pairs of individuals selected for mating. A random choice is made, where the probability of crossover being applied is typically between 0.6 and 0.9.

Mutation

Mutation is applied to each child individually after crossover. It randomly alters each gene with a small probability (generally not greater than 0.01). It injects a new genetic character into the hromosome by changing at random a bit in a string depending on the probability of mutation.

Optimization Methods: Advanced Topics in Optimization - Evolutionary Algorithms for

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is mutated as 10111**1**11

It is seen in the above example that the sixth bit '0' is changed to '1'. Thus, in mutation process, bits are changed from '1' to '0' or '0' to '1' at the randomly chosen position of randomly selected strings.

Real-coded GAs

As explained earlier, GAs work with a coding of variables i.e., with a discrete search space. GAs have also been developed to work directly with

continuous variables. In these cases, binary strings are not used. Instead, the variables are directly used. After the creation of population of random variables, a reproduction operator can be used to select good strings in the population.

Results

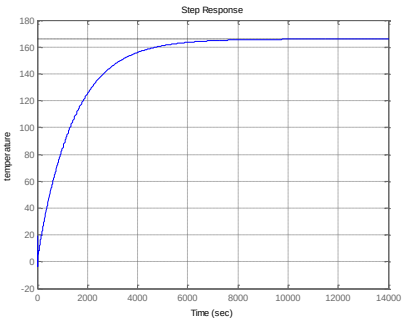

Fig 3 ZN FOPID based temperature system

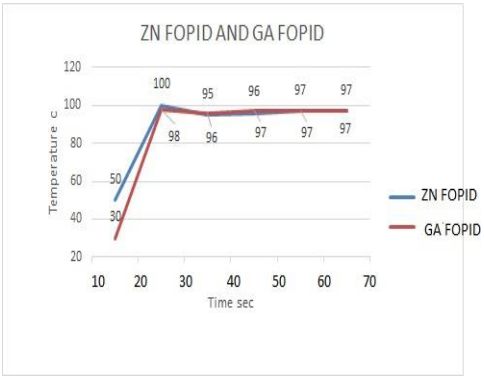

Fig 4 ZN FOPID and GAFOPID based temperature system

Conclusion:

Design and Implementation method of the fractional order PID controller for Fractional order process[2] in MATLAB simulation has been done and results are compared with ZN FOPID[1] controller. The settling time, rise time of the GA FOPID controller are better compared to that of ZN FOPID controller. In future try to find the better solution using new algorithms.

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About author

G.Sridhar received the **Ph.d** degree in electronics and instrumentation engineering from the SR university,India, in 2015, the **M.E.** degree in Control and Instrumentation from Anna University, Chennai, India, in 2012. He is currently working as a Professor in Department of ECE, Malla Reddy College of Engineering, Hyderabad. His research interests include communication and networks,wireless communication networks, Control systems, Fuzzy logic and Networks, **AI**, Sensor Networks.

Non-conventional Low Power Circuit Design Techniques

N. Raj, P. Anil Kumar, A.K. Singh and P. John Paul

***Abstract*— In this paper, few non-conventional circuit design techniques has been reviewed. The techniques discussed are widely used for realizing low power analog circuits by operating the circuits at low voltage. The discussed techniques are: Bulk Driven, Floating and Quasi-floating Gate followed by operation of Bulk Driven in Floating and Quasi-floating Gate mode. In all the approach, the threshold voltage restriction is removed from the input signal path. The adverse effect is reduced performances of MOSFET parameters compared to conventional gate driven MOSFET shown in this paper through simulations. The simulations are done with the help of HSpice simulator on 180nm technology.**

***Index Terms*-Bulk Driven, Floating gate, Quasi-floating gate, threshold, low power.**

I. Introduction

THE trend of CMOS technology scaling towards increasing density of components on chip and prolonging lifespan of battery powered portable and implantable medical devices has pushed the research to adopt hybrid techniques for realizing low voltage (LV) low power (LP) circuits. Though such techniques provide promising results but at the same time shows degraded characteristics [1, 2]. In modern technology era, especially for low voltage analog circuits the threshold voltage has been continuously an obstacle during design requirements. In this regard, the minimum supply voltage cannot be scaled below the threshold voltage of MOSFET. Few widely adopted low voltage (LV) low power (LP) techniques which have proved its potential are subthreshold (weak inversion) region [3], level shifter technique [4], Bulk Driven technique [5], Floating Gate (FG) structure [6], Quasi-floating Gate (QFG) structure [7, 8], and Bulk driven floating/quasi-floating Gate (BDFG/BDQFG) structure [9]. These LV LP techniques are categorized as non-conventional technique. Depending upon the desired performance parameter enhancement, the selection of technique is done. The main disadvantage of using these techniques is visible in low transconductance compared to gate driven (GD) MOSFET which results in low bandwidth analog circuits. The key features of FG and QFG MOST lies in terms weighted sum operation of multi input capacitive connection and makes the threshold scalable favouring low voltage operation. However, comparing the features of FG with QFG MOST, the QFG MOST gained potential interest. The main disadvantage with FG MOST is the initial charge trapping at FG node and also the DC convergence issue which is not the case with QFG MOST. Also the QFG MOST shows improved gain-bandwidth product and wide-band operation over FG MOST. Besides floating gate technology, another widely acceptable low power approach is using the BD MOST which has gained popularity due to simple structure. Also the technique best suits to medical devices since the biological signals are of low amplitude (in range of micro to milli volts) and low frequency range (fraction of a hertz to kilohertz) [10]. However, the poor body transconductance of BD MOST forces its application limited to low gain low frequency application. In this context, BDFG/BDQFG technique improved the frequency characteristics of BD MOST. These structures combine the features of BD with FG/QFG MOSFET [9] due to which transconductance is increased and also the frequency range. The paper is organised as follows. Section II covers the brief discussion on non-conventional circuit design techniques highlighting the important features. The supporting simulations for these techniques are shown in Section III followed by conclusion in Section IV.

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II. Low Power Circuit Design Techniques

In this section, the low voltage low power techniques namely: BD, FG, QFG, BDFG and BDQFG are included.

A. Bulk Driven (BD) MOSFET

The conventional MOS transistor (MOST) is a four terminal device, i.e. drain (D), gate (G), source (S) and bulk (B) whose fourth terminal, the bulk is usually connected either negative/positive supply for N-channel/P-channel transistor, respectively, or to their respective source terminal. But by using the bulk-terminal as a signal input instead of connecting it to any of the supply voltage or source terminal, the threshold voltage limitation can be removed. The BD MOST based circuit was first reported in [11]. The working of BD is similar to that of junction field effect transistor (JFET). Moreover, since the BD MOST acts as a depletion type device, it can be operated under negative, zero, or even slightly positive biasing conditions [12]. As in GD MOST, the gate-to-source voltage controls the drain current likewise in BD MOST threshold voltage becomes the function of the bulk-to-source voltage

which controls the drain current. The DC bias voltage at gate terminal forms the conduction channel of MOSFET which makes the input pathway free from threshold and the input signal applied at bulk is able to modulate the drain-to-source current even with very low ampitude of signal. Using BD, the circuits can be easily realized for sub-volt supplies. The most significant drawback related to the BD is its small body transconductance (g_{mb}) which is 3 to 5 times smaller than gate transconductance (g_m) and poor transition frequency (f_T) [13]. Despite of this drawback, BD has gained its potential interest by battery-powered medical devices. Since bio-signals are small in amplitude and have low frequency range in KHz, the low value of g_{mb} of BD helped to realize Gm-C low pass filter for bio-signal processing [14]. The literature survey has shown that most of the recent research articles are based on BD [15, 16] where by using appropriate circuit design techniques the BD MOST drawbacks have been alleviated. The symbol of GD and BD NMOST are shown in Fig. 1(a) and (b) respectively.

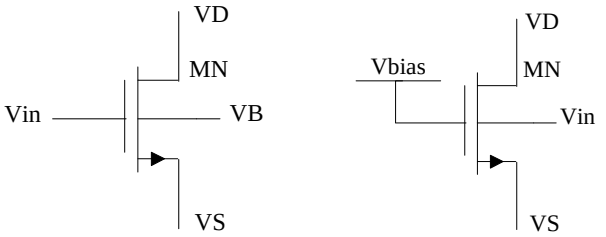

Fig. 1 Symbol of N-channel: (a) GD MOST; (b) BD MOST

Unlike the GD technique the input V_{in} is fed to the bulk terminal and a constant DC bias voltage V_{bias} is applied at the gate terminal. The overall advantage and disadvantage using BD MOST is summarized as follows:

Advantage:

- Input pathway free from threshold voltage
- Wide input common mode range
- Rail-to-rail operation
- Less complex

Disadvantages:

- Poor transconductance
- Isolated bulk require special Process
- Poor frequency response
- Degraded Latch up Immunity

B. Floating Gate (FG) MOSFET

The very first application of FG MOST was used to store data in EPROM, EEPROM and flash memories [17]. During the last decades, a number of different applications have revealed its applicability in many other different fields besides its programmability feature. The best use of FGMOS has been found for tuning in analog CMOS amplifiers to achieve high linearity and also remove offset errors which occur due to device mismatch [18]. Based on FG MOST, various articles have been reported in literature focused on realizing low voltage low power circuits [19-21]. The input capacitor in FGMOS transistors creates a capacitor divider network which causes the input signal to attenuate and hence increases the linearity.

Unlike the conventional GD MOST, the FG MOST has its gate electrically isolated from inputs, i.e. gate in floating state such that there are no resistive connections to its inputs. The FG is fabricated using the gate electrode (poly1) layer completely surrounded by two SiO2 insulator layers (upper and lower) and thus get electrically isolated from the rest of the device contacts. The inputs are then deposited on top of upper SiO2 layer and fabricated using a second layer of polysilicon (poly2). This creates a capacitive connection between the FG and actual inputs. Using capacitive connections a number of secondary gates/inputs can be deposited above the floating gate (FG) and the architecture got popularity with the name multi-input FG MOST device. These capacitor values are determined by the sizes of the input electrodes and are varied according to the requirements. In terms of its DC operating point, the FG acts as a floating node. The schematic for an N-input N-channel FGMOS transistor is shown in Fig. 2.

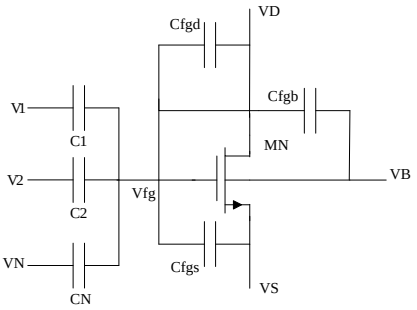

Fig. 2 Schematic of N-input N-channel FG MOST

The gate of MOST MN is at floating state (V_{fg}) under DC condition whereas it is capacitively connected to inputs $V_{1...N}$ via second layer of ploysilicon. The input capacitor $C_{1...N}$ formed is referred as poly-poly (PIP) capacitor while others $(C_{fgs}, C_{fgd}, C_{fgb})$ are the parasitic capacitance associated the floating gate node. The overall advantage and disadvantage using FG MOST is summarized as follows:

Advantage:

- Reduced the circuit complexity
- Threshold voltage scalable
- Low voltage operation
- Simplify the signal processing
- Inherently act as level shifter

Disadvantage:

- Large chip area
- Poor transconductance
- Increased conductance
- Charge trapping

C. Quasi-floating Gate (QFG) MOSFET

The QFG MOST circuits are wide-band ac coupled circuits which operate at much lower supply than

conventional GD MOST [22]. While working with FGMOS transistor two major issues were encountered: (i) Initial charge trapping at FG node; and (ii) Poor gain-bandwidth (GB) product.

In context above issues, a new modified architecture of FGMOS was proposed very much similar to FGMOS named as QFG MOST. In QFGMOS device, a large value resistor is used as a replacement for bias capacitor. Such high value resistor is realized by leakage resistance $\left(R_{l\arg e}\right)$ of a reverse biased junction of MOST operating in cut-off region. This high value leakage resistance connects the FG node weakly to the desired DC level and this changes the gate potential floating state to quasi-floating. Moreover, the small value of parasitic gate-to-drain capacitance of cut-off MOST used does not degrade the GB product as much like in case of FG MOST [23]. The capacitor divider network at input helped in design of very linear programmable circuits like CMOS OTA to implement tunable MOS resistors [24], GM-C filter [25], current conveyor [26], current mirror [27] etc. The experimental verification of QFG based circuits in these articles has proved it to be a better option for realizing low voltage low power circuits. The circuit implementation of QFG MOST transistor is similar to that of FG MOST. The schematic of an N-channel QFGMOS along with its parasitic capacitances is shown in Fig. 3. The P-channel MOST (MP) has its gate connected to positive supply rail VDD which makes it to work in cut-off region and realize a very high value resistance $R_{l\arg e}$.

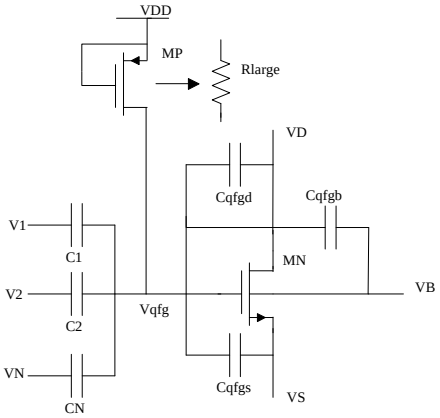

Fig. 3 Equivalent circuit of N-input N-channel QFG MOST

The effective gate potential for QFG MOST under ac in s-domain is expressed as

$$V_{qfg} = \left(\frac{sR_{l\arg e}C_{T,QFG}}{1+sR_{l\arg e}C_{T,QFG}}\right) \left(\frac{\sum_{i=1}^{n} C_i V_i + C_{qfgs}V_S + C_{qfgd}V_D + C_{qfgb}V_B}{C_{T,QFG}}\right) \quad (1)$$

where $C_{T,QFG} = \sum_{i=1}^{n} C_i + C_{qgs} + C_{qgd} + C_{qgb} + C_{gd,MP}$, C_i is the coupling capacitor of the i^{th} input branch whereas C_{gs}, C_{gd}, C_{gb} are the associated parasitic of NMOS to the floating gate, and $C_{gd,MP}$ is the parasitic capacitance associated with PMOS transistor MP. As observed the equation (1) represents a high-pass filter with cut-off frequency of given by $f_0 = 1/2\pi R_{l\arg e}C_{T,QFG}$. So, using QFGMOS, applications where very low cut-off frequency is required generally below 1 Hz can be easily achieved by tuning $R_{l\arg e}$, for example in bio-amplifiers [28]. The overall advantage and disadvantage using QFG MOST over FG MOST is summarized as follows:

Advantage:

- Prevent initial charge trapping issue
- Low voltage operation
- Less silicon area compared to FG MOSFET
- Acts as HPF supporting cut-off frequency below 1 Hz
- Improved gain-bandwidth over FG MOSFET

Disadvantage:

- Output conductance slightly higher over FG MOSFET
- Increased static power dissipation

D. Bulk Driven Floating Gate (BDFG) MOSFET

The bulk-driven floating gate (BDFG) MOST is similar to that of BD MOST, except the difference lies in gate-node potential. In BDFG instead of applying gate to a fixed DC potential, it is configured in floating state. The structure overcomes the major drawback of BD MOST, i.e. low transconductance and poor frequency response. The schematic of an N-channel BDFG MOST along with its parasitic capacitances is shown in Fig. 4.

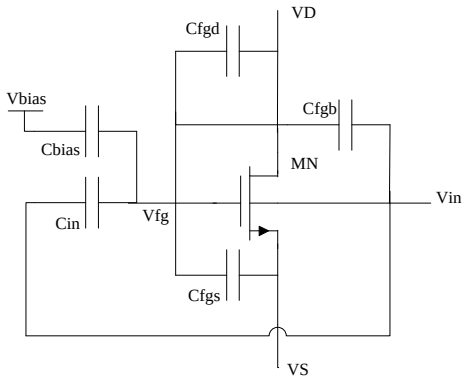

Fig. 4 Bulk driven floating gate NMOST

In Fig. 4, the gate of MOST MN is converted in floating state using input capcitor $\left(C_{in}\right)$ and its other end connected to bulk so as to make it bulk controlled device. A large value biasing capacitor $\left(C_{bias}\right)$ is used at gate of MN to keep BDFG MOST in saturation mode. In DC condition, the BDFG performs as BD MOST whereas for AC it combines the characteristics of BD and FG MOST which results in effective transconductance higher than alone BD or FG MOST but remians below GD MOST.

E. Bulk Driven Quasi-floating Gate (BDQFG) MOSFET

The bulk-driven quasi-floating gate (BDQFG) MOST is similar to that of BDFG MOST, except the difference lies in gate-node potential. In BDQFG instead of applying gate to a

fixed DC potential, it is configured in quasi-floating state. The structure overcomes the issues of BDFG MOST and hence got popularity in an exponential manner. The schematic of an N-channel BDQFG MOST along with its parasitic capacitances is shown in Fig. 5. Likewise BDFG, BDQFG MOST is formed with the difference only in state of its gate potential which is changed in quasi-floating state via large value resistance (R_{large}) of P-channel MOS transistor (MP) working in cut-off region. Moreover, absence of C_{bias} in BDQFG does improve the effective transconductance compared to BDFG and so the gain-bandwidth product. Under DC, the BDQFG performs as BD MOST whereas for AC it combines the characteristics of BD and QFG MOST which results in effective transconductance higher than alone BD or QFG MOST.

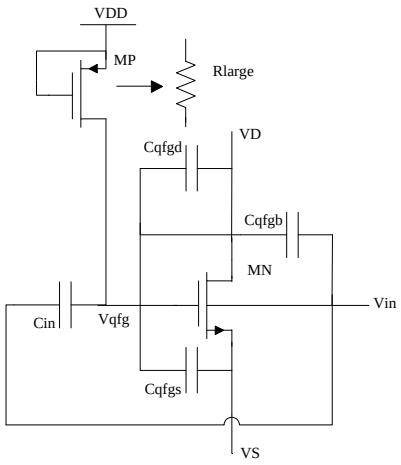

Fig. 5 Bulk driven quasi-floating gate NMOST

It is worth here to be noted that the effective transconductance of BDQFG is almost equal to GD MOST which can be observed in [29] where experimental validation has been shown. Few recent articles reporting this approach in the design of current mirrors has been presented in [30-33].

So overall, it can be concluded that using BDQFG the performances is almost similar to GD MOST with an added advantage of low power consumption.

III. Simulation Results for Performance Analysis

The effect of aforementioned techniques on N-channel MOST (NMOST) performance parameters is shown with the help of HSpice simulations and compared to GD based NMOST. During simulation the NMOST taken have width and length on 100 μm and 0.54 μm respectively and considered to be working in saturation mode. The simulations have been achieved under the same environment using the MOSFET model of UMC 0.18 μm technology at a supply of 0.5 volt. The other assumed parameters include input capacitance (C_{in}) and bias capacitance (C_{bias}) of 1pf respectively along with MOST dimension of W/L=0.36 μm /0.36 μm used for realizing R_{large} wherever applicable.

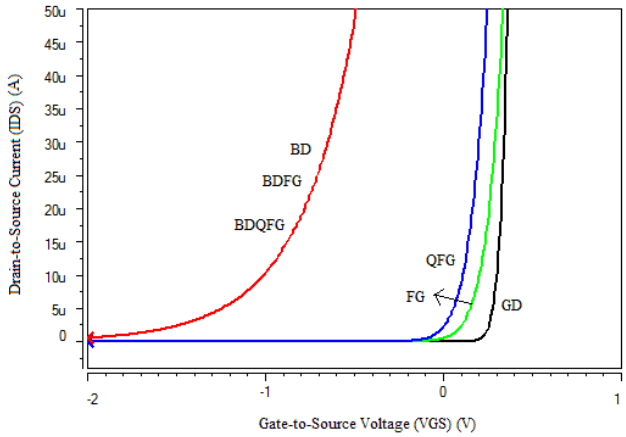

Fig. 6 Input characteristics

The plots include threshold voltage, transconductance, output resistance and transitional frequency. The plot of drain-to-source current of GD, BD, FG, QFG, BDFG and BDQFG is shown in Fig. 6. From plots it is quite clear that for BD approach the NMOST turns-ON in negative voltage and the same graph observed for BDFG and BDQFG since as stated earlier under DC conditions BDFG and BDQFG functions as simple BD NMOST. For FG and QFG, the current flow can be observed at smaller Vgs compared to GD which clearly indicate the low voltage requirements by the techniques. Similarly, the simulation of comparison of transconductance is shown in fig. 7. As observed the highest is observed in normal GD NMOST whereas in case of discussed techniques, the highest is observed for BDQFG NMOST followed by QFG and then BDFG, FG and lastly the lowest by BD NMOST. So, in terms of transconductance using BDQFG is better option.

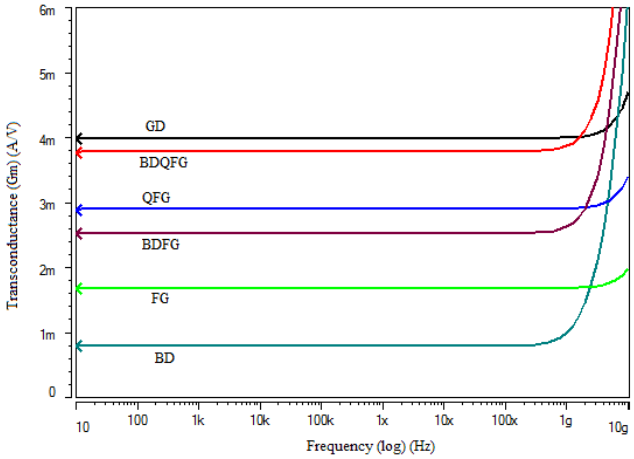

Fig. 7 Transconductance plots

Likewise, the plot for output resistance and the transitional frequency is shown in fig. 8 and fig. 9 respectively. However, in Fig. 8, as observed the output resistance is degraded which is due to feedback capacitances.

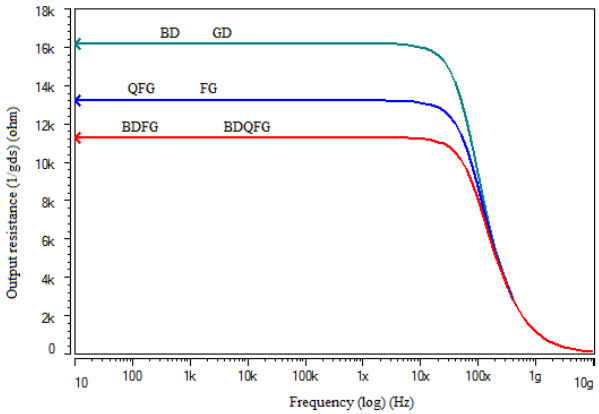

Fig. 8 Output resistance plots

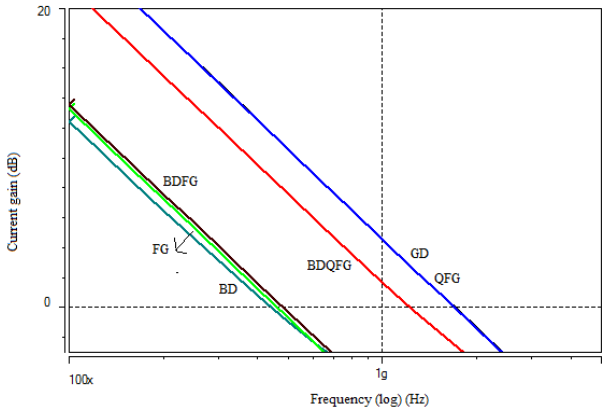

Fig. 9 Current gain plot for calculating transitional frequencies

IV. Conclusion

From the discussed techniques, it can be concluded that using FG and QFG a comparable performance to GD can be achieved at low power. The only issue related with both FG and QFG MOST is the lack of simulation model due to which approximate models are used for simulations. Also, the BDFG MOSFET suffers the similar drawbacks as like of FG MOST, i.e. large silicon area and initial charge trapping on the floating gate. So, it can be concluded that using BDQFG the frequency domain performances can be achieved almost similar to GD MOST with an added advantage of having low power consumption.

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Mobility based Energy Efficient Tracking using Firefly Algorithm in Wireless Sensor Network

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ABSTRACT:

This paper is about the Tracking of moving object by using firefly algorithm in wireless sensor network . Firefly algorithm is can determine the path ,position and locations (past, present and future) of the object. Firefly algorithm is a met heuristic optimization algorithm that represents the social behavior of the fireflies, The fireflies attraction depends on brightness of the firefly. The speed and accuracy of the firefly algorithm is better compare to existing algorithms. In sensor network the power consumption is more (by using the nodes) to track the object. To over come this problem we activate the nodes which are near to the object and reaming nodes are in rest(sleep mode) position. The Simulations and results indicate that the proposed firefly algorithm is superior to existing metaheuristic algorithms.

Keywords: Tracking, firefly algorithm, Mobility based tracking,

INTRODUCTION:

Object tracking has a great deal of attention in recent years.The reason is that object tracking has found its way in many real world applications, for example Surveillance, Vision based control,and robotics ,and in military regions. By using the firefly algorithm sensors are used to collect information about moving target position and to monitor the moving pattern in sensor field .wireless sensors networks must rely on the sensors used and collaborative signal processing todynamically manage nodes resources and effectively process distributed information. Along the direction,moving target tracking will be considered in wireless networks. Moving target continuously reports the position to a central base station. The open issues in object tracking are detecting the moving objects change in direction, varying speed of target precision, prediction accuracy and fault tolerance and missing target recovery. In all tracking process more energy is consumed for messages are transmission between the sensor nodes or between the sensor and sink. In target tracking application the sensor nodes which can sense the target at a particular time are kept in active mode,while the remaining nodes are to be in inactive mode so to conserve energy until the target approaches to nodes.The sensor whose sensing range contains the queried object will reply to the query. Clearly, this approach is inefficient because a considerable amount of energy will be consumed when the network scale is large or when the query rate is high. The power consumption is one of the most critical issues in object tracking. Energy dissipation in sensors is different,depending on the condition of the each sensor. Therefore each sensor must minimize the battery for longevity of network operation. The object tracking algorithm should be designed in such a way that result in good quality tracking with low energy consumption by using the firefly algorithm.

OPTIMIZATION AND TRACKING

I. Optimization:-

It is defined as finding an alternative with the most cost effective or highest achievable performance under the given constraints, by maximizing desired factors and minimizing undesired ones. In comparison, maximization means trying to attain the highest or maximum result or outcome without regard to cost or expense. Practice of optimization is restricted by the lack of full information, and the lack of time to evaluate what information is available.optimization includes finding "best available" values of some objective function given a defined domain.

II. Tracking:-

A process of determining the current and past locations Tracking system track the moving target in a WSN(Wireless sensor network) by sensing the capability of sensors. since sensor nodes have limited battery power and replacement of

battery is impossible, and energy saving is an issue in tracking process.

III. Target Detection:

A target detection is scheme in which each sensor works autonomously until a target is acquired.

MOBILITY BASED TRACKING USING SENSORS:

With rapid advances in sensor fabrications, recent sensors are designed to be power aware, changing their condition (eg., shut down sensing processor or radio) when they do not need to run the components to perform a given task in a sensor field. Most sensors can operate under the three different conditions: Active, Idle and sleep. It is important to completely shut down the radio rather than put it in the idle mode when it needs not sensing. Power management of sensor components is very important because energy consumption depends on their duties.To save energy resource and thus extend the network lifetime, it is desirable that only the nodes that surround the mobile target are responsible for observing the target For example, when the target passes through the t1 point as shown in Fig. 1,all nodes do not need to join in the task for tracking a mobile target. Instead, it is more energy efficient for only the nodes S1 around the mobile object to join in collecting information of the target and performing collaborative work among them. Other nodes located far from the target don not need to waste their powers to detection and tracking with surveillance. Alsoeachmonitors the target. If we can predict the next location of the mobile object in advance, we can organize the group membership dynamically which should join in tracking mission. As shown in Fig.1, for example, the number of participating nodes may be minimized, which allows us to further extend the whole network lifetime if we predict future location of the mobile target accurately.

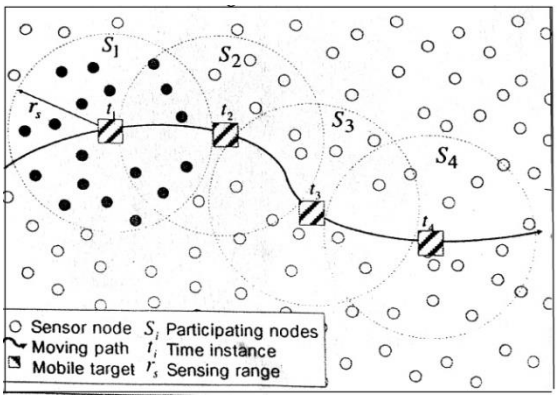


Fig.1.A concept of tracking of mobile object

As the mobile object moves, the tracking nodes may migrate to the moving direction of the target tokeep on monitoring as shown in Fig. 1,where a thick line indicates the moving path of mobile target and blacked circles inside the dotted circle are tracking nodes at time 1 t. Thus, sensor nodes need to control their states by themselves based on prediction of target's movement. We assume a sensor network where N sensors with the same communication and sensing range are distributed randomly in the environment that is being monitored. We also assume that each node knows its own location by using GPS or other location awareness techniques and we utilize triangulation for localization of a mobile target. Consequently at least 3 sensors join the target detection and tracking with surveillance. Also each node keep information about its neighbors such as location through the periodically message change. And each individual sensor node is equipped with appropriate sensory devices to be able to recognize the target as well as equipped with appropriate sensory devices to be able to recognize the target as well as to estimate its distance based on the sensed data. Further, we assume that we predict the location of the mobile targets every one second (or minute), and each sensor records the movement pattern of the mobile object. basically we used a moving average estimator to predict the future location of the mobile target based on the measurement of direction and the velocity of the mobile target.

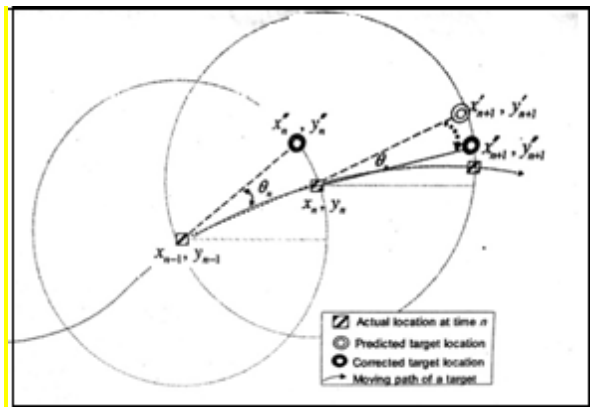


Fig:2.Tracking of the mobile target in wireless sensor network

The Concept of tracking of object

When the mobile target will move during the time interval[n,n+1].Given the current location (X_n,Y_n),the first predicted location of the mobile object at the time instant of (n+1) denoted as (X_{n+1},Y_{n+1}) is

$X'_{n+1}=X_n+\tilde{v}_{X(n+1)}$

$Y'_{n+1}=Y_n+\tilde{v}_{Y(n+1)}$

Where $V_{x(n+1)}$and $V_{Y(n+1)}$ represent the future speed estimates of the mobile object in the direction of x and y respectively, during the time period [n,n+1].

These speed estimates based on the previous speed value

$$\square X(n+1) = \frac{\sum_{i=n-h+1}^{n} x(i)}{h}$$

$$\tilde{v}(n+1) = \frac{\sum_{i=n-h+1}^{n} v(i)}{h}$$

Where h is the predefined number of the past history based on the which we predict the next moving factor that is future speed of a moving average of acceleration of an object can be determined. It is possible to exactly predict the future location of the mobile object that moves linearly. But the estimation is no longer effective when the object moves in the non linear fashion and velocity information is used to predict the future location. A small correction mechanism to get the exact estimation.Finally we predict the next location (x''_{n+1},y''_{n+1}) of the mobile target by correcting the angle from the first location.

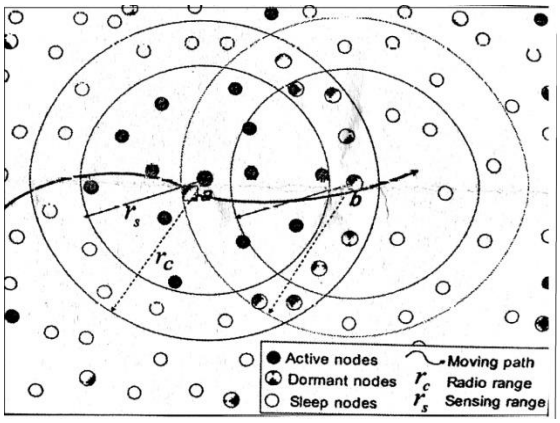


Fig:3 State change at each sensor node as the mobile target moves

FIREFLY ALGORITHM:

In mathematical optimization the firefly algorithm is a met heuristic proposed by Xin-She Yang and inspired by the flashing behavior of fireflies.

1. All fireflies are unisex so that one firefly will be attracted to other fireflies regardless of their sex.

2. Attractiveness is proportional to their brightness, thus for any two flashing.

3.Fireflies, the less bright one will move towards the brighter one. The attractiveness is proportional to the brightness and they both decrease as their distance increases. If there is no brighter one than a particular firefly, it will move randomly.

4.The brightness of a firefly is affected or determined by the landscape of the objective function.

BEHAVIOUR OF FIREFLY:

The flashing light of fireflies is an amazing sight in the summer sky in the tropical and temperate regions. There are about two thousand firefly species, and most fireflies produce short and rhythmic flashes. The pattern of flashes is often unique for a particular species. The flashing light is produced by a process of bioluminescence, and the true functions of such signaling systems are still debating. However, two fundamental functions of such flashes are to attract mating partners (communication), and to attract potential prey. In addition, flashing may also serve as a protective warning mechanism. The rhythmic flash ,the rate of flashing and the amount of time form part of the signal system that brings both sexes together. Females respond to a male's unique pattern of flashing in the same species, while in some species such as postures, female fireflies can mimic the mating flashing pattern of other species so as to lure and eat the male fireflies who may mistake the flashes as a potential suitable mate. We know that the light intensity at a particular distance R from the light source obeys the inverse square law. That is to say, the light intensity I decrease as the distance r increases in terms of $I \propto 1/r2$. Furthermore, the air absorbs light which becomes weaker and weaker as the distance increases.

These two combined factors make most fireflies visible only to a limited distance, usually several hundred meters at night, which is usually good enough for fireflies to communicate. The flashing light can be formulated in such a way that it is associated with the objective function to be optimized, which makes it possible to formulate new optimization algorithms. In the rest of this paper, we will first outline the basic formulation of the Firefly Algorithm (FA) and then discuss the implementation as well as its analysis in detail.

Pseudo code of the firefly algorithm (FA).

Objective function f(x), x = (x1, ...,xd);
Generate initial population of fireflies
xi (i = 1, 2, ..., n)
Light intensity Ii at xi is determined by f(xi)
Define light absorption coefficient
while (t <Max Generation)
fori = 1 : n all n fireflies
forj = 1 : i all n fireflies
if (Ij> Ii), Move firefly i towards j in d-dimension;
end
if
Attractiveness varies with distance r via exp[−r]
Evaluate new solutions and update light intensity
end for j

end for i
Rank the fireflies and find the current best
end while
Post process results and visualization

In the firefly algorithm, there are two important issues: the variation of light intensity and formulation of the attractiveness. For simplicity, we can always assume that the attractiveness of a firefly is determined by its brightness which in turn is associated with the encoded objective function.

In the simplest case for maximum optimization problems, the brightness I of a firefly at a particular location x can be chosen as I(x) / f(x). However,the attractiveness _ is relative, it should be seen in the eyes of the beholder orjudged by the other fireflies. Thus, it will vary with the distance rij between firefly i and firefly j. In addition, light intensity decreases with the distancefrom its source, and light is also absorbed in the media, so we should allowthe attractiveness to vary with the degree of absorption. In the simplest form,the light intensity I(r) varies according to the inverse square law I(r) = Is/r2where is the intensity at the source. For a given medium with a fixed lightabsorption coefficient , the light intensity I varies with the distance r. Thatis I = I0e−r, where I0 is the original light intensity. In order to avoid thesingularity at r = 0 in the expression Is/r2,

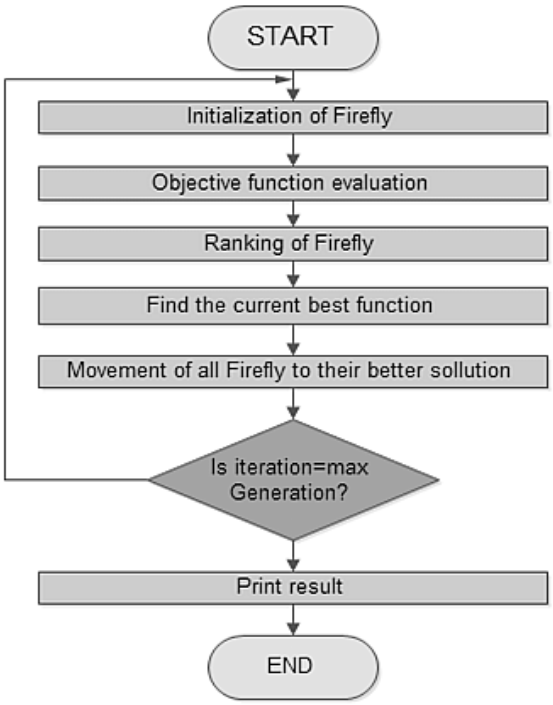
The combined effect of both the inverse square law and absorption can be approximated using the following Gaussian form
$I(r) = I0e^{-r2.}$

Sometimes, we may need a function which decreases monotonically at a slower
rate. In this case, we can use the following approximation
I(r) =I0/(1 + r2) .
At a shorter distance, the above two forms are essentially the same. This is because the series expansions about r = 0
e^{-r2}~ 1 − yr^2+1/2y^2r^4+….. 1 /(1+ yr^2)~- yr2 +y^2r4 +……
are equivalent to each other up to the order of O(r3).As a firefly's attractiveness is proportional to the light intensity seen by adjacent fireflies, we can now define the attractiveness _ of a firefly by
$\beta(y)= \beta_0 e^{-yr\ 2}$

where β0 is the attractiveness at r = 0. As it is often faster to calculate 1/(1 + r2) than an exponential function, the above function, if necessary, can conveniently be replaced by β=β/(1+yr^2) .the above equation defines a characteristic distance r = $1/y^{1/2}$over which the attractiveness changes significantly from β_0 to $\beta_0 e^{-1}$

In the implementation, the actual form of attractiveness function _(r) can
be any monotonically decreasing functions such as the following generalized form$\beta(r)= \beta_0 e^{-yr\ m}$ (m>1)
For a fixed , the characteristic length becomes r = y $^{1/m}$ tends to 1 as 1.tends to infinite Conversely, for a given length scale r in an optimization problem, the parameter Y can be used as a typical initial value that is y= $1/r^m$

FLOWCHART FOR THE FIREFLY ALGORITHM:



RESULT:

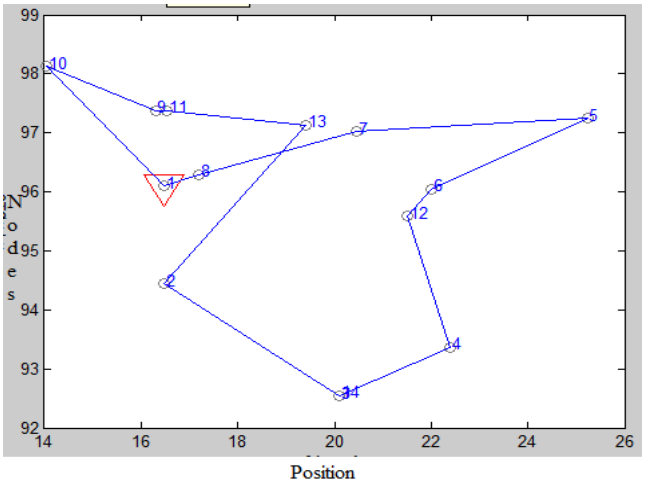


Fig 4:moving object tracking using firefly algorithm

CONCLUSION:

In this paper networks of small, densely distributed wireless sensor nodes are capable of solving a variety of collaborative problems such as monitoring and surveillance. We develop a simple algorithm that detects and tracks a moving target, and alerts sensor nodes along the projected path of the target. The algorithm involves only simple computation and localizes communication only to the nodes in the vicinity of the target and its projected course. An energy efficient tracking method is used to reduce the number of nodes participating in target tracking.
By using pos algorithm we can find position ,probability best and global best of the object and in Firefly Algorithm we find position and path of the object , and also the locations of the object is determined .

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AN OPEN BOUND ESTIMATOR UNDER CHANNEL DIVERSITY IN HETEROGENEOUS NETWORK

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Abstract:
In the propagation model of a wireless network, variant format of estimation logic are been proposed in past. With the evolution of new network models and variant channel condition, the conventional estimators are limited under the utilization of the evolving new models. To achieve a better estimation in heterogeneous network under Multi input multi output (MIMO) for channel diversity condition, in this work, a new estimator logic based on a open bound estimator using min-max approach. The proposed approach is validated for different channel condition, and the observation reveals the suitability of the proposed approach under diverse condition.

Index Term: channel estimation, propagation model, MIMO, open bound estimation logic.

1. Introduction

With the increase in offered service level and upcoming new architecture, new network models and devices are emerging. The next generation services demands a very high service quality, and the available resources will be getting constraint to cope with the demanded services. To achieve a higher service quality with optimal resource utilization, new architectures are evolving. In these architectural enhancement, Heterogeneous network is observed to be a very optimal network structure upcoming. A heterogeneous network (HetNet) is acquired as a cluster of distinct sub networks, which are grouped together to maintain long-range communication with different wireless communication architectures. The integrated mode approach of communication has resulted in efficient communication, with higher throughput performance for wireless communication. The architecture is in development to suite the upcoming requirements of demanded services for next-generation wireless communication. Such networks are evolving towards a new mode of communication. Various wireless-enabled networks are integrated together to support a long-range communication, and the optimality issues with respect to resource utilization and usage are under investigation. In the process of service provisioning in heterogeneous network, the prime issues observed are the processing overhead due to multiple network interfacing. The HetNet has the provision of providing higher network connectivity, however, HetNet are limited with the device capability. Towards improving the performance of HetNet operation, various past developments were observed. For optimal resource allocation, spectrum allocation, routing optimization, and power efficiency. For the development of optimal resource allocation in heterogeneous networks, an approach for the optimal allocation of resources in terms of spectrum efficiency, fairness and battery power during communication is outlined in **Error! Reference source not found.**[1]. A multi-attribute scheduling algorithm approach is proposed, where these parameters are used for resource scheduling. This multi- attribute approach is significant because it controls the allocated data rate based on an optimized utility function in the HetNet. This optimization is proved w.r.t. optimal rate allocation over maximization of the spectrum efficiency and fairness factor. In order to be fair to the user, an interference alignment (IA) scheme for resource allocation was presented in[2]. A spectral coexistence mechanism to mitigate the interference in heterogeneous networks was presented. The resource allocation in terms of optimal interference management was advised. In **Error! Reference source not found.Error! Reference source not found.Error! Reference source not found.**[3], the optimality issue of resource allocation with respect to traffic density was outlined. The offered capacity for transmission, was governed by the solution of a continuous linear programming (LP) approach, where a solution is derived by a scheduler unit based on the number of mobiles in the network. A weighted distribution scheme for all the available weights in the network is presented in [4]. The approach of resource allocation based on an existing wireless network for user preference and mobile terminal power is presented. A cost optimization approach was derived for different

networks of macro-Pico-femto-and relay-based communication approaches towards service uniformity in these networks. In [5], a topology-governed inference management for enhancing the performance of a heterogeneous network is outlined. To obtain the objective of optimal resource allocation in heterogeneous networks, an adaptive interference coordination in inter-cellular interference for smart resource allocation is presented. An intracellular fairness objective was suggested. In [6],[7], a new dynamic scheduling over a heterogeneous network, following packet scheduling, was presented. A media independent handover concept has been realized to offer efficient transmission of multimedia services using a heterogeneous network. For provisioning of the spectral efficiency in a heterogeneous network, a cell range expansion (CRE) problem was addressed in [8],9] by setting a positive bias factor in the short-range communication network. The objective was derived as the average area weighted load per cell, defined as the weighted spectrum efficiency and energy efficiency approach. With a similar objective for the spectral efficiency in [10],11], the spectrum efficiency (SE) and energy efficiency (EE) derived over a realistic network were presented. An operation relation and quality governance for efficient coding was suggested. In [12] SE and EE objectives were analyzed using a biased inter-and intra-radio access technologies (RAT) offloading technique. The analysis yields a multi-objective optimization problem, maximizing the SE and EE subjected to the bounding quality of services. Most of the approaches are developed for resource optimization, and the offering quality of services is an observable parameter. To offer QoS in heterogeneous networks, a quality objective with regard to an interference constraint across the cell coverage is presented in [13]. The QoS parameters are defined as a function of link bandwidth, node buffer and queuing service and are employed at the router level in a heterogeneous network. In [14], an end-to-end QoS framework for heterogeneous networks is focused on. The objective of QoS provisioning was made over multiple autonomous systems. In [15],16], a routing algorithm based on proactive coding, was suggested and a QoS driven control selection was outlined. A general backward utility formation was introduced to observe the dynamic QoS variation in the network. With respect to the resource variation issue and governing of QoS, multihop communication with regard to homogeneous and heterogeneous networks was presented in [17]. The variant parameter of a micro-site with regard to a traffic load condition was analyzed.

2. Feedback estimator logic

The channel imperfection in wireless medium lead to diversity in signal estimation. In the estimation process, the estimator are designed to estimate the data based on estimates or prior channel information. However with the increase in demand for greater services and faster data transmission, these estimators are getting limited with processing speed. The concern of such estimator is the convergence period. The convergence issue for an estimator unit is a primal requirement in wireless communication. It is required to have a faster convergence to give fast processing efficiency in wireless communication system. To improve the processing accuracy and overhead minimization, the conventional 2 way LMS logic is improved. A selective logic is defined to obtain proper signal selection under multipath coding. Under channel diverse condition, the bit sparsing control the channel impact observed. In addition the convergence performance for the estimator is also required to give the system output faster.

The uncertainty in channel conditions has degraded the estimation performance of conventional channel estimator logic and needs an updating. The feedback estimators are developed to achieve the estimation performance under variant channel condition.

In the approach, of wireless communication, data are communicated over wireless medium from a source to sink. The communicating channel offers various noise effects to the transmitting data resulting in signal degradation. In the propagation mode for a communication system, signal $x_p$is transmitted over a channel, giving the impact of noise effect, the received signal at the receiver is observed as,

$$r(t) = \sum_{n=1}^{k} x_n \delta(t - NT) \quad (1)$$

The transmitted signal x_p is generated at a baud-rate $1/T$ through a time dispersive channel response $h(t)$. Here the channel offers a signal delay of δ, giving a time shift of NT time shift to the original signal time period. The received signal r(t) is observed to be an integrated model of multiple channel effected signal for paths 1..k.

It is required to estimate the channel effect, the proposed weighted 2 way LMS logic minimized the error objective. However, the convergence performance under the randomized channel condition is required. Assuming perfect synchronization and carrier-residual elimination, baud-rate sampling produces the discrete-time output

$$r_n = X_n + v_n = \sum_k h_k x_{n-k} + v_n \quad (2)$$

Where,

$$x_n = x(nT) \quad (3)$$

These interferences are to be estimated and equalized to improve the retrieved quality of a receiver unit. The estimation process at time domain /frequency domain or time-frequency domain are suggested for the analysis of received signal r(t) to regenerate x(t). However, these approaches are accurate when the channel is dual of the estimator and degrades in quality when the channel is dynamically changing. The estimation, of the degraded channel is carried out using recursive estimation.

Recursive filter estimates a process by using a form of feedback control, where the filter estimates the process state at some time and then obtains feedback in the form of measurements. The recursive filter operates in two states, time updation and measurement of updates. The time update state is responsible for projecting forward (in time) the current state and error covariance estimates to obtain the a priori estimates for the next time step. The measurement update state are responsible for the feedback-i.e. for incorporating a new measurement into the a priori estimate to obtain an improved a posteriori estimate. The time update stateis processed as a predictor equation, while the measurement update stateis operated as a corrector equation. Indeed the final estimation algorithm resembles that of a predictor-corrector algorithm.

The estimator tries to estimate the signal, from the received signal stabilizing the state of estimates by a linear estimate equation defined by,

$$x_k = Ax_{k-1} + Bu_{k-1} + w_{k-1} \quad (4)$$

with a measurement z that is,

$$z_{k=Hx_k+v_k} \quad (5)$$

the estimation feedback error is derived from the estimated signal, where z is taken as the estimated channel reference derived from the received signal. The measurement of the state stability is governed by the detection of the channel impulse H and noise parameter v_k from the estimate. The impulse response matrix H is defined as a $m \times n$ matrix in the measurement equation relating the state to the measurement z_k . In this Recursive filtering, the estimation method, minimizes "average" estimation error. More precisely, the Recursive filter minimizes the variance of the estimation error. But it is observed that the a Recursive filter has an assumption which limits its usage under channel diversity condition.

1. The Recursive filter assumes that the noise properties are known. If the system is unknown recursive filter fails to predict the effect.
2. The Recursive filter minimizes the "average" estimation error. if it is prefer to minimize the worst-case estimation error, the recursive filter fails.

This assumptions, leads to open loop issues in estimation and noise suppression, and leads to system instability. Under diverse channel condition, where signal travels through multiple paths as defined by H matrix of m x n size, where 'm' is number of information bit passed from each transmitting antenna with 'n' simultaneous channel. This m x n channel diversity result in imperfect channel condition, which leads to unstable error. To resolve these issue, a recursive estimator logic using min-max convergence criterion is proposed.

3. Unbound Loop Feedback Min-Max estimation

In the proposed approach, the estimation is preformed as a recursive estimation, with feedback error. The optimization criterion in this case is kept as a linear range of estimates, rather to a fixed limit as observed in conventional modeling. The least error or minimum square error approach, is best applicable to linear channel model, where as this estimate is not observed to be optimal in this scenario. To open the estimate limits, a minimum and maximum error bound factor is defined, called as 'Min-Max bound limits'. This open limits leads to a estimation stabilization under diverse channel condition.

The proposed approach optimizes the open loop estimation error criterion. Here, the proposed open bound filter minimizes the maximum singular value of the transfer function from the noise to the estimation error. While the Recursive filter requires knowledge of the noise statistics of the filtered process, the open bound filter requires no such knowledge. In the recursive estimation the states x of a linear dynamic system defined as,

$$\begin{aligned} x_{k+1} &= A x_k + B u_k + w_k \\ y_k &= C x_k + z_k \end{aligned} \quad (6)$$

where A, B, and C are known matrices, k is the time index, x is the state of the system, u is the known input to the system, y is the measured output and w and z are noise parameters.

The estimate in this case is observed to be uncertain, and estimation of y is predicted.

Using the Recursive loop to estimate the state referring estimate of *x* as $\hat{x}$, the filter equations is given by,

$$\hat{x}_{k+1} = \left(A\hat{x}_k + Bu_k\right) + K_k\left(y_{k+1} C\hat{x}_k\right) \quad (8)$$

Where,

$$K_k = AP_kC^T\left(CP_kC^T + S_z\right)^1 \quad (9)$$

and

$$P_{k+1} = AP_kA^T + S_w \quad AP_kC^TS_z^1CP_kA^T \quad (10)$$

where S_w and S_z are the covariance matrices of w and Z, k is the Recursive gain, and P is the variance of the estimation error.

The conventional error in this case works well only when the average value of the process noise, W_k, is zero, and the average value of the measurement noise, Z_k, is zero. However in a real time communication scenario under channel diversity this condition is not achievable, as the time series observation of the channel is non linear. To overcome this issue, the open bound filter performs a min-max estimation, where the vector norm of the original signal is computed, defined given by,

$$\|x\| = \sqrt{x^T x} \tag{11}$$

Which is also defined as,

$$\|x\|^2 = x^T x \tag{12}$$

A weighted vector norm is used to adapt the estimates, and is defined as

$$\|x\|_Q^2 = x^T Q x \tag{13}$$

where Q is a diagonal matrix, where the elements of Q serve to weight the elements of x when the norm is computed. Taking the weighted norm matrix the system triews to solve the convergence problem of

$$\min_{\hat{x}} \max_{w,v} J \tag{14}$$

Where J is the cost function defining the estimation limit computing the noise terms w and v which are dynamic in nature.

The cost function J is defined as:

$$J = \frac{ave\left\|x_k - \hat{x}_k\right\|_Q}{ave\|w_k\|_W + ave\|v_k\|_V} \tag{15}$$

Where the averages are taken over all time samples k. Here the estimate tries to minimize J, to find a $\hat{x}$ that is close to the original signal x.

The average weighted norm function in the denominator of the cost function, relate to the minimizing of cost function, wherein, the improvement in the estimation of original signal x is observed at the numerator term, relating to the maximization of estimation accuracy. This builds to the equilibrium criterion of min-max stabilization. The estimate where the two terms result into min J is then considered as the estimate value for equalization.

4. Results and Discussion

The proposed approach is evaluated for a MIMO-OFDM model under channel Variant condition. The developed approach of open bound estimation modeling is used for estimation and compared with the conventional LMS estimation approach. A random set of information bits are taken as input bits. A set of the processing bit is shown in figure 1.

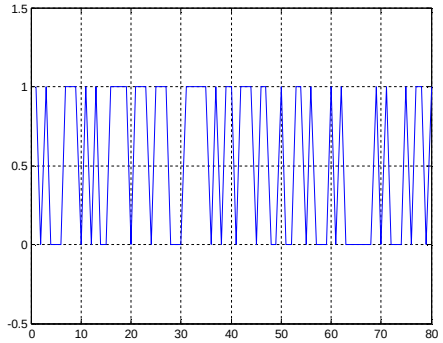

Fig. 1: original message signal

These information bits are modulated using a Quadrature modulation scheme, where the real distribution of the complex modulated data is shown in figure 2.

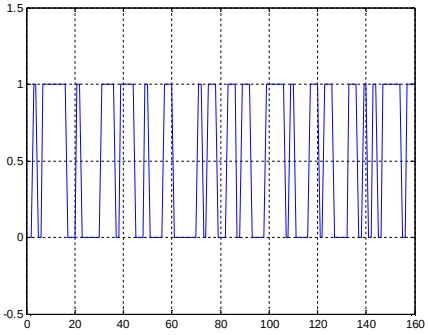

Fig 2: Modulated signal output

This information bit is block coded and transmitted over the channel. The effected signal for this transmitted bit is shown in figure 3.

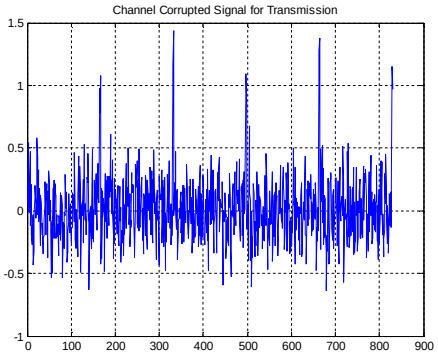

Figure 3: Channel effected signal

For this effected signal the channel estimation logic is applied. The estimated received bits are as illustrated in figure 4.

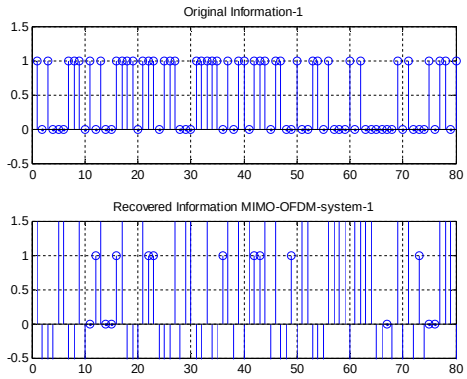

Figure 4: Recovered information bit

The error performance for the developed approach is as illustrated in figure below.

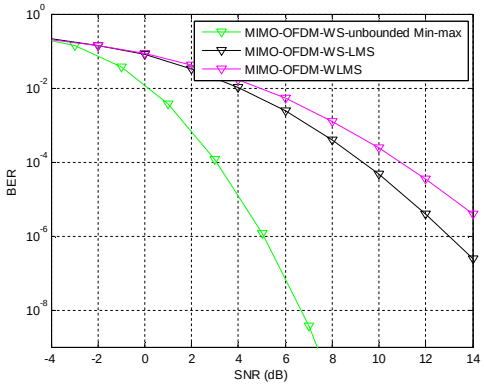

Fig5: SNR V/s BER comparison plot between MIMO-OFDM-unbound-Min-Max with conventional approaches

The above graph gives the observation for SNR v/s BER of both the conventional and proposed methods. It is clearly observed that the bit error rate of conventional approaches is more when compared with the proposed unbound-Min-Max approach.

A similar test is carried out for a simulation parameter of noise density of 14 dB, and fading factor of 15 KHz, is simulated. The observed result is shown in figure 6.

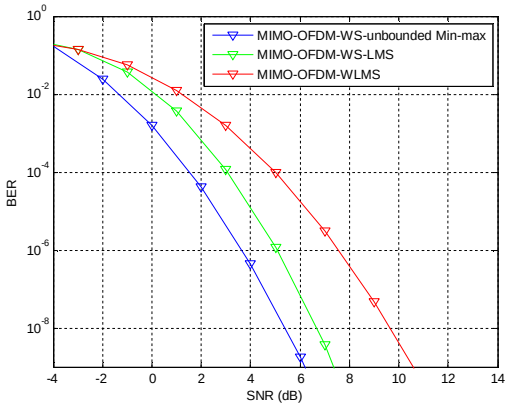

Fig 6: Simulation result for the developed approach under noise density of 14dB and fading factor of 15 KHz.

The convergence performance of the developed approach over the conventional estimator is presented in figure 7.

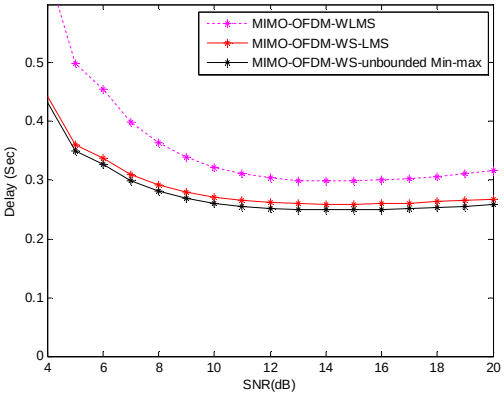

Fig 7: Convergence performance for the developed approaches

5. Conclusion

An open Min-Max convergence logic is developed for a MIMO-OFDM communication model. The approach defines a new cost optimization for MIMO-OFDM system, where the channel is divers in condition. The randomized channel condition as observed in real time scenario is simulated for the developed approach, and evaluated under different channel condition. The observation obtained defines the performance improvement of the suggested approach, where the convergence for the proposed system is observed to be achieved at 0.25 Sec as in comparison to 0.28 by LMS system. The error

performance is also improved due to faster estimation process, which is reduced to be 0.0038 for the proposed models as compared to 0.0012 for the conventional LMS model.

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Analysis of Energy Efficient Tracking In Wireless Sensor Networks

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ABSTRACT:

When a problem is large or difficult to solve, computers are often used to find the solution. Traditional methods of finding the answer may not be enough. It is in turning to nature that inspiration can be found to solve these difficult problems. Nature-inspired algorithms are among the most powerful algorithms for optimization. This paper tends to provide a detailed information of the firefly algorithm in tracking method that can reduce by an accurate estimation of the target location. we will compare the firefly algorithm with the particle swarm optimization. Energy saving is the critical issue for object tracking in sensor networks. The number nodes surrounding the mobile target should be responsible for observing the target to save the energy consumption and extend the network lifetime. Simulations and results indicate that the proposed firefly algorithm is superior to particle swarm optimization .In particle swarm optimization the present location of the object and by probability best and Global best the future location of the object is determined and energy consumption is more compared to firefly algorithm .In firefly algorithm the past, present and future locations and path of the object is determined, the accuracy is more and the time consumption is less in the mobile target.

KEY WORDS: Tracking ,particle swarm optimization ,Mobilty based Tracking,Firefly.

INTRODUCTION:

Object tracking has a great deal of attention in recent years. The reason is that object tracking has found its way in many real world applications, for example Surveillance ,Vision based control, and robotics ,and in military regions. Sensors are used to collect information about moving target position and to monitor the moving pattern in sensor field .wireless sensors networks must rely on the sensors used and collaborative signal processing to dynamically manage nodes resources and effectively process distributed information. Along the direction, moving target tracking will be accuracy and fault tolerance and missing target recovery. In all tracking process more energy is consumed for messages are transmission between the sensors nodes or between the sensor and sink. In target tracking application the sensor nodes which can sense the target at a particular time are kept in active mode, while the remaining nodes are to be in inactive mode so to conserve energy until the target approaches to nodes. The sensor whose sensing range contains the queried object will reply to the query. Clearly, this approach is inefficient because a considerable amount of energy will be consumed when the network scale is large or when the query rate is high. The power consumption is one of the most critical issues in object tracking. Energy dissipation in sensors is different, depending on the condition of the each sensor. Therefore each sensor must minimize the battery for longevity of network operation. The object tracking algorithm should be designed in such a way that result in good quality tracking with low energy consumption by using the firefly algorithm.

This paper aims to introduce the new Firefly Algorithm and to provide the comparison study of the FA with PSO algorithms. We will first outline the particle swarm optimization, then formulate the firefly algorithms and finally give the comparison about the performance of these algorithms. The FA optimization seems more promising than particle swarm optimization in the sense that FA can deal with wireless sensor network more efficiently and naturally.

OPTIMIZATION AND TRACKING:

Optimization is defined as finding an alternative with the most cost effective or highest achievable performance under the given constraints, by maximizing desired factors and minimizing undesired ones. In comparison, maximization means trying to attain the highest or maximum result or outcome without regard to cost or expense. Practice of optimization is restricted by the lack of full information, and the lack of time to

evaluate what information is available. optimization includes finding "best available" values of some objective function given a defined domain.

TRACKING: A process of determining the current and past locations Tracking system track the moving target in a WSN(Wireless sensor network) by sensing the capability of sensors. since sensor nodes have limited battery power and replacement of battery is impossible, and energy saving is an issue in tracking process. A target detection is scheme in which each sensor works autonomously until a target is acquired. Most sensors can operate under the three different conditions: Active, Idle and sleep. It is important to completely shut down the radio rather than put it in the idle mode when it needs not sensing.

Tracking in Our System is Performed by :

1.DISCOVERY: when a sensor node around the mobile object detects the target and initializes tracking ,it becomes estimation node which act as the master node temporarily.[3]

2.LOCALIZATION:A set of nodes those become aware the appearances of the mobile target compute the target's current position. The coordinates of the mobile target may be accomplish by the triangulation and their collaborative works.[3]

3.ESTIMATION:An estimation node predicts the future movement path of the mobile target and transmits message about the approaching location to its neighbor nodes .The prediction is carried out by the two steps: approximate a prediction and correction step that is explained above. The moving factors of a target ,such as direction and velocity can be obtained by sensors nodes through collecting moving patterns of the tracked target.[3]

4.COMMUNICATION:As the mobile target moves each node may hand off the initial estimate target location to the next node in turn, each node changes its duty cycle along the movement of the target. [3]

Operation of the Sensor Network

The nodes that surround the mobile target are responsible for observing the target For example, when the target passes through the t1 point as shown in Fig. 1,all nodes do not need to join in the task for tracking a mobile target. Instead, it is more energy efficient for only the nodes S1 around the mobile object to join in collecting information of the target and performing collaborative work among them. Other nodes located far from the target don not need to waste their powers to detection and tracking with surveillance. Also each monitor the target. If we can predict the next location of the mobile object in advance, we can organize the group membership dynamically which should join in tracking mission. As shown in Fig.1, for example, the number of participating nodes may be minimized, which allows us to further extend the whole network lifetime if we predict future location of the mobile target accurately. [3,4,5]. As the mobile object moves, the tracking nodes may migrate to the moving direction of the target to keep on monitoring as shown in Fig. 1,where a thick line indicates the moving path of mobile target and blacked circles inside the dotted circle are tracking nodes at time 1 t. Thus, sensor nodes need to control their states by themselves based on prediction of target's movement. We assume a sensor network where N sensors with the same communication and sensing range are distributed randomly in the environment that is being monitored [3]. We also assume that each node knows its own location by using GPS or other location awareness techniques and we utilize triangulation for localization of a mobile target. Consequently at least 3 sensors join the target detection and tracking with surveillance. Also each node keep information about its neighbors such as location through the periodically message change. And each individual sensor node is equipped with appropriate sensory devices to be able to recognize the target as well as equipped with appropriate sensory devices to be able to recognize the target as well as to estimate its distance based on the sensed data. . Further, we assume that we predict the location of the mobile targets every one second (or minute), and each sensor records the movement pattern of the mobile object. Basically we used a moving average estimator to predict the future location of the mobile target based on the measurement of direction and the velocity of the mobile target.

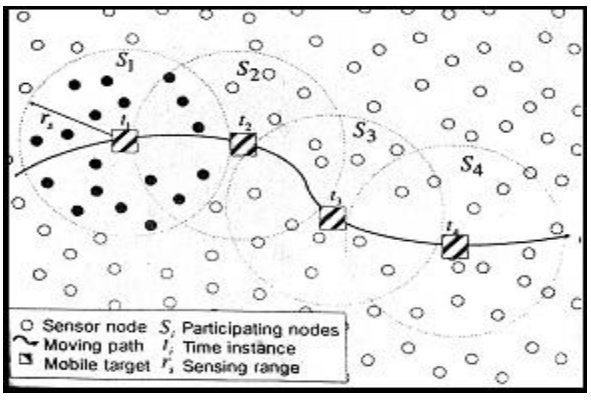

FIG 1:Concept of Traking mobile object

Particle Swarm Optimization

The PSO algorithm searches the space of the objective functions by adjusting the trajectories of individual agents, called particles, as the piecewise paths formed by positional vectors in a quasi-stochastic manner. There are now as many as about 20 different variants of PSO[2,3,4]. Here we only describe the simplest and yet popular standard PSO.

The particle movement has two major components: a stochastic component and a deterministic component. A particle is attracted toward the position of the current global best g* and its own best location x_i* in history, while at the same time it has a tendency to move randomly. When a particle finds a location that is better than any previously found locations, then it updates it as the new current best for particle i. There is a current global best for all n particles. The aim is to find the global best among all the current best solutions until the objective no longer improves or after a certain number of iterations. For the particle movement, we use x_i* to denote the current best for particle i, and g*≈ min or max {f(xi)}(i =1,2,...,n) to denote the current global best. Let xi and vi be the position vector and velocity for particle i, respectively. The new velocity vector is determined by the following formula

$$V_i^{t+1i} = V_i^t + \alpha\varepsilon 1\ (g^* - X_i^t) + 2\ \beta\ \varepsilon 2(X_i^* - X_i^t) \text{-- (1)}$$

Where ε1and ε2 are two random vectors, and each entry taking the values between 0 and 1. The Hadamard product of two matrices u ⊙ v is defined as the entry wise product, that is [u ⊙ v]ij= uij.vij. The parameters α and β are the learning parameters or acceleration constants, which can typically be taken as, say, α ≈ β≈2. The initial values of X_i^t=0i can be taken as the bounds or limits a=min(xj),b=max(xj) and V_i^t=0i= 0. The new position can then be updated by

$$X_i^{t+1} = X_i^t + V_i^{t+1}. \text{-------(2)}$$

Although vi can be any values, it is usually bounded in some range [0, vmax]. There are many variants which extend the standard PSO algorithm, and the most noticeable improvement is probably to use inertia function θ(t) so that v_i^t is replaced by $\theta(t)v_i^t$ where θ takes the values between 0 and 1. In the simplest case, the inertia function can be taken as a constant, typicallyθ≈0.5∼0.9. This is equivalent to introducing a virtual mass to stabilize the motion of the particles, and thus the algorithm is expected to converge more quickly

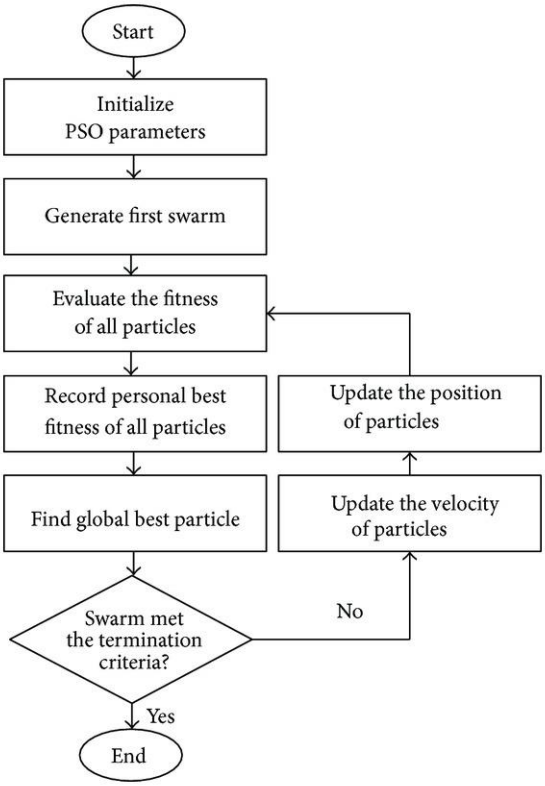

Fig 2: Flow Chart for PSO algorithm

BEHAVIOUR OF FIREFLY :

The flashing light of fireflies is an amazing sight in the summer sky in the tropical and temperate regions. [4,5]There are about two thousand firefly species, and most fireflies produce short and rhythmic flashes. The pattern of flashes is often unique for a particular species. The flashing light is produced by a process of bioluminescence, and the true functions of such signaling systems are still debating. However, two fundamental functions of such flashes are to attract mating partners (communication), and to attract potential prey. In addition, flashing may also serve as a protective warning mechanism. The rhythmic flash ,the rate of flashing and the amount of time form part of the signal system that brings both sexes together. Females respond to a male's unique pattern of flashing in the same species, while in some species such as photuris, female fireflies can mimic the mating flashing pattern of other species so as to lure and eat the male fireflies who may mistake the flashes as a potential suitable mate. We know that the light intensity at a particular distance R from the light source obeys the inverse square law. That is to say, the light intensity I decreases as the distance r increases in terms of I∝1/r2. Furthermore, the air absorbs light which becomes weaker and weaker as the distance increases.

These two combined factors make most fireflies visible only to a limited distance, usually several

hundred meters at night, which is usually good enough for fireflies to communicate. The flashing light can be formulated in such a way that it is associated with the objective function to be optimized, which makes it possible to formulate new optimization algorithms[5]. In the rest of this paper, we will first outline the basic formulation of the Firefly Algorithm (FA) and then discuss the implementation as well as its analysis in detail.

FIREFLY ALGORITHM:

In mathematical optimization the firefly algorithm is a metaheuristic proposed by Xin-She Yang and inspired by the flashing behaviour of fireflies.

1. All fireflies are unisex so that one firefly will be attracted to other fireflies regardless of their sex.
2. Attractiveness is proportional to their brightness, thus for any two flashing
3.Fireflies, the less brighter one will move towards the brighter one. The attractiveness is proportional to the brightness and they both decrease as their distance increases. If there is no brighter one than a particular firefly, it will move randomly.
4.The brightness of a firefly is affected or determined by the landscape of the objective function.

Pseudo code of the firefly algorithm (FA):

Algorithm

Objective function f(x), x = (x1, ..., xd)T
Generate initial population of fireflies xi (i = 1, 2, ..., n)
Light intensity Ii at xi is determined by f(xi)
Define light absorption coefficient
while (t <Max Generation)
for i = 1 : n all n fireflies
for j = 1 : i all n fireflies
if (Ij > Ii), Move firefly i towards j in d-dimension; **end if**
Attractiveness varies with distance r via exp[−r]
Evaluate new solutions and update light intensity
end for j
end for i
Rank the fireflies and find the current best
end while
Post process results and visualization

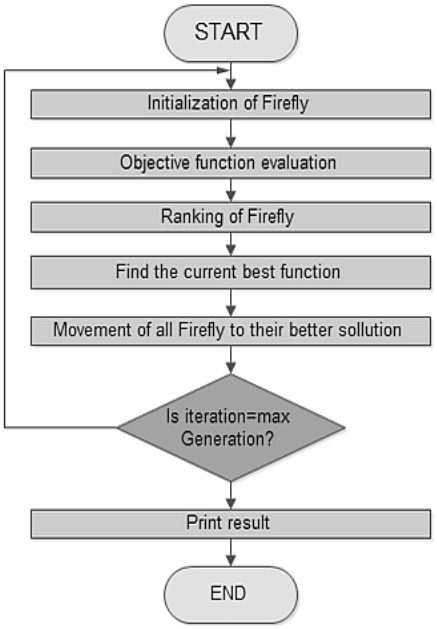

FIG 3: Flow Chart for Firefly algorithm

In the firefly algorithm, there are two important issues: the variation of light intensity and formulation of the attractiveness. For simplicity, we can always assume that the attractiveness of a firefly is determined by its brightness which in turn is associated with the encoded objective function.

In the simplest case for maximum optimization problems, the brightness I of a firefly at a particular location x can be chosen as I(x) / f(x).[4,5] However, the attractiveness _ is relative, it should be seen in the eyes of the beholder or judged by the other fireflies. Thus, it will vary with the distance rij between firefly i and firefly j. In addition, light intensity decreases with the distance from its source, and light is also absorbed in the media, so we should allow the attractiveness to vary with the degree of absorption. In the simplest form, the light intensity I(r) varies according to the inverse square law I(r) = Is/r2 where Is is the intensity at the source. For a given medium with a fixed light absorption coefficient , the light intensity I varies with the distance r. That is I = I0e−r, where I0 is the original light intensity. In order to avoid the singularity at r = 0 in the expression Is/r2,

The combined effect of both the inverse square law and absorption can be approximated using the following Gaussian form

$$I(r) = I0e^{-r2.}\text{------(1)}$$

Sometimes, we may need a function which decreases monotonically at a slower
rate. In this case, we can use the following approximation

$$I(r) = I0/(1 + r2) \text{ .------(2)}$$

At a shorter distance, the above two forms are essentially the same. This is because the series expansions about r = 0

$$e^{-r2} \sim 1 - yr^2 + 1/2y^2r^4 + \ldots.. \quad 1/(1+ yr^2) \sim - yr2 + y^2r4 + \ldots\ldots\ldots(3)$$

are equivalent to each other up to the order of O(r3).As a firefly's attractiveness is proportional to the light intensity seen by adjacent fireflies, we can now define the attractiveness _ of a firefly by

$$\beta(y) = \beta_0 e^{-yr^2} \text{ -------(4)}$$

where β0 is the attractiveness at r = 0. As it is often faster to calculate 1/(1 + r2) than an exponential function, the above function, if necessary, can conveniently be replaced by $\beta=\beta/(1+yr^2)$ .the above equation defines defines a characteristic distance r = $1/y^{1/2}$ over which the attractiveness changes significantly from β_0 to $\beta_0 e^{-1}$

In the implementation, the actual form of attractiveness function _(r) can

be any monotonically decreasing functions such as the following generalized form

$$\beta(r) = \beta_0 e^{-yrm} \quad (m>1)\text{------(5)}$$

For a fixed , the characteristic length becomes r = $y^{1/m}$ tends to 1 as 1.tends to infinite Conversely, for a given length scale r in an optimization problem, the parameter Y can be used as a typical initial value that is y = $1/r^m$ [4,5]

Distance and Movement:

The distance between any two fireflies i and j at x_i and xj, respectively, is the Cartesian distance $r_{ij=}$

$$\sqrt{\sum_{k=1}^{d}(Xik - Xjk)} \quad \text{—(6)}$$

where xi,k is the k th component of the spatial coordinate xi of the firefly. In2-D case

$$rij = \sqrt{(xi - xj)2} + \sqrt{(yi - yj)2}$$

The movement of a firefly i is attracted to another more attractive (brighter) firefly j is determined by

$$X_i = X_i + \beta_0 e^{-\gamma r2}{}_{ij}(x_j - x_i) + \alpha(\text{rand}-1/2)$$

The parameter γ now characterizes the variation of the attractiveness, and its value is crucially important in determining the speed of the convergence and how the FA algorithm behaves.

RESULT:

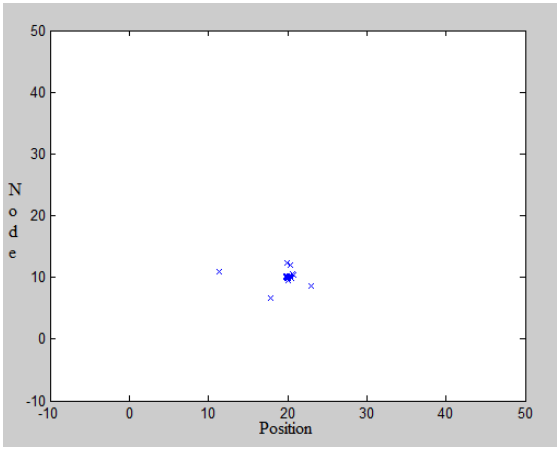

FIG 4: Object Tracking by using PSO

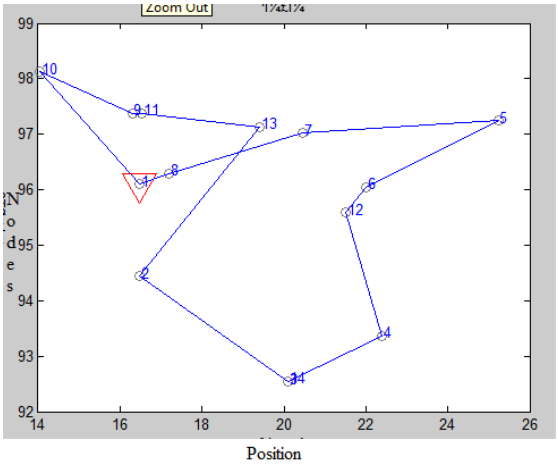

FIG 5: Object Tracking by using FA

CONCLUSION:

In this paper, we have formulated a new firefly algorithm and analyzed its similarities and differences with particle swarm optimization. We then implemented and compared these algorithms. Firefly is better than PSO in terms of the time taken to track the moving object. In PSO algorithm we can find the probability best and Global best to detect the future location of the object ,but by using the firefly algorithm the present, past, future locations and path of the object is determined .The speed and accuracy of the firefly algorithm is better than the particle swarm optimization.

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Combination of Iris Feature and palm print Features for security applications

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***Abstract*— A Biometric framework is basically an example acknowledgment framework that makes utilization of biometric characteristics to perceive people. Confirmation frameworks based on just a single biometric methodology may not satisfy the necessities of requesting applications as far as properties, for example, execution, adequacy and uniqueness. The greater part of the unimodal biometric frameworks have issues, for example, clamor in gathered information, intra-class varieties ,between class varieties, non all inclusiveness and so forth some of these restrictions can be overwhelmed by various wellspring of data for setting up character; such frameworks are known as multimodal biometric frameworks. In this paper a multimodal biometric arrangement of iris and palm print in light of wavelet parcel investigation is depicted. The most remarkable phenotypic component obvious in a man's face is the point by point surface of each eye's iris. Palm is the internal surface of a hand between the wrist and the fingers. palm print is alluded to vital lines, wrinkles and edges on the palm. The obvious surface of a man's iris and palm print is encoded into a conservative succession of 2-D wavelet bundle coefficient, which create a "component vector code". \in this paper, we propose a navel multi determination approach in light of Wavelet Packet Transform (WPT) for surface examination and acknowledgment of iris and palm print. The advancement of this approach is persuaded by the perception that overwhelming frequencies of iris surface are situated in the low and center recurrence channels. With a versatile limit, WPT sub pictures coefficients are quantized into 1,0or-1as iris signature. This mark introduces the neighborhood data of various irises. By utilizing wavelet parcels the extent of the biometric mark of code achieved is 960 bits. The mark of the new example is thought about against the put away example in the wake of figuring the mark of new info design. Recognizable proof is performed by processing the hamming separation.**

***Keywords*—Biometric, iris pattern, palm print, multimodal, wavelet packet transform, score level fusion**

1. INTRODUCTION

The word iris is generally used to denote the colored portion of the eye. It is a complex structure comprising muscle, connective tissues and blood vessels [1]. The image of a human iris thus constitutes a plausible biometric signature for establishing or confirming personal identity. Further properties of the iris that makes it superior to finger prints for automatic identification systems include, among others, the difficulty of surgically modifying its texture without risk, its inherent protection and isolation from the physical environment, and its easily monitored physiological response to light. Additional technical advantages over finger prints for automatic recognition systems include the ease of registering the iris optically without physical contact. Besides the above fact, the process of feature extraction is easier due to its intrinsic polar geometry.

Palm is the inner surface of a hand between the wrist and the fingers. Palm print is referred to principal lines, wrinkles and ridges on the palm. The principal lines are formed between the 3rd and 5th months of pregnancy and superficial lines appear after we born. Although the principal lines are genetically dependant, most of the other creases are not so. Even identical twins have different palm prints.

Palm print has been used as a powerful means in law enforcement for criminal identification because of its stability and uniqueness. The rationale to choose hand features as a base for identity verification is originated by its user friendliness, environment flexibility and discriminating ability.

11. EXISTING METHODS

The first successful implementation of iris recognition system was proposed by J.Daughman in 1993[3]. This work though published more than 29 years ago still remains valuable since because it provides solutions for each part of the system. It is worth mentioning that most systems implemented today are based on his work. They are based on Gabor wavelet analysis [1] [2] [3] in order to extract iris image features. It consists in convolution of image with complex Gabor filters. As a product of this operation, phasors (complex coefficients) are computed. In order to obtain iris signature, phasors are evaluated and coded by their location in the complex plane. However the Daugmen"s method is patented which blocks its further development.

In another approach suggested, by Lye Wil Liam and ali Chekima in their paper [4], the iris image is pre processed for contrast enhancement. After preprocessing, a ring mask is created and moved through the entire image to obtain the iris data. By using this data the iris and pupil are reconstructed from the original picture. Using the iris center coordinate and radius, the iris was cropped out from the reconstructed image. The iris data(iris donut shape) is transformed into a rectangular shape. Using a self organized feature map the iris pattern is matched. The network contains a single layer of Euclidean weight function. Manhattan distances are used to calculate the distance from a particular neuron X to the neuron Y in this neighborhood. Manhattan
distances without a bias and a competitive transfer function is used to upgrade the weight.

In another method followed by Jie Wang [7] the iris texture extraction is performed by applying wavelet packet transform (WPT) using Haar wavelet. The iris image is decomposed in to sub images by applying WPT coefficients are encoded.
K.Grabowski and W.Sankowski have designed another mehod for iris features extraction method. In their paper [8], Haar wavelet based DWT transform is used.

Ajay kumar and Helen C. Shen [9] proposed an approach in which Gabor filter is used for palm print recognition. Fang Li et al. [10] proposed an approach utilizing Line Edge Map (LEM) of palm print as the feature and Hausdorff distance a s the distance matching algorithm.

The content of this paper is organized as follows. Section III describes the steps involved in multimodal Recognition system. Section IV presents our proposed approach using Wavelet packets based approach. Section V gives the result of Wavelet packet Transform based approach on the iris and palm print database. Finally, conclusions and perspectives are given in section VI.

III. MULTI MODAL BIOMETRIC SYSTEM

A generic biometric system has 4 main modules namely a) Sensor module, b) Feature extraction module, c) Matching module, d) Decision module. In a multimodal biometric system, information reconciliation can occur in any of the previously mentioned modules as a) fusion at the sensor level where the combination of raw biometric data takes place, b) fusion at data or feature level,(data/features) where combination of different feature vectors are obtained, c) Fusion at the match score level, d) Fusion at the decision level. It is shown in figure 1.

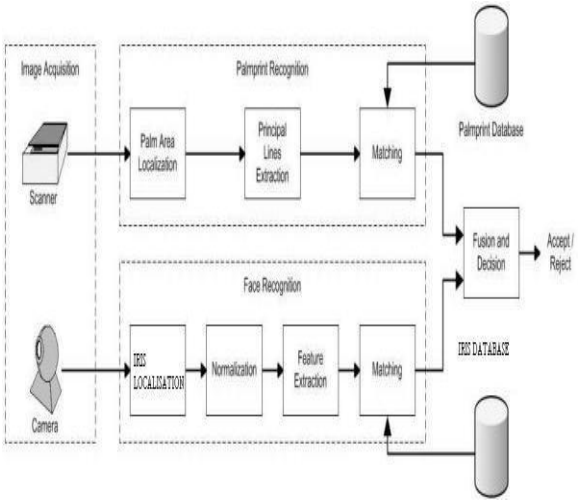

Figure 1. Scenario in a multi modal biometric system

In this paper fusion at feature level is presented. Feature vectors are obtained from iris data and palm print separately and then fused. Finally matching is performed and decision is taken,

A. Iris recognition System

An iris recognition system can be decomposed into three modules : an iris detector for detection and location of iris image, a feature extractor to extract the features and a pattern matching module for matching. The iris is to be extracted from the acquired image of the whole eye. Therefore, before performing iris pattern matching, the iris is to be localized and extracted from the acquired image.

a) Iris Localization

The first step is iris localization. Using the Integrao differential operator (IDO) (I) the iris is localized.

$$\max_{(r,x0,y0)} \left| G_\sigma * \frac{\partial}{\partial r} \oint_{r,x0,y0} \left(\frac{I(x,y)}{2\pi r} \right) ds \right| \qquad (1)$$

Where I(x,y) is a raw input image. The IDO (1) suggested by J.Daughman [1] [2] searches over the image domain (x,y) for the maximum in the blurred partial derivative with respect to increasing radius r, of the normalized contour integral of I(x,y) along a circular arc ds of radius r and center coordinates (x0,y0). The symbol * denotes convolution and G_σ ®

is a smoothing function such as a Gaussian of scale σ. It searches iteratively for the maximal contour integral derivative at successively finer scales of analysis through the three-parameter space (x0,y0,r) defining a path of contour integration. It finds both papillary boundary and the outer boundary of the iris. The results are shown in figures 2 to 5.

Figure 2. Iris Image 1

Figure 3. Iris Image 2

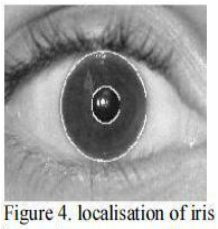

Figure 4. localisation of iris Image 1

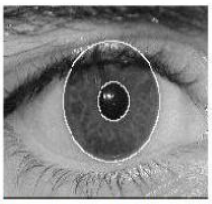

Figure 5. Localisation of iris Image 2

b) Iris Normalization

After the iris is localized the next step is normalized (iris enrollment). Using the equations (2) the iris data are extracted. Different circles with increasing radius and angle arre drawn starting from the pupil centre till it reaches near the iris coordinates. The information is extracted.

$x = c(x) – r*\sin(\Theta)$
$y = c(y) – r*\cos(\Theta)$

where c(x,y) denotes center coordinates, (x,y) denotes coordinates of the image, Θ is the angle and r denotes the radius. Figure 6 and 7 shows the extracted (normalized) iris data.

Figure 6. Normalized data (Extracted iris data) of iris image 1

Figure 7. Normalized data (Extracted iris data) of iris image 2

c) Wavelet Packet Transform (WPT Approach)

The standard discrete wavelet transform (DWT) is a very powerful tool used successfully to solve various problems in signal and image processing. The DWT breaks an image down into four sub-sampled images. The results consist of one image that has been high passed in the horizontal and vertical directions (HH), one that has been low passed in vertical and high passed in the horizontal (LH), one that has been high passed in the vertical and low passed in the horizontal (HL) and last that has been low pass filtered in both directions (LL) where, H and L mean the high pass and low pass filter, respectively. While HH means that the high pass filter is applied to signals of both directions, represent diagonal feature of the image, HL correspond to horizontal structures, LH correspond to vertical information and LL is used for further processing.

Wavelet packets Transform (WPT) is a generalization of wavelet Transform that offers a richer signal analysis. With WPT, it is possible to zoom into any desired frequency channels for further decomposition. Compared with WT, WPT offers a finer decomposition. When processing some oscillating signals, partition of low frequency parts is not fine enough. WPT can overcome this problem via decomposing high frequency components and more details obtained in WPT yield better representation of signals. As a progressive texture classification algorithm, WPT gives reasonably better performance because the dominant frequencies of iris texture are located in the low and middle frequency channels.

Biometric texture extraction with WPT and encoding procedure involves three steps:

1. Decomposition. At each stage in the decomposition part of a 2-D WPT, four output sub images are generated. The images contain approximation (A) ,horizontal detail (H), vertical detail (V) and diagonal detail (D) coefficients respectively. After 3-level WPT, an image has a quad tree with 64 output sub images, each representing different frequency channels [11]. It is shown in Figure 8.

2. Selection of sub images for feature encoding

Processing wavelet coefficients of every sub image is a fair amount of work; furthermore, some of them are representations of high frequency noise which reduce our ability to distinguish each iris. It is advisable to choose a subset of all possible sub images to make our encode process. The useful sub images with entropy criterion to make our analysis much more efficient and just as accurate using (3).

$$Entropy = -\sum_{i}\sum_{j} S_{i,j}^{2} \log(S_{i,j}^{2})$$

In equation (3) $\boldsymbol{S_{i,j}}$ is the coefficient of the sub image. It is found that sub-image 10 retains higher entropy than other sub images. Hence it is chosen as the candidate sub image for feature extraction.

3.Iris Feature encoding

A code matrix can be achieved by quantizing the coefficients of candidate sub image and LL3, HL3 or LH3 into one data element each with a suitable threshold T as shown in equation (4).

$$C_{ij} = 1 \text{ if } S_{ij} > T\,;\; C_{ij} = 0\,,\; |\, S_{ij} \,| < T\,;\; C_{ij} = -1,$$
$$S_{ij} < \text{-T}; \qquad (4)$$

Where sij is the coefficient of a sub image, cij is the corresponding code element and t is threshold is a positive number. Equation (4) has 2 abilities of de-noising and finding singular points. T is chosen as T=3 **σ** and **σ** is the variance of the noise. It is reported that the Standard Deviation of the WPT high frequency coefficients (sub-image 84) are having the good estimation of **σ** . The code matrix gives a good description of both frequency and location content of an image. The chosen sub image is called candidate sub-image.

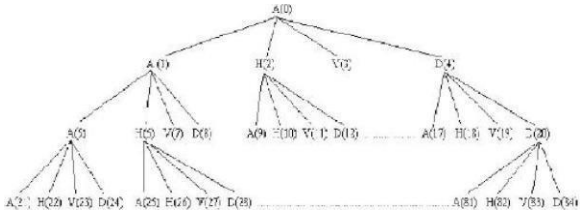

Figure 8. Wavelet packet decomposition

4. *Iris Matching* for matching the biometric codes Modified Hamming Distance HD as shown in (5) is Used.

$$HD = \frac{codeA \otimes codeB}{n} \qquad (5)$$

In equation (5) codeA and codeB are the iris codes of 2 iris to be compared, (8) denotes bit wise exclusive OR operation and n is number of bits in code A.

B. *Palm print Recognition System*

Before feature extraction, it is necessary to obtain a sub-image from the captured palm print image and to eliminate the variations caused by rotation and translation. After extracting the sub image as region of extraction by preprocessing, the texture features of the palm prints are extracted by Gabor filters decomposition scheme. The Gabor filter is an effective tool for texture analysis and has the following general form.

$$G(x, y, \mu, \omega, \theta) = \frac{1}{2\pi\sigma^2} \exp\left(\frac{-x^2 + y^2}{2\sigma^2}\right) \exp(2\pi i)(\mu x \cos\theta + \mu y \sin\theta) \qquad (6)$$

where i = -1, u is the frequency of the sinusoidal wave, q controls the orientation of the function and s is the standard deviation of the Gaussian envelope. The sample point in the filtered image as shown in Figure 9 is coded in to two bits (b" bi) . Depending on the phase value of complex vector generated, using table 1 phase bits are generated. Thus palm print code of 960 bits is generated.

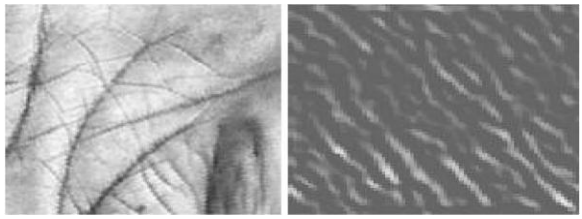

Figure 9. Preprocessed pal m print and extracted palm print features

IV. MULTI MODAL BIOMETRIC SYSTEM

In this particular approach, the iris images are encoded using wavelet packets to formulate a template. The palm print images are encoded using Gabor filters. Instead of traditional multi resolution analysis (MRA) scheme, a novel lifting technique is used to construct the biorthogonal filters[8].

The main advantage of this scheme over the classical construction is that it does not rely on the Fourier transform. Also, it allows faster implementation of wavelet transform. The basic idea behind the lifting scheme is shown in Figure l0.

It starts with trivial wavelet, the "Lazy wavelet"; which has the formal properties of wavelet, but is not capable of doing the analysis. The lifting scheme then gradually builds a new wavelet, with improved properties, by adding in a new basis function.

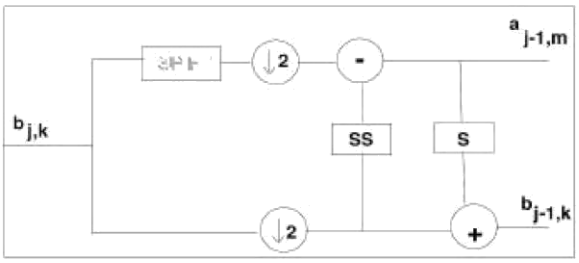

Figure 10. Lifting scheme

The lifting scheme then gradually builds a new wavelet, with improved properties, by adding in a new basis function. The lifting scheme can be visualized as an extension of the FIR (Finite Impulse Response) schemes [8].

It first calculates the Lazy wavelet transform, then calculates the $a_{i-1,m}$ and finally lifts the b_{j-1-k}. It is known that any two-channel FIR sub band transform can be factored into a finite sequence of lifting steps. Thus, implementation of these lifting steps is faster and efficient. The biorthogonal filter family is shown in Figure 11 [11]. The frequency content of the resulting coefficients is adjusted each time to get separated band structure.

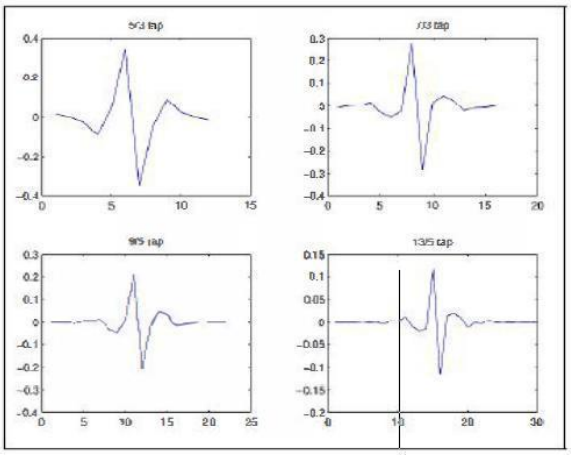

Figure. I I Biorthogonal filter family

For fusion of feature vectors from iris and palm print concatenation and shifting technique is used. In this work we have used Symlets and Biorthogonal as mother wavelets for constructing iris feature vector. We have decomposed the normalized image up-to third level of decomposition. In order to create the feature vector we tried different combinations of LH3, HL3, and HH3 with candidate sub-images (of iris and palm print). The results obtained from different combinations are compared to find the best. The binary feature vector that is generated by quantizing the feature vector obtained by the combination of LH3, HH3 with the candidate sub-image is found suitable for encoding in our work.

V. RESULTS

From UBIRIS database, 8 diverse iris pictures of 30 people are taken (240 specimens of iris) and code grid is shaped. From UBIRIS database of palm print, 8 diverse palm pictures of 20 people are taken and code grid is framed. By link and moving the element vector s are melded. At the point when another iris and palm picture are displayed as an information, the code grid of the pictures is discovered. Utilizing the changed hamming separation, the example coordinating is performed. In light of this esteem, the class to which the new picture has a place with is figured. With this data the False Acceptance Ratio (FAR) and False Rejection Ratio (FRR) for each class are figured for testing pictures. The acknowledgment execution of iris include alone utilizing wavelet bundle change is given in table 1. The computed False Acceptance Ratio (FAR) and False Rejection Ratio (FRR) utilizing Gabor wavelets are given in Table 2.

TABLE I. RECOGNITION PERFORMANCE OF IRISFEA TURE VECTOR USING DIFFERENT MOTHER WAVELETS

Recognition performance		
Wavelet type	*Accuracy in %*	*Feature vector length*
Sym2	*81.50*	*288*
sym3	*90.50*	*480*
sym4	*89.00*	*460*
sym6	*90.00*	*640*
sym8	*91.50*	*960*
bior 1.5	*92.00*	*640*
bior 2.6	*85.00*	*480*
bior 3.9	*93.00*	*1280*

TABLE II. RECOGNITION PERFORMANCE OF PALM PRINT FEATUREVECTOR

Palm print recognition performance						
Threshold	*0.82 76*	*0.75 89*	*0.66 91*	*0.56 46*	*0.76 48*	*0.63 99*
FAR	*89%*	*73%*	*40%*	*14%*	*76%*	*31%*
FRR	*6%*	*23%*	*49%*	*77%*	*20%*	*57%*

TABLE Ill. PERFORMANCE OF FEATURE VECTOR FOR MULTI MODAL BIOMETRIC

Modality	Accuracy in %	Feature vector length
Iris	91.50	960
Palmprint	89.46	960
Combination of Iris and Palmprint	94.42	960

The Performance of the proposed iris recognition system using Symlets and biorthogonal wavelets are shown in the figures 12,13. In these figures classes refer to the image classes of iris images. Class 1 refers to the user 106 and class 8 refers to user113.

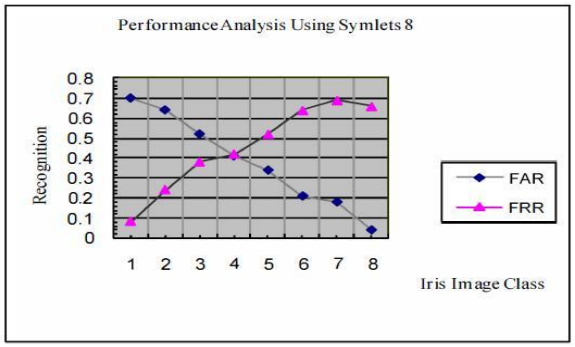

Figure. 12 Iris recognition performance using symlets

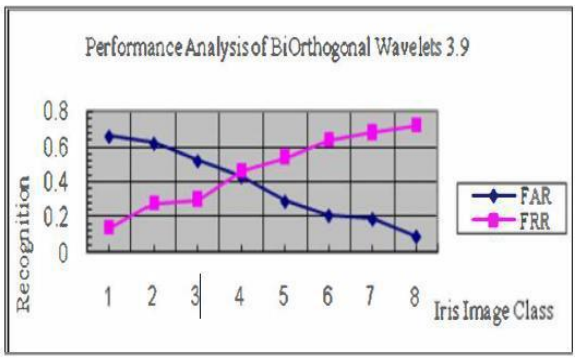

Figure.13 Iris recognition performance using Biorthogonal wavelets

From the figures 12 and 13 it can be seen that the EER value of recognition system decreases as the mother wavelet chosen is varied. For Symlets wavelets the EER value is 0.41 whereas for biorthogonal wavelets the EER is 0.39. The accuracy of the proposed system varies when different feature vector isc hosen. The performance curve of the system in term of accuracy for feature vector using various mother wavelets are is shown in figure 14.

The performance analysis of palm print recognition system using Gabor filters are shown in figure 15. By choosing the 3rd scale and 3'd orientation filtered image as candidate image for encoding, the FAR and FRR are calculated and EER obtained is 0.42%. This value is found to be high. To improve the EER value, further the palm print input image is filtered using other scales. When Gabor filter of scale 6 and orientation 3 is used, low EER rate obtained as 0.26%. It is shown in figure 16.

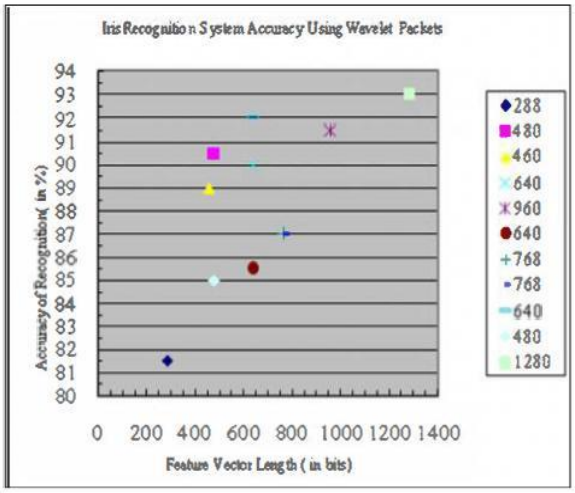

Figure.14 Iris recognition system performance in terms of feature vector length

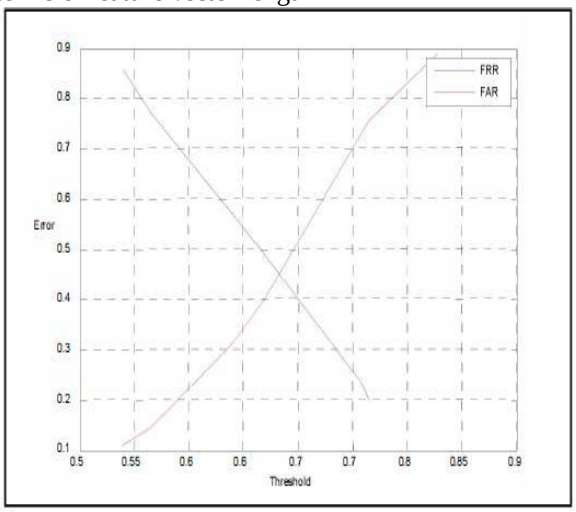

Figure.15 performance analysis of palm print recognition using Gabor filter

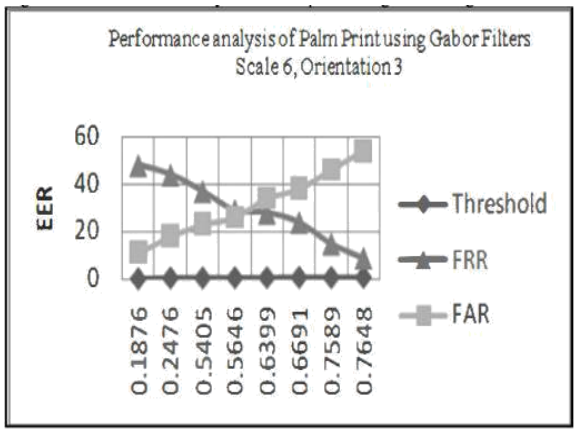

Figure 16. Performance analysis of palm print recognition using Gabor filters with scale 6, orientation 3

VI. RESULTS

The exploratory outcomes obviously show that the element vector comprising of linking the hopeful sub picture, LH3 and HH3 (shaping iris highlight vector) and third introduction of sixth scale deteriorated palm print include vector gives better outcomes. By the combination of coordinating of palm print and iris highlight vector, score of general acknowledgment is made strides. Then again, the Symlets wavelet is Particularly reasonable for executing high-precision iris check ID frameworks, as highlight vector length is in any event contrasted with different wavelets. The Coiflets wavelets gives better EER execution contrasted with other wavelet parcels. Be that as it may, the component vector estimate is minimal high contrasted with biorthogonal wavelets. For a diminishment of 3% exactness, the length of the component vector and no of bits required to speak to the iris mark is decreased significantly on account of biorthogonal wavelets. The bior3.9 wavelet gives an exactness of 93.00% however the component vector length is around 5 times bigger contrasted with include vector acquired utilizing Symlets wavelet By joining the iris and palm print acknowledgment conspire the precision of the acknowledgment is enhanced .

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DESIGN OF NOISE FREE FILTER FOR SERIAL DATA COMMUNICATION USING MEJORITY VOTER CONCEPT

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Abstract

The present study explains structural design of UART on the basis of Advanced RRS filter. UARTs are used for asynchronous serial data communication between remote embedded systems. If channel is noisy then, serial data bits get corrupted during transmission. The UART core described here, utilizes Advanced RRS filter to remove noisy samples. Input signal is directly sampled with system clock and samples are accumulated with a window size. The window size is user programmable and it should be set to one fifth of required bit period. The intermediate data bit is decoded using magnitude comparator. A majority voter is used to retrieve actual data bit from five intermediate data bits. The advantage of this architecture is that baud rate is decided by the window size so there is no need of any external "timer module" which is normally required for standard UARTs. VHDL language used to implement the modules and design of The Advanced RRS filter with window size of M. This project implementation includes many applications in wireless data communication Systems like RF, Blue tooth, WIFI, ZigBee wireless sensor applications. Total coding written in VHDL language. Simulation in ISE Simulator, Synthesis done by XILINX , Spartan-3E

Keywords: Serial data, Clock, Samples, Baud Rate, Noise

1. Introduction

(UART) is used for asynchronous serial data communication between remote embedded systems. Standard UART cores utilize five mid-bit samples to decode the serial data bit and the sampling rate is derived from external timer module. But if the physical channel is noisy then data bits get corrupted during transmission and it leads to wrong data decoding at receiver. To overcome the noise problem a digital low pass filter based architecture is proposed in this paper.

Recursive Running Sum (RRS) is simple low pass filter; it can be used to remove noise samples from data samples at receiver [5]. Serial receive data signal is directly sampled with system clock and samples are fed to

RRS filter. The window size of the filter is user programmable and it decides baud rate.RRS filter hardware implementation is described in section-2. Window size selection criteria are described in section-3. The UART Architecture is described in section-4 while section-5 gives simulation results and comparison with standard UART core. The robust UART core described here is designed using VHDL and implemented on Xilinx FPGA.

2. RRS Filter Implementation

The Recursive Running Sum (RRS) filter with window size of M is described by following equations.

$$H(z) = \frac{1 - z^{-M}}{1 - z^{-1}}$$

$$y(n) = x(n) + y(n-1) - x(n-M)$$

The hardware realization of the above equation is as shown in the Figure-1. It requires a Adder, subtracter, a unit delay and a M samples delay element. The window size (M) is related to baud rate which is user programmable. So M is variable, if a 16 bit register is used to hold value of M, it can have values from 0 to 65535. The hardware implementation of variable delay with above range would require 65535 D flip-flops and large number of combinatorial logic for MUX and selection logic implementation. So this implementation is not feasible for FPGA or ASIC platform.

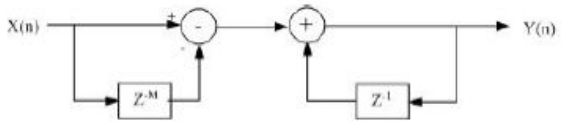


Figure-1 Hardware realization of RRS filter

The Other approach for hardware realization of RRS filter using a factor of M decimator is shown in Figure-2. It requires a Adder, subtracter, two unit delays and a down sampler of factor M. The implementation of down sampler requires a 16 bit counter and a magnitude comparator which is much simpler than previous approach. So this

approach is selected for UART implementation.

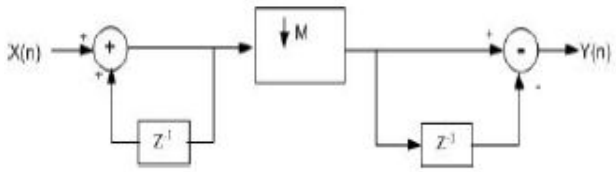


Figure-2: Implementation of RRS using down sampler

The other redused approach for hardware realization of RRS filter using one adder, one unit delay element and a Down sampler only is shown in Figure-3. Normally these Reduced RRS filter called as a RRS filter, in all over the paper, for convenient.

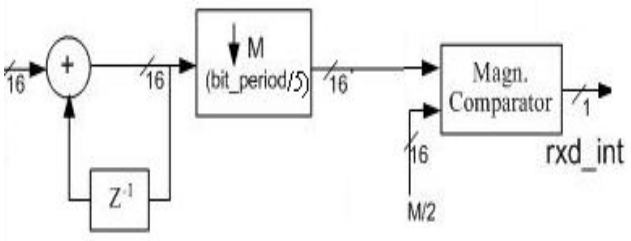


Figure-3 Reduced RRS filter

3. Window Size Determination

The selection of window size (down sampling factor-M) is important for correct data decoding. The input data signal (rxd_in) is sampled at system clock and fed to RRS filter as input x(n), output data samples y(n) are available at the interval of M samples because of the down sampler. For application of the above filter in the asynchronous communication where data bits are transmitted asynchronously, the offset between window and start bit is important. When the window size (down sampling factor-M) is equal to bit period, different scenarios of offset between window and start bit is shown in the figure-4.

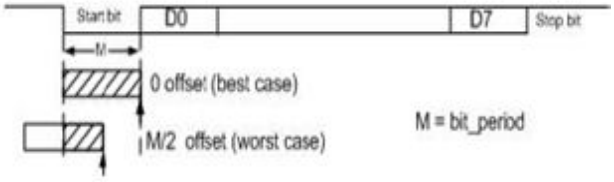
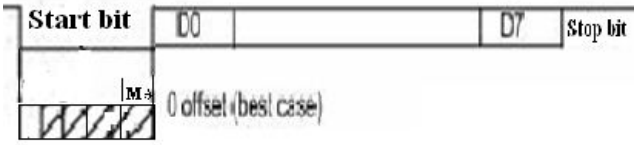


Figure 4: Window offset when M = bit_period

The offset between window and start bit can vary from 0 to M/2. In the worst case offset of M/2, half of the samples in current window are from previous bit and remaining half samples are from current bit, so this will lead to wrong decoding of the data bits. To overcome above problem the window size should be chosen smaller than bit period so that multiple windows are available in one bit period. Odd number of windows should be chosen in one bit period so that a majority voter can be used to decode a bit from the odd number of the samples. From above considerations a factor of 3 is chosen so that 3 windows are available in one bit period.



window size=bit period/5

For this case, different scenarios of offset between window and start bit is shown in the figure. So five samples are available in a bit period. In the worst case also three full windows are available in one bit period so three out of five samples are correct is shown in Figure-5, so bit will be correctly decoded by the majority voter.

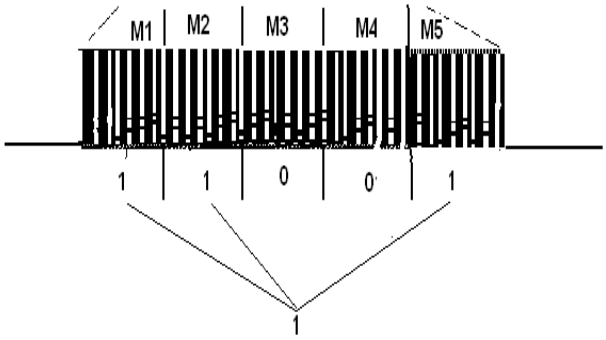


Figure-5 Majority voting process

Thus window size equal to one fifth of bit period is optimum selection.

4. UART Architecture

The architecture of UART receiver is shown in the figure-6. The incoming rxd_in signal is sampled at system clock. These one bit samples are padded with zeros and made a 16 bit number x(n). It is fed to recursive running sum filter with window size equal to one fifth of bit period. The output of RRS filter is a 16 bit value which is number of ones in the window duration. It is fed to magnitude comparator, where it is compared with M/2, if the value is greater than M/2 then the window samples (intermediate

data bit) is decoded as '1' otherwise '0'. Thus 16 bit value is converted back to 1 bit.

$$\text{rxd\_int(n)} = \text{'1' when } \sum_{k=0}^{M-1} x(n-k) \geq \frac{M}{2}$$

'0' otherwise.

This intermediate data bit is fed to 3 stage shift register.These 3 bits are used to detect start bit and they are also fed to majority voter for data bit and stop bit decoding. The further process is similar to standard UART,there is a 8 bit shift register to hold the data byte and the finite state machine generates control signals for the shift register and other modules. Transmission from the UART is similar to standard UART, using a shift register. The baud rate for serial communication is decided by the window size (M), so there is no need of any external timer for baud rate generation unlike standard UART. The baud rate equation is as follows.

$$Baud\_rate = \frac{clock\_freq}{M * 5}$$

Where, clock_freq is system clock frequency, M is window size, (1 to 2^{16})

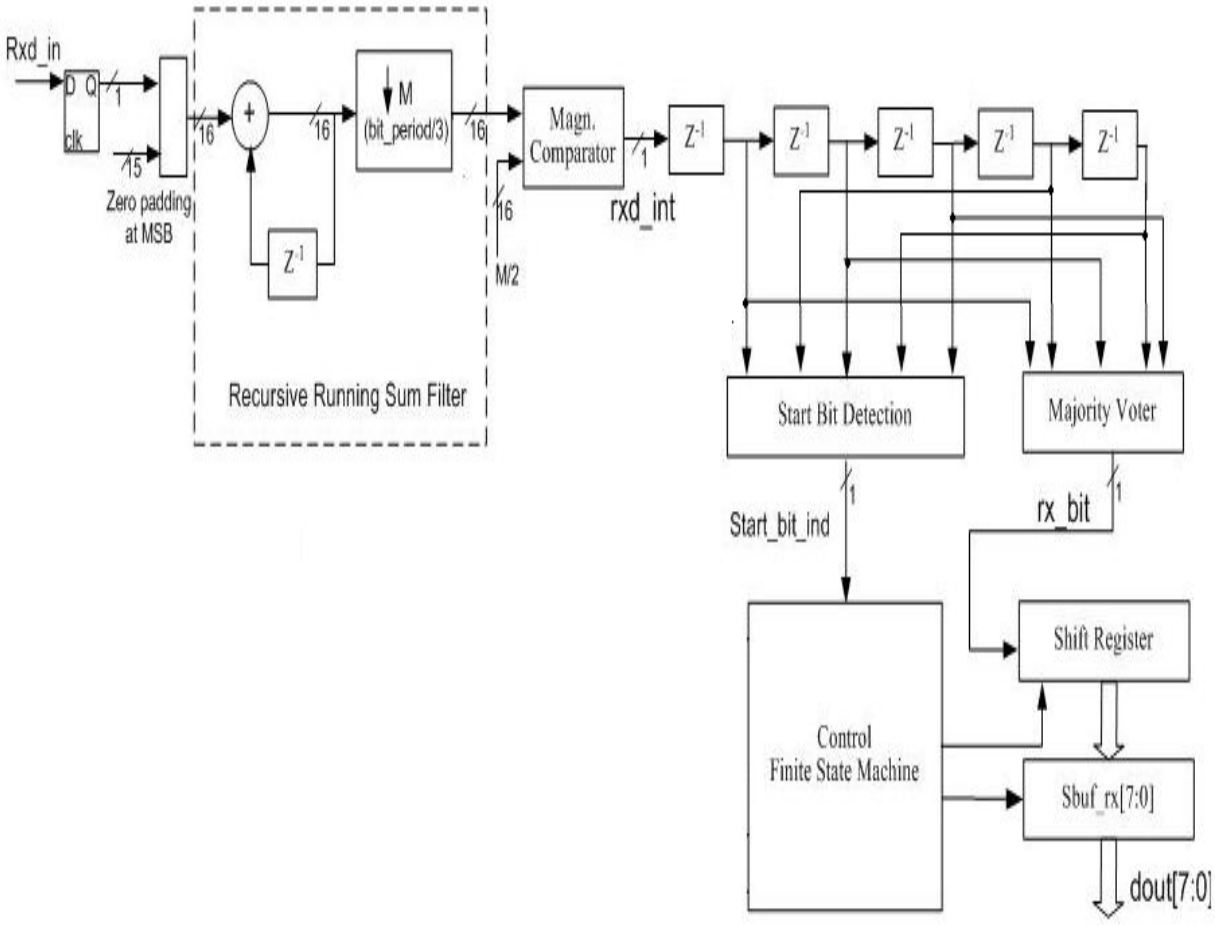
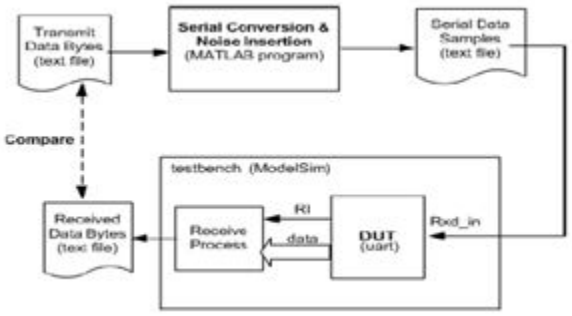
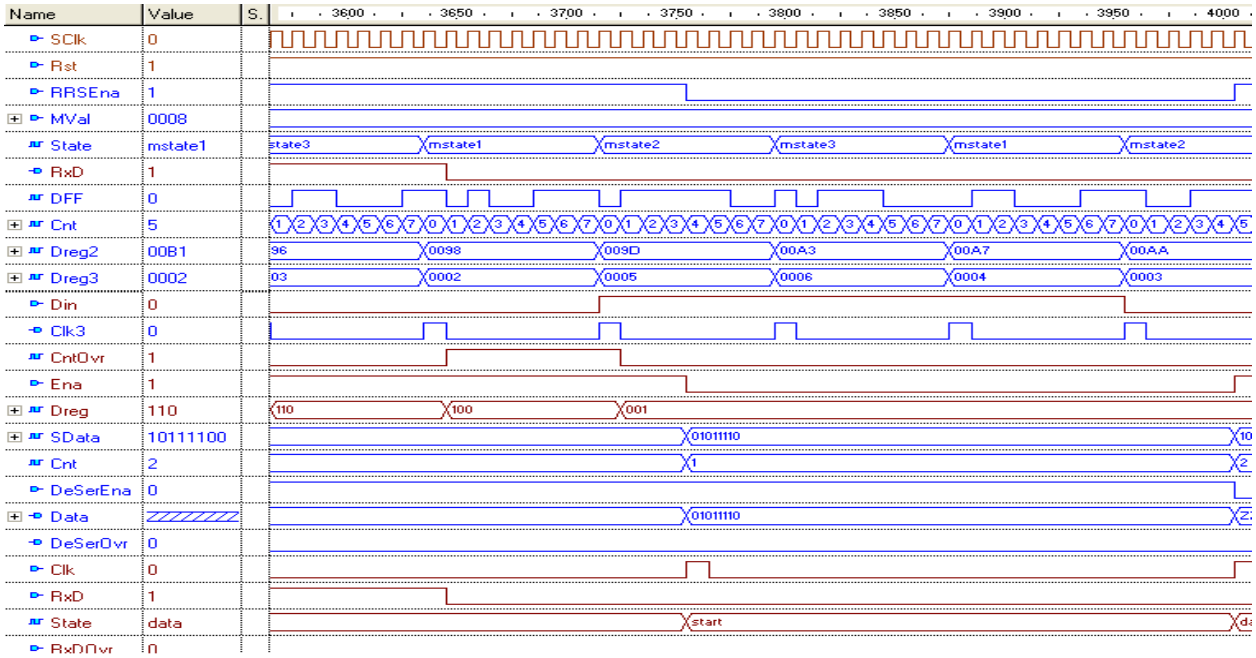


Figure-6 Reduced UART Architecture with **5** Windows & only one delay element

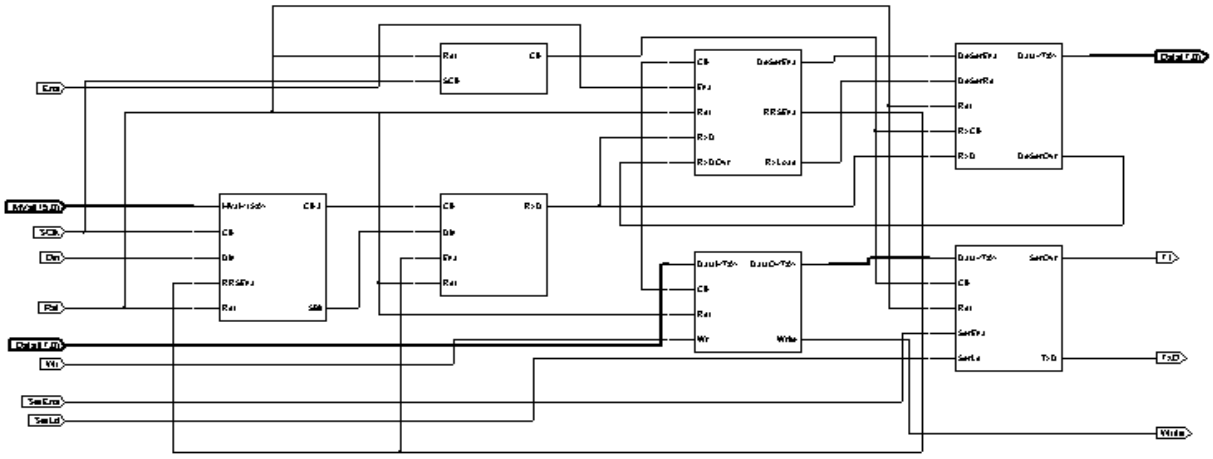
5. Results

The UART core described here has been designed using VHDL. Noise insertion is done using MATLAB® program. The core has been simulated using Xilinx ISE simulator® while hardware implementation is done on Xilinx FPGA.





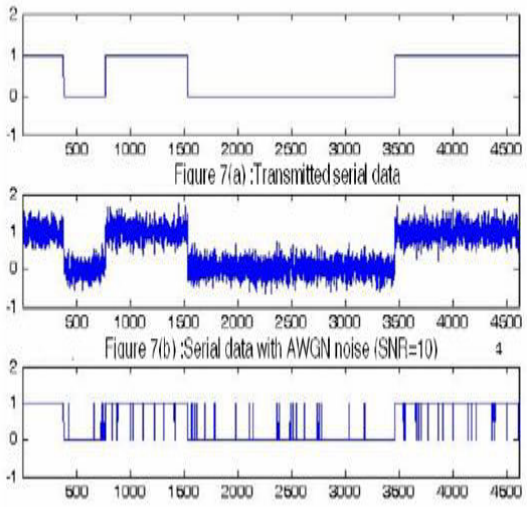
RRS UART Simulation Results



RRS UART RTL Schematic

5.1 Test Methodology

Figure-6: Test Methodology The test methodology is described in the figure 6, Serial data to be transmitted to UART is written in a text file. Typically randomly generated few thousand data bytes are written in the text file. A MATLAB® program converts parallel bytes to serial and adds start and stop bit, it also adds AWGN (Additive White Gaussian Noise) at different SNR (Signal to Noise Ratio) level.Figure 7 shows MATLAB® simulation results, figure -7(a) shows transmitted serial data, figure-7(b) shows serial data with AWGN noise, figure-7(c) shows serial data samples at receiver, these samples are written in a text file and give as input to VHDL test bench. The UART is instantiated in testbench and serial data samples from the text file is fed to input rxd_in. The output bytes from UART is written in a text file. Figure -8 shows ISE® simulation waveform, rxd is input serial data which contains lot of noise while rxd_bit_decode is output of majority voter and sbuf_rx_reg is 8 bit data output.



rrs5project Project Status (05/13/2002 - 01:34:52)			
Project File:	rrs5project.ise	**Current State:**	Placed and Routed
Module Name:	RRSUART	**• Errors:**	No Errors
Target Device:	xc3s400-5pq208	**• Warnings:**	7 Warnings
Product Version:	ISE 10.1 - WebPACK	**• Routing Results:**	All Signals Completely Routed
Design Goal:	Balanced	**• Timing Constraints:**	All Constraints Met
Design Strategy:	Xilinx Default (unlocked)	**• Final Timing Score:**	0 (Timing Report)

rrs5project Partition Summary	[-]
No partition information was found.	

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	112	7,168	1%	
Number used as Flip Flops	110			
Number used as Latches	2			
Number of 4 input LUTs	145	7,168	2%	
Logic Distribution				
Number of occupied Slices	104	3,584	2%	
Number of Slices containing only related logic	104	104	100%	
Number of Slices containing unrelated logic	0	104	0%	
Total Number of 4 input LUTs	191	7,168	2%	
Number used as logic	145			
Number used as a route-thru	46			
Number of bonded IOBs	32	141	22%	
IOB Flip Flops	1			
Number of BUFGMUXs	1	8	12%	

Summary and Synthesis Report

5.3 FPGA Implementation

The robust UART described in this paper has been Implemented on Xilinx XC3s400 FPGA [9]. The thus UART core occupies very small area as per above synthesis report.

6. Conclusion

This paper describes an Advanced UART architecture based on RRS filter for removal of channel induced noise. The baud rate of serial communication is decided by the window size of the filter, which is user programmable and should be set to one fifth of required bit period, it does't require any external module for baud rate generation.
Comparison of simulation results shows that the performance of Advanced UART has far better performance than standard UART at higher noise levels and based on synthesis results area occupied on FPGA very low.

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MEDICAL IMAGE DENOISING USING DUAL-TREE WAVELET COMPLEX TRANSFORM SHRINKAGE

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ABSTRACT

In this paper, an efficient DT-CWT based method for medical ultrasound images despeckling is presented. The ultrasound images are often deteriorated by speckle noise, this noise is a random granular texture that obscures anatomy in ultrasound images and degrades the detectability of low-contrast lesions. Speckle noise occurrence is often undesirable, since it affects the tasks of human interpretation and diagnosis.Different from many other schemes with wavelet transform are used on one side in which the studies have dealt more with the standard DWT case. However, the Discrete Wavelet Transform (DWT) has some disadvantages that undermine its application in image processing.In this study we investigated a performances complex wavelet transform (DT-CWT) combined with Bivariate Shrinkage.The proposed method was tested on a noisy ultrasound medical image, and the restored images show a great effectiveness of DT-CWT method compared to the classical DWT.

Keywords

Medical image denoising, Medical ultrasound , speckle noise, Dual-tree wavelet transform , Complex wavelet , Bivariate shrinkage

1. INTRODUCTION

We Ultrasound echography technique is one of the most widely used in medical analysis and diagnosis domain, since it permits to observe all kinds of soft tissues in a non-invasive way.

The interpretation of ultrasound images remains a difficult task due to the inherent speckle noise in the images which affects the detectability of low contrast lesions.

The speckle noise is usually described than it is created by complex interference of ultrasound echoes and variations in tissues attenuation, propagation and scattering properties make echoes interfere in complex ways [1].

Many techniques have been developed in the goal to restore ultrasound images such as adaptive filters [2] anisotropic diffusion [3] [4][5] and wavelet shrinkage [6] [7].

The last one have become more prevalent in the transform domain despeckling community owing to their excellent spatial localization, frequency spread and multiresolution characteristics, which are similar to theoretical models of the human visual system (HVS) [8].

Many challenges have been made to remove this noise using wavelet transform [9][10]. A comparative study have been reported by Mariana Carmen and al where it has been proved that the discrete wavelet transform gives a much better result than the spatial filtering methods for despeckling ultrasound images[11].

In the wavelet domain, the Discrete Wavelet Transform (DWT) have limits and major disadvantages that undermines its application for some image processing as; lack of shift invariance, poor directional selectivity for diagonal features and others [12].

Being motivated by applications and advantages of wavelet transform domain, considering these previous results in the literature, in the ultrasound images denoising, we focus our approach by working to put the extension in Dual-Tree Wavelet transform (DT-CWT) case, to its best directional selectivity and using steps of pre- and post- processing, providing significant stake in the study of statistical noise[8].

The most promising Dual-Tree wavelet Transform (DT-CWT) proposed by N. Kingsbury, used two classical wavelet trees developed in parallel with filters forming (approximate) Hilbert pairs looking into the benefits such as good directional selectivity in two-dimensions (2D) approximate shift invariance, the orientation of the wavelets and perfect signal reconstruction (PR) have come to resolve all these problems [13].

To restore the ultrasound images in the complex wavelet domain is very easy and provides the spatially varying spectral characteristics required for de-noising in additional the existence of dual tree is the advantage in the study of statistical noise.

In this, an efficient DT-CWT combined with a Bivariate estimator based method for despeckling ultrasound medical images is proposed.

2. SPECKLE NOISE STUDY

The presence of scatters smaller than the wavelength creates the so-called speckle noise. It is a random, deterministic image patterning caused by the interference of the sub-resolution scattered echoes. Its texture does not contain information about the underlying tissue.It mean brightness does in principle reflect the brightness of the tissue.

Speckle has been widely studied in the literature. In this context Pioneering and distinguishing works have been done by Goodman [14].

The first discussion of ultrasound speckle using statistical optics can be found by Burckhardt [15]. A classic paper on the second-order statistics of speckle is by Wagner et al. [14].

A discussion of Rician statistics in tissue characterization was being studied by Insana and al. [2].

Assuming that the statistics of the RF signal are White Gaussian and the scatters are independent.The envelope-detected signal follows a Rice distribution equation:

$$P() = \frac{}{\sigma^2}\exp\left(-\frac{^2+s^2}{2\sigma^2}\right) I_0\frac{}{\sigma^2}, \geq 0 \qquad (1),$$

Wherea is the mean scatter spacing s is the strength of a specular reflector, σ is the standard deviation of noise and I_0 is the incomplete Bessel function of order zero. The Rician PDF is parameterized by a single parameter k, which is defined as:

$$k = \frac{s}{\sigma} \qquad (2)$$

The Rician distribution reduces to the Rayleigh distribution for the special case $s = 0$, that is, when there are no bright scatters. Then the image consists in purely speckle patterning due to sub-resolution scatters. The Rayleigh distribution is defined in [2] by equation:

$$P() = \frac{}{\sigma^2}\exp\left(-\frac{^2}{2\sigma^2}\right), \geq 0 \qquad (3)$$

However log-compression changes the characteristics of the signal probability distribution.

In particular, it affects the high intensity tail of the Rayleigh and Rician more than the low intensity part. Strictly the log-compression on Rician document is a Fisher-Tippett distribution is expressed as:

$$P() = \frac{\exp(-z)^2}{\beta} \qquad (4)$$

And

$$z = \exp\left(\frac{-u}{\beta}\right) \qquad (5)$$

However, some approximations can be made. If it is considered as Gaussian, Kao et al. [16] demonstrate that speckle noise distribution can be approximated as an additive colored Gaussian PDF. Abd-Elmoniem et al. assume that in a reasonably high number of scatters; that is not too low SNR additive white Gaussian noise is a good approximation. From our experiments, the additive colored Gaussian noise is the most satisfying model.

Many techniques have been proposed to reduce speckle including spatial filtering [3][5][17]18] temporal integration [19] frequency compounding [20] and spatial compounding [21][22].

Generally speckle is modeled as multiplicative noise and its reduction is done by multiplying wavelet coefficients by speckles reduction ratio.

The mathematical expression for a signal observed at point whose coordinates $(x\ y)$ in the ultrasound image is as follows: Assuming that speckle noise to be fully developed and independent of 'f' so we can write:

$$g(x,y) = f(x,y).\mu(x,y) + \varepsilon(x,y) \qquad (6)$$

With $g(x\ y)$, $f(x\ y)$ and $\mu(x\ y)$, where (x, y)$^{-th}$ pixel's ultrasound image andthe corresponding tissue-reflectivity at the speckle noise.

$\varepsilon(x\ y)$ is an additive noise [23] and can be ignored in practice.

$\mu(x\ y)$ is a noise independent from the signal. In the following the model used for the ultrasound image is:

$$g(x,y) = f(x,y) * \mu(x,y) \qquad (7)$$

Where g is the observed intensity of the image and f is is the free noise intensity. Within homogenous regions this model offers as good approximation [24][25].

To cover the multiplicative noise an additive one the noise image is log-transformed yielding.

$$G(x,y) = F(x,y) + U(x,y) \qquad (8)$$

Where G, F and U are the logarthms of g, f and μ respectively. Now it is demonstrated that speckle noise distribution can be approximated as additive Gaussian [16]. In considering the linearity Property in the noise study as with any redundant frame analysis; when a stationary noise even if white is subject to a dual decomposition tree statistical dependencies appear between coefficients [26][27]. After applying the DT-CWT on (8), we obtain:

$$\eta\ ,\quad \eta\ ,\quad \eta\ , \qquad (9),$$

Where, $G_\eta(x,y)$, ,$F_\eta(x,y)$ and $U_\eta(x,y)$, denote $(x,y)^{-th}$ wavelet coefficient at level of a particular detail subband of the DT-CWT of G,F and U respectively and η (η= 1,2…,J).

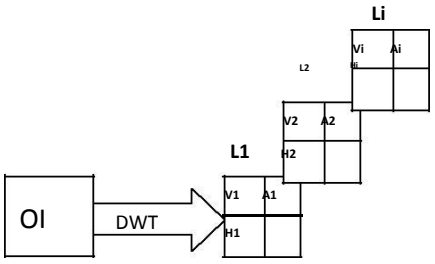
3. WAVELET TRANSFORM APPROACH

3.1 Discrete Wavelet Transform (DWT)

The implementation of an analysis filterbank for a single level 2D-DWT with the algorithm of Mallat on the decomposition of an image, with two filter banks low pass and high pass respectively .

This structure produces detailed sub-images (HH,HL and LH) corresponding to three different directional-orientation (horizontal, vertical and diagonal) and a lower resolution sub-image (LL) [28].

The filter bank structure can be iterated in a similar manner on (LL) channel to provide multilevel decomposition as illustrated in Fig. 1.



OI :orignal image

Li :level

V :vertical detail or (LH)

H : horizontal detail or (HH)

D :diagonal detail or (HL) and (A :LL:Approximation)

A : approximation

Figure 1.Multilevel decomposition hierarchy of image with DWT

The classical discrete wavelet transform (DWT) provides a means of implementing a multiscale analysis based on a critically sampled filter bank with perfect reconstruction [21]. However questions arise regarding the good qualities or properties of the wavelets and the results obtained using these tools; the standard DWT suffers from the following problems described as below.

-Shift sensitivity: it has been observed that DWT is seriously disadvantaged by the shift sensitivity that arises from down samples in the DWT implementation [12][13].

-Poor directionality: an m-dimension transform (m>1) suffers poor directionality when the transform coefficients reveal only a few feature in the spatial domain.

-Absence of phase information: filtering the image with DWT increases its size and adds phase distortions; human visual system is sensitive to phase distortion [16]. Such DWT implementations cannot provide the local phase information.

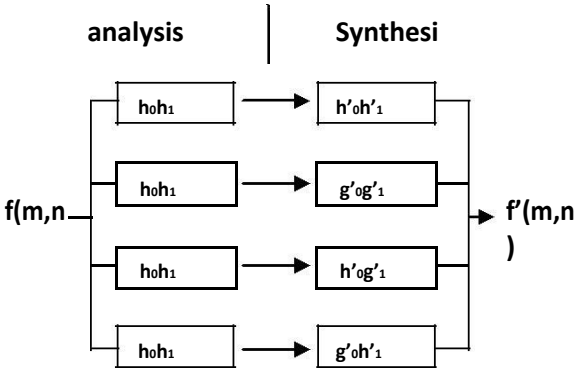
In other applicationsand for certain types of images it is necessary to think of other more complex wavelets which gives a good way because the complex wavelets filters which can be made to suppress negative frequency components. As we shall see the CWT has improved shift-invariance and directional selectivity [29].

3.2Dual-Tree Complex Wavelet Transform (DT-CWT)

The discrete and complex dual tree wavelet transform (DT-CWT) was introduced by N. Kingsburg around in 1990.

This implementation uses consists in analyzing the signal by two different DWT trees, with filters chosen so that at the end, the signal returns with the approximate decomposition by an analytical wavelet.

The dual-tree structure has an extension of conjugate filtering in 2-D case, this structure is shown in Fig. 2



Imaginary trees

Figure.2. Filterbank structure for DT-DWT

This structure needs four trees for analysis as well as for synthesis. The pairs of conjugate filters are applied to two dimensions (0 and 1), wich can be expressed as:

$$(h_0 + jg_0)(h_1 + jg_1) = (h_0h_1 - g_0g_1) + j(h_0g_1 + g_0h_1) \quad (10)$$

The synthesis of filters suitable for this structure was performed by several people.

The wavelet corresponding to the tree's "imaginary part" is very close to the Hilbert transform of the wavelet corresponding to the trees "real part" [30].

For J level decomposition, the corresponding details subbands at leven ŋ are denoted: $HL_ŋ^{real}$, $HL_ŋ^{im}$,$LH_ŋ^{real}$, $LH_ŋ^{im}$, $HH_ŋ^{real}$ and $HH_ŋ^{im}$, where ŋ = 1,2,….,J.

Because of the existence of two trees, it appears that the second noise coefficients moments from such decomposition can be precisely characterized.

The DT-CWT ensures filtering of the results without distortion and with a good ability for the localization function and the perfect reconstruction (PR) of signal.

In the noise study, as with any redundant frame analysis, when a stationary noise, even if white, is subject to a dual decomposition tree, statistical dependencies appears in coefficients [12][26][27]because of the existence of two trees.It appears that the second noise coefficients moments from such decomposition can be precisely characterized.

We observe a decorrelation between primal and dual coefficients located at the same spatial position and an inter-scale correlation which allows us to choose between several estimators taking this phenomenon into account.

If we consider an image degraded by a Gaussian n white centered additive Gaussian noise with a spectral density; the decomposition coefficients are also affected by that same noise as part of the linearity property.

The noise spectral density can be known or not, we can use a robust estimator calculated from the coefficients of the higher frequency bands [29][31][32].

With this advantage we can choose an appropriate estimator for denoising and by the case of DT-DWT we will estimate the spectral density in each tree.

4. THE BIVARIATE MAP ESTIMATOR

Implemented by LeventSendur and Ivan W. Selesnick [33] gives a performance for image denoisingexploiting the statistical dependence between wavelet coefficients and their 'parents'.

In considering these image as corrupted by additive independent white Gaussian noise with variance σ^2_b

In the multiresolution domain, if we use the orthogonal wavelet transform, the de-noising problem can be formulated as follows:

$$y = w + b \quad (11)$$

$y$being the noise coefficient, w, the original coefficient, and b, corresponding to the Gaussian independent noise. Our goal is to estimate w from y. To do this we will use an MPE (Maximum Posterior Estimator) filter [34].

Let $w_{2,l}$represent the'' parent'' of $w_{1,l}$; where $w_{2,l}$ is the wavelet coefficient at the same position as the ŋth wavelet coefficient $w_{1,l}$, but at the next coarser scale .

In wavelet domain the problem have been formulated as *follow:*

$$y_{1\eta} = w_{1\eta} + b_{1\eta} \text{and} y_{2\eta} = w_{2\eta} + b_{2\eta} \quad (12),$$

Where

$y_\eta = (y_{1\eta}, y_{2\eta})$: noisy coefficient (child and parent)

$w_\eta = (w_{1\eta}, w_{2\eta})$: original coefficients

$b_\eta = (b_{1\eta}, b_{2\eta})$: Gaussian independent noise .

If the y_1 coefficient is the considered an detail and y_2 is considered its "parent" (the detail coefficient located in the same geometric position, but calculated in the next iteration.

Each sub-band "parent" coefficient will be over-sampled for the same number of elements than that of the corresponding "children" coefficients shown in Fig3.

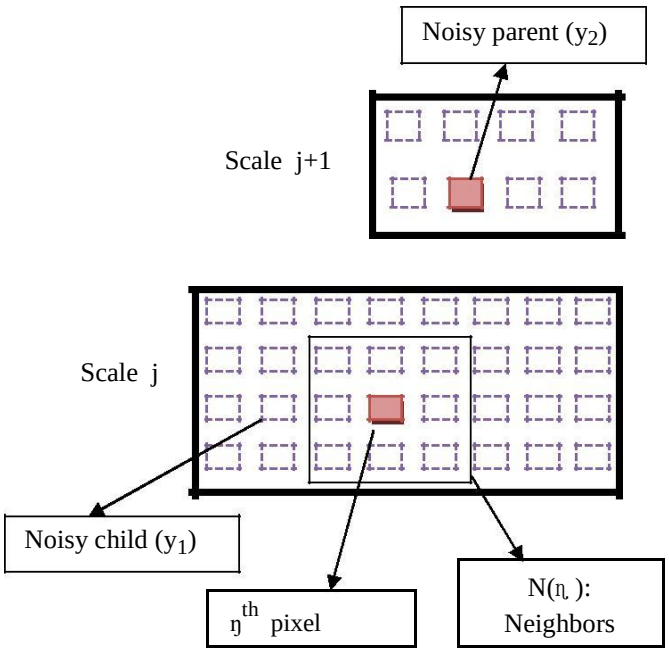


Figure3.Dependency across scales of wavelet coefficients (neighborhood N(ŋ) illustration)

The standard MAP estimator for ω given the corrupted observation y is:

$$\hat{w}(y) = \text{argmax}_w \left[\left(\ln\left(P_{b_\eta}\left(y_\eta - w_\eta\right)P_{w_\eta}\left(w_\eta\right)\right)\right)\right] \quad (13)$$

In considering than image as corrupted by additive white Gaussian noise with zero mean we can write:

$$P_{b_\eta}\left(b_\eta\right) = \frac{1}{2\pi\sigma_b^2} e^{\frac{b_{1\eta}{}^2 + b_{2\eta}{}^2}{2\sigma_b^2}} \quad (14)$$

Using the notation as:

$$f\left(w_\eta\right) - \ln\left(P_{w_\eta}{}^{\cdot}w^{\cdot}\right)) \quad (15),$$

Proposed in [34] the model for useful image in wavelet transform as:

$$P_{w_\eta}\left(w_\eta\right) = \frac{3}{2\pi\sigma^2} e^{\frac{\sqrt{3}}{\sigma}\sqrt{\left(w_{1\eta}^2\right) + \left(w_{2\eta}{}^2\right)}} \quad (16)$$

Where, w_{η} represents the set of coefficients on the ŋth of wavelet transform of useful image calculated to ŋth iteration and $w_{2\eta}$ is the set of coefficients of the useful image calculated to the next iteration.

The equation of the MAP filter defined in (13) and (14) takes the form defined in:

$$\widehat{w_\eta}(y_\eta) = argmax_{w_\eta}\{-\frac{(\ldots - \ldots)^2 + (\ldots - \ldots)^2}{2\sigma_\eta^2} + f(w_\eta)\} \quad (17)$$

This form is equivalent to the equation system:

$$\frac{\left(y_{1\eta} - w_{1\eta}\right)^2}{\sigma_b^2} + \frac{\alpha f\left(w_\eta\right)}{2w_\eta} = 0$$
$$\frac{\left(y_{2\eta} - w_{2\eta}\right)^2}{\sigma_b^2} + \frac{\alpha f\left(w_\eta\right)}{2w_\eta} = 0 \quad (18)$$

i.e :

$$\frac{\left(y_{1\eta} - w_{1\eta}\right)^2}{\sigma_b^2} + f_1\left(w_\eta\right) = 0$$
$$\frac{\left(y_{2\eta} - w_{2\eta}\right)^2}{\sigma_b^2} + f_2\left(w_\eta\right) = 0 \quad (19)$$

Considering the definition of the function f, we can write :

$$f\left(w_\eta\right) = \ln\ P_{w_\eta}\left(w_\eta\right) \quad (20)$$

Taking into account the density of probability expressed in (14), the system of equation in the form as:

$$\frac{\left(w_{1\eta} - y_{1\eta}\right)^2}{\sigma_b^2} - \frac{\sqrt{3}}{\sigma}\frac{\widehat{w_{1\eta}}}{\sqrt{w_{1\eta}{}^2 + w_{2\eta}{}^2}} = 0$$
$$\frac{\left(w_{2\eta} - y_{2\eta}\right)^2}{\sigma_b^2} - \frac{\sqrt{3}}{\sigma}\frac{\widehat{w_{2\eta}}}{\sqrt{w_{1\eta}{}^2 + w_{2\eta}{}^2}} = 0 \quad (21)$$

The nth solution of the last equations system is as follows:

$$\widehat{w_{1\eta}} = \frac{\left[\sqrt{x_1{}^2 + y_2{}^2} - \frac{\sqrt{3}\sigma_\eta^2}{\sigma}\right]_+}{\sqrt{x_1{}^2 + y_2{}^2}} . y_{1\eta} . \quad (22)$$

Which can be interpreted as a bivariate shrinkage function. Here (g)+ is defined as:

$$(g)_+ = \begin{cases} 1, & si\ g<0 \\ 0, & otherwise \end{cases} \quad (23)$$

The marginal variance $\sigma^2$is also dependent on the coefficient index ŋ and sigma for ŋth coefficient will be estimated using neighboring coefficient the region N(ŋ); where N(ŋ) is defined as all coefficients within a square shaped window that in centered at the ŋth coefficient .Fig3 [33]..

The noise variance σ^2_b is estimated from the robust median estimator as follow:

$$\hat{\sigma}_b^2 = \frac{median(|y_i|)}{0.6745} \quad y_i \in sous - band\ HH \quad (24)$$

From this observation model, one gets;

$$\sigma^2 = \sigma_\eta^2 - \sigma_b^2 \quad (25),$$

where$\sigma_{ŋ}^2$is the marginal variance of noisy observations y_1 and y_2.Since y_1 and y_2 are modeled as zero mean,$\sigma_{ŋ}^2$can be found empirically by:

$$\hat{\sigma}_\eta^2 = \frac{1}{M}\sum_{y_i \in N()} y_i^2 \quad (26)$$

'M' is the size of the neighborhood N(ŋ), than … can be estimated as :

$$\hat{\sigma} = \sqrt{\left(\hat{\sigma}_\eta^2 - \hat{\sigma}_b^2\right)_+} \quad (27)$$

4. PROPOSED EXPERIMENTAL METHOD

Consider that the speckle is a multiplicative and with the appropriate estimator (Bivariate shrinkage) method which exploits the inter-scale dependencies relations between the coefficients and their parents; we can to restore the image with best quality [34].

The key idea of wavelet shrinkage is that the wavelet representation can separate the signal from the noise.

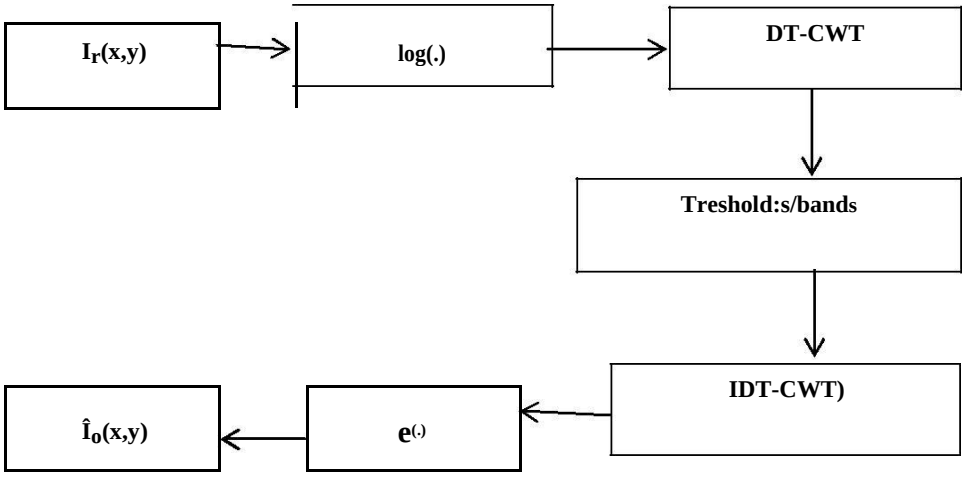


Fig 4: Diagram of despeckling proposed method.

The despeckling diagram involves the following steps shown in diagram Fig. 4:

(1)Transform the multiplicative noise into an additive, one by taking the logarithm of noised image

(2)Compute the DT-CWT(dual-tree complex wavelet) of the log-transformed image,

(3)Compute the threshold value for each pixel for Visu shrink or applying Bivariate MAP estimator, in all sub band details wavelet coefficients.

(4)We compute the IDT-CWT(inverse dual-tree complex wavelet) and take exponent for obtained the de-noised image

In the case of the classical DWT, we use the estimator on the coefficients obtained.

For DTT, as mentioned above, we used two coefficients sets obtained from the primal and dual trees and treated separately, as if we had two independent wavelet compositions, which brings us back to the application of two estimators, one on each coefficient set.

The logarithm is applied at the image for to transform a multiplicative noise an additive noise before computing it with DT-CWT .

After computing the details wavelet coefficients, will be threshold with appropriates filters chosen, we compute the IDT-CWT this data, finally we obtain the de-noised estimate image $\hat{I}_0(xy)$ after inverse logarithm.

The performance of the proposed approach is measured in one side by the quantitative measures namely MSE (mean square Error) and PSNR (peak Signal to Noise ration) between host and restored images are determined as :

$$MSE = \frac{1}{MN}\sum_{i=1}^{M}\sum_{j=1}^{N}(X(ij)\_Y(ij))^2 \quad (14)$$

And,

PSNR (dB) = 10 log10 (2552 /MSE) (15)

On the other hand, to meet the expectations of clinicians, a test has been increased to physician echograph address, on the quality of images; this test methodology is as follows:

Considering the ultrasound images were anonymized first-time summers and echographs were asked the question, whether the image presented to them is acceptable to the diagnosis and answer, yes or no.

Secondly, restored image compared to the image host for each case placed side by side, this time the original is revealed, the observer will quantify on a scale of 1-9 shown:

1: Inacceptable for diagnosis; 9: No visible difference; 7: No loss of diagnostic information; 5: In the limit the loss of information, discrete anomalies can be omitted; 3: Important diagnostic information can be omitted, degradation affects the interpretation and 1: Unsatisfactory for diagnosis.

In the other hand, to meet the expectations of clinicians, a test

5. RESULTS AND DISCUSSION

Here we present the results, the method described were applied on a two ultrasound images

Fig.5. shows a clean ultrasound imageat leftthis corrupted version atrightand a real medical noisy ultrasound image atmiddle.

Figure. 5. Tree ultrasound noised images (a $_0$.:clean ultrasound image left,b.his noisy image and a. ultrasound noisy image)

The first set of image is obtained by corrupting a clean ultrasound medical image pixels with noising having various standard deviation (ao,b)and the second speckled image is a ultrasound medical image obtained from (www.ee.nmt.ed).A performance of this approach is compared using forward wavelet transform combined withVisu-Shrinkage and Bivariate Shrinkage for each case.

In considering the two cases of despeckling,it is clear from the performance of tables and figures that despeckling capability of CWT(namely DT-CWT) is superior than standard DWT.
In both cases, Visu Shrinkage filtering [36] performs poorer whereas Bivariate Shrinkage performs better.
For each case the performance results for noise conditions as follows:
The first results exhibits better contrast in those areas, are the results obtained with Bivariate shrinkage Fig.6 for each ultrasound medical images.
The result in each figure are presented in the order follow as: DWT at left, real DWT in middle and CWT at right.

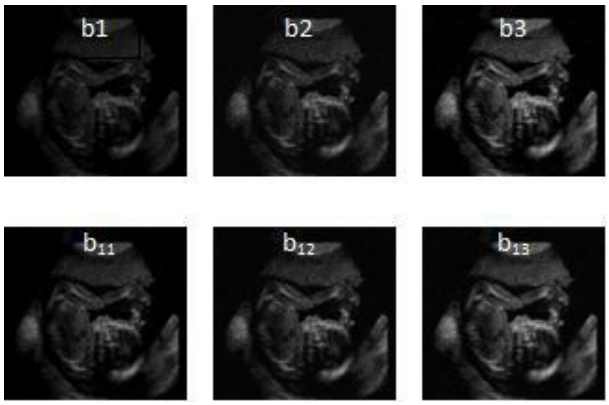


Figure. 6.Shows despeckled medical images with Bivariate Shrinkage (above) and Visu Shrinkage (below); $b_1$and b_{11} shows a poor contrast, in general the speckle is efficiently reduced and structures are enhanced with almost no loss or noticeable artifact in other images.

The results of these experiments are confirmed it, in Table I**.** Fig.6.a1and b1 shows a poor contrast, in general the speckle is efficiently reduced and structures are enhanced with almost no loss or noticeable artifact in other images of Fig.6. The results of these experiments are confirmed it, in Table 1.
For the noisevarianceestimated in order 0.04 in the real speckled medical image, the PSNR values are shown in Table 1, it can be observed that a combined DT-CWT and Bivariate shrinkage gives better results.

TABLE.1.PSNRs VALUES BETWEEN REAL SPECLED IMAGE(..0.04) AND IMAGES DESPLECKING WITH BIVARIATE SHRINKAGE AND VISUSHRINKAGE.

Real medical ultrasound imge	BIVARIATE SHRINKAGE(,PSNR en dB)	VSUSRHINKAGE (PSRRen dB)
DWT	27.92	26.96
Real DWT	29.145	28.08
CWT	**30.837**	**30.01**

Fig.7, illustrates that, compared to other decompositions, the DT-CWT in CWT version leads to better quality results with fewer artifacts. It can also be seen ,it preserves thin lines or diffuse with DWT. By observed the PSNR values in Table 2, we can confirm the superiority of DT-CWT combined with Bivariate Shrinkage than with Visu Shrinkage.

TABLE.2.PSNRs VALUES BETWEEN NOISED IMAGES HAVING VARIOUS STANDARD DEVIATIONS AND IMAGES DESPLECKING WITH VISU SHRINKAG (above) AND BIVARIATE

Noise Variance	0.02	0.03	0.04
DWT	27.85	24.19	23.89
Real DWT	30.75	29.13	28.02
CWT	**31.21**	**30.51**	**29.02**
CWT	**32.29**	**31.61**	**30.03**
Real DWT	30.60	30.01	26.10
DWT	28.15	26.48	25.70

SHRINKAGE (below).

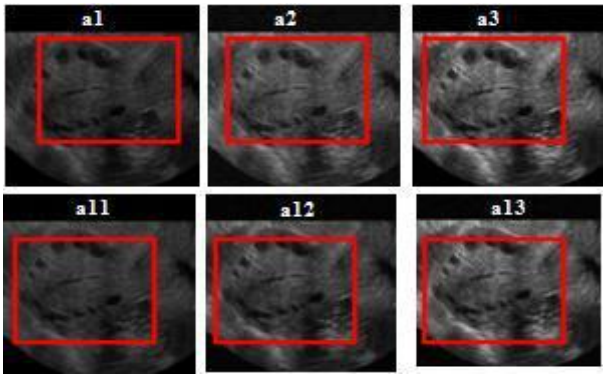


Figure7.shows the despeckled (corrupted) images with Bivariate Shrinkage (ebove) and Visu Shrinkage (below), it's shown a strong contrast ,with DWT, admissible results with RDWT and better for CWT.

In comparison the despeckling or thresholding methods chosen, it may be noted that the poorer performances are obtained with DWT, which remains well below the Bivariate Shrinkage.The results are shown in quite similar as shown in Fig 8& 9. Where the graph shows this superiority.

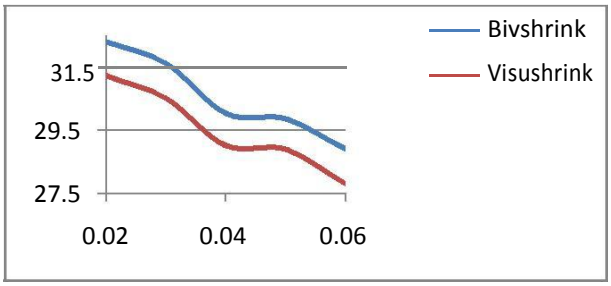


Fig8. Comparison Chart of PSNR of DT-CWT applying with Bivariate estimator and VisuShrinkage in the set of corrupted medical ultrasound images

In additional for the test result it shows the following observation for each case**:**
In case where original image is revealed, we have the following result:
Each ultrasound medical images were considered acceptable for diagnosis by all observers for all DT-CWT in CWT and real version with each estimator.
In case where original image is revealed, we have the following result:
Real ultrasound spekled image: 75% of observers found no significant loss of diagnostic information by real DWT and CWT.
An observer too suggested that the images DWT are degraded to be retable with Visu Shrinkage.
Corrupted image: an observer has seen a restored image with DWT recorded 5. Overall the test result supports the previous confirmations in all case.
All observers agreed on the absence of significant loss of diagnostic information for real DWT and CWT images with the Bivariate estimator Figures Shown.

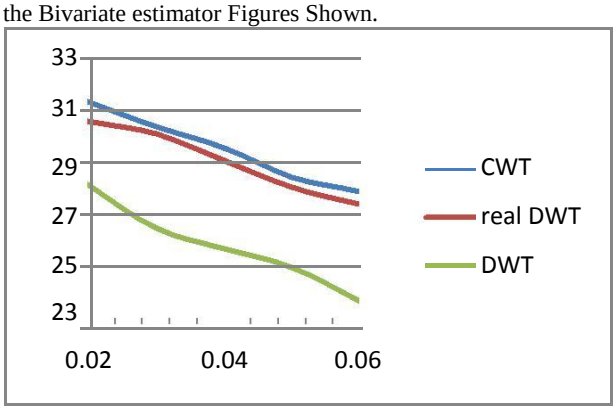


Fig9. Comparison Chart of PSNR of forward wavelet transforms applying in the set of corrupted medical ultrasound images with Bivariate estimator.

6.CONCLUSION

We developed and implemented a technique to combine DT-CWT domain and Bivariate shrinkage from different ultransoud medical images to reduce noise and restored the image degraded by this speckle. the presented combined techniques may permit improving the performance of despeckling algorithm.
CWT, which showed to be best in image despeckled did not show the same degree of improvement as in ultrasound medical images for the combined with VisuShrinkage application he experimental results show that the proposed method considerably improves the image quality without generating any noticeable artifact, and provides an additional better performance compared the existing algorithm in the literature.
Noise within ultrasound images was reduced in some techniques, although this showed to have less relevance for clinical practice than border delineation. The analysis shows that there are regions were noise was completely eliminated without affecting either edges or texture. Since all sub-images of details of a given DWT have zero mean value the denoising method proposed the approximation sub-images are not filtered.
The Bivariate Shrinkage filter does not change the mean of processed images; the results obtained with the proposed approach have been made availed to clinicians and proved diagnoses.

7.ACKNOWLEDGEMENTS

The authors would like to thank Pr. ERIVES Hector (www.ee.nmt.edu) for the excellent scientific comments and for providing the ultrasound medical speckled image which we used in this paper.

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Multimode Graded-Index polymer Optical Fiber for High-Capacity Long Haul Multiplexed Transmission

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Abstract: Data traffic is growing exponentially due to the emergence of various network services. Although the transmission capacity of optical fibers has dramatically increased thanks to advanced communication technologies such as Copper based technologies but Copper based technologies suffer strong susceptibility to electromagnetic interferences and have limited capacity for digital transmission as well as the presence of crosstalk. Compared to these copper based technologies, optical fiber has smaller volume; it is less bulky and has a smaller weight. In comparison with data transmission capability, optical fiber offers higher bandwidth at longer transmission distances. The main objective of Polymer Optical Fiber(POF) to integrate voice, video, and data streams over all-optical systems as communication signals make their way from LANs down to the end user by Fiber-To-The-x (FTTx), offices, and in-homes. This paper reviews the major achievements of our polymer optical Fiber based MMF research and development.

Keywords: Graded index polymer optical Fiber, wavelength division multiplexing, Multimode optical Fiber, LAN.

1. INTRODUCTION

At present, twisted pair and coaxial cables are commonly used as the physical medium to deliver telecom services within the customer's premises. However, these two transmission medium suffer from serious shortcomings when they are considered to serve the increasing demand for broad-band services. For instance, twisted pair has a limited bandwidth and it is susceptible to electromagnetic interference (EMI). Coaxial cable offers a large bandwidth, but it poses practical problems due to its thickness and the effort required to make a reliable connection. Moreover, the coaxial cable is not immune to EMI. Optical fiber is extensively used for long-distance data transmission and it represents an alternative for transmission at the customer premises as well. Optical fiber connections offer complete immunity to EMI. Optical silica-glass fibers, however, are not suitable for use within the customer premises because of the requirement of precise handling, and thus, the high costs involved. Polymer optical fibers are very attractive for use within the customer premises with their easy handling and low cost. This is mainly due to their relatively thick core. In fact, several polymer fiber-based systems are commercially available. However, these systems are based on the use of the multimode step index polymer optical fiber (SI-POF), whose bandwidth distance product is limited to a few MHz km.

The way toward broad-band POF systems is opened by the use of graded-index polymer optical fiber (GI-POF). The high bandwidth of the GI-POF (typically 2 GHz km) compared to SI-POF, is attributable to the graded-index profile in the core. The transmission media used at present are not suited for provisioning high-bandwidth services at low cost. For instance, today's wiring in LANs is based mainly on copper cables (twisted pair or coaxial) and silica (glass) fiber basically of two kinds: single mode optical fiber (SMF) and multimode optical fiber (MMF). Copper based technologies suffer strong susceptibility to electromagnetic interferences and have limited capacity for digital transmission as well as the presence of crosstalk. Compared to these copper based technologies, optical fiber has

smaller volume ,it is less bulky and has a smaller weight. In comparison with data transmission capability, optical fiber offers higher bandwidth at longer transmission distances. However, the use of MMFs is at a cost of a bandwidth penalty with regards to their SMF counterparts, mainly due to the introduction of modal dispersion.

This is the reason MMF is commonly applied to short-reach and medium-reach applications due to its low intrinsic attenuation despite its limited bandwidth. In particular, in the access network, the use of MMF may yield a considerable reduction of installation costs although the bandwidth-times length product of SMF is significantly higher than that of MMF. As in the access network, the fiber link lengths are less than 10km, however, the bandwidth of presently commercially available silica MMFs is quite sufficient. On the other hand, compared to multimode silica optical fiber, polymer optical fiber (POF) offers several advantages over conventional multimode optical fiber over short distances (ranging from 100m to 1000m) such as the even potential lower cost associated with its easiness of installation, splicing and connecting. This is due to the fact that POF is more flexible and ductile, making it easier to handle. Consequently, POF termination can be realized faster and cheaper than in the case of silica MMF. This POF technology could be used for data transmission in many applications areas ranging like in-home, fiber to the building, wireless LAN.

2. Fundamentals Of Multiple Optical Fiber

2.1. Step- index multimode POF

Conventional commercial POFs are dominantly step- index multimode (SI-MM) fibers from extrusion. These commercial POFs typically have 1mm outer diameter with a core diameter of 980nm. There are activities to develop novel POFs smaller size and lower numerical aperture with higher bandwidth.

	Core	**Cladding**
Material	PMMA	Fluorinated polymer
Diameter (typical)	980 μm	1000 μm
Young's modulus	3.09 GPa	0.68 GPa
Poisson's ratio	0.3	0.3
Refractive index	1.492	1.405
Yield strength	82 MPa	
Transmission loss (@ 650 nm)	200 dB/km	
Maximum operating temperature	70 °C	

Table1. Specification of a SI-MM POF (ESKA CK40).

2.2 Graded- index multimode POF

Graded-index multimode (GI-MM) POFs with both low loss and high bandwidth have been developed with well-tailored index profiles. Since early 1990s, intensive research has been carried out to produce a graded-index POF which would have significantly larger band width length product.

3. POF As Transmission Medium

3.1 Attenuation

Attenuation in fiber optics, also known as transmission loss, is the reduction in the intensity of the light beam with respect to distance traveled through a transmission medium, and being an important factor limiting the transmission of a digital signal across large distances. The attenuation coefficient usually uses units of dB/km through the medium due to the relatively high quality of transparency of modern optical transmission media. Attenuation in optical fiber is caused primarily by both scattering and absorption. Polymer Optical Fiber (POF) arebased on non-fluorinated polymers such as PolyMethylMethAcrylate (PMMA), widely used

as core material for graded-index fiber in addition with the utilization of several kinds of dopants. Although firstly developed PMMA-GIPOFs were demonstrated to obtain very high transmission bandwidth compared to that of Step-Index (SI) counterparts, the use of PMMA is not attractivedue to its strong absorption driving a serious problem in the PMMA-based POFs at the near-IR (near-infrared) to IR regions.. As a result, PMMA-based POFs could only be used at a few wavelengths in the visible portion of the spectrum, typically 530nm and 650nm, with typical attenuations around 150dB/km at 650nm. Now-a-days almost all gigabit optical sources operate in the near-infrared (typically 850nm or 1300nm).

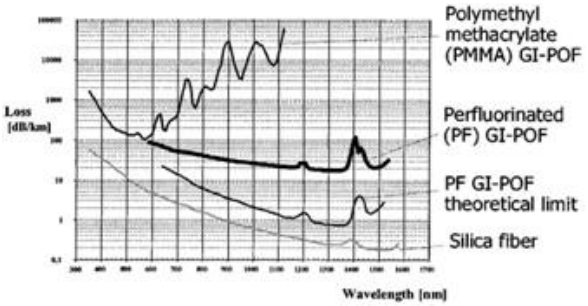

Fig. 1. Attenuation of graded index POF.

3.2 Dispersion

For multimode fibers, modal dispersion and chromatic dispersion are the relevant processes to be considered. Chromatic dispersion is introduced by the effect that the speed of propagationoflightofdifferentwavelengthsdifferent resulting in a wavelength dependence of the modal group velocity. The end result is that different spectral components arrive at slightly different times, leading to a wavelength-dependent pulse spreading, i.e. dispersion. In PF-based POFs the chromatic dispersion is much smaller than in silica MMF for wavelengths up to 1100nm. For wavelengths above 1100nm, the dispersion of the PF-based GIPOF retains and the dispersion of silica MMF increases. On the other hand, modal dispersion is caused by the fact that the different modes (light paths) within the fiber carry components of the signals at different velocities, which ultimate results in pulse overlap and a garbled communications signal.

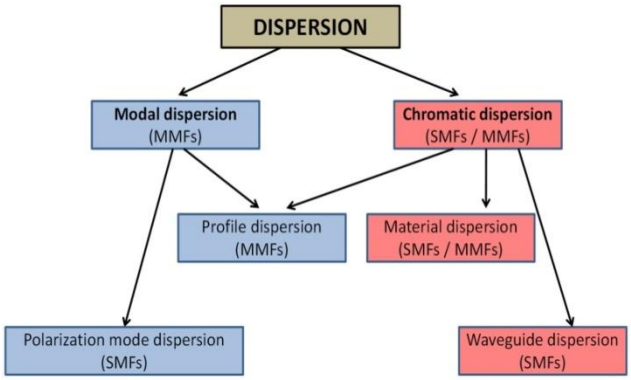

Figure2.Dispersionmechanismsinopticalfibers.

3.3Bandwidth of POF

The advantage in bandwidth of the low material dispersion of PF polymer-based GI-POF has been theoretically and experimentally clarified. It has been shown that the low attenuation and low material dispersion of the PF polymer enables 1- and 10-Gb/s transmission at 850- and 1300-nm wavelengths, respectively, as the PF polymer-based GI-POF has a very low material dispersion (0.0055 ns/nm km at 850 nm), as compared with the conventional PMMA-based POF, and compared with the multimode silica fiber (0.0084 ns/nm km at 850 nm).

4. Transmission Experiment

In this section, we present a review of transmission experiments using POF as the transmission medium. Their experimental setup and enabling technologies are described in detail. Several experiments have been performed to investigate the validity of theoretical models developed to predict the bandwidth of the fiber. The experiments have also shown the feasibility of POF links for high-capacity transmission.

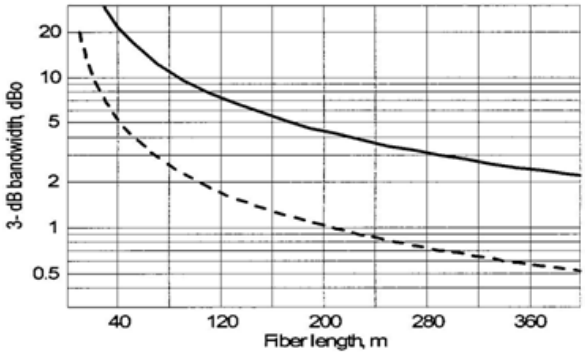

Fig3. Bandwidth of graded index POF.

4.1 2.5-Gb/s Transmission Over 200 m of PMMA GIPOF

A 2.5-Gb/s system experiment over 100 m, using a PMMA GI-POF, a visible light laser at 650-nm wavelength and a sil-icon PIN photodiode has been reported earlier. In our experi-ment, the transmission distance is doubled to reach 200 m. Key elements used in the experiment are a silicon avalanche photo-diode (APD) receiver with a record sensitivity of 29 dBm at 2.5 Gb/s .

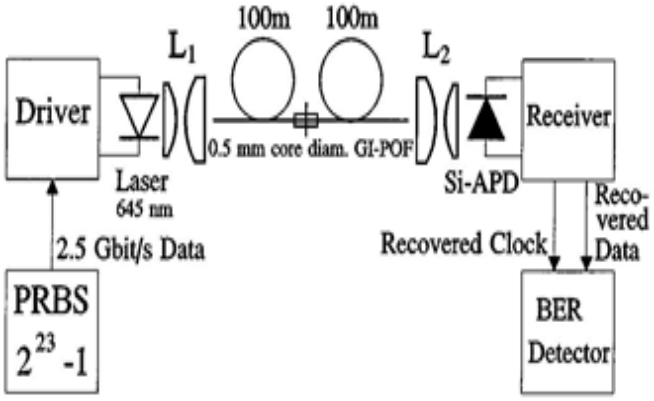

Fig. 4. 2.5-Gb/s transmission over 200 m of PMMA GI-POF.

maximum coupling efficiency. The eye diagram of back-to-back measurement and after 200-m of GI-POF are nearly identical, indicating a sufficient bandwidth (see Fig. 4).

The BER curve against received average power at the input of the APD receiver in the back-to-back and after 200 m GI-POFtransmission has been measured (see Fig. 5). The back-to-back measurement has been carried out with a short piece of GI-POF of a few meters between transmitter and receiver. The received power has been changed by altering the distance between laser and GI-POF. The sensitivity of the receiver was 29 dBm at 2.5 Gb/s for a BER of 10 . The laser output power was 6.8 dBm, so the available power budget was 35.8 dB.

The attenuation of the 2 100 m GI-POF was 32.8 dB. The power penalty due to modal dispersion of the fiber was 2 dB (see Fig. 6). The total coupling losses where 0.6 dB, so a power budget of 35.4 dB was needed. Moreover, the optical output spectrum of the modulated laser at an average output power of 6.8 dBm has been measured (see Fig. 6). The width of the spec-trum, 3 dB below the maximum value is 0.4 nm, which limits pulse broadening due to dispersion of the fiber.

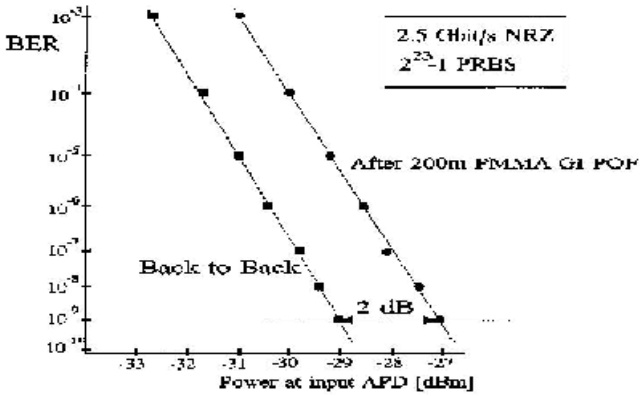

Fig.5 BER measurement results.

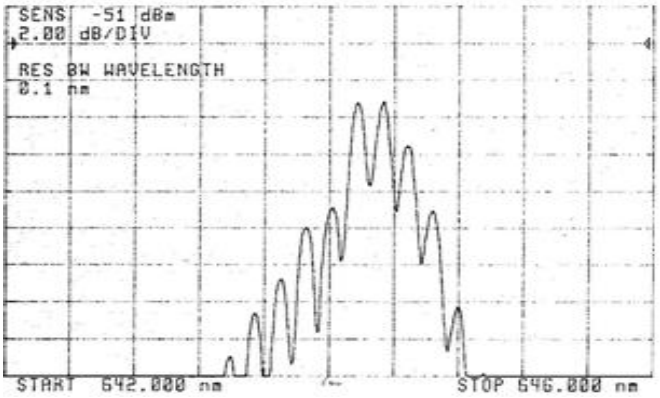

Fig. 6.Measured optical spectrum of the modulated laser.

4.2 WDM Experiments

Per-fluorinated polymer based graded index polymer optical fiber(GI_POF) has a low loss wavelength region from 500 to 1300nm, so many WDM transmission can be applied over a broad wavelength range, which can be separated easily with low-cost devices. As a start of this development, a demultiplexer for splitting up the wavelengths 645, 840, and 1310 nm has been realized with planar interference filters.

In Fig.7, the principle of operation of the demultiplexer is shown.First, the light from the input GI-POF is transformed into a parallel beam by means of lens 1. Interference filter 1

First, the light from the input GI-POF is transformed into a parallel beam by means of lens 1. Interference filter 1 deflects the light in the 645-

nm wavelength region. The other wave diode of the 645-nm receiver. The light in the 840- and 1310-nm wavelength regions, which passed through filter 1, is split up by filter 3 Light in the 840-nm wavelength region is deflected by filter 3, filtered by filter 4, and focused on the detector of the 840-nm receiver by lens 3. The remaining 1310-nm light is focused on the 1310-nm detector by lens 4. The measured insertion losses for all three wavelengths from GI-POF input to photo detectors are smaller than 1.6 dB. Measured crosstalk levels are smaller than 30 dB.

The demultiplexer has been used for a three channels operating at 2.5 Gb/s over 200-m GI-POF WDM experiment with a record bit rate times distance product. A block diagram of the setup is shown in fig 8. For this experiment the transmitter and receiver described in section4.1 and 4.2 have been used. This experiment carried out using the wavelength 840nm and 1310nm and a GI-POF fiber with a length of 328m of one piece. Because this fiber sample has been an attenuation of more than 100dB/m at 640nm, this wavelengyh could not be used. A block diagram is shown in fig 9.

5. CONCLUSION

The transmission distances of PF GI-POF-based systems are increasing very fast. At bit rates of 2.5 Gb/s, system spans of 300 m at 645-nm wavelength, and 550 m at 840- and 1310-nm wave-lengths have been reached. Using WDM transmission, system capacities have been further enhanced. For instance, we have reported a three-channel 2.5-Gb/s GI-POF WDM transmis-sion over 200-m experiment and a two-channel 2.5 Gb/s over 328-m experiment with record bit-rate distance products. These experiments show the feasibility of high-capacity transmission over POF. It also has been shown that 2.5-Gb/s transmission over 4 km of large-core (148 and 185 m) graded index silica fiber can easily be realized. Maximum transmission distances of the large-core graded index silica fibers are much larger com-pared with the graded index polymer fibers. There is a large dif-ference in attenuation between silica and polymer fibers. The diameter of silica fibers is limited because of the inherent inflex-ibility of glass materials. Because of the difference in mechan-ical properties of silica and polymer the handling techniques are different.

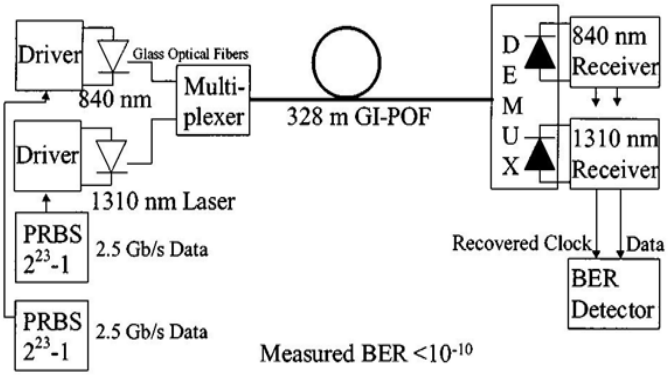

Fig. 7. Principle of operation of the 645-, 840-, 1310-nm DE-multiplexer.

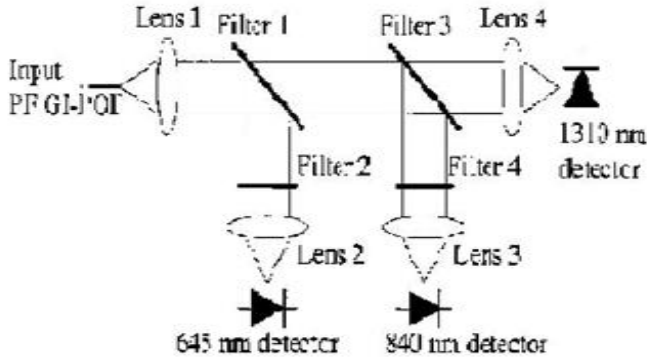

Fig.8. Block diagram of the 3 2 2.5-Gb/s WDM experiment over 200-m GI-POF.

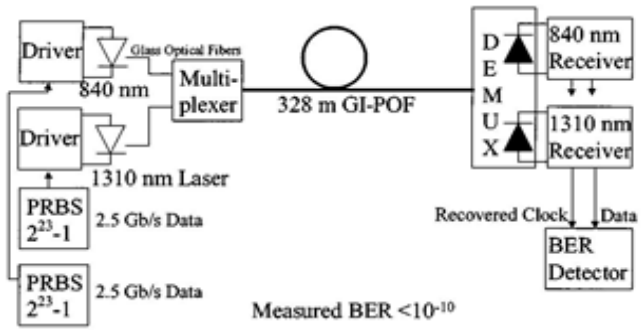

Fig.9. Block diagram of the 2 2 2.5-Gb/s WDM experiment over 328-m GI-POF.

The applicability of Multimode graded index polymer optical fiber for customer premises and Wide area networks to integrate voice, video, and data streams over all-optical systems are used for data transmission in many applications areas ranging like in-home, fiber to the building,

wireless LAN backbone or office LAN among others

The experimental results resorted in this paper clearly show the applicability of graded index polymer optical fiber for cus-tomer premises and local area networks. We believe that the record results reported here are important milestones that may encourage the development of polymer fiber systems and net-works.

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SMART WATER SPRINKLER BASED ON MICROCONTROLLER

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ABSTRACT:

The system is designed to implement a "Smart water sprinkler which is based on Arduino Microcontroller". Today whole world is facing scarcity of water including India. In irrigation the water requirement is large and in the process lot of water is wasted too. In addition the plants require continuous observation. The main motive of designing this system is to impart a water delivering schedule to the plants. This smart system aims at minimizing the water loss and also reducing the constant supervision required for plants. It also avoids the damaging of plants by providing the exact amount of water which is needed by the plants. The system contains a soil moisture sensor which acts as a sensing element in the system. A gateway unit which consists of Arduino Microcontroller, switching device, actuators like servo motor and pump is present. A program is developed in accordance with the threshold values of the sensing element and the actuators. The Arduino microcontroller used here acts as the data processing element it processes the input data from sensing element and accordingly takes decision based on its predefined values. The switching device used here is a relay which controls the pump according to the instruction provided by the microcontroller. The servo motor acts as an actuator which provides water to the direction where it is needed. This system is highly efficient with high accuracy and low cost. It consumes low power which makes it a resource efficient technology.

Keywords:

Arduino Microcontroller, Soil moisture sensor, Servo motor, Water pump.

1. INTRODUCTION

Embedded Systems:

Embedded systems are computer systems that are part of larger systems and they perform some of the requirements of these systems. Some examples of such systems are auto mobile control systems; industrial processes control systems, mobile phones, or small sensor controllers. Embedded systems cover a large range of computer systems from ultra small computer-based devices to large systems monitoring and controlling complex processes. The overwhelming number of computer systems belongs to embedded systems: 99% of all computing units belong to embedded systems today.

Water is a resource that is needed by all living species. So it is necessary for us to check the water usage and preserve it for the future generation to come. One industry that uses large amount of water is the agriculture industry. In India still 14.5% of GDP is dependent on agriculture which shows the status of agriculture in India. A large amount

of water resource is wasted also by this industry. So in this project report an efficient smart sprinkler system is designed which will check the water usage and will also reduce the human supervision required. The smart model implements sensor technology with Arduino microcontroller to make a smart switching device. The system displays the basic switching mechanism of motor and pump using sensors. This system will avoid over watering of already saturated soil. There are many innovations done in this area but some are very expensive and some cannot be implemented on the ground. This system is implemented easily and also it is cost effective. It is user friendly and can be easily reprogrammed for any requirement.

2. LITERATURE REVIEW

In this paper, soil moisture sensor is placed in the root zone of plant/field. The sensor sends information and transmits the data to the microcontroller. An algorithm was developed to measure threshold value soil moisture sensor that was programmed into a microcontroller to monitor the humidity content of the soil. This paper designs a model of automatic irrigation system which is based on microcontroller ATMEGA328. Temperature and soil moisture sensors are placed in the field. Sensors sense the moisture content of the soil and give the information to farmer through GSM Module. Farmer gets to know the status of the pump installed in the field via GSM Module without going into the field. When the moisture content reaches above the desired threshold value the pump automatically turns off and the message is conveyed to the farmer.

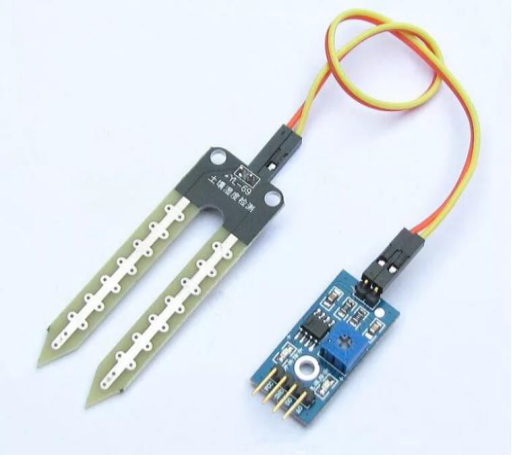
3. COMPONENTS USED

3.1 Arduino Microcontroller:

The Arduino Uno microcontroller board used here is based on Atmega328P. It consists of 14 digital input/ output pins, 6 analog inputs, a 16 MHz quartz crystal, a USB connection, a power jack, an ICSP header and a reset button.

3.2 Soil Moisture Sensor:

A capacitive contact soil moisture sensor is used. Soil moisture sensor measures the volumetric water content of the soil by some indirect methods which include measuring different properties of soil like electrical resistance, dielectric constant and interaction with neutrons. It has one probe like structure which will be dipped inside the soil. The circuit part of the sensor contains 4 pins i.e. Vin, ground, AO (analog output), DO (digital output). The moisture sensor provides an analogue output which can be easily interfaced with the Arduino. Figure.1. Soil Moisture Sensor



Soil moisture sensor

3.3 Relay:

Relay is a switch which is operated electrically. Relay is used when it is necessary to control a circuit by separate low power signal. Here it is used to control the water pump. The relay used here also contains an inbuilt motor driver required for the pump.

3.4 Servo Motor:

Servo Motor is used as a rotary actuator here. It allows the precise control of angular position which is required. The servo motor is a closed loop servo mechanism that uses position feedback to control its motion and position.

3.5 Water Pump:

A pump is used to transport the water from the tank or reservoir.

3.6 Connecting leads and Pipe

Connecting leads are required to connect all components and pipe to transfer water.

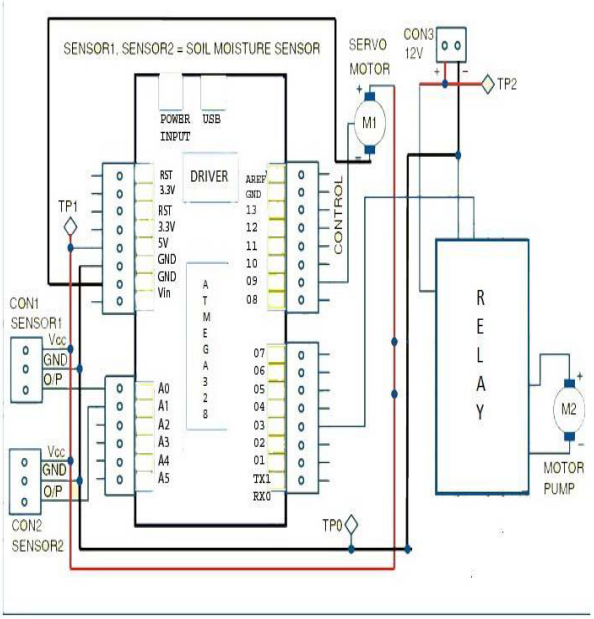
4. SOFTWARE DESCRIPTION

Arduino IDE:

The Arduino Integrated Development Environment contains a text editor for writing code in the embedded C language, a message area, a text console, a toolbar with buttons for common functions and a series of menus. It connects to the Arduino and Genuine hardware to upload programs and communicate with them.

5. WORKING

At first the moisture sensor will sense the amount of moisture present in the soil and accordingly it will send its output to the microcontroller through the input/output pins provided in the Arduino board. The program allows the microcontroller to read the moisture value every 20 seconds. If the value reaches the threshold value as determined initially. It will first moves the horn of the servo motor along with the pipe which is attached to it towards the plant whose moisture level decreased. The servo motor is connected to the 9th number output pin of Arduino board through which the microcontroller is giving instruction to the motor. Then the microcontroller will start the water pump which is connected to the 3rd number output pin of the board, the pump will pump water for some time interval. Then the microcontroller will bring the servo motor's horn back to the initial position. The switching of the water pump is done by the relay which controls the AC power supply which is provided to the pump. Initially the relay is in NO (normally open) condition which signifies that the motor is in normal position and pump is in OFF state. As soon as the signal that soil is dry from the moisture sensor reaches the microcontroller the motor horn turns to the direction of the plant and the NO changes to NC (normally closed), due to which pump starts pumping water to the plants.



Block diagram of the water sprinkler

6. RESULTS ANALYSIS

This Smart sprinkler system is tested in the garden plants on a small scale. It has shown best results. A plant requires an average of 600-800mm of water every day. In Arduino code the moisture range is set as 300-700 which delineates the corresponding resistance value in digital format. It is proved to be a good care taker of the plants in absence of the human. Moreover it is pretty cheap and a robust design as compared to the similar design available in the market.

7. CONCLUSION

As the smart sprinkler system has a user friendly design so it can be used by the household users as well as the commercial user. Further this system will reduce the human supervision and also make the irrigation automated and tech friendly. The best benefit is that it will reduce the wastage of water during irrigation and helps in saving the due to precious water resource. Also it consumes less power the usage of the microcontroller.

8. FUTURE SCOPE

This Smart system can be further enhanced by using a Webscaper which will help the Smart system to work according to the weather forecast, if heavy rain is forecasted then less water is supplied to the plants.

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Lung Cancer Detection Techniques Using Gradient Operators

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ABSTRACT

The diagnosis of lung cancer at an early stage is important to cure and save lives. Prediction of lung cancer is most challenging problem due to structure of cancer cell.
Edge detection techniques are commonly used to detect the affected cell region and make the investigation easy. In this paper, the different edge detecting techniques like sobel, Robert, prewitt, and canny are used to detect the lung cancer affected cells along with morphological operators. The performance of the proposed method is analyzed and the results are tabulated.

Key words: CT scan image, cancer detection, Sobel, Robert ,Prewitt, Canny operators.

I.INTRODUCTION

Cancer is the leading cause of death worldwide, accounting for 8.8 million deaths in 2015.the most common causes of cancer deaths are lung cancer, liver cancer,colorectal cancer, stomach cancer ,breast cancer. Lung cancer also known as lung carcinoma is a malignant lung tumor characterized by uncontrolled cell growth in tissue of the lung.

Cancer is a group of diseases characterized by the uncontrolled growth and spread of abnormal cells. If the spread is not controlled it can result in death. the reasons for many Lung cancers are tobacco use and excess body weight ,and non modifiable(internal) factors, such as inherited genetic mutations, hormones and immune conditions.

Now a days CT scan images are commonly used to detect the lung cancer rather than X-rays and MRI scan images. CT images are less noisy than other modality images. MATLAB software is used for study of lung cancer.

This paper comprises as follows section II literature survey and the proposed work is in section III results are discussed in section 4 and conclusion is in section V.

II.LITERATURE SURVEY

In [1] proposed an approach for detection of cancer cells from lung CT scan images. It reduces the error in the detection part made by the doctors for medical study.It is based on Sobel edge detection and label matrix.

In [2] a system using computer aided diagnosis(CAD) for finding the edges from scan images of lung, for detection of diseases..In [3] Prathamesh used watershed algorithm to detect cancer affected portion of lung .

In [4],Arvind Kumar Tiwari discussed about the prediction of lung cancer using various image processing techniques with their accuracy. In [5],Shiva kumar discussed various fuzzy c-means techniques to detect lung cancer..Hala Al-shamlan et al [6],explained about features like geometric,texture and gradient values of lung cancer affected cells. In paper [7], canny edge detector is used to find the cancer regions in CT scan images.Mokhled et al [8] discussed about various image processing techniques for lung cancer detection.

The main idea of this paper is to detect the tumor edges accurately ,and decide whether it is cancerous or not using enhanced CT scan images using and various edge detection operators.

III.PROPOSED WORK

The input CT scan image is converted into gray scale image for easy processing.

Since isolated points and lines of unitary pixel thickness are in frequent in most practical application. Edge detection is the most common approach in gray level discontinuity segmentation. An edge can be defined as a set of connected pixels that form a boundary between two disjoint regions. An edge is a boundary between two regions having distinct intensity level. It is very useful in detecting of discontinuity in an image. The changes of intensity

in an image can be estimated using first-order derivative and second-order derivative.

First order derivatives responds whenever there is discontinuity in intensity level and value remain positive at leading edge and negative at the trailing edge. Let output function of two variables, f(x,y). In the two variable case x and y are the variables.

The edge representation of an image significantly reduces the quantity of data to be processed, yet it retains essential information regarding the shapes of objects in the scene. This explanation of an image is easy to incorporate into a large amount of object recognition algorithms used in computer vision along with other image processing applications. The major property of the edge detection technique is its ability to extract the exact edge line with good orientation as well as more literature about edge detection has been available in the past three decades. On the other hand, there is not yet any common performance directory to judge the performance of the edge detection techniques.

The performance of an edge detection techniques are always judged personally and separately dependent to its application. Edge detection is a fundamental tool for image segmentation. Edge detection methods transform original images into edge images benefits from the changes of grey tones in the image. In image processing especially in computer vision, the edge detection treats the localization of important variations of a gray level image and the detection of the physical and geometrical properties of objects of the scene. It is a fundamental process detects and outlines of an object and boundaries among objects and the background in the image. Edge detection is the most familiar approach for detecting significant discontinuities in intensity values. Edges are local changes in the image intensity. Edges typically occur on the boundary between two regions.

In this work different edge detection techniques are used to find the edge of a tumor cell.

Gaussian filtering is used to blur images and remove noise and detail. In one dimension, the Gaussian function is given in equation 1:

$$G(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{\frac{-x^2}{2\sigma^2}} \quad \text{----------(1)}$$

Where σ is the standard deviation of the distribution The distribution is assumed to have a mean of 0. In this work, 2D Gaussian filter is used to remove noises

The gradient based edge detectors [9] are explained in the following section.

The proposed work flow is shown in figure 1.

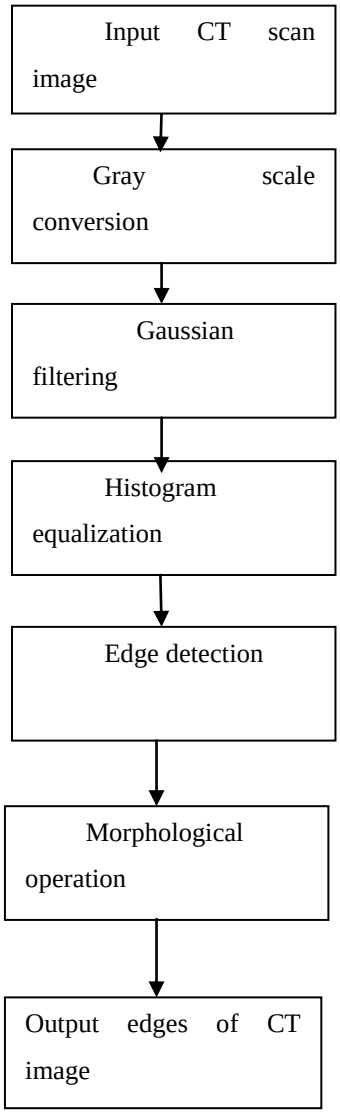

Fig 1.Proposed work

A.SOBEL EDGE DECTECTION

The Sobel edge detection method is introduced by Sobel in 1970. The Sobel method of edge detection for image segmentation finds edges using the Sobel approximation to the derivative.It precedes the edges at those points where the gradient is highest. The Sobel technique performs a 2-D spatial gradient quantity on an image and so highlights regions of high spatial frequency that correspond to edges. In general it is used to find the estimated absolute gradient magnitude at each point in n input grayscale image. This is very alike to the Roberts Cross operator. The sobel the kernels G_X , G_y are shown below figure 2.

-1	-2	-1
0	0	0
1	2	1

G_X

-1	0	1
-2	0	2
-1	0	1

G_Y

Fig.2. Sobel masks

B.PREWITT EDGE DECTECTION

The Prewitt edge detection is proposed by Prewitt in 1970. To estimate the magnitude and orientation of an edge Prewitt is a correct way. Even though different gradient edge detection wants a quite time consuming calculation to estimate the direction from the magnitudes in the x and y-directions, the compass edge detection obtains the direction directly from the kernel with the highest response. It is limited to 8 possible directions; however knowledge shows that most direct direction estimates are not much more perfect. This gradient based edge detector is estimated in the 3x3 neighborhood for eight directions. All the eight convolution masks are calculated. One complication mask is then selected, namely with the purpose of the largest module. the kernels G_X , G_y are shown below figure 3.

-1	-1	-1
0	0	0
1	1	1

G_x

-1	0	1
-1	0	1
-1	0	1

G_y

Fig.3. Prewitt masks

Prewitt detection is slightly simpler to implement computationally than the Sobel detection, but it tends to produce somewhat noisier results.

C.CANNY DECTECTION

In industry, the Canny edge detection technique is one of the standard edge detection techniques. To find edges by separating noise from the image before find edges of image the Canny is a very important method. Canny method is a better method without disturbing the features of the edges in the image afterwards it applying the tendency to find the edges and the serious value for threshold. The algorithmic steps are as follows:

- Convolve image f(r, c) with a Gaussian function to get smooth image f^(r, c) and is given in equation 2.

  f^(r, c)=f(r,c)*G(r,c,) ----------(2

- Apply first difference gradient operator to compute edge strength then edge magnitude and direction are obtain as before.

- Apply critical suppression to the gradient magnitude. Apply threshold to the non-maximal suppression image.

Unlike Roberts and Sobel, the Canny operation is not very susceptible to noise.

D. ROBERTS EDGE DECTECTION

The Roberts edge detection is introduced by Lawrence Roberts (1965). It performs a simple, quick to compute, 2-D spatial gradient measurement on an image. This method emphasizes regions of high spatial frequency which often correspond to edges. The input to the operator is a grayscale image the same as to the output is the most common usage for this technique. Pixel values in every point in the output represent the estimated complete magnitude of

the spatial gradient of the input image at that point. the kernels G_X , G_y are shown below figure 4.

-1	0
0	1

Gx

0	-1
1	**0**

Gy

Fig.4 Robert masks

E. HISTOGRAMS

An image histogram is a type of histogram that acts as a graphical representation of the tonal distribution in a digital image. It plots the number of pixels for each tonal value. Histogram equalization is used to enhance the quality of the image

F. MORPHOLOGICAL PROCESS

Morphological image processing is a collection of non-linear operations related to the shape or morphology features . in an image.operations rely Possible locations in the image and it is compared with the corresponding neighbourhood of pixels. Some operations test whether the element "fits" within the neighbourhood , while others test whether it "hits" or intersects the neighbourhood. In this work, the detected edges are made thin using morphological operator ‘thin’.

IV. EXPERIMENTAL RESULTS

Lung cancer images of CT type are applied to test the proposed work. The CT image is converted to gray scale image to perform the gradient edge detector operations. the various edge detection techniques are applied after the enhancing the image. The CT scanned image with cancer infected lung obtained from database is given in figure 5 and the corresponding gray scale image is shown in figure 6.

Fig. 5. cancer affected lung cancer CT image

Fig.6. Gray scale image

The Gaussian filtered image is shown in figure 7.

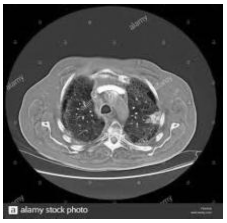

Fig.7.Gaussian filtered image

The robert edge detected output of lung cancer is shown in below figure 8.

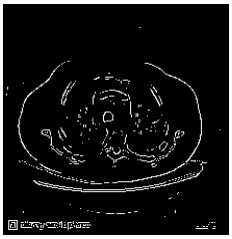

Fig. 8. Robert edge detected output

The sobel edge detected output of lung cancer is shown in below figure 9.

Fig. 9. sobel edge detected output

The prewitt edge detected output is shown in below figure 10.

Fig. 10. Prewitt detected output

The log edge detected output is shown in below figure 11.

Fig. 10.Log detector output

The canny edge detected output is shown in below figure 11.

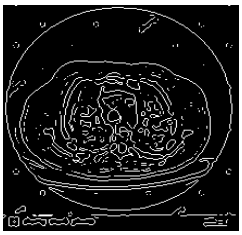

Fig.11.canny edge detected output

The morphological edge detected cancer tumor for canny operator is shown in figure 12.

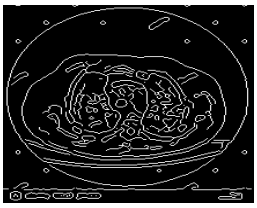

Fig.12.Morphological edge detected cancer tumor

The performance of the processes are tabulated in table1.This performance is compared with unenhanced condition of CT scan image.

Table 1. Comparison of edge detection techniques

Input Image	Number of edges detected without enhancement				Number of edges detected without enhancement			
	Robert	Sobel	Prewitt	Canny	Robert	Sobel	Prewitt	Canny
Image 1	2198	1775	1764	3994	1423	1858	1798	7116
Image 2	2115	1762	1746	4490	1476	1853	1813	8293
Image 3	3895	4074	4030	12574	3622	4337	4278	14058
Image 4	1857	2187	2148	5041	1546	1808	1773	5175

From the above table -1 we can observe that the number of edges detected in the case of enhanced image are always greater than the number of edges in the unenhanced case. The performance of the canny edge detector is better than other gradient operators since the number of edges produced are approximately 4 times grater than the other operators. The increased number of edges leads increasing in accuracy of lung cancer detection.

V. CONCLUSION

The Proposed lung cancer consists of preprocessing ,edge detection and morphological processing for detecting the lung cancer affected regions in an image. The results show that edge detection accuracy is better than the unenhanced CT scan image. The proposed work is more suitable for early stage lung cancer detection. this work will be extended to find the dimension and area of cancer affected cells in an image using suitable feature extraction techniques.

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Segmentation of Brain Tumour Affected Cells using Simulink Model

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Abstract— **This paper analysis brain tumor affected cells segmentation using simulink model for MRI (Magnetic Resonance Imaging) images. The proposed simulink model uses various edge detection operators for segmenting the affected cells. The statistical analysis of affected cells are also calculated and compared with the normal cells in the image. Edge detection forms a pre-processing stage to remove the redundant information from the input image, thus dramatically reducing the amount of data to be processed while at the same time preserving useful information about the boundaries. Here various edge detection techniques simulink models and the segmented output statistical analysis are discussed.**

Keywords— ***Simulink, Segmentation, Sobel, Perwitt, Robert***

I. INTRODUCTION

To obtain the quality images and to provide the image accuracy Image processing plays an important role. Image processing is a type of signal processing in computer vision where the input is an image. Image processing output can be a image or parameters related to image. In segmentation image is subdivided into its constituent objects or regions. It partitions the digital image into multiple regions and extracting meaningful region known as ROI region of interest.ROI varies with applications. For multi- domain simulation and model based design of dynamic system simulink is a platform. For modeling simulink is an interactive tool and is ideal for digital signal processing, control system design and communication system design simulation option [1][2]. In most of the image processing applications edge detection is a fundamental tool used to obtain frames information before extracting features and segmentation [3] of objects. Edge detection detects object outlines, boundaries and background in the image. The matrix area gradient operation is a basic edge detection operator which determines the variance levels between pixels. Sobel, Prewitt and Robert operators are the examples of gradient based edge detectors.

II. EDGE DETECTION TECHNIQUES

The boundary between two homogeneous regions forms an image. The process of locating and identifying sharp discontinuities in image refers to edge detection. Edge detection detects the outlines and the background in image. Different types of edge detection operators are available each designed to be sensitive to certain types of edges. Many edge detection methods exist like Sobel [4][5][6], Prewitt [7], Robert. The amount of data in the image is significantly reduced during preservation of most important structural features of the image [8]. Blocks used for simulink implementation is shown in Table 1.

Table 1: Blocks used in simulink for implementation

BLOCK	LIBRARY
Image from workspace	Computer vision system toolbox>source
Edge detector	Computer vision system toolbox>analysis and enhancement
Video viewer	Computer vision system toolbox>sinks
Sum of elements	Simulink>math operations
Constant	Simulink>commonly used blocks
Divide	Simulink>math operations
Display	Simulink>sinks
2D standard deviation	Computer vision system toolbox>statistics
2D variation	Computer vision system toolbox>statistics

1. *Sobel edge detection:*

Sobel is one of the edge detection methods which produce edges with less noise. Two masks are used in sobel edge detection like vertical mask and horizontal mask. These masks generally use 3x3 matrices. Especially, the matrices which have 3x3 dimensions are used in Matlab. With the Sobel approximation to the derivative the Sobel method finds edges. The operator consists of a pair of 3x3 convolution kernels as shown in Table 2 and the block representation of sobel operator is

shown in figure1. The edges running vertically and horizontally relative to the pixel grid [5] these kernels are designed to respond maximum.

Table 2: Sobel mask

-1	0	+1
-2	0	+2
-1	0	+1

Gx

+1	+2	+1
0	0	0
-1	-2	-1

Gy

Gradient $|G| = |Gx| + |Gy|$

Magnitude $|G| = \sqrt{Gx^2 + Gy^2}$

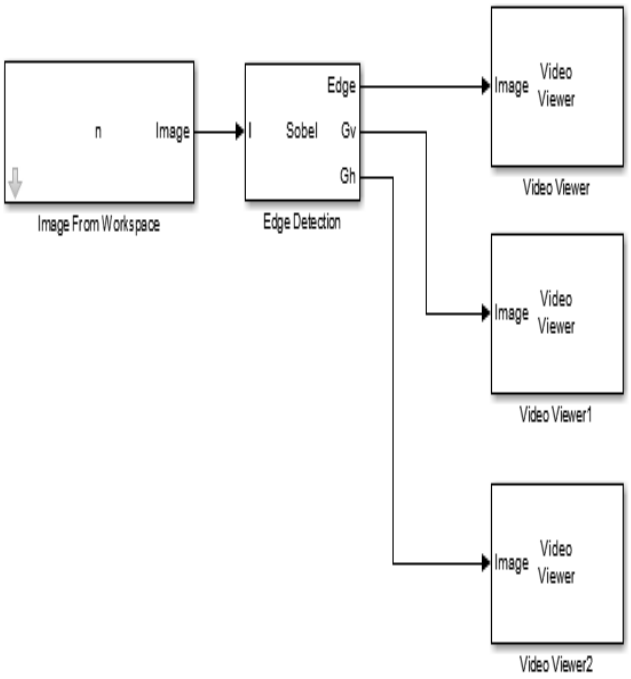


Fig1: Sobel operator for edge detection

A. Results of sobel operator

The MRI image of brain is subjected for edge detection in sobel operator. The image is resized and first 3D image is converted into 1D gray scale image and then output is generated.fig 2 shows the edge detected output, vertical gradient output and horizontal gradient output of sobel operator. The edges are more clear in sobel edge detection operator.

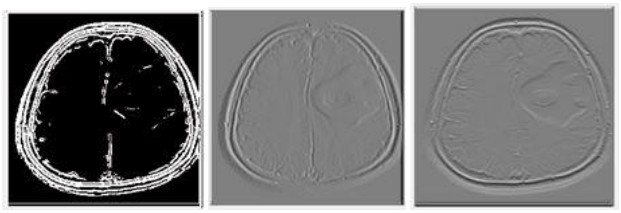


Fig2: Edge detection output, Vertical gradient output, Horizontal gradient output

2. *Prewitt operator:*

By using the Prewitt approximation to the derivative the Prewitt method finds edges. The masks of Prewitt operator are shown in Table 3 and simulink model is shown in Fig 3. It is similar to the Sobel operator and is used for detecting Vertical and horizontal edges of an image.

Table 3: mask operator for Prewitt operator.

-1	0	+1
-1	0	+1
-1	0	+1

G_x

+1	+1	+1
0	0	0
-1	-1	-1

G_y

Gradient $|G|=|Gx|+|Gy|$

Magnitude $|G| = \sqrt{Gx^2 + Gy^2}$

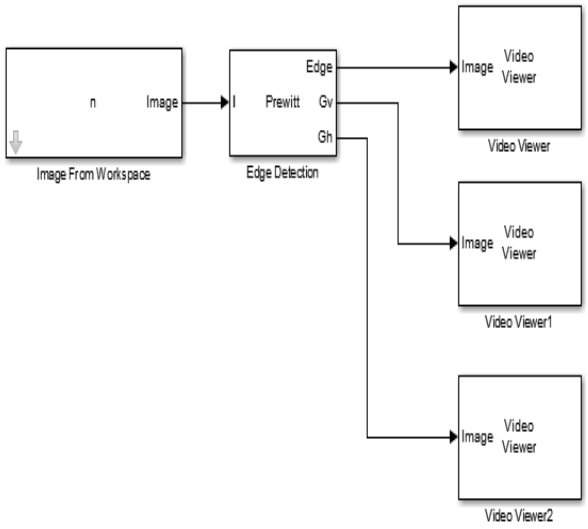


Fig 3: Prewitt operator for edge detection

B. Results of Prewitts operator

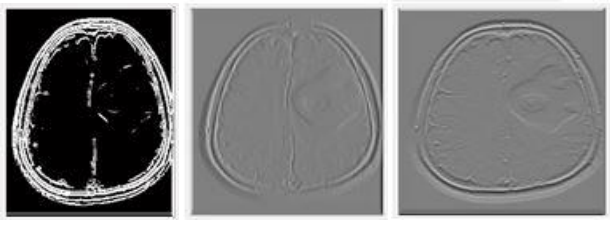


Fig 4: Edge Detection, vertical gradient output, horizontal gradient output

The MRI image of brain is subjected for edge detection in sobel operator. The image is resized and first 3D image is converted into 1D gray scale image and then output is generated. Fig 4 shows the edge detected output,

vertical gradient output and horizontal gradient output of Prewitt operator.

3. *Robert operator:*

The Roberts operator is easy, simple, quick to compute 2-D spatial gradient measurement on an image. Pixel values at each point in the output represent the estimated absolute magnitude of the spatial gradient of the input image at that point. The operator consists of a pair of 2×2 convolution kernels. This is very similar to the Sobel operator. The masks for Robert edge detection is shown in Table 4.

The kernels are designed maximally to respond to edges running at 45° to the pixel grid, one kernel for each of the two perpendicular orientations. The kernels can be applied separately to the input image, to produce separate measurements of the gradient component in each orientation. These can then be combined together to find the absolute magnitude of the gradient at each point and the orientation of that gradient.

Table 4: Mask operator for Robert edge detection.

+1	0
0	-1

G_x

0	+1
-1	0

G_y

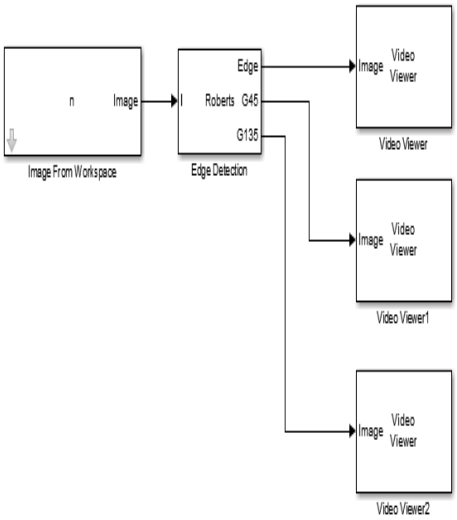


Fig 5: Robert operator for edge detection

C. Results of Robert operator

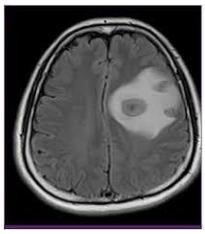
Fig 6: Edge detected output, Vertical gradient, Horizontal gradient

The MRI image of brain is subjected for edge detection in sobel operator. The image is resized and first 3D image is converted into 1D gray scale image and then output is generated. Fig 6 shows the edge detected output, vertical gradient output and horizontal gradient output of Robert operator.

III. Results and Comparison

Three different MRI images are taken for analysis. The ROI is segmented [9] using edge detection techniques. The normal region and the tumor affected region statistical parameters are calculated in Table 5. The simulink block model for calculating mean, variance and standard deviation are shown in the Fig 7.from the table the normal region has less variance and standard deviation when compared to abnormal region.

Table 5: Statistical parameters of MRI images

Image	ROI Type	Mean	Variance	Std Deviation
	Normal	3.563	0.004946	0.07033
	Abnormal	5.848	0.02041	0.1429
	Normal	3.356	0.0102	0.101
	Abnormal	2.055	0.1894	0.4352
	Normal	3.145	0.01611	0.1269
	Abnormal	4.002	0.01078	0.1038

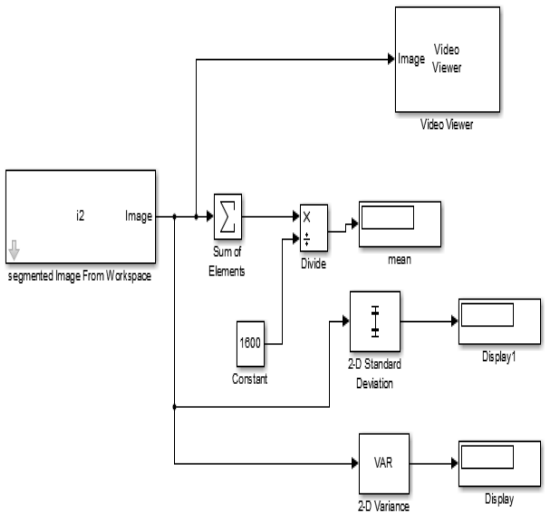


Fig.7. Simulink Model for Calculating Statical Parameter

IV. Conclusion

The image segmentation using various edge detection operators are discussed in the paper. The proposed simulink model analyzes the input image and segments the tumour affected cells using edge detection. The statistical values of the affected cell portion are compared with normal cells portion in the image and is useful for image diagnosis. In future, this can be implemented in real time applications using FPGA kits.

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Analysis of Multispectral Image Compression

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Abstract— **Remote sensing multispectral image compression encoder requires low complexity, high robust, and high performance because it usually works on the satellite where the resources, such as power, memory and processing capacity are limited. For multispectral images, compression algorithms based on 3D transform (like 3D DWT, 3D DCT) are too complex to be implemented in space mission. In this paper, image compression techniques such as JPEG, JPEG2000, SPIHT and EZW techniques are analyzed for multispectral image compression and the results are compared.**

Keywords— ***Multispectral image, SPIHT, JPEG2000, Compression, DCT.***

I. INTRODUCTION

A multi-spectral image is a collection of several monochrome images of the same scene, each of them taken with a different sensor. Each image is referred to as a band. A well known multi-spectral (or multi-band image) is a RGB color image, consisting of a red, a green and a blue image, each of them taken with a sensor sensitive to a different wavelength. Multispectral imaging technique has been widely applied in many fields, like science research, airborne and airspace remote sensing, medical devices, environment monitoring, geological survey, agricultural monitoring, military applications and so on. In multispectral images, because of more than one band, the amount of data to be transmitted is more when compared to the normal images. And also the multispectral image data processing, storage and transmission also complicated. These problems can be significantly reduced by using some form of data compression before transmission over wireless channel [1-3]. For transmission of high quality multispectral images through wireless communication channels it is necessary to achieve efficient compression that maintains the good image quality without increasing the transmission bandwidth. A number of techniques have been proposed in the last few years for the compression and transmission of multispectral images [4].

The most commonly multispectral image techniques can be used the lossless or lossy compression lossless coding is reversible processes in which the original images can be recovered from the encoded image without any loss of information but the compression ratio will be small value rarely exceed 2:1, and this ratio is not enough for many applications of multispectral images. So that we used some lossy compression techniques [5] are used in this paper. The JPEG (DCT), JEPEG2000 (DWT), Embedded Zero tree Wavelet (EZW) and Set Partitioning In Hierarchical Trees (SPHIT) [5- 7] are used. And these compression techniques are implemented on land sat multi-spectral image.

The paper is organized as follows. Section II describes literature survey, Section III describes various techniques. Result and discussion is in section IV. The analysis is concluded in Section V.

II. EXISTING WORK

Remotely sensed multispectral images have been in use for a long time. The Landsat-1 system was the first one for remote sensing application in the year 1972.Multispectral images are not similar to conventional 2D images. It has the third dimension as spectral data. Initially KL transform is used to de correlate the bands and after that conventional 2D transforms are applied for compression. For high fidelity color reproduction of multispectral images in the visual band, weighted KLT and adaptive quantization techniques are applied [8].A new automatic onboard multispectral image compression system was proposed by Guoxia et al [9] for Low Earth Orbit Earth Observation systems. In that work JPEG 2000 compression standard is used for compression. Based on the importance of the data, multispectral images may be compressed using lossy compression or Lossless compression techniques. Consultative Committee for Space Data System (CCSDS) produced an image data compression recommendation suitable for space applications in the year 2005.In this standard, Discrete Wavelet transform is combined with Bit plane coding is used for encoding the data. Conventional image compression techniques like transform based coding, predictive coding and encoding techniques like SPIHT SPECK algorithms are discussed in [10].

Multispectral compression based on DSC Combined with CCSDS-IDC for improved compression in on board

applications is discussed in paper [11]. In that Stepian Wolf based on QC-LDPC by deep coupling way to remove the residential redundancy between adjacent pixels.

For transmission of high quality multispectral images through wireless communication channels it is necessary to achieve efficient compression that maintains the good image quality without increasing the transmission bandwidth. A number of techniques have been proposed in the last few years for the compression and transmission of multispectral images in India. Enhanced Block truncation coding is proposed C.Senthilkumar [12] for color and multispectral image compression. In this technique, the given multispectral image is converted into component image and transformed into Matrix format. Then the component image is divided into blocks. Based on the block values like sum, mean and variance the encoding is done.

PCA with Lifting scheme technique is used for hyper spectral image compression by Mahendran et al [13] In that work, feature extracted using PCA and then wavelet transform is applied to the extracted data. The SPECK encoding technique is used to encode the coefficients.
A lossy multispectral image compression technique is proposed by Bhakiyaraj [14], In that work, Low resolution multispectral image is converted into high resolution image by interpolation. Then décorrelated spectral bands transformed by discrete wavelet transform. Next from the coefficients, the maximum entropy coefficients are selected and these bands are encoded using improved SPIHT coding.
.Edge preserved shearlet transform is proposed by Thayammal S et al (2016), for multispectral image compression[15].

III. TECHNIQUES

A.JPEG COMPRESSION

JPEG (Joint Photographic Experts Group) is an international standard for still image compression, it uses the 2-D Discrete Cosine Transform (DCT), which transforms a signal from a spatial representation into a frequency representation [1]. Lower frequencies are more obvious in an image than higher frequencies.DCT provides good decorrelation between low and high frequency coefficients. so using low frequency coefficients, an image can be reconstructed without sacrificing too much image quality.

B.JPEG 2000 COMPRESSION

JPEG2000 is a modified version of JPEG which it uses DWT (discrete wavelet transform) instead of DCT in JPEG. The 2-D DWT of images is a transform based on the tree Structure that can be implemented by using filters [6]. The image will be processed by the two pre- designed filters, one of which is a low-pass filter and the other is a high-pass filter [9]. The resulted two images after filtering are then down-sampled by 2 in an arbitrary dimension. The resulted two data sets were processed again using the same low- pass and high-pass filters and down sampled by 2 in the other dimension. Four data sets were obtained, each of which only consists a quarter of the original data sets. The obtained data sets are referred to 2-D DWT coefficients. These four data sets were stored in four quarter blocks of the first level and the four blocks are named LL, HL, LH and HH (L represents low, while H represents high), respectively. The three level decomposition of an image using DWT is shown in figure 1 and it has 10 subbands.

C.SPIHT COMPRESSION

SPIHT is a wavelet-based image compression coder. It first converts the image into its wavelet transform coefficients and then transmits information about the wavelet coefficients. The decoder uses the received signal to reconstruct the wavelet coefficients and performs an inverse transform to recover the image. SPIHT provides significant improvement in the image quality when compared to the vector quantization [16]. The suitability of SPIHT compressions are as follows [17].

- Good image quality with a high peak signal-to-noise ratio (PSNR).
- Fast coding and decoding.
- A fully progressive bit-stream.
- Ability to code for exact bit rate or PSNR.

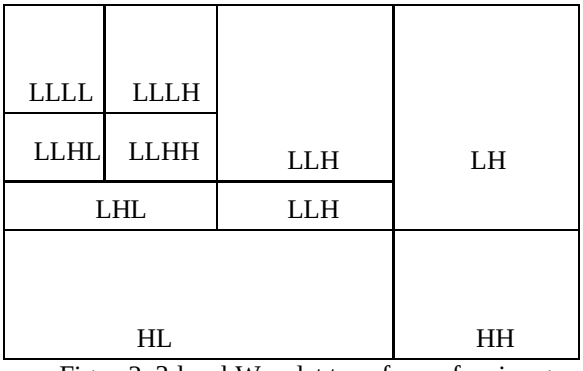

Figure2: 3-level Wavelet transform of an image

D.EZW COMPRESSION

EZW is also a wavelet-based image compression coder. It first converts the image into its wavelet transform and then transmits information about the wavelet coefficients [7]. The decoder uses the received signal to reconstruct the wavelet

and performs an inverse transform to recover the image. In EZW, data set is not maintained as like SPIHT.

IV. Results and Comparison

The land Sat multi-spectral image, ‘‘paris.lan’’ is taken as an input image for the analysis. The image compression techniques are implemented using MATLAB. Firstly the multispectral image is decomposed into a set of gray scale images called bands and then we compress each band by the different techniques. The original image and its different bands are shown in figure2a and 2b respectively.

The performances of the algorithms are measured by calculating the PSNR, MSE, Compression ratio and Bits per pixel. The mathematical formulae for the both MSE and PSNR are described in equations (1) and (2).

$$PSNR = 20*\log (255/\sqrt{MSE}) \quad \ldots \quad (1)$$

$$MSE = 1/MN \quad \sum_{y=1}^{M}\sum_{x=1}^{M}[I(x,y) - I'(x,y \quad \ldots (2)$$

Where I(x,y) is the original image, I`(x,y) is the decompressed image and M,N are the dimensions of the image. The simulated results of different algorithms are tabulated in Table 1.

Table 1: Results OF bpp, MSE and PSNR of Applying Different Compression Techniques on Multispectral Image.

Multispectral image compression techniques	Bits per pixel (bpp)/Q level	Mean square Error (MSE)	Peak to Signal to noise ratio (PSNR)
JPEG	50	12.35	30.44
JPEG 2000	50	11.12	33.567
EZW	3.2365	10.47	36.7057
SPHIT	1.5886	9.85	42.5409

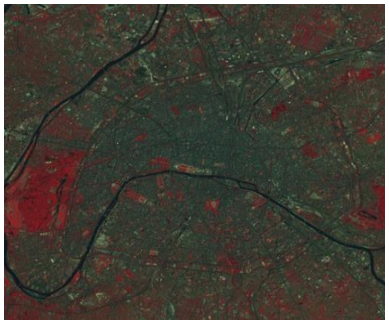

Fig 2.a. Multispectral Original Image

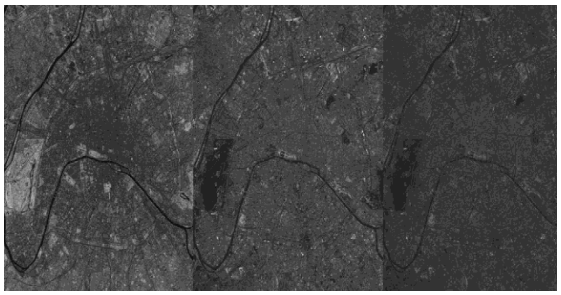

Fig2 b. Restored Multispectral Image using DCT

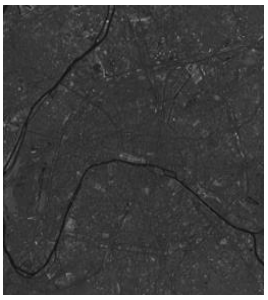

Fig 3 a. Restored Multispectral Image using DWT

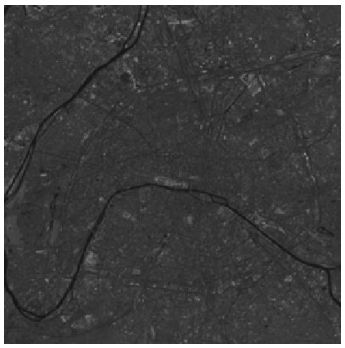

Fig 3 b. Restored Multispectral Image Compression using EZW

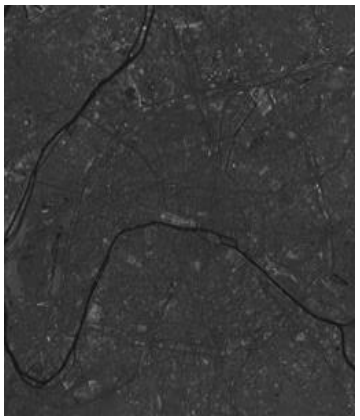

Fig 3c. Restored Multispectral Image Of SPIHT

The restored multispectral image using various techniques is shown in figure 3a, 3b and 3c.The SPIHT algorithm provides high PSNR value when compared to the other algorithms.

V. CONCLUSION

Image compression techniques such as JPEG, JPEG2000, SPIHT and EZW techniques are analyzed for multispectral image compression. SPIHT algorithm's performance is high when compared to other techniques. And also it gives better results in image quality at low SNR environments.

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DUAL AXIS SOLAR TRACKER USING MICRONTROLLER

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ABSTRACT: Solar energy is coming up as a major source of energy. The need of the hour is renewable energy resources with cheap running costs. With the current systems for solar energy harvesting, we have high production only at fixed times mostly noon. This project proposes a dual axis solar tracker system that increases the productivity by a significant margin. As we are in increasing demand of power these days, power sector has been playing a vital role in our day today life. Heading towards the damp increasing power, solar energy comes to the picture or in our mind why because it is one of the most important renewable energy sources on the earth which must be collected and should be utilized to its maximum efficiency. The single axis model have reached up to 50% efficiency and we have tried to increase the efficiency again by 20-30%.This paper describes the design of a dual axis model of solar panel which tracks the maximum solar energy with the help of microcontroller. No doubt our system encircled by solar panel, microcontroller, gears, sensors and stepper motor.

KEYWORDS: Solar cell, solar panel, solar tracker, Driver, microcontroller, sensor, stepper motor.

I.INTRODUCTION

In recent years there has been increasing interest in the solar cell as an alternative source of energy. When we consider that the power density received from the sun at sea level is about 100 mw/cm^2, it is certainly an energy source that requires further research and development to maximize the conversion efficiency from solar to electrical energy[1]. This document explicitly describes the controlling of solar panel with the help of microcontroller to track maximum solar energy. The precise control of solar panel is done by stepper motor. Having said that microcontroller is the heart of the design for controlling action. Microcontroller is going to sense the photon energy with the help of sensor which will provide the interrupt to turn on the controlling action. Photon energy is captured at right angles to the solar panel by stepper motor. Solar panel consist of series of solar cells whose output power in terms of electrical voltage is provided to the battery for the storage purpose. The efficiency calculations are provided at the end to have an exact idea of dual axis model. This dual axis model is totally interactive in nature due to the microcontroller action.

Energy is an essential factor for the development of nations. Most of the energy production depends on fossil fuel. The resources of the fossil fuel are limited; therefore, there is a growing demand on energy from renewable resources such as solar, geothermal and ocean tidal wave. Solar energy is more popular than other renewable energy resources to take over the scarcity of hydrocarbon in future. Photovoltaic (PV) panels convert the sun radiation to electricity[2]. Maximizing output power from a solar system is desirable to increase efficiency. In order to maximize the output power from solar panels, they must be kept aligned with the sun. As such, a means of tracking the sun is required.

In solar tracking systems, solar panels are mounted on a structure which moves to track the movement of the sun throughout the day. There are three methods of tracking: active, passive and chronological tracking. These methods can then be configured either as single-axis or dual-axis solar trackers. In active tracking, the position of the sun in the sky during the day is continuously determined by sensors.

The sensors will trigger the motor or actuator to move the mounting system so that the solar panels will always face the sun throughout the day. This method of sun-tracking is reasonably accurate except on very cloudy days when it is hard for the sensor to determine the position of the sun in the sky thus making it hard to reorient the structure.

Solar tracker is a device that keeps photovoltaic or photo thermal panel in an optimum position perpendicularly to the solar radiation during daylight hours. This can increase the amount of collected energy from the sun by up to 40%[3]. Usually, fixed PV panels cannot follow the sun movement. The single axis tracker follows the sun East-West movement whereas the two-axis tracker follows the sun a long a changing altitude angle movement. Many tracker system technologies have been developed by many scholars.

Dual axis solar trackers have more efficiency than both fixed angle panels and single axis solar tracker systems. But, this advantage is at the expense of more system complexity.

Therefore, in this paper a dual axis sun tracking system is designed and implemented. Its power generation performance is evaluated and compared with fixed panel systems under different temperature and cell covering situation at the geographical area of Kirkuk city-Iraq.

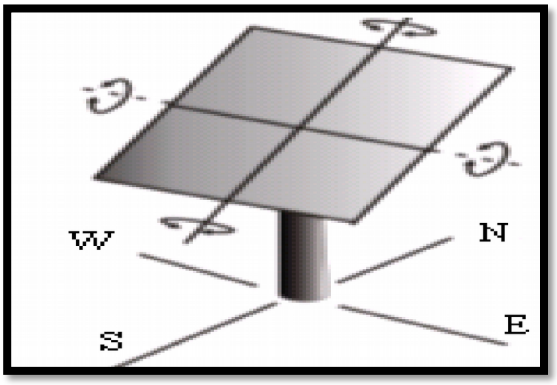


Figure: Dual axis solar tracker

II. EVOLUTION OF SOLAR TRACKER

Since the sun moves across the sky throughout the day, in order to receive the best angle of exposure to sunlight for collection energy[5]. A tracking mechanism is often incorporated into the solar arrays to keep the array pointed towards the sun.

A solar tracker is a device onto which solar panels are fitted which tracks the motion of the sun across the sky ensuring that the maximum amount of sunlight strikes the panels throughout the day[4]. When compare to the price of the PV solar panels, the cost of a solar tracker is relatively low.

Most photovoltaic (PV) solar panels are fitted in a fixed location- for example on the sloping roof of a house, or on framework fixed to the ground. Since the sun moves across the sky though the day, this is far from an ideal solution.

Solar panels are usually set up to be in full direct sunshine at the middle of the day facing South in the Northern Hemisphere, or North in the Southern Hemisphere. Therefore morning and evening sunlight hits the panels at an acute angle reducing the total amount of electricity which can be generated each day.

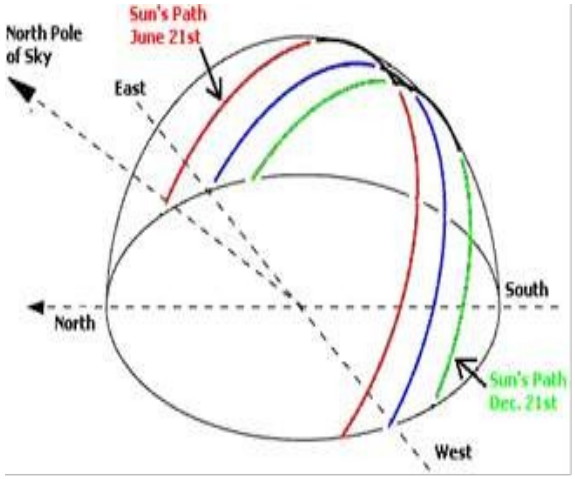


Figure: Sun's apparent motion

During the day the sun appears to move across the sky from left to right and up and down above the horizon from sunrise to noon to sunset[6]. Figure shows the schematic above of the Sun's apparent motion as seen from the Northern Hemisphere.

To keep up with other green energies, the solar cell market has to be as efficient as possible in order not to lose market shares on the global energy marketplace. There are two main ways to make the solar cells more efficient, one is to develop the solar cell material and make the panels even more efficient and another way is to optimize the output

by installing the solar panels on a tracking base that follows the sun. The end-user will prefer the tracking solution rather than a fixed ground system to increase their earnings because:

- The efficiency increases by 30-40%
- The space requirement for a solar park is reduced, and they keep the same output
- The return of the investment timeline is reduced
- The tracking system amortizes itself within 4 years (on average)

In terms of cost per Watt of the completed solar system, it is usually cheaper (for all but the smallest solar installations) to use a solar tracker and less solar panels where space and planning permit.

Types of Solar Trackers

The sun's position in the sky varies both with the seasons (elevation) and time of day as the sun moves across the sky. Hence there are also two types of Solar Trackers.

1. Single Axis Solar Tracker.

2. Dual Axis Solar Tracker.

1. Single Axis Solar Tracker:-Single axis solar trackers can either have a horizontal or a vertical axle. The horizontal type is used in tropical regions where the sun gets very high at noon, but the days are short. The vertical type is used in high latitudes (such as in UK) where the sun does not get very high, but summer days can be very long.

2. Dual Axis Trackers: - Double axis solar trackers have both a horizontal and a vertical axle and so can track the Sun's apparent motion exactly anywhere in the world this type of system is used to control astronomical telescopes, and so there is plenty of software available to automatically predict and track the motion of the sun across the sky. Dual axis trackers track the sun both East to West and North to South for added power output (approx 40% gain) and convenience.

BLOCK DIAGRAM DESCRIPTION:

Microcontroller: It is the major part of the system. The microcontroller controls all the operations. The solar panel is aligned according to the intensity of sunlight under the control of the microcontroller

Sensor:-The system consists of two sensors, each composed of LDR. One unit is made up of four LDRs. These are placed at the four corners of the solar panel. The intensity of sunlight is sensed by the LDR and the output is sent to the controller. The control unit analyses it and decides the direction in which the panel has to be rotated, so that it gets maximum intensity of light. The other unit of sensor is also composed of LDRs which is meant for the control of a lighting load.

Stepper motor:-Stepper motor is used to rotate the panel in desired direction. It is controlled by the controller.

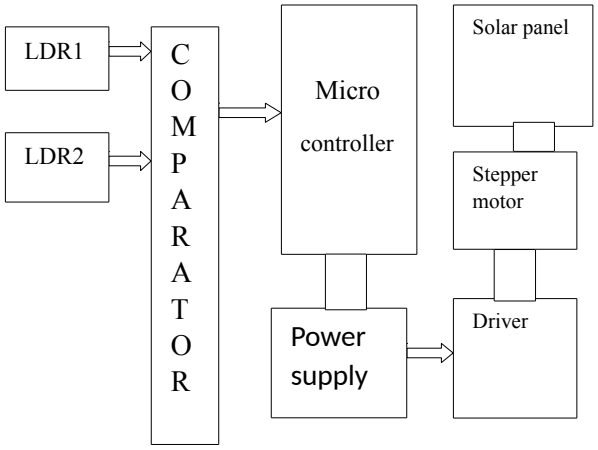


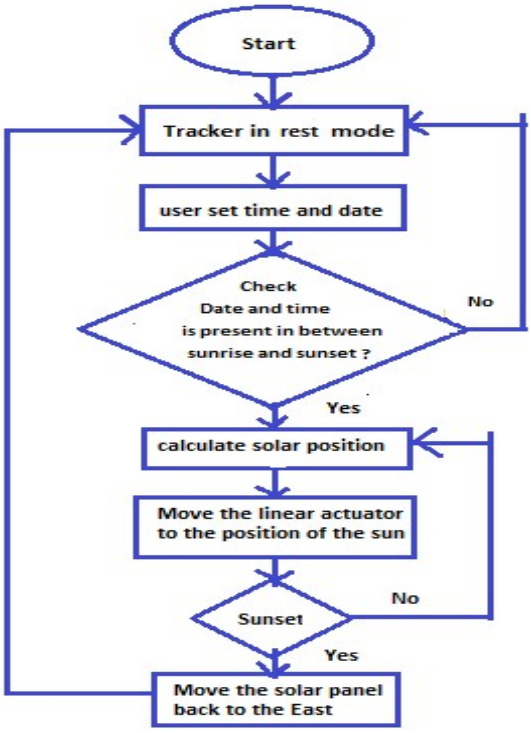
Figure: Block diagram of dual axis model

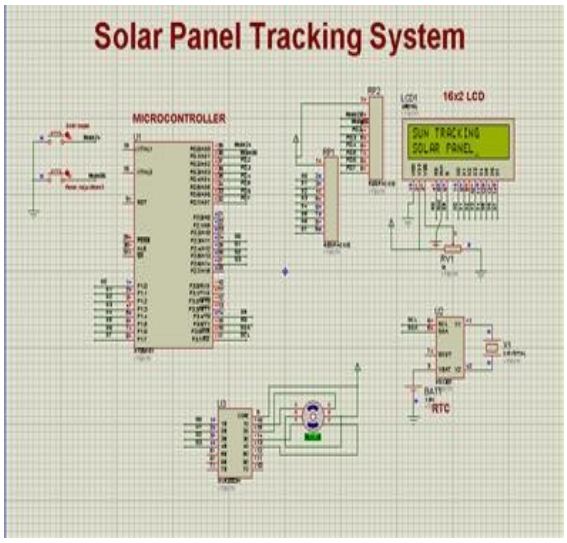
Solar panel: Solar panel is used for the conversion of solar energy directly into electricity. It is composed of photo voltaic cells, which convert solar energy into electrical energy.

PROCESS FOR SOLAR TRACKING:

Initially user first enter the date and time . Microcontroller calculate whether date and time is present in between sunrise and sunset. otherwise microcontroller returns to step. Microcontroller proceeds to step only in the daylight hours and calculate the position of the sun based on longitude

and latitude, as well as date and time.





The main goal of this project is to develop and implement a prototype of two-axis solar tracking system based on a microcontroller. The parabolic reflector or parabolic dish is constructed around two feed diameter to capture the sun's energy. The focus of the parabolic reflector is theoretically calculated down to an infinitesimally small point to get extremely high temperature. This two axis auto-tracking system has also been constructed using AT89C51 microcontroller. The assembly programming language is used to interface the AT89C51 with two-axis solar tracking system. The temperature at the focus of the parabolic reflector is measured with temperature probes. This auto-tracking system is controlled with two 12V, 6W DC gear box motors. The five light sensors (LDR) are used to track the sun and to start the operation (Day/Night operation). Time Delays are used for stepping the motor and reaching the original position of the reflector. The two-axis solar tracking system is constructed with both hardware and software implementations. The designs of the gear and the parabolic reflector are carefully considered and precisely calculated and the solar tracker can be still enhanced additional features like rain protection and wind protection which can be done as future also dual axis solar tracker can be constructed using AVR microcontroller such as ATmega 8/16/32 which has inbuilt 32 KB flash memory and inbuilt Analog to Digital converter.

III. LITERATURE SURVEY:

Till date, several groups have successfully reported the construction and functioning of microcontroller based solar tracking system.

Author name	**publisher**	**Method**	**Advantage**
Asmarashid ponniran,Ammar Hashim and Ariffuddin Joret	University Tun Hussein onn Malaysia	Single axis tracker	Generally lower cost. Used in residential area
Jing-min wang and Chia-liang Lu	MDPIAG (Multi disciplinary Digital Publishing Institute)	Dual axis tracker without micro controller	More efficient compared to normal form. Energy output increases by 30%-40% compared to normal form.

IV. CONCLUSION

In this design, we used Atmel 8051 microcontroller. This design represents a new system design technology, and Keil C - Compiler helped us see the powerful design technologies of software and hardware systems. Most traditional circuit designs are composed of hardware components building on a printed circuit board (PCB), we used same. If errors are found or the system needs to be improved or upgraded, the PCB must be redesigned. Adjusting and modifying the PCB is very inconvenient and increased the design cost and development period. This implementation has great future scope because the Sun is important source of energy which available in free of cost. As today's world need greater amount of energy it can be satisfy by our project use.

In this paper we have come to a conclusion that dual-axis solar tracker is more efficient in terms of the electrical energy output when compared to the single axis tracker and fixed solar panel. The gain of the dual-axis tracking system is about 25-30% compared with the fixed system. For the temperature and covers, they decrease the output power of the solar panel. Therefore, any covering such as dust protection covers will have a negative effect on the amount of power generated by the solar panel.

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Power Estimation and Optimization Techniques using VLSI

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***Abstract*- With the headway in minimal, versatile and high-thickness small scale electronic gadgets and frameworks, the power dispersed in substantial scale incorporated (VLSI) outline circuits has turned into a basic concern. Precision and productivity in control estimation involvedin the outline stage is imperative so as to meet power determinations without high cost overhaul process. This paper, displays a survey of the power enhancement hypothesis approach and the estimation strategies of late recommendation. VLSI configuration has intriguing application region for all combinationcircuit advancement. Invirtual setting all established blend improvement issues, happen in naturalway as subtasks. The fast mechanical progression and major hypothetical idea propels the arithmetic of VLSI outline, which has changed essentially finished the most recent two decades. This study paper additionally gives a current record on the key factors in improvement design.And presents a study of format procedures keeping in mind the end goal to configuration low power advanced CMOS circuits. It depicts the issues looked by the architects at the physical designabstraction and surveys a portion of the procedures which are proposed to defeat these troubles.**

***Keywords*- optimization, VLSI, physical design, layout, placement, routing, MED, BDD, CMOS.**

I. INTRODUCTION

In the past decades, the main concerns of VLSI designers were area, performance, cost involved and reliability; power consumption was mostly of only secondary importance to other things. However, this has begun to change and, with major priority, power consumption is given comparable importance to area and speed. Numerous factors have contributed to this. Portable computing and communication devices demand high-resolution of fast computation and complex functional style with reduced power consumption. Heat generation in high-end computer products limits the feasible packing and performance of VLSI circuits and increases the packaging and cooling costs. Circuit and device reliability deteriorate with increased heat dissipation, and thus the die temperature. Heat pumped into the rooms, the electricity consumed and the office noise diminishes with low power LSI chipset. Our goal in writing this paper is to provide background and outlook for people interested in using or developing low power design methodologies and techniques.

Even though we tried to be complete, some significant research work might have been unintentionally left out. The paper is organized as follows. First, we describe sources of power dissipation in CMOS circuits and degrees of freedom in the low power design space. We then present an in-depth survey (and in many cases analysis) of power minimization techniques and describe some of the frontiers of the research currently being pursued. We conclude by summarizing the major low power design challenges that lie ahead of us.Managing the power of an IC design adds to a growing list of problems that IC designers and design managers have to contend with. Computer Aided Design (CAD) tools are needed to help with the power management tasks.

In CMOS and Bi-CMOS technologies, the chip components (gates, cells) extract power supply current only if a logical transition takes place(ignoringsmall leakage current). While considered an attractive low-power feature technology, it also makes the power-dissipation greatly dependent on the switching activities inside these circuits. Simply put, a more active circuit will consume more power. This complicates the power estimation problem because the power becomes a moving target-it is input pattern dependent. Thus the simple and straight-forward solution of estimating power by using a simulator is severely complicated by this pattern-dependence problem. Input signals are generally unknown during the design phase because they depend on the system (or chip) in which the chip (or functional block) will eventually be used. Furthermore, it is practically impossible to estimate the power by simulating the circuit for all possible inputs.

Recently, several techniques have been proposed to overcome this problem by using probabilities to describe the set of all possible logic signals, and then studying the power resulting from the collective influence of all these signals. This formulation achieves a certain degree of pattern-independence that allows one to efficiently estimate and manipulate the power dissipation.

Sources of Power Dissipation

Power dissipation in digital CMOS circuits is caused by four sources as follows.

- The leakage current, which is primarily determined by the fabrication technology, consists of two components:

1) Reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a MOS transistor, and
2) The sub-threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage,

- The standby current which is the DC current drawn continuously from Vdd to ground,
- The short-circuit (rush-through) current which is due to the DC path between the supply rails during output transitions,
- The capacitance current which flows to charge and discharge capacitive loads during logic changes.

The term static power dissipation refers to the sum of leakage and standby dissipations. Leakage currents in CMOS circuits can be made small with proper choice of device technology. Standby currents are important only in CMOS design styles like pseudo-nMOS and nMOS pass transistor logic. In this article, we assume that the standby dissipation is insignificant, thus limiting ourselves to CMOS technologies, logic styles and circuit structures [1] in which this condition holds.

The dominant source of power dissipation CMOS circuits is the charging and discharging of the node capacitances (also referred to as the capacitive power dissipation) and is given by:

$$P = 0.5 C_L V_{dd2} E(sw) f_{clk} \quad (1)$$

Where C_L is the physical capacitance at the output of the node, V_{dd} is the supply voltage, $E(sw)$ (referred to as the switching activity) is the average number of out-put transitions per $1/f_{clk}$ time, and f_{clk} is the clock frequency.

The term dynamic power dissipation refers to the sum of short circuit and capacitive dissipations. Using the concept of equivalent short-circuit capacitance described above, the dynamic power dissipation can be calculated using equation (1) if we add C_{SC} to C_L. Short-circuit currents in CMOS circuits can be made small with appropriate circuit design techniques [2]. In most of this article, we will thus focus on capacitive power dissipation.

II. Power Minimization Techniques

The challenge to reduce power, the semiconductor industry adopted a multi-faceted approach, attacking the problem from many fronts:

1. Reduction in chip and packaging capacitance: Achieved through process development, SOI with partially or fully depleted wells, CMOS scaling to submicron device design size, and advanced interconnected substrates such as Multi-Chip Modules (MCM).

2. Scaled supply voltage: Very effective in reducing the power dissipation, but requires new IC fabrication process system. Supply voltage scaling also requires support circuitry for low-voltage operation.

3. Improving design techniques: Can bevery successful as the cost to reduce power by design is relatively small in comparison to the other approaches and considered high in potential.

4. Power management strategies: various static and dynamic power managing techniques are application dependent, but, alsoprove to be significant.

III. Physical Design Automation

It provides the automatic layout of circuits minimizing some objective function subject to given constraints. Depending on the target design style, the packaging technology (pcb, multi-chip modules, wafer-scaled integration) and the objective function (area, delay, power, reliability), various optimization techniques are used to partition, place, resize and route gates. Layout problems become more complicated under a real-delay model, which accounts for glitches in the circuit, because layout optimization operations influence the glitch activity in ways that cannot be accurately and reliably predicted.

In the recent past, post-layout optimization techniques (such as buffer and wire sizing, local restructuring and re-mapping) for power reduction (or area and delay recover given a fixed power budget) have become commonplace. The advantage of these techniques is that re-synthesis tools allow more global changes to the circuit structure compared to layout tools. At the same time, the re-synthesis tools have access to detailed post-layout information that allows accurate estimation of circuit area, delay and power dissipation.

Circuit Partitioning

Netlist partitioning is key in breaking a complex and large design into smaller pieces which are subsequently optimized and implemented as separate blocks. This is often needed to satisfy I/O pin constraints on the blocks, reduce the complexity of subsequent optimization steps, or improve performance. Traditionally, the objective functions for partitioning have been the cut-size and/or the circuit delay while the constraints have been I/O pin count per block and block size. Partitioning for low power has recently become an important problem.

Node Clustering

As a result of logic extraction, it is possible to increase the circuit depth to such an extent that the circuit delay becomes unacceptably large. This problem is often mitigated by a reduce depth operation that implements a depth optimal node clustering algorithm based on [3].

This algorithm however makes no attempt to explore alternative clustering solutions that result in the same logic depth, but have lower power dissipation. This is achieved by enumerating, in post order, all candidate clusters of up to a maximum cluster size and selecting the power-optimal cluster solution for each delay value at every gate in the circuit. The algorithm produces optimum delay solutions for general directed acyclic graphs, but the results are not power-optimum because of the possible logic duplication at the multiple fan-out nodes in the circuit. Thus, it is often necessary to perform a delay constrained power-recovery step as a post-process.

Floor planning

Floor planning is assigning shapes, pin positions and locations to a set of macro-cellular or modules for minimizing area of the floor plan. A successful floor planning approach is based on computing the shape functions (height versus width trade-off curves) during a post order traversal of a cluster tree that captures the connectivity among modules. The optimal floor plan topology, block shapes and room assignments, and pin positions (or block orientations) are determined during a pre order traversal of this tree [4, 5]. The two dimensional shape function curves can be indexed by the power cost, that is, for each distinct power dissipation value, one shape function is built. These indexed shape functions can then be used during the pre order traversal to compute the optimal power solution which also leads to minimum chip area as in [6].

Global Routing

Global routing produces routing trees for all nets in the circuit so as to minimize the interconnect length and/or chip area. The routing trees for multi-terminal nets are often constructed as Rectilinear Spanning or Steiner trees. In routing a single net to achieve lower power dissipation, the goal is to minimize the physical capacitance which coincides with the minimum length objective used in conventional routing. Therefore, there is no new routing problem here. The main tasks of a global router for Standard Cell layouts are to generate the routing topology for each net and to determine the number of feed through cells required on each cell row. They assign a feed through penalty to each cell row which characterizes the additional cost (in terms of layout area) that a routing tree edge accrues if it crosses that row. Parallel routing algorithms alleviate the net ordering problem by constructing routing trees for all nets concurrently. One can modify the feed through insertion and net segment assignment steps in these routers to generate tree connections with smaller lengths for nets that are driven by gates with higher switching rates [7].

Detailed Routing

Detailed routing produces the wiring geometries and layer assignments within a routing channel, switchbox or general area. Again, we will only consider channel routing techniques commonly used in Standard Cell layouts. Given the channel length, top and bottom terminal lists, left and right connection lists, and the number of routing layers, the channel routing problem is to find interconnections of all the nets in the channel including the connection sets so that the channel achieves minimum height. The objective function for low power routing becomes the switched capacitance within the channel, that is, high activity nets should assume their shortest possible route at the expense of low activity nets. One must however achieve this with no or little increase in channel height, since otherwise, the increase in wire lengths due to larger layout area will more than compensate the reduction of switched capacitances within the routing channels.

Super Buffer Design

Super buffer design is a chain of inverters designed to derive a large capacitive load with minimal signal propagation time. A power-optimal buffer sizing technique applicable to the design of super buffers at high speed is presented in [8]. This work is based on an analytic relationship among signal delay, power dissipation, driver size and interconnect load which is in turn derived from the I-V characteristics of CMOS transistors. This work shows that optimal-power sizing requires a variable tapering (scaling) factor for the inverter chain.

Power Distribution

When supply voltage is reduced, the noise margins are effectively removed, and thus, small voltage drops in the power distribution system may have a relatively big influence on the systemcircuit speed. Careful power distribution is thus becoming more important at lower supply voltages. In [9], a technique for concurrent topology design and wire sizing in power distribution networks is presented. The objective is to minimize the layout area while limiting the average current density to avoid electro-migration-induced reliability problems and large resistive voltage drops. This technique is based on the observation that when two sinks do not draw currents at the same time, narrow wires can be used for power distribution to those sinks, thus reducing the layout area.

Probabilistic Simulation (CREST)

This approach [10, 11] requires the user to specify typical signal behaviour at the circuit inputs using probability waveforms.

A probability waveform is a sequence of values indicating the probability that the signal is high for certain time intervals, and the probability that it makes low-to-high transitions at specific time points. The transition times,they are not random. This allows the computation of the average, as well as the variance, of the current waveforms drawn by the individual gates in the design in one simulation run. The average current waveforms can then be used to compute the average power dissipated in each gate and the total average power of the circuit.

Transition density (DENSIM)

The averagedamount of transitions per-second at single node in the circuit has been called the transition density in [12], where an efficient algorithm is presented to propagate the density values from the inputs throughout the circuit. This was implemented in the program DENSIM for which the required input specification is a pair of numbers for every input node, namely the equilibrium probability and transition density. In this case, both signal values and signal transition times are random.

Using a BDD

The technique proposed in [13] attempts to handle both spatial and temporal correlations by using a BDD to represent the successive Boolean functions at every node in terms of the primary inputs, as follows. The circuit topology defines a Boolean function corresponding to every node that gives the steady state value of that node in terms of the primary inputs. The intermediate values that the node takes before reaching steady state are not represented by this function. Nevertheless, one can construct Boolean functions for them by making use of the circuit delay information, assuming the delay of every gate is a specified fixed constant.Using a BDD to perform these tasks implicitly means that the BDD variables are assumed independent. The reason is that temporal and spatial independence are effectively assumed at the primary inputs. One disadvantage of this technique is that it is computationally expensive. Since the BDD is built for the whole circuit, there will be cases where the technique breaks down because the required BDD may be too big. As a result, this approach is limited to moderate sized circuits.

Power of individual gates (MED)

This recent technique [13] is a modification of the McPower approach that provides both the total and individual-gate power estimates, with user-specified accuracy and confidence. One reason why one may want to estimate the power consumed by individual gates is to be able to diagnose a high power problem, and find out which part of the circuit consumes the most power.

Other reasons have to do with the fact that estimating gate power is essentially equivalent to estimating the transition density at every node. Indeed, the implementation of this technique in the program MED provides the transition density at every gate output node, in addition to the total power.

IV. CONCLUSION

Power estimation tools are required to manage the power consumption of modern VLSI designs during the design phase, so as to avoid a costly redesign process. Since average power dissipation is directly related to the average switching activity inside a circuit, it would not make sense to expect to estimate power without some information about the circuit input patterns. This information is usually much more readily available to designers than specific input patterns are. All these techniques use simplified delay models, so that they do not provide the same accuracy as, say, circuit simulation. But they are fast, which is very important because VLSI designers are interested in the power dissipation of large designs. In general, it is not clear that any one approach is best in all cases, but we feel that the second statistical approach (MED) offers a good mix of accuracy, speed, and ease of implementation. It may be that a combination of the different techniques can be used for different circuit blocks. The requirement for lower power systems is adapted by many market segments. There are several approaches to reducing power, and the highest economical is through designing for low power. The problem is further complicated by the need to optimize the design for power at all design phases. In summary, low power design requires a rethinking of the conventional design process, where power concerns are often overridden by performance and area considerations. This presented papershowed coverage of low power design methodologies and techniques for estimating the optimization in powerof device circuits and systems.

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A Review on Health Monitoring System by Wireless Sensor Network

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Abstract: In this paper the main focus is on system for smart way of health caring system based upon an advanced wireless sensor networks (WSN). It is specially assisted for living residents and remote health monitoring consumers. We present the advantages, objectives, and status of the design of system. Usually patient visits the doctor periodically TO MONITOR THEIR health condition. By using wireless sensor networks (WSN) technology, the health condition of the patients can be monitored from distant place with ease. We focus on wireless personal area networks methods, WiMAX, Wi-Fi and Zigbee.

Keywords: wireless sensor networks (WSN), Wireless personal area networks (WPAN),* Wi-Fi, *Zigbee.

I. INTRODUCTION

As the day by day world population increases, the number of persons are suffering different diseases is also increased. In health monitoring system we need one observer (nurse) for monitoring the health condition and reporting to doctor. In some emergency applications we need fast response for caring them, these type of situation we also needed one observer. In the case of some delay in any one we loss one life. So we introduced one system that monitors health position of the patients with wireless sensor networks (WSN). This sensors sends the information to doctor. No need of one carrier to send information. In this system we deploy the wireless sensors into patient body and those interconnected using wireless personal area networks like Zigbee, Wi-Fi. Generally wireless personal area networks are working with ultralow power, high data rate and low cost. These wireless sensor networks are transmitted the information from patient to doctor and problem is rectified by the doctor. No need of doctor checking periodically. In this paper a network architecture for smart way of health monitoring system which show the path for continuous observation of resident patients [1,2]. We can reduce the high installation cost and also implement different systems using future applications of medical field as integrity and web sensors. The wireless sensor networks (WSN) has following properties:

- **PORTABILITY:** We are inserting small devices and its collects the information and send's through wireless environment and also operating with low voltages.

- **EASE OF DEPLOYMENT:** The devices which are used for wireless sensor network was occupied less space compare to wired network system and also wireless system can replace with even wired system wasn't placed.

- **REAL-TIME AND ALWAYS ON:** Physiologically and environmental data can be monitored continuously and allowing real-time response by emergency or healthcare workers even though the network was whole was always – on, individual sensors still must conserve energy through smart power management and on-demand activation.

- **RECONFIGURATION AND SELF- ORGANISATION:** In this system there are no fixed installations, adding and removing sensors instantly reconfigures the network. Doctors may re target the aim of the network as medical need change. Sensors self-organize to form routing paths, collaborate on data processing.

II. ARCHITECTURE

In figure 1 shows the WBAN (wireless body area network) technology is a consequence of WSN technology. In this WBAN the sensors placed on the human body and create a wireless body area network that can monitor various vital signs. The system consists of multiple sensor nodes and these sensors give the body motion to ECG. Data controlled by the medical sensors is mainly transmitted to the coordinator and sensors are activated continuously transmit data to the coordinator .by using this sensors the overall operational time is reduced.

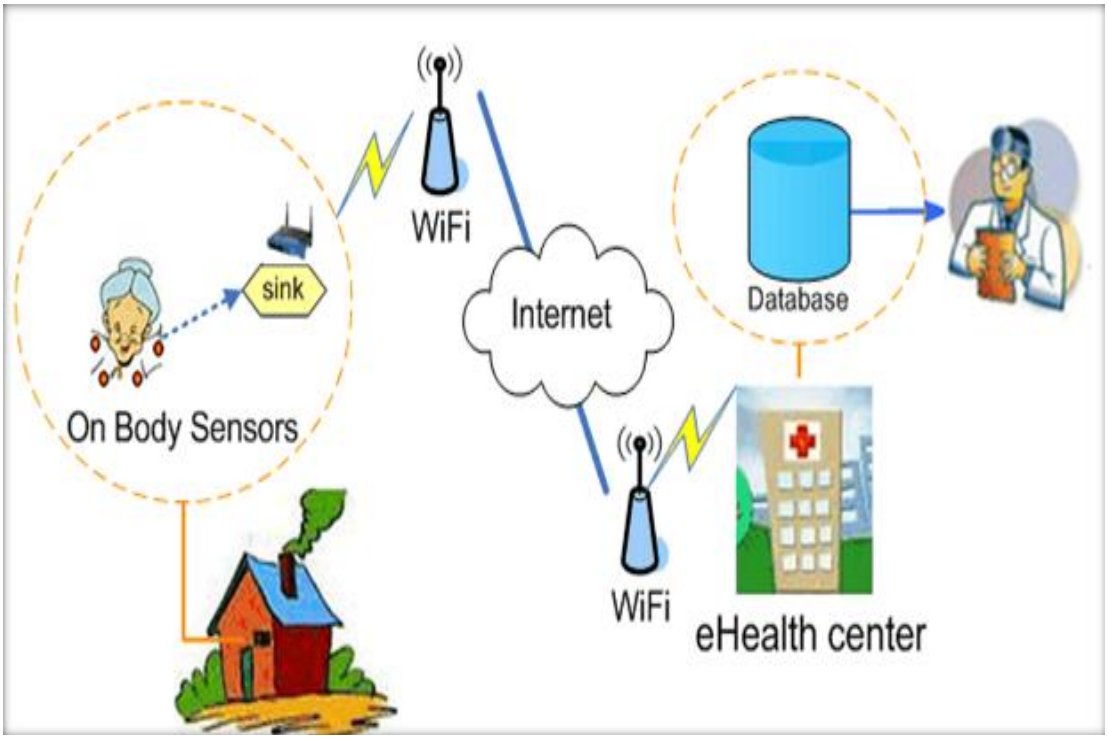

Figure 1 Wireless Body Area Network

In figure 2 represents the other form of WBAN in that various form of the multiple nodes transmitted through the internet to multiple sensors. These systems have low power consuming, accurate and with less latency. Some popular protocols for WBAN which are TMAC, SMAC, Zigbee MAC and Baseline MAC [1-3].

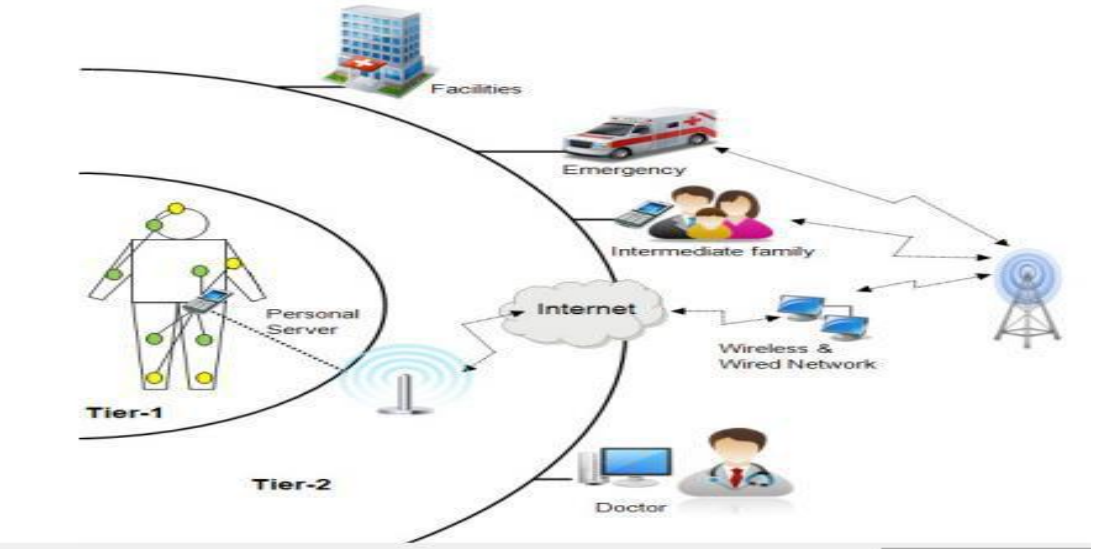

Fig 1: Another form of WBAN architecture MAC protocols are used in WBAN

III. CHALLENGES OF WBAN NETWORKING

The following are the main challenges:

- **Energy Efficiency:**
  Communication amongst the sensor hubs intakes additional energy when contrasted with detecting and processing. For embedded bio-therapeutic sensors, it is not feasible to restore the power source, while for wearable bio-therapeutic sensors restoring the batteries may direct to inconvenience of patients. Subsequently, energy utilization and network lifetime are key challenges in WBANs [4].

- **Antenna Design**
  The modifications in the structure of the antenna depend on the state of the body, indicating the requirement of stretchy, fabric antennas. Nonetheless, these sorts of antenna are not effortlessly amendable to body motion as these are largely placed on top of substrates with little bending ability [5].

- **Diverse environment**
  Particular uses of WBANs may require diverse information gathering from different sensors of distinctive sampling values. Hence, Quality of Service support in WBANs possibly will be demanding [6].

- **Limited Resources**
  Communication abilities, existing memory and computational power are inadequate for hubs in WBANs, especially those embedded in the body. In addition, energizing or altering batteries in WBANs are not reasonable for gadgets which require a long lifetime [6].

- **Energy Absorption and Overheating**

  The node temperature is increased by radiation absorption and power utilization of node [10], which influences the heat susceptible organs of the human body and cause harm to some tissues [11]. The routing protocols need to be carefully developed for routing protocols to keep tissues of human body in safe zone from overheating [8].

- **Path loss**

  The reduction in power density of an electromagnetic wave as it travels via the wireless channel is called path loss. [8]. The wireless communication between the embedded sensor hubs in human body, where the path loss vary from 4 to 7 [7], which is extremely high as compared to the free space, where it is two. Path loss should be taken into account while designing routing protocols for wireless body area networks.

- **Security**

  Security issues require effective and efficient validation techniques in BANs. However the security is the main apprehension in the majority networks and the security conditions anticipated for other networks are not valid to WBANs.

IV. CONCLUSION

Wireless Body Area Networks are a very useful technology which offers a wide range of uses not only to patients but also to the whole society by continuous monitoring. Thus WBANs ensure in improving the quality of life. Even though Body Area Networks are projected to play a predominant role in numerous aspects of daily life, but, as of today, use of these types of networks is fairly restricted. Different standards which can be used in different application domains of WBANs are also discussed. One of the major challenges in WBANs is security management. So, to safeguard the user's information some techniques are discussed. Also different channel models are discussed.

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Spatial Methods for Multispectral Pansharpening: Demystified and Multiresolution Analysis

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Abstract

The majority of multispectral (MS) pansharpening methods may be labeled as spectral or spatial, depending on whether the geometric details that shall be injected into the interpolated MS bands are extracted from the panchromatic (P) image by means of a spectral transformation of MS pixels or a spatial transformation of the P image, achieved by means of linear shift-invariant digital filters. Spectral methods are known as component substitution; spatial methods are based on multi-resolution analysis (MRA). In this paper, the authors show that, under the most general conditions, MRA-based pansharpening is characterized by a unique separable low-pass filter, which can be parametrically optimized based on the modulation transfer function (MTF) of the MS instrument, possibly followed by decimation and interpolation stages. This happens for the discrete wavelet transform (DWT) and its undecimated version (UDWT), for the "a-trous" wavelet (ATW) transform and their decimated versions, i.e., the generalized Laplacian pyramids (GLP), and for nonseparable wavelet transforms, such as the nonsubsampled contourlet transform (NSCT). Hybrid methods, in which MRA fusion is performed on the intensity component derived from a spectral transformation, are equivalent to MRA fusion with a specific detail injection model. ATW and GLP are preferable to DWT, UDWT, and NSCT, because of computational benefits and of a looser choice of the low-pass filter, unconstrained from the requirement of generating a perfect reconstruction filter bank. Ultimately, GLP outperforms ATW, because its decimation and interpolation stages allow the aliasing impairments intrinsically present in the original MS bands to be removed from the pansharpened product.

INTRODUCTION

PANSHARPENING refers to the fusion of a panchromatic (P) and a multispectral (MS) image simultaneously acquired over the same area, with spatial resolution greater for the former. This can be seen as a particular problem of data fusion since one would aim at combining the spatial details resolved by P (but not present in MS) and the spectral diversity Manuscript received August 4, 2015; revised October 16, 2015; accepted November 19,2015.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TGRS.2015.2503045 of the MS image (against the single band of P) in a unique product. Nowadays, P and MS images can be obtained in bundle by several commercial optical satellites such as IKONOS, Geo-Eye, OrbView, Landsat-8, SPOT, QuickBird, WorldView, and Pleiades. The spatial resolution may be even below half a meter for P, and the spectral resolution can be up to eight bands captured in the visible and near-infrared wavelengths for the MS product. The fusion of the P and MS images constitutes the sole possibility for achieving images with the highest resolutions in both the spatial and spectral domains, because physical constraints on spatial and spectral resolutions and signal-to-noise ratio (SNR) preclude this goal from being achieved by using a single MS instrument.

The demand for pansharpened data is continuously growing, due to the increasing availability of commercial products using high-resolution images, such as Google Earth and Bing Maps. Furthermore, pansharpening constitutes an important preliminary step for enhancing images for many remote sensing tasks, such as change detection [1], object recognition, visual image analysis, and scene interpretation [2], The interest of the community in pansharpening is evident by reviewing the recent technical literature. Detailed surveys of pansharpening algorithms can be found in [3] and [4], A first comprehensive textbook thoroughly devoted to remote sensing image fusion, which covers progresses in pansharpening

over the last two decades, has been recently published by the authors [5].

The focus of this paper is on one of the two main approaches, namely, spectral and spatial, that are traditionally considered for pansharpening: the component substitution (CS) and the multiresolution analysis (MRA), respectively. This hard categorization is brought back to a previous effort of the authors [6], in which it is proven that there exists a duality between the classes of spectral and spatial methods featuring complementary properties of robustness to spatial and spectral impairments, respectively.

The MRA approach consists of the injection of spatial details, which may, in principle, be obtained through a multiresolution decomposition of the P image, into the MS bands interpolated at the scale of P. The spatial details can be extracted according to several modalities of MRA: decimated wavele transform (DWT) [8], undecitnated wavelet transform (IJDWT) [9], "a-trous" wavelet (ATW) transform [10], Laplacian pyramid (HP) [11], and nonseparable transforms, either based on wavelets (e.g., contourlet [12]) or not (e.g., curvelet [13]). In addition, mixed approaches, in which MRA is coupled to a spectral transformation, typically IHS or PCA, are possible.

The math notation used in the next sections is detailed in the following. Vectors are indicated in bold lowercase (e.g., x), with the *th element indicated as x*. Two- and three-dimensional arrays are expressed in bold uppercase (e.g., X). An MS image M = $\{M_{fc}\}_{fc=1\ N}$ is a 3-D array composed of N bands indexed by the subscript k = 1, . . . , N; accordingly, M_{fc} indicates the kth band of M. A generic P image is a 2-D matrix and will be indicated as P. In addition, M_{fc} and Mfc indicate the interpolated and sharpened fcth MS bands, respectively.

The remainder of this paper is organized as follows. Section II presents a review of the CS, or spectral, approach, providing a synthetic description of the three most popular algorithms belonging to this class. Section III is devoted to reviewing spatial methods since their origin. Evidence is also provided that any MRA fusion method can be achieved by means of a unique low-pass filter, possibly followed by decimation and interpolation stages. Section IV formalizes the behavior of fusion schemes based on CS and on either undecimated or decimated MRA, in the presence of aliasing impairments that are intrinsically present in the MS data set. Simulations are reported together with a detailed discussion of results. Finally, conclusions are drawn in Section V.

II. SPECTRAL TECHNIQUES FOR PANSHARPENING

This class of techniques is based on the projection of the MS image into another vector space, assuming that this transformation splits the spatial structure and the spectral information into different components. Subsequently, the transformed MS image can be enhanced by replacing the component containing the spatial structure with the P image. Accordingly, the greater the correlation between the P image and the replaced component, the lower the distortion introduced by this fusion approach [3], To this purpose, histogram matching of the P image to the selected component is performed before the substitution takes place. Thus, the histogram-matched P will exhibit same mean and variance as the component to replace. Finally, the pansharpening process is completed by bringing the data back to the original space through the inverse transformation.

This approach is global (i.e., it operates in the same way on the whole image), leading to advantages and limitations. In greater details, techniques belonging to this class are usually characterized by high fidelity in rendering the spatial details in the final product [24], and they are generally fast and easy to implement. On the other hand, they are not able to account for local dissimilarities between the P and MS images originated by the spectral mismatch between the P and MS channels of the instruments, which may produce significant spectral distortions [3],

A new formalization of the CS approach was proposed by Tu et al, [25] and then analyzed in subsequent works [24], [26], It was shown that, under the hypothesis of a linear transformation and the substitution of a single component, the fusion process can be obtained without the explicit calculation of the forward and backward transformations, but through a proper injection scheme. This observation leads to a faster implementation of these methods. A general formulation of CS fusion is given by

$$Mfc = Mfc + fffc(P - I),\ k = 1, \ldots, N \qquad (1)$$

in which the subscript k indicates the fcth spectral band, g = [g\, . . . , gu, g N] is the vector of the injection gains, whereas I is defined as

$$\mathbf{I} = \sum_{i=1}^{N} \qquad (2)$$

in which the weight vector w = [w i, . . . , «y, . . . , w_N] is the first row of the forward transformation matrix and may be chosen, whenever possible, to measure the degrees of spectral overlap among the MS and P channels.

Fig. 1 shows a flowchart describing the fusion process of the CS approach. Specifically, it is possible to notice the presence of blocks aimed at the following: 1) interpolating the MS image for matching the scale of P; 2) calculating the intensity

component by means of (2); 3) matching the histograms of the P image and the intensity component; and 4) injecting the extracted details according to (1).

The CS family includes many popular pansharpening approaches, such as the IHS [25], PCA, and GS [4], [24] methods, which differ by the projections of the MS image used in the process. Due to the lack of a unique transform for extracting the component most suited for substitution, methods based on its adaptive estimation have been proposed; they are known as adaptive CS [24], [27], [28], In the following, a more detailed description of the main CS methods is presented.

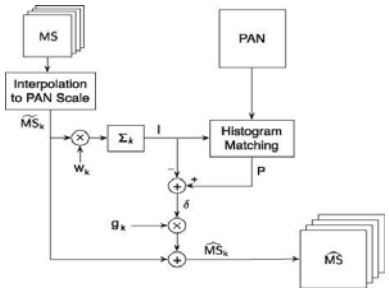


Fig. 1. Flowchart presenting the blocks of a generic pansharpening procedure based on the CS approach.

A. **GIHS**

The IHS pansharpening method [5] exploits the transformation into the IHS color space that mimics the human visual system in processing the intensity (I), hue (H), and saturation (S) information. The IHS transform can be only applied to RGB true color images, leading to a major limitation for processing MS images. In [25], the authors have generalized the concept of IHS to images with more than three bands (GIHS). Subsequent studies [26] have proven that GIHS can be formulated for any arbitrary set of nonnegative spectral weights as in n which I follows from (2). In general, the coefficients {m»}fc=i N are ecl[ua]l 1° 1/^ [25]. The spectral weights must be nonnegative and may not sum to one. In that case, the injection gains provide the proper rescaling [26], IHS (N = 3) may be implemented as a fast IHS, which avoids the sequential computation of the direct transformation, substitution, and the final backward step. GIHS is implicitly fast, because the transformation does not exist for N > 3.

In (1), defining space-varying local injection gains G, such that

$$G_{fc} = \wedge, \quad k = 1, \ldots, N \qquad (4)$$

yields

$$M_{fc} = M_{fc} + \wedge \bullet (\mathbf{P} - \mathbf{1}) = M_{fc} \bullet y \qquad (5)$$

which is the widely known Brovey transform (BT) pansharpening method [5], Thus, BT may be achieved by the general model (1) with the choice of injection gains (4) and represents a multiplicative, rather than an additive, sharpening [29], i.e., a spatial modulation of spectral pixels.

B. **PCA**

PCA, a.k.a. Karhunen-Loeve transform or Hotelling transform, is another spectral transformation that has been widely employed for pansharpening [5], PCA is achieved through a multidimensional rotation of the original coordinate system of the (V-dimensional vector space, i.e., a linear transformation of the data, such that the projection of the original spectral vectors on the new axes, which are the eigenvectors of the covariance matrix along the spectral direction, produces a set of scalar images, which are called principal components (PCs), that are statistically uncorrelated to each other. PCs are generally sorted for decreasing variance, which quantifies their information content.

Specifically, the hypothesis underlying the use of PCA for pansharpening is that the spatial information, originally shared by all the channels, is concentrated into the first component (PCI), whereas the spectral information (specific to each single band) is accounted by the other N — 1 components. However, the equivalent spectral response of PCI, combination of the spectral responses of the MS instrument, may not match the spectral response of the P instrument. Severe spectral distortions may occur from the spectral mismatch between PCI and P. Again, the fusion process can be described by the general formulation stated by (1), where the w and g coefficient vectors are derived by the PCA procedure on the MS image. In general [25], [26], w is the first row of the forward transformation matrix; g is the first column of the backward transformation matrix, which is equal to its transpose for PCA, whose matrix X is data dependent.

C. **GS**

The GS orthogonalization procedure is the basis for defining a powerful pansharpening method, patented by its inventors in 2000 for Eastman Kodak and implemented in ENVI, release 4.3 onward, as GS spectral sharpening. The GS transformation is a common technique used in linear algebra and multivariate statistics to orthogonalize a set of vectors.

Since GS is a generalization of PCA, in which PCI may be arbitrarily chosen and the remaining components are calculated to be orthogonal/uncorrelated to one another and to PCI, the procedure may be still be described by the flowchart in Fig. 1. Again, the fusion process is described by (1), with the injection gains given by [24] $\mathrm{cov}(M_{fc}, I)\ \mathrm{var}(I)$ in which cov(X, Y) indicates the covariance between two images X and Y, and

var(X) is the variance of X. The notation gk highlights that the injection model is global for the fcth band. In addition, space-varying local injection gains G_{fc} can be calculated according to (6) [30], This way, however, the fusion method is no longer GS spectral sharpening.

Several versions of GS are obtained by changing the method for generating I. The simplest way to obtain the low-resolution approximation of P consists of simply averaging the MS components (i.e., setting $w_{„} = 1 / N$, for all i = 1this modality is simply called GS or GS mode 1. In [24], the authors proposed an enhanced version, which is called adaptive GS

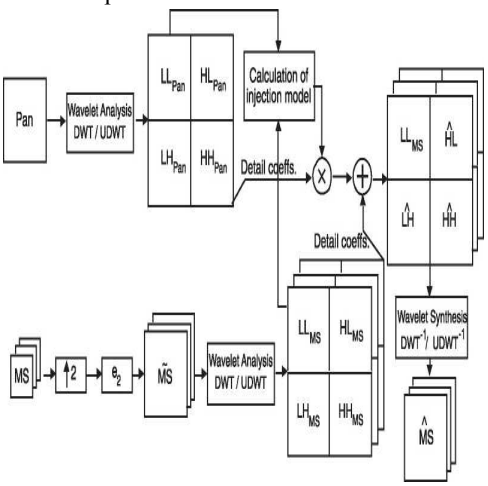


Fig. 2. Flowchart of MRA-based pansharpening exploiting DWT/UDWT. For simplicity of flow, the scale ratio is r = 2.

(GSA), in which I is generated by a weighted average of the MS bands, with mean square error (MSE)-minimizing weights with respect to a low-pass-filtered version of P, i.e., P_p

$$PL = \hat{}w_{fc}M_{fc}. \quad (7)$$

The set of optimal weights $\{iv_k\}_{k=1\ N}$ is calculated as the minimum MSE solution of (7).

A further option for generating the low-resolution intensity image I entails the application of a low-pass filter to the original P image and is referred to as GS mode 2, leading to a hybrid approach, which is no longer based on CS, but actually belongs to the MRA-based class.

III. Spatial Techniques for Pansharpening

The spatial approach to pansharpening relies on the injection of spatial details, obtained through a multiresolution decomposition of the P image, into the resampled MS bands [31], The spatial details can be extracted according to several modalities of MR A: (decimated) DWT [8], UDWT [9], ATW transform [10], generalizedLP (GFP) [11], [32], and nonseparable transforms, either based on wavelets (for example, contourlet [12]) or not (curvelet [13]). For a concise review of MRA within the framework of pansharpening fusion, the reader is referred to [5], [31], and [32],

This paradigm has been denoted by Amelioration de la Resolution Spatiale par Injection de Structures (ARSIS), where the French acronym stands for spatial resolution enhancement by injection of structures to highlight that the purposes of these methods are the preservation of the whole content of the MS image and the addition of further information obtained from the P image, through spatial filtering [33], Originally conceived and developed for DWT, ARSIS can easily accommodate other types of MRA, such as ATW and GFP [34],

Although the forerunners of the spatial approach were not based on a formal MRA, pioneering MRA-based methods [35]—[38] strictly used DWT. Fater, the favorable features of UDWT (translation invariance, looser choice of filter banks, absence of aliasing artifacts [39]) led to a brief period of popularity. However, DWT and UDWT were quickly abandoned after GFP and ATW were introduced for fusion in [40] and [41], respectively.

In the assumption of a dyadic tree-split MRA (DWT/UDWT), the steps of the generic pansharpening procedure for MS and P data, whose scale ratio r is a power of 2, are the following.

1) Interpolate MS to match the scale of P and exactly overlap to it [42],
2) Calculate the MRA of each of the MS bands with a depth equal to $\log_2(r)$.
3) Calculate the MRA of the P image with a depth equal to $\log_2(r)$.
4) Calculate the band-dependent injection gains $\{_9k\}k=i\ n$ trom the base bands of each MS band and of P, namely, FF_{MS} and FF_{PAN}-
5) Add the detail subbands of P (HH-horizontal, HF-vertical, HH-diagonal), weighted by the injection gain to the corresponding subbands of each MS band.
6) Apply the inverse transform to the enhanced subbands of each MS band to yield the pansharpened MS image.

Fig. 2 illustrates the fusion procedure for the case of UDWT and r = 2. In the case of DWT, the flowchart is identical; only the subbands are smaller in size, due to decimation. The corresponding frequency partition is presented in Fig. 3.

A. Fast MRA-Based Pansharpening

In the seminal paper by Tu et al, [25], the mathematical development that led to the fast algorithm of GIHS was also applied to the MRA fusion achieved through ATW. In addition, the fusion described by the flowchart in Fig. 2 allows a

fast implementation, which does not require computation of the forward and inverse transform (either DWT or UDWT). Fet us first consider the undecimated scheme (UDWT). Fet also assume that the low-pass filter of the analysis filter bank is symmetric with zero phase. Such a condition imposes that the filter bank cannot be orthogonal.

	7T	U y	
7T	**HH MNNI .....**	**LH**	**HH**
	m.	**LL**	**HL**
	HH	**LH**	**HH**
	—7r		

Fig. 3. Spatial frequency plane partition of DWT and UDWT: the four subbands of a depth-one decomposition correspond to as many regions labeled as LL, HL, LH, and HH, depending on the filters (L = low-pass, H = high-pass) applied along the x- and y-axes of the image plane, respectively.

applications, including JPEG 2000, because of its favorable characteristics.

The linearity of the transformation makes the backward transform of the forward transform of P, in which the LL subband has been set equal to zero, to be equal to P — PL, where PL =LLPAN. In addition, the forward transform of the interpolated MS, i.e., M_{fc}, is no longer necessary, because the addition of details is performed in the spatial domain. The injection model shall be calculated between M_{fc} « LL_Ms and PL = LLPAN- The fast algorithm holds in the assumption of additive combination of details, which is formally more correct than the substitutive combination [41], because the former thoroughly preserves the original information of the MS image. In principle, Mfc ^ LL_Ms; in practice, they are equivalent. If the scale ratio is not 2, but a power of 2 (r = 4 is the most typical case), the low-pass filter that generates PL as a linear separable convolution is not the low-pass filter of the analysis filter bank, which is the 1:2 filter bank, but the low-pass filter of the equivalent 1:4 filter bank [5], [32], which is easily calculated from the prototype 1:2 filter bank.

The main result of this study is that only the equivalent low-pass filter that generates the baseband image affects the pansharpened image. The number and orientation of high-pass subbands are totally irrelevant, because the injected term is proportional to the backward transform of the forward transform of P minus the baseband, that is, the backward transform of all the detail subbands. Hence, the contribution of the P image to the fused product is achieved by calculating the difference between P and its low-pass version achieved by means of the low-pass analysis filter h, i.e.,

$$P_L = P \circledR 1_I. \quad (8)$$

This strictly holds for UDWT; there is a difference in the case of DWT because of aliasing introduced by decimation. Since DWT can be obtained by decimating the output of UDWT, the low-pass approximation of P in the decimated case will be obtained as

$$P_L = (((P <*> h) 4. r) t >') <5> h \quad (9)$$

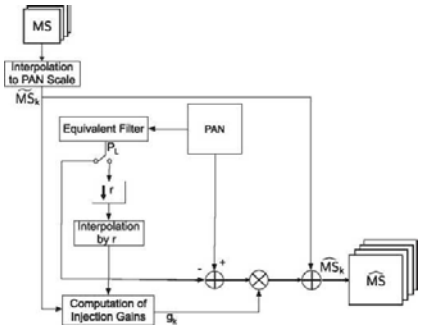


Fig. 4. Flowchart of a generic pansharpening algorithm belonging to the MRA class. The switch on the low-pass-filtered P enables a decimated (GLP, DWT) or an undecimated (ATW, UDWT) type of analysis.

in which h and h are the low-pass filters of the analysis and synthesis filter banks, respectively.

Given also the results of [25] in the case of ATW, the most general MRA-based fusion model, in the absence of decimation, may be stated as

$$M_{fc} = M_{fc} + 3_{fc}(P - P\_L) \quad V k = 1, \ldots, N. \quad (10)$$

According to (10), the different approaches and methods belonging to this class are uniquely characterized by the low-pass filter employed for obtaining the image PL and by the set of injection gains $\{gk\}_k$=i,...,N-

The general scheme of MRA fusion methods is reported in Pig. 4. Accordingly, the required blocks are devoted to the following: 1) interpolate the MS image to reach the panchromatic scale; 2) calculate the low-pass version P_L of the P image by means of the equivalent filter for a scale ratio equal to r; 3) compute the band-dependent injection gains $\{gk\}_k$=i n> and 4) inject the extracted details according to (10). Note that, apart from the filter, there is a difference if PL is decimated- interpolated or not.

Interpolation is less crucial than for CS methods, because, if the original data sets are intrinsically misaligned by constant values along rows and columns, e.g., by 1.5 pixels for 4:1 scale ratio between MS and P (see [42]), the subsequent

step may realign the details extracted from P, provided that linear nonzero phase filters are used for MRA.

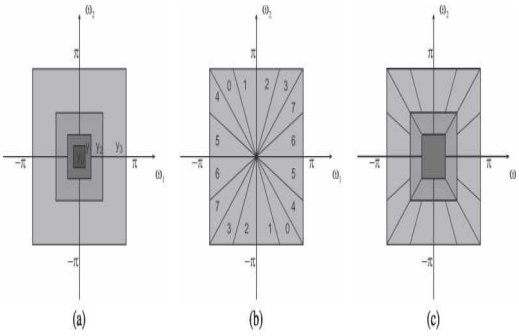


Fig. 5. Spatial frequency analysis of NSCT. (a) Octave decomposition of spatial frequency plane, (b) Eight-subband directional decomposition of frequency plane, (c) Directional octave decomposition achieved by NSCT.

B. ***Nonseparable MRA***

As a result of a separable extension from 1-D bases, 2-D wavelet representations are capable of isolating the discontinuities at edge points, but do not efficiently describe the smoothness along the contours. In addition, separable wavelets can capture only limited directional information, which are an important and unique feature of multidimensional signals [12]. Nonseparable MRA not only allows images to be successively approximated, from coarse to fine resolutions using localized coefficients in both the spatial and scale domains, but it also contains basis elements *oriented* at a variety of directions, much more than the few directions that are offered by separable wavelets. In addition, to capture smooth contours in images, the representation contains basis elements using a variety of elongated shapes with different aspect ratios.

The curvelet transform [13] is conceptually a multiscale pyramid with many directions and positions at each length scale, as well as needle-shaped elements at fine scales. The representation provided by contour let [12] achieves the optimal approximation rate for 2-D piecewise smooth functions with C^2 (twice continuously differentiable) contours.

In image fusion applications, curvelets have been directly applied to pansharpening in [44], and contour lets have been used in a PCA-based scheme [45], An alternative approach equivalent to nonseparable MRA, which has been applied to pansharpening [46], is dual-tree complex DWT (DTC-DWT). However, despite the elegance of nonseparable transformations and the potentiality offered by directional subbands in a variety of applications, already in [44], the authors noticed that, unless a nonlinear injection model is specifically designed and applied in the directional transformed domain, e.g., soft thresholding of coefficients for noise reduction of P, the linearity of the transformation makes no advantages whatsoever stem from the use of nonseparable rather than separable transforms. Now, we can add that, in the case of nonselective injection of all directional details, the behavior of the transformation depends only on the equivalent low-pass filter that generates the baseband approximation, which is separable, unlike all the high-/ bandpass filters. Fig. 5(c) highlights the regions in the spatial frequency plane spanned by the directional subbands and by the baseband, which is not directional.

C. ***Optimization of MRA Based on Instrument MTF***

Here, we will review the main results of [47], in which evidence is given that optimization of the unique low-pass filter used for MRA-based fusion can be achieved if its response in the spatial frequencies matches the modulation transfer function (MTF) of the imaging instrument. The MTF is equal to the modulus of the Fourier transform of the point spread function (PSF) of the imaging system. In principle, two spectral replicas originated by 2-D sampling of the radiance signal with the same sampling frequency along and across track should cross each other at the Nyquist frequency (half of the sampling frequency) with magnitude values equal to 0.5. However, the scarce selectivity of the response prevents from using a sampling frequency that yields a Nyquist frequency with a magnitude equal to 0.5. As a tradeoff between (maximum) spatial resolution and (minimum) aliasing of the sampled signal, the sampling frequency is usually chosen such that the corresponding magnitude at the Nyquist frequency is comprised between 0.2 and 0.3.

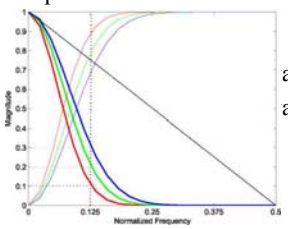
Ultimately, the problem may be stated in the following terms: an MS band resampled at the finer scale of the P image lacks high-spatial frequency components, which may be inferred from the P image via a suitable interscale injection model. If the high-pass filter used to extract such frequency components from the P image is taken to approximate the complement of the MTF of the MS band to be enhanced, the high-frequency components that have been damped by the MTF of the instrument can be restored. Otherwise, if spatial details are extracted from the P image by using a filter having normalized frequency cutoff at exactly the scale ratio between P and MS (e.g., 1/4 for 1-m P and 4-m MS), such frequency components will not be injected. This occurs with critically subsampled wavelet decompositions, whose filters are constrained to cutoff at exactly an integer fraction (usually a power of 2) of the Nyquist frequency of P data, corresponding to the scale ratio between P and MS.

An attractive characteristic of the

redundant pyramid and wavelet decompositions proposed by the authors [32], [47] is that the unique low-pass reduction filter used to analyze the P image may be easily designed such that it matches the MTF of the band into which the details extracted will be injected. Fig. 6 shows examples for three values of magnitude cutoff. The resulting benefit is that the restoration of spatial frequency content of the MS bands is provided by the MRA of P through the injection model. Such a facility is not immediate with conventional DWT and UDWT decompositions [48], However, if prior knowledge of the nonseparable non-Gaussian MTF is inadequate, the optimization of spatial methods may be directly achieved by analyzing the MS image [49],

M_{fc} *D.* ***Hybrid Methods*** $(P-P_L)$, I.....

In several cases, MRA has been coupled with a spectral transformation, with the presumable intent of combining the assets of both classes in a unique method.



ar(M_{fc})
ar(PCl) ’

$k = l, \ldots, N$ (15)

Fig. 6. Normalized 1-D frequency responses of equivalent filters for separable 2-D 1:4 MRA: Gaussian-shaped low-pass filters with magnitudes of 0.1, 0.2, and 0.3 at Nyquist frequency. The dashed line represents the spectrum of the P image, whose high-frequency content is

Mfc = M(selected by each high-pass filters for $(P-Pi$ $k = 1, \ldots, N.$ (16)

injection in the corresponding spectral band. The dotted vertical line marks the Nyquist frequency of MS, one fourth of the Nyquist frequency of P, which is half the sampling frequency of P (equal to one in normalized plots).

1) ***AWLP:*** The first and perhaps most notable case is the additive wavelet luminance (AWL) method [41], in which the nonlinear IHS triangle transform, originally used standalone for fusion, is the first step, and a subsequent step involving ATW is used to spatially enhance the intensity component. The intrinsic limitation of dealing with only three bands at a time was overcome in a subsequent study of the same authors, who noticed that AWL corresponds to injecting the spatial details of P proportionally to the modulus of the MS pixel vector, hence the new denomination *additive wavelet luminance proportional* (AWLP) [50],

According to the formalization of the fast MRA-based pan- sharpening, AWLP can be recast as

$$M_{fc} = M_{fc} + \hat{} \cdot (P - P_L), k=l,...,N \quad (11)$$

in which P is the P image histogram matched to I. The model (11) may be achieved by setting the *space-varying* injection gains

$$G_{fc} = \hat{}, k = l,...,N \quad (12)$$

that is, AWLP is equal to a fast MRA fusion without decimation, with the prototype filter derived from the choice of a B_3 cubic spline as the scaling function of MRA and with injection gains given by (12). Again, I is given by (2), with spectral weights equal to 1 */N.*

2. *GIHS + MRA:* This case consists of calculating the generalized intensity (2), histogram matching the P image to I and injecting the high-pass details of the histogram-matched P into the interpolated MS bands. In formulas -l $k = 1, \ldots, N$ (13)

in which P is the P image histogram matched to I. Since the spectral gains usually sum to one, apart from the different matching of the P image, there is no substantial difference from plain MRA fusion. That is the reason for which this method has been seldom investigated in the literature.

1) PC A + MRA: The coupling of PCA with MRA has been the object of extensive investigations [45], [51], The basic method, in principle, consists of calculating the PCA of the MS image, matching the histogram of the P image to that of the first component PCI, sharpening PCI by means of the histogram- matched P, and reversing the PCA transform to yield back the fused MS image. By applying both the fast PCA transform [5], [30], in which only PCI must be calculated and the application of reverse transform is not required, and the fast MRA (10), the following relationship is found:

$$\frac{cov(Mfc, PCI)}{var(PCl)}$$

in which P is the P image histogram matched to PCI. As it appears, the effect of PCA is embedded in the injection model

$$\_ \frac{cov(Mfc, PCI)}{var(PCl)}$$

$$= CC(Mfc, PCI) \bullet$$

which may be written as a function of the correlation coefficient (CC) and is analogous to Gram-Schmidt's projection coefficients (6).

2) GS + MRA: The coupling of GS with MRA has never been investigated in the literature, because it is implicit in the option (GS mode 2), in which the low-pass approximation of the P image that is used as intensity component is achieved by its low-pass filtering. Histogram matching of P to I is no longer necessary because, in this case, I =

P_L- The relationship is cov(M_{fc},P_L)

var(P_L)Unlike (14), the projection is made on V_L instead of on PCI. It is expected that (16) is better than (14), because both inject the detail P - P_L proportionally to the projection coefficients of individual bands, but the former on P_L, the latter on PCI. Since P_L is the low-pass component of P, it seems more reasonable that the high-pass component P - P_L is injected into one band proportionally to the projection coefficient of the low-pass component onto the same band.

IV. SENSITIVITY TO ALIASING OF FUSION METHODS

An imaging system can be modeled as a continuous 2-D optical system followed by a sampler onto a finite grid of detectors and an analog-to-digital converter (ADC). The continuous optical system, whose PSF, accounting for the effects of platform motion and vibration and the finite sampling grid, integrates the at-sensor radiance before the (ideal) sampler and the ADC, is described by the MTF. Fig. 6 shows 1-D examples of MTFs having amplitude values equal to 0.1,0.2, and 0.3 at the Nyquist frequency (half the sampling frequency, of the MS scanner, assuming that the sampling frequency of P is four times greater). As it appears, the higher the amplitude at Nyquist, the larger the amount of signal contained in the passband, the greater the amount of aliasing originated by the folding of the tail of the spatial frequency spectrum (represented by the MTF of the spectral channel) across the Nyquist frequency.

Aliasing introduces a jagged appearance of oblique linear step edges and is particularly annoying in the interpolated versions of the MS images that are the starting point of fusion. Due to the linearity of the system, the (interpolated) aliased image can be regarded as the superposition of an aliasing-free image, represented, e.g., by any of the three Gaussian-like spectra in Fig. 6, plus a zero-mean aliasing pattern image, whose spatial frequency spectrum is the difference between the spectrum of the aliased image, having the tail folded across the Nyquist frequency, and the spectrum of the aliasing-free image, in which the tail is unfolded and spans beyond the Nyquist frequency.

Now, let us derive an extension to aliased MS images of the general equation for either CS- or MRA-based pansharp- ening, i.e.,

$$Mfc = Mfc + Gfc \bullet (5, k = 1, \ldots, N \quad (17)$$

in which S represent the details of the P image to be injected in the interpolated MS bands, and G_{fc} represents the band- dependent matrix that weighs the P details, through a point- to-point multiplication. Starting from (17), the schemes in Figs. 1 and 4 can be translated into simple equations describing how the two families work.

Let us consider M_{fc}, that is, the fcth band of the MS image interpolated at the spatial scale of the P image. As pointed out at the beginning of this section, the term M_{fc} is supposed to be generated by the superposition of an interpolated_aliasing-free image M£ and of an interpolated aliasing pattern A_{fc}. The general expression (17) of the fused fcth band, that is, M_{fc}, becomes

$$Mfc = Mfc + Gfc \bullet S = Mfc + Afc + Gfc \bullet S. \quad (18)$$

A. *CS-Based Methods*

For CS-based methods, (17) is changed into

the assumption that $G_{fc} \bullet JVmjAj = A_{fc}$, which is reasonable since interpolated aliasing patterns of spectrally correlated

bands are similar, and $G_{fc} \bullet {}^{w}i \sim 1$, which is exactly true for GIHS [25], as shown in [30], (21) becomes

$$M_k = Ml + G_k - (p -]Tm_{;}, \bullet Mjj = Ml \quad (22)$$

That is, the sharpened images produced from aliased MS bands (and aliasing free P) are identical to the products generated by the same algorithm starting from MS and P that are both aliasing free. This means that CS-based methods described by (1) are capable of exactly recovering aliasing impairments in the ideal case or, more realistically, to have a very low sensitivity to them.

B. MRA-Based Methods

In order to properly model the difference between ATW and GLP, let us reference Fig. 4. For MRA-based methods, (17) becomes

$$M_{fc} = M_{fc} + G_{fc} \bullet (P - P_L) = Ml + A_k + G_k \blacksquare (P - P_L) \quad (23)$$

where the term M_{fc} is supposed, as in (19), to be generated by the superposition of an interpolated aliasing-free image M£ and of an interpolated aliasing pattern A_k.

1) *ATW-Based Fusion: For ATW-based fusion, the low- resolution P version P_L is obtained by low-pass filtering, that is, $P_L = P \circledR h$, where h is the low-pass filter defining ATW, possibly equal to the MTF of the fcth spectral channel. Consequently, (23) is modified into*

$$M_{fc} = Mfc + A_{fc} + G_{fc} \bullet (P - P \circledR h). \quad (24)$$

Equation (24) can be rewritten as

$$Mfc = Mfc + Afc + Gfc \bullet (P — P (5) h) = Mfc + Afc \quad (25)$$

thus showing that the ATW fused image produced starting from aliased MS bands (and aliasing free P) contains the same aliasing pattern that appears in the interpolated MS image. Therefore, in this case, the aliasing pattern has not been compensated in the fusion process.

2) *GLP-Based Fusion: For GLP-based fusion, (23) becomes*

$$Mfc = Mfc + Afc + Gfc \bullet (P\text{-}expand,, ((P \circledR h) 4. r)) \quad (26)$$

in which expand,,(X) = X and is achieved as in Fig. 4 through upsampling by r and linear

convolution with a low-pass filter with 1/r frequency cutoff. The interpolation filter is totally unconstrained from the analysis filter h; this is one of the advantages of GLP compared with DWT.

Let us assume that the low-pass filter h is identical to the MTF of the fcth spectral channel, so that when its output is decimated by r, it would approximatively generate the same aliasing pattern as the one which has been produced by the MTF filter in the acquisition of the kth MS band. Then, the following relationship holds:

$$P - expand,, ((P \circledR h) 4- r) = P - P\pounds - A_P \quad (27)$$

in which P^ IP l, if the filter h exhibits a frequency response that is nonzero beyond one rth of the Nyquist frequency, as it generally happens with the MTF of the instrument. The term A_P represents the interpolated version of the aliasing pattern generated by decimation. The further assumption that $A_{fc} = Gfc \bullet A_P$, which is likely because G_{fc} rules the transformation of P details into MS details, yields

$$\begin{aligned} Mfc &= M\pounds + Afc + G_{fc}. \ (P - Pi - Ap) \\ &= M^{\wedge}, + Afc + Gfc \bullet (P - PJJ - Gfc \bullet A_P \\ &= Mfc + Gfc \bullet (P — PJJ . \end{aligned} \quad (28)$$

If the previous approximations hold, by comparing (28) with (25), it is apparent that the fusion products of the GLP method with MTF-matched reduction filter in the presence of aliased MS (and aliasing-free P) are identical to the products generated by the same algorithm starting from MS and P that are both aliasing free, because, in that case, the MTF-matched analysis filter of P would not generate aliasing patterns. It is noteworthy that the aliasing compensation is direct for CS-based (spectral) methods, because, in that case, the opposite aliasing patterns that are generated do not depend on P, but only on MS. In principle, spectral methods are capable of correcting aliasing also when P is not perfectly coregistered and even to correct both aliasing and misregistration at the same time. Conversely, the compensation is indirect for the MRA-GLP fusion, because it is made between patterns of original MS bands and of the low-pass-filtered and decimated P image. Thus, if MS and P are affected by residual misregistration, aliasing cancellation may not occur. This fact can be also space dependent or scene dependent, so that it is possible to remove the aliasing pattern in some areas and not in other ones. Consequently, the compensation of the GLP method is statistically less robust than that of CS-based methods.

C. *Results and Discussion*

Fusion simulations will be devoted to demonstrate, both visually and numerically, the theoretical results that have been obtained in Section IV-A and B. For this purpose, a test image acquired by IKONOS will be considered. Quality and distortion indexes will be calculated at the degraded scale, so that distortion/quality plots can be drawn as a function of the amount of aliasing. Simulated Pleiades and QuickBird data will be used for fusion simulation at the full spatial scale. In the former case, the availability of a high-resolution reference MS image allows several interesting considerations to be made on fusion products in the presence of aliasing.

In addition to simulations of a CS method, already reported in [6], in this study, GLP and ATW-based methods, both using the same MTF filters [47] and the same global injection gain [30], will be compared to show the advantages of GLP over ATW in the presence of aliasing of the MS bands. The advantage of considering degraded images is twofold. On one hand, different amounts of aliasing can be generated by tuning the passband of the low-pass filter preceding the downsampler. On the other hand, fusion simulations carried out on degraded data allow reference originals to be used for quality evaluation according to the synthesis property of Wald's protocol [3], [33],

The dotted vertical line marks the Nyquist frequency of MS, one fourth of the Nyquist frequency of P. As the amplitude at Nyquist increases, the signal in the passband increases, together with the tail in the stopband, which originates the aliasing after decimation (by four in this example).

In this case, a true reference being available, quality/distortion indexes can be used, namely, the average spectral angle mapper (SAM), measuring spectral distortion to originals of fusion products, the ERGAS index [33], measuring the average radio- metric distortion, and the Q4 index [52], jointly measuring the spectral and radiometric quality of fusion.

Numerical results will be presented in terms of quality/ distortion global score indexes (SAM, ERGAS, Q4) for increasing amounts of aliasing, measured by the amplitude at Nyquist frequency of the Gaussian-like low-pass filter simulating the average MTF of the individual spectral channels of the instrument. GLP and ATW-based methods, both using the same MTF filters [47] and the same global injection gain [30], will be compared to show the advantages of GLP over ATW in the presence of aliasing of the MS bands. The aforementioned two MRA-based methods will be compared also with a CS-based method, i.e., the GSA spectral sharpening [24],

Progressively increasing amounts of aliasing have been generated by applying Gaussian-shaped low-pass filters with moduli of frequency responses at cutoff Nyquist frequency increasing from 0.1 to 0.6 at steps of 0.1, before decimation is performed. The coefficients of the filters are reported in Table

I. The corresponding frequency responses are plotted in Fig. 7. Fig. 8 reports the values of the SAM, ERGAS, and Q4 indexes

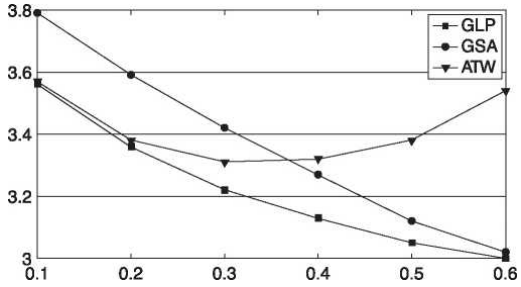
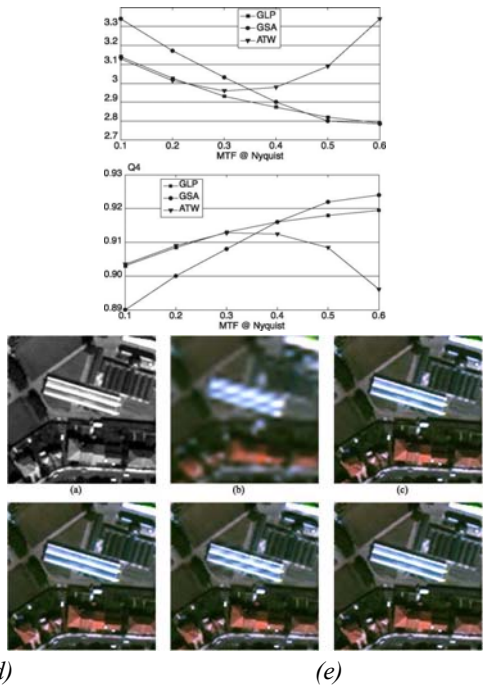


Fig. 8. Quality/distortion indexes measuring the sensitivity of the performances of the GSA, GLP, and ATW methods to an increasing amount of aliasing, obtained by changing the amplitude at the Nyquist frequency of the Gaussian-like low-pass filter simulating the MTFs of the MS instrument. The original IKONOS image is 512 x 512 (MS) and 2048 x 2048 (P) in size and was taken over the city of Toulouse, France, in 2001.

calculated between fusion products at 4 m, achieved from MS and P data spatially degraded by four along rows and columns, and original 4-m MS.

ERGAS



(d) *(e)*

Fig. 9. Details of simulated Pleiades data (256 x 256 at 0.7-m scale), original and fused, (a) Synthetic panchromatic (P = (G + R)/2). (b) 2.8-m MS bicubically interpolated at 0.7 m. (c) Original 0.7-m MS for reference, (d) GLP with MTF-matched reduction filter and 23-tap interpolator, (e) ATW transform with MTF-matched filter, (f) GSA spectral sharpening [24].

The MTF of an MS scanner generally stems from a tradeoff between amplitude in passband, that is, retained signal, and amplitude in stopband, that is, aliasing: the greater the amount of signal in the passband, the greater the amount of aliasing that occurs. Note that the original IKONOS data exhibit MTF values of spectral channels slightly lower than 0.3. Not surprisingly, all fusion methods benefit from aliasing up to a simulated MTF approximately equal to 0.3, because the quality reference features an amount of aliasing as it had been generated by the same MTF. After that value, GSA steadily follows the same trend, leading to better and better fusion performances, as otherwise found in [6]. Conversely, the two MRA-based methods, i.e., ATW and GLP, follow opposite trends, leading to poorer and poorer performances of ATW and better and better performances of GLP, as the amount of aliasing increases. Note that, in [6], it is proven that GSA and analogous CS-based methods remove aliasing, whereas ATW does not; the advantages of GLP, due to decimation followed by interpolation, have not been investigated.

The ideal case of simulated Pleiades data has the twofold advantage that the system MTF is exactly known, same as in simulations at degraded scale, and misalignments between MS and the P image synthesized from the same MS bands are identically zero. In practical cases of fusion at full scale, the MTF is known with approximations, because it is not strictly Gaussian as in the widely adopted model, it is nonseparable, because of cartographic projection (rotation and resampling) and differences in resolution along and across track, and it is difficult to estimate from the in-orbit data because of sampling. In fact, in aliasing-free sampling, the original signal that is reconstructed does not depend on rigid shifts of the sampling grid over the focal plane. Instead, the versions of the signal reconstructed from the sequences of aliased samples depend on how the radiance image is subpixel shifted over the sampling grid. As a consequence, in the full-scale presentation of results on a test QuickBird image of Trento, Italy (see Fig. 10), the aliasing mitigation capability of GLP is much less noticeable than in the tests in Fig. 9. Conversely, GSA thoroughly removes aliasing, thanks to its direct cancellation (21), (22), whereas the cancellation of GLP (28) is indirect, being achieved through P.

V. CONCLUSION

At the origin of pansharpening, the high-pass filtering technique, employing a simple boxcar filter, was the first example of a spatial fusion method. Later, pansharpening fusion was contextualized within the framework of MRA.

As a consequence, a

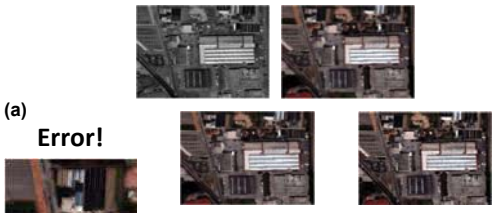


Fig. 10. Details ofQuickBird image data (512 x 512 at 0.7-m scale), original and fused, (a) Original panchromatic, (b) 2.8-mMS bicubically interpolated at 0.7 m. (c) GLP with MTF-matched reduction filter, (d) ATW transform with MTF-matched filter, (e) GSA spectral sharpening [24]

myriad of fusion schemes appeared in the literature. They were based on Mallat's DWT and its undecimated version (UDWT), on ATW transform and GLP, which can be regarded as the decimated version of ATW, and on nonseparable directional MRA, in which most notable are the curvelet, contourlet, and dualtree complex discrete wavelet transforms. In addition, hybrid schemes, in which a spectral transformation, such as linear/ nonlinear IHS or PCA, is coupled with any type of MRA, were introduced.

As a fundamental result of this paper, practically the totality of spatial and hybrid methods developed over the last 20 years may be achieved by means of a unique Gaussian-shaped low- pass filter, which can be parametrically optimized on the basis of the spatial response of the imaging system. The addition of a decimation stage followed by an interpolation stage accounts for all methods based on a critically or a noncritically decimated MRA, that is, DWT or GLP.

A unifying framework is introduced to describe fusion carried out through separable (DWT, UDWT, ATW, GLP) and nonseparable transforms. The undecimated/decimated schemes differ only by a cascade of a downsampler, followed by an interpolator in the latter. Notwithstanding that their flowcharts are formally identical, apart from the prototype low-pass filters, ATW/GLP allows a looser choice of the analysis filter and of the possible interpolation filter (only for decimated schemes), no longer subject to the constraints of a perfect reconstruction filter bank, as it happens with UDWT/DWT.

As a further result, in the case ATW/GLP, it is proven that GLP is slightly affected by intrinsic aliasing of the original MS data, due to the decimation of low-pass-filtered P, which generates opposite aliasing patterns in the details to be injected, with a consequent cancellation of the interpolated aliasing impairments. However, in practical cases involving geocoded images, i.e., rotated and resampled, approximate knowledge of the non-Gaussian and nonseparable MTF and possible local misalignments between MS and P may reduce the aliasing mitigation capability, with respect to the ideal case.

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Applications of ARM Processors in Industries

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Abstract—

In these days industrial automation plays a vital role in various fields such as power plants, weather monitoring, medicine storage, Signal processing etc. This paper describes applications of ARM processors in Industries. Arm based control can be implemented in two ways one is to sense the room temperature, pressure, humidity values at a time in the system and other method is for office premises in which user can login into his account at anywhere and anyplace and ensure all parameters at a single window. ARM 32 bit RISC CPU has features of image/object detection and video processing by using various features and classification algorithms for object detection. Image processing is a form of signal processing for which the input is an image, such as a photograph or video frame and the output of image processing may be either an image or a set of characteristics or parameters related to the image. The ARM based applications in medical field and image processing are discussed.

Keywords— ARM, Processor, medical, image processing

I. INTRODUCTION

In industries, systems are becoming very complex. Industries system needs to test the site equipments and environmental so it can track state of system in real time. This system requires design which has to be flexible and adaptable, for that microcontroller based systems can be used. This is more reliable and provides high performance to the system. Microcontroller is very practical and successfully utilized, the conventional 8 and 16-bit Microcontroller has its deficiencies when compared with 32-bit. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of micro programmed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being

executed, its successor is being decoded, and a third instruction is being fetched from memory

ARM based embedded system will be more functional, reliable, cost effective, less in size and low power consumption. Microcontroller has low speed and poor memory, so it can only execute simple control tasks.

This paper is organized as follows. Literature survey is in section II. Arm processor Architecture is explained in Section III. The applications in medical field and signal processing are explained in section IV. The conclusion is in section V.

II. LITERATURE SURVEY

Mehta Karankumar D., Mehta Shreya B., Raviya Kapil S. [1] This paper proposed to monitor and control multi sensors values. Here using various sensors to sense the environment and send the signal to raspberry pi. It has inbuilt ARM processor which process the data and send it to internet through LAN/ETHERNET and user can log into account and can check all parameters within single window by GUI and data base system. User can set a limit range parameters then it will give control signal to hardware and it will turn ON/OFF devices. This system design a user can remotely monitor the room temperature, humidity & pressure from anywhere which could save the human expenses. Renuka P.Gore [2] had focused to employ a system which uses ARM Processor through Amol A. Dharmapurikar,R.B. Waghmare [3] this paper is described on development of embedded web server based on Raspberry Pi for the communication in automation. By using GPRS technology for effective designing & implementing a system. In the world the system is easily accessible GSM from anytime and anywhere by using GPRS technology along. And multi sensors are to interface the system with microcontroller. By using GPRS technology we can accomplish speed transmission of large amount of data in very less time. Ajith Kumar P. Shetty,K. Ketan and M. Shanmugasundaram [4] this paper is deals for a remote data acquisition system which is controlled by Linux portable ARM processor and web server application with General Packet Radio Service (GPRS) technology. After the monitoring data is to collection accompanied by a Short Message Service (SMS), an email alert. This is initiated in order to avoid the occurrence of a critical event. Bhuvaneswari.S, Sahaya Anselin Nisha[5] this system describes by using Xbee to design the raspberry pi hardware. Here microcontroller to interfaced the some sensors. To measure the temperature values. Next, which values are transmitted to PC during SPI serial protocol. In values are uploaded in internet at receiver by using internet cable. In industry from any place all devices can monitor in web browser by typing IP address

III. ARM PROCESSOR OVERVIEW

ARM is the industry's leading supplier of microprocessor technology offering the widest range of microprocessor cores to address the performance, power and cost requirements for

almost all applications markets. Combining a vibrant eco system with over 1000 partner delivering silicon, development tools and software, and more than 50 billion processors sold , ARM truly is" the architecture for digital world". The figure.1 shows the overview of ARM Processor.

Fig. 1. An Overview of ARM ProcessorArm processor classified into following series-

- Cortex –A series
- Cortex –R series
- Cortex –M series
- Securcore

Cortex –A series: Cortex –A32, Cortex –A57, Cortex – A53, Cortex – A17, Cortex –A15, Cortex –A9, Cortex – A7, Cortex–A5.

Cortex-R series: *Cortex-R5, Cortex-R7, Cortex-R4 :*

Embedded Real-time processors are primarily focused on delivering highly deterministic real-time behavior in a wide range of power sensitive applications. These processors often execute a Real-Time Operating System (RTOS) alongside user-developed application code requiring only a Memory Protection Unit (MPU) as opposed to the MMU available in the Application Processors.

Cortex-M series: Cortex-M processors are the optimal solution for low-power embedded computing applications. The 32-bit Cortex-M processor family is the key to transforming all sorts of embedded systems into smart and connected systems. Often provided as a "black box" with pre-loaded applications, they have limited capability to expand hardware functionality and in most case no screen. Applications for this class of processors include: Merchant MCUs, Automotive Control Systems and Motor Control Systems and White Goods controllers, Smart Meters, Sensors and Internet of Things. The Cortex-M processor series has been designed to deliver industry-leading deterministic behaviour, lowest sleep and dynamic power, and smallest area possible while maintaining high processing efficiency. The series comprises of Cortex-M0+ processor for ultra-low-power performance, the low power Cortex-M0, the general purpose Cortex-M3 processor, and Cortex-M4 and Cortex-M7

processors for digital Signal control applications.

SECURCORE processor: *SC000, SC100, SC300:* ARM SecurCore processor applications include: SIMs, Smart Cards, Advanced Payment Systems, Electronic Passports, Electronic Ticketing and Transportation. A number of SecurCore processors are available enabling Partners to choose the solution that fits the specific criteria of their application based on desired performance, die area, size, dynamic and static power, and other considerations. The SC000 processor is based on the ultra-low-power Cortex-M0 processor. The SC100 processor is based on the popular ARM7TDMI® processor. The S C300 is based on the modern Cortex-M3 processor, making it ideal for interrupt driven and power sensitive applications.

IV. APPLICATIONS

A. Medical Field

With the tremendous growth in medical technology, there is cure for many dreadful diseases through the intake of several new medicines. The number of medicines to be taken by each person has increased. It has become hard for us to remind ourselves to take the medicines at particular time. This Smart Medicine Box helps us in reminding us of the medicine that we should take at that particular time.

Components used in Smart Medicine Box

ARM7 LPC2148 Micro controller: The ARM LPC2148 is a 32-bit microcontroller with real-time emulation and embedded trace support, that combines it with embedded high speed flash memory ranging from 32 kB to 512 kB. A 128-bit wide memory interface and unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty. Due to their tiny size and low power consumption, LPC2148 are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. Serial communications interfaces ranging from a USB 2.0 Full-speed device, multiple UARTs, SPI, SSP to I2C-bus and on-chip SRAM of 8 kB up to 40 kB, make these devices very well suited for communication gateways and protocolconverters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-

bit ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers suitable for industrial control and medical systems. It also includes an in-built Real Time Clock (RTC) which plays the key role in our present application.

1) Keys: Keys are used for the user or nurse to enter the information of time when the smart box would send

"reminder" (displaying numbers and playing synthesized voice). It is also used for the user to enter a number to command a specific pill box to open on a specific time. (say, open No.1 pill box), and user can also enter the frequency information to take pills for each day. Keys contain four buttons. Alarm, enter, increment, decrement.

2) Liquid Crystal Display (LCD)*:* The 2 line, 16 characters LCD screen is used to display the instruction information, that the pills need to be

taken now, and the current time and date.

3) Speaker Module: The speaker module is used to play the synthesized sound to remind the user to take pill.

4) Pill boxes: We used a pillbox system containing 3 separate small pillboxes. Each box has an led display placed on the box. For our pill system, the user can store up to three different types of pills, which can be stored in those three small separate boxes. He or she can also specify the different combinations of pill boxes to be open for each day. Microcontroller: ARM LPC2148 is used to execute all the commands mentioned above.

249. ***Real time clock in ARM7:*** ARM LPC2148 has an Real Time Clock Built into it. The real time clock running in our system is implemented by using MCU 16-bits timer to generate 1-second base. Firstly, we will open the compare match interrupt service routine, and set the compare value to Also, we scale the running frequency of timer1 to 1/64. Then, the interval time between each interrupt routine is 0.001 second. We have a volatile variable to run the clock function every 1000 interrupt routines. Then, in the clock function, it will run like a clock. We have separated variable for two digits of seconds, minutes and one variable for hours. We do not store the year information because we think it is unnecessary.

Working

As we switch on our device, the current time and date that is stored in the RTC is displayed on LCD. The device initially asks the user to set the alarm timings using the keys. A speaker module is connected to the ARM7 microcontroller. The playback voice should be initially recorded in it through the microphone in it. The alarm time is compared to the current time by the microcontroller and when they match, an interrupt is generated. Then the LED on the pillbox glows and a voice play back is also generated indicating which pill should be taken.

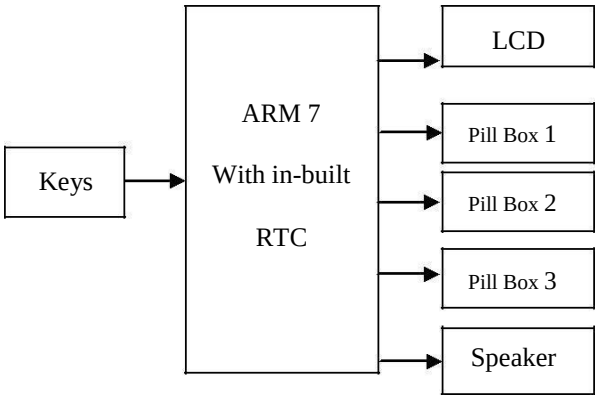

Fig. 2. Block Diagram of Smart Medicine Box

B. Image Processing

An image is defined in the ―real world‖ is considered to be a function of two real variables, for example, a(x,y) with a as the amplitude (e.g. brightness) of the image at the real coordinate position (x,y). Modern digital technology has made it possible to manipulate multi-dimensional signals with systems that range from simple digital circuits to advanced parallel computers. The goal of this manipulation can be divided into three categories:

- Image processing (image in -> image out)
- Image Analysis (image in > measurements out)
- Image Understanding (image in > high-level description out)

1) Object Detection

The process of image object detection deals with determining whether an object of interest is present in an image/ video frame or not. An

image will subsequently search to find possible objects of interest. This search is done by extracting smaller regions from the frame, called search windows, of m x n pixels (m can be equal to n), which go through some form of preprocessing (histogram equalization, feature extraction), and are then processed by a classification algorithm to determine if they contain an object of interest or not. However, the object of interest may have a larger size than that of the search window, and given that the classification algorithm is trained for a specific search window size, the object detection system must have a mechanism to handle larger objects.

To account for this, an object detection system can increase the size of the search window and rescan the image, which implies that different classifiers are used for each window size. Alternatively, the size of the input image can be decreased (downscaling); consequently, the size of the object of interest will be reduced so it can be enclosed within the search window. All subsequent downscaled versions of the input image, are therefore reexamined using the same search window size. The downscaling process is often preferred as it is computationally less expensive [42]. Downscaling is done in steps to account for various object sizes, down to the size of the search window. Hence, many downscaled images are produced from a single input image/video frame, each in turn producing a number of search windows, which increases the amount of data that must be processed by the classification algorithm. Search windows are extracted every few pixels, and the number of pixels that are skipped is called the window overlap.

2) Haar Object Detection

Haar-like features are digital image features used in object recognition. They owe their name to their intuitive similarity with Haar wavelets and were used in the first real-time face detector. Historically, working with only image intensities (i.e., the RGB pixel values at each and every pixel of image) made the task of feature calculation computationally expensive. A publication by Papageorgiou et al. discussed working with an alternate feature set based on Haar wavelets instead of the usual image intensities. Viola and Jones adapted the idea of using Haar wavelets and developed the so-called Haar-like features. A Haar-like feature considers adjacent rectangular regions at a specific location in a detection window, sums up the pixel intensities in each region and calculates the difference between these sums. This difference is then used to categorize subsections of an image. For example, let us say we have an image database with human faces. It is a common observation that among all faces the region of the eyes is darker than the region of the cheeks. Therefore a common haar feature for face detection is a set of two adjacent rectangles that lie above the eye and the cheek region. The

position of these rectangles is defined relative to a detection window that acts like a bounding box to the target object (the face in this case).

In the detection phase of the Viola–Jones object detection framework, a window of the target size is moved over the in- put image, and for each subsection of the image the Haar-like feature is calculated. This difference is then compared to a learned threshold that separates non-objects from objects. Because such a Haar-like feature is only a weak learner or classifier (its detection quality is slightly better than random guessing) a large number of Haar-like features are necessary to describe an object with sufficient accuracy. In the Viola Jones object detection framework, the Haar-like features are therefore organized in something called a classifier cascade to form a strong learner or classifier. The key advantage of a Haar-like feature over most other features is its calculation speed. Due to the use of integral images, a Haar-like feature of any size can be calculated in constant time (approximately 60 microprocessor instructions for a 2-rectangle feature).

3) Rectangular Haar-like features

A simple rectangular Haar-like feature can be defined as

the difference of the sum of pixels of areas inside the rectangle, which can be at any position and scale within the original image. This modified feature set is called 2-rectangle feature. Viola and Jones also defined 3-rectanglefeatures and 4-rectangle features. The values indicate certain characteristics of a particular area of the

image. Each feature type can indicate the existence (orabsence) of certain characteristics in the image, such as edges or changes in texture. For example, a 2-rectangle feature can indicate where the border lies between a dark

region and a light region.

V. CONCLUSION

In this paper, we discussed about the applications based on ARM processors which are today's requirement of industries.Mainly we have focused on ARM processor based application which are related medical and image processing fields and is very necessary in development of technology. Since the embedded system is able to deal with Multi-Tasks and can run operation systems, field operations, supervisions and managements. The applications systems , which are very much useful for industry automation and image processing based security systems can be designed using ARM processors with low cost.

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Low Power Fault Tolerant ALU

F. Begum and N. Raj

***Abstract*— Parity-preserving reversible gates, when used with an arbitrary synthesis strategy for reversible logic circuits, allow any fault that affects no more than a single logic signal to be detectable at the circuit's primary outputs. Fault tolerance can be achieved in a system by using parity bits. The main aim of this paper is study of fault tolerant ALU design based on parity preserving reversible logic gates with improved quantum cost and power overhead as compare to existing fault tolerance based ALU designs. Making a reversible circuit robust or fault tolerant is much more difficult than a conventional logic circuit. Fault Tolerant reversible logic is one class of reversible logic that maintains the parity of the input and the outputs.**

***Index Terms*— ALU, Parity, Fault tolerant, Quantum Cost, Reversible**

I. Introduction

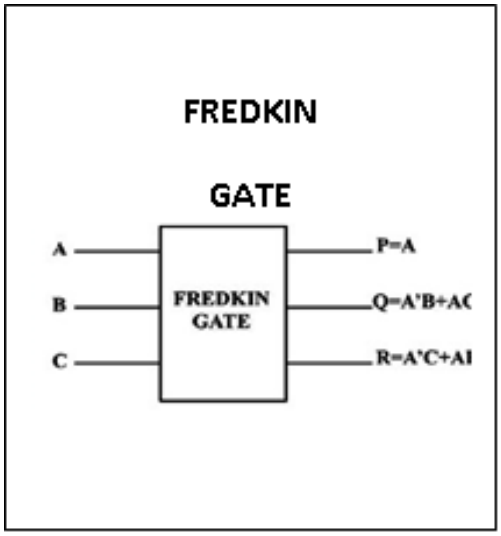
A parity preserving gate is the one in which the parity of the input and the output vectors is the same. Parity checking is one of the methods for error detection in digital logic system. In parity preserving reversible circuit, parity preserving reversible logic gates are used in which parity if input vector must match parity of output vector. A reversible circuit will be parity preserving if its individual gate is parity preserving. As parity preserving reversible logic gates used between fault side and output are information lossless. Hence an error at fault side will be immediately seen at output.

Parity preserving reversible gates allows detecting such faults at output which won't affect more than a single logical signal. Conservative logic gates exhibit property that there are equal numbers of 1's in output as there are in input. Every conservative gate is parity preserving but every parity preserving gate is not conservative. Classical gates like two input AND, OR, NAND, NOR, XOR and XNOR are irreversible as we can't uniquely reconstruct input states from output states. Here two-bit input state is mapped to one-bit output state leads to the erasure of one bit and consequently loss of energy. We can avoid this energy loss by mapping n bit input states to n bit output states so that input states can be uniquely recovered from output states and under such circumstances, a gate is said to be reversible. The number of inputs in a reversible logic circuit should be equal to number of outputs and fan out is not allowed. Parity checking is one of the oldest, as well as one of the most widely used, methods for error detection in digital systems. Its most common use is for detecting errors in the storage or transmission of information, primarily because most arithmetic and other processing functions do not preserve the parity of the data.

Making a reversible circuit fault-tolerant is much more difficult than classical circuit, since reversible logic allows no feedback or fan-out. A reversible logic gate will be parity preserving if the EXOR of the inputs matches the EX-OR of the outputs i.e., the parity of the input and the output remains the same. If I1, I2, …, IN and O1, O2,…, ON are the inputs and outputs of an NxN reversible logic gate, it will be parity preserving if they satisfy I1 EXOR I2 EXOR .....EXOR IN=O1 EXOR O2 ..EXOR ON.

II. Literature Review

Some of the parity preserving reversible logic gates that are useful in the discussion are the NFT gate proposed in ,Islam Gate (IG) , Double Feynman Gate,F2PG, and PPPG.Also the Fredkin gate is a parity preserving reversible logic gate. All the mentioned gates have been shown in Figure 1.



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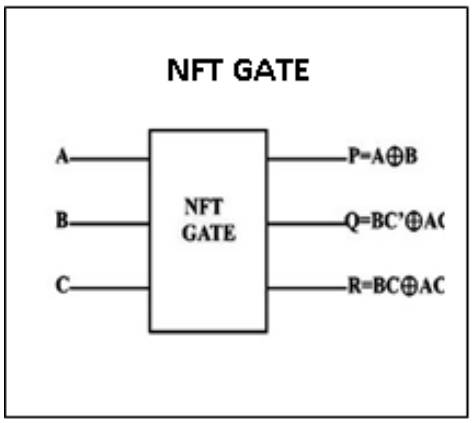

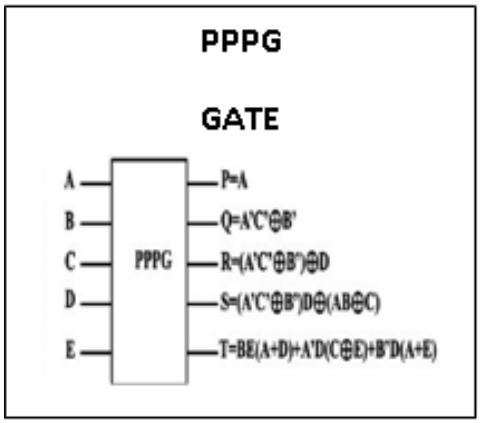

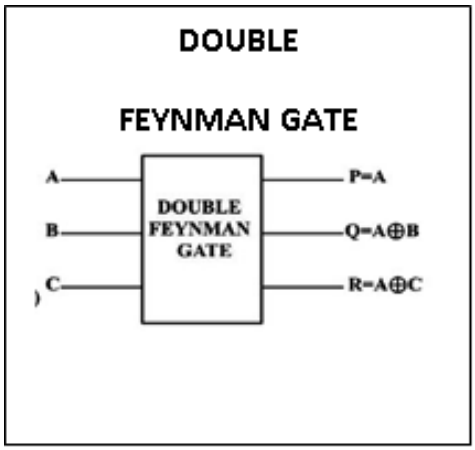

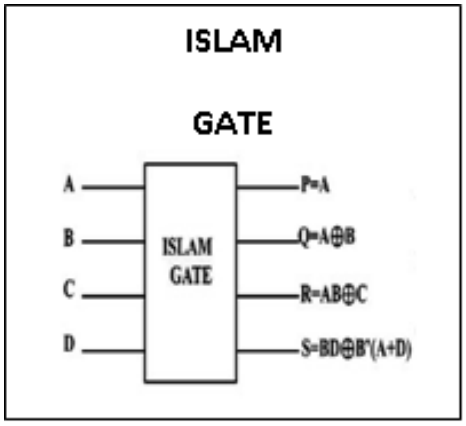

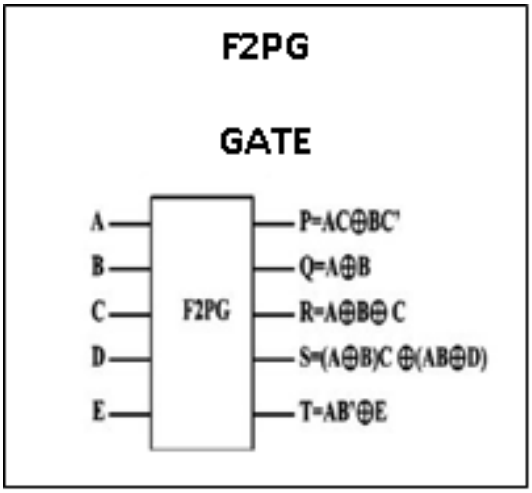

Figure 1. Parity Preserving Reversible Logic Gates

III. RELATED WORK

A. Arithmetic Logical Unit

ALU is a data processing unit, which is an important part in CPU. Different kinds of computers have different ALUs. In logical operations, there are NOT, OR, AND, XOR, etc. while in arithmetic operations there are addition, subtraction, etc. After a detailed analysis of the various designs of ALU, It has been concluded that each ALU could be divided on following two parameters based on their design.

1. Dedicated Design
2. Control Unit with Adder

In the similar fashion these ALUs are also divided into further two categories, named as:.

1. Single line output
2. Multi line output

B. Existing ALU Designs.

Existing ALU designs with their proposed methodologies are given below:

Design1. Matthew et al.proposed a novel 5*5 reversible logic gate popular as MG i.e. Morrison gate that is used in designing of a novel reversible ALU along with HNG gate . Reversible ALU designed with MG and HNG gates performs arithmetic operations such as addition and subtraction and logical operations as AND, OR, NAND, NOR, XOR, and buffer. After that, the comparison heading towards the flowing factors such as the ripple-carry, carry-select, logged stone carry-ahead adders is being observed.

Design 2 and Design3.Syamala and Tilak reversible one-bit ALU.have proposed two approaches of ALU design i.e. control structure based reversible one-bit ALU and multiplexer based

Design 4. Zhijin et al.proposed ALU design which consists of two main parts i.e. reversible function generator as control unit

and reversible mode selection unit. These two parts are cascaded by combinations of Toffoli and NOT gates.

Design 5. Ravi et al.dscussed realization of with the help of a carry save adder block which are not based on propagation of carry bits. This approach results in improved of 20% and 17% regarding the gatel count and quantum cost respectively, whie comparing with earlier works in reversible ALU designs. This design has a dedicated unit for the logical and the arithmetic operations, which is a combination of Carry save adder, Fredkin, Toffoli and CNOT reversible logic gates. But having the multiple outputs, to make this ALU functional more gates need to be added so that it can be implemented logically.

IV. COMPARISON

The different designs are compared based on the quantum cost; the number of gates, divide and conquer approach, types of gate used, garbage outputs and fault tolerance property. Design 5 consists of least number of gates, produces less garbage outputs and quantum cost obtained is also very less as compare to Design 1. The main limitation of circuit is absence of divide and conquers approach and fault tolerance property. Design 4 performs highest number of arithmetic and logical operations yet suffers from high quantum cost and absence of fault tolerance property. Design 3 performs very few arithmetic and logical operations yet quantum cost is comparatively high.

Table 1.Power Consumption Comparison of Various ALU Design.

Power consumption(mw) Parameter	Design 1	Design 2	Design 3	Design 4	Design 5
Logics	0.19	0.02	0.01	0.16	0.06
Signals	0.47	0.07	0.04	0.36	0.18
IOS	34.36	6.95	4.67	57.99	28.49
Total	35.01	7.04	4.72	58.22	28.73

Table 2. Optimization Metrics Comparison of Various ALU Design.

ALU DESIGNS/papers	Design1	Design 2	Design3	Design 4	Design5
No. of Gates	8	9	9	14	5
Quantum cost	35	41	34	55	24
Arithmetic & Logic operations	9	5	4	29	8
Types of Gates used	HNG, MG, Feynman, Fredkin	Feynman, Fredkin, Toffoli	Feynman, Fredkin, Peres	CNOT, Toffoli	CSA,Toffoli,Fredkin CNOT
Garbage outputs	6	6	9	8	3
Fault tolerance	No	No	No	No	No
N bit ALU(Divide and Conquer approach)	Not Possible	Not Possible	Not possible	Possible	Not Possible

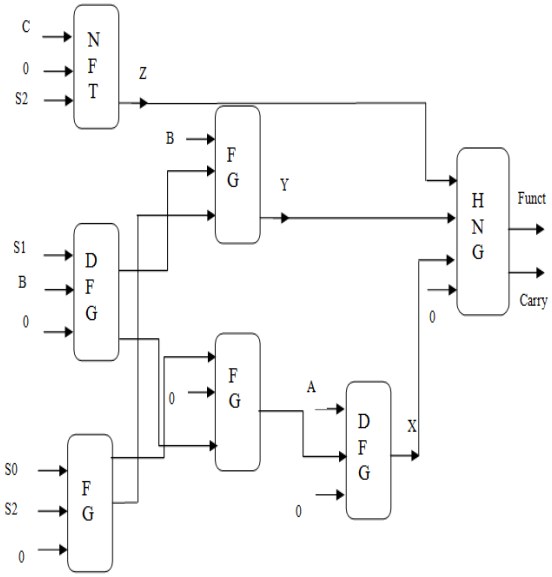

Fig. 2. Block diagram of fault tolerant ALU

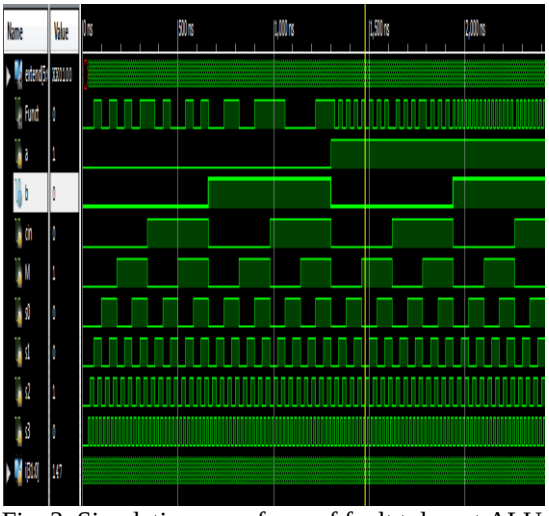

Fig. 3. Simulation waveform of fault tolerant ALU

V. CONCLUSION

Fault tolerance approach using parity preserving gates in combination with other methods will prove to be advantageous for ultra low power robust integrated circuit demanded by many industrial and commercial applications. ALU is the most prominent component of any computing system. Thus designing of ALU needs thorough optimization in terms of its gate design and architecture complexity. One major factor that needs to be catered in designing any ALU is that it must be made resistant to faults. Also since ALU has to continually perform during the working of any processor, the power dissipation factor plays a major role and should be taken into account.

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DESIGN OF AN AREA- EFFICIENT MILLION- BIT INTEGER MULTIPLIER

Proceedings of International Conference on Latest Trends in Electronics and Communication - ISBN 978-93-85100-14-7

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Abstract- **The project explains a double modulus NTT method to enlarge the digit size of NTT and introduced hybrid NTT approach to eliminate the reorder operations is proposed. Here, each NTT point is processed simultaneously under two moduli, and the final result is accumulated. In existing system double modules is not used and the sample size is 24 bits which degrades the efficiency of the proposed system. The employment of double modulus enlarges the permitted NTT sample size from 24 to 32 bits and thus improves the transform efficiency. Based on the proposed double modulus method, a design of million-bit integer multiplier with the Schönhage–Strassen algorithm is accomplished, which is more area-efficient. Xilinx software is used for this implementation.**

Index Terms- **Million bit integer multiplier, Number theorectical transform(NTT), Two modulus.**

1. INTRODUCTION

Gentry–Halevi FHE schemes and integer–based FHE schemes, large integer multiplication is the most computationally intensive operation. The high timing and area cost of large integer multiplier has been a major restrictive factor in the feasibility of such FHE schemes. To the best of our knowledge, Wang *et al.* [5] first implemented million-bit multiplication for FHE on graphics processing unit platform. Döroz *et al.* [6] then realized a million-bit multiplier in custom hardware employing fast fourier transform (FFT) based recursive multiplication algorithm. After that, Wang and Huang [7] proposed an architecture design of a 768k-bit multiplier on the Stratix-V FPGA based on 4k-point and 16-point combined FFT blocks. Cao *et al.* [8] proposed a supersize integer-FFT multiplication architecture with different choices of number theoretical transform (NTT) modulus. Wang [9] proposed a VLSI design of a 768k-bit integer-FFTmultiplier based on a memory in-place architecture. Most of the previous works focus on reducing the multiplication time but give little consideration to the area efficiency. Area efficiency is also quite important, because high area cost gatecount ASIC platform, both of which are too costly for practical applications. The objective of this brief is to design a fast million-bit integer multiplierwithout compromising its area efficiency. We use the Schönhage–Strassen algorithm and NTT for better efficiency.Our contributions are as follows: we propose a double modulus NTT method to enlarge the permitted word size of NTT from 24 to 32 bits; a hybrid NTT approach is introduced to eliminate the reorder operations in hardware NTT; and the VLSI architecture of an area-efficient million-bit integer multiplier is designed and verified on Altera Stratix-V FPGA. The rest of this brief is organized as follows. Section II gives an introduction to Schönhage–Strassen multiplication algorithm and NTT. Section III presents our proposed multiplication architecture based on the double modulus method and hybrid NTT approach. Section IV shows the VLSI architecture of our proposed design. The implementation results and comparisons are given in Section V. Conclusions follow in Section VI.

2. SCHONHAGE-STRASSEN MULTIPLICATION ALGORITHM

General Gentry–Halevi scheme requires multiplication of operands with a maximum word length used . Traditional multiplication methods, such as grammar school method Karatsuba–Ofman method, and Toom–Cook method become inefficient. Proposed algorithm is used large integer multiplication The complexities are given below.

TABLE 1:

Algorithm	**Complexity**
Grammar-school	$O(N^2)$
Karatsuba-ofman	$O(N^{\ln 3/\ln 2})$
Toom-cook	$O(N^{\ln(2k-1/\ln(k)})$
Schonhage- Strassen	O(NlogNloglogN)

Algorithm the complexity of multiplying two integers with *N* digits is O(NlogNloglogN). Table I lists the complexities of different multiplication algorithms when multiplying two *N* digits integers. When *N* is quite large, Schönhage–Strassen algorithm with a complexity of O(NlogNloglogN) outperforms its best competitor Toom–Cook method, which has a complexity of $O(N^{\ln(2k-1)/\ln(k)})$.

ALGORITHM- 1 :

- Adding zero padding in the inputs.
  - A[i] = 0
  - B[i] = 0
- Compute number theoretical transform of inputs.
- Compute the digit wise multiplication of NTT(A) and NTT(B).
- C′[i] = NTT(A)[i] . NTT(B)[i].
- Compute the inverse NTT of C: C INTT(C′).
- Final output.

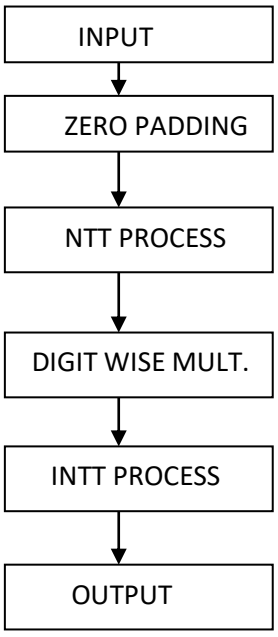

FIG 1 : Flowchat of Schonhage- Strassen Algorithm

NUMBER THEORETICAL TRANSFORM

The NTT used in the Schönhage–Strassen algorithm is a special kind of discrete Fourier transform (DFT) defined over a finite field Zp = Z/pZ.

Let ω be a primitive nth root of unity in Zp. **a** = (a0, a1, . . . , an−1) be a vector of degree n, where coefficient ai ∈ Zp, i = 0, 1, . . . , n −1.

The n-point NTT of vector **a** (by $NTT^{\omega}{}_{\omega}(\mathbf{a})$) is defined as

$$Ai = NTT^{n}{}_{\omega}(\mathbf{a})i = \sum_{J=0}^{n-1} a_j \omega^{ij} \bmod p$$

The n-point inverse number theoretical transform (INTT) of vector **A** (denoted by $INTT^{n}{}_{\omega}(\mathbf{A})$) is defined as

$$INTT^{n}{}_{\omega}(\mathbf{A})i = n^{-1} * \sum_{J=0}^{n-1} a_j \omega^{-ij} \bmod p.$$

3. PROPOSED MULTIPLICATION ARCHITECTURE USING DOUBLE MODULUS

A.PROPOSED ARCHITECTURE

In common one modulus NTT, in order to prevent digitwise overflows during the intermediary computations of NTT, the digit size b and digit number N should be restricted by the modulus P. Commonly, modulus p is a 64-bit prime number, b is chosen as 24 bits. Then, N can be chosen as either 2^{16} to achieve 768k-bit multiplication or 3×2^{15} to achieve 1152k-bit multiplication, as work [6] and [9] did, respectively

$$N/2\ (2^{b} - 1)^{2} < p.$$

The proposed double modulus NTT method, the permitted word length is enlarged from 24 to 32 bits. As a result, compared with work [9], we achieve a 33% larger multiplication size at the same number of digit samples *N*. Compared with work [6],we achieve a 10% smaller multiplication size at a 33% reduced digit number *N*, which means less clock cycles are needed.

B. HYBRID NTT APPROACH

Since NTT is a kind of DFT over finite field, FFT algorithms,which are originally used to accelerate DFT also works for NTT. Generally, there are two major sorts of FFT algorithms, NTT algorithm and INTT algorithm.

ALGORITHM 2 : NTT ALGORITHM

Let ω be a primitive n-th root of unity in Zp. **a** = (a0, a1, . . . , an − 1) be the coefficient vector of degree n, where, ai ∈ Zp, i =0, 1, . . . , n − 1.

Input: a,ω, n, p

Output: A = $NTT^{n}{}_{\omega}(a)$.

1: **A**← **a**

2: **for** m = log2^n − 1 **to**0 **do**
3: **for** j = 0 **to**2^m − 1 **do**
4: t ← $\omega^{jn/2m+1}$
5: **for** i = 0 **to**$n/2^{m+1}$ − 1 **do**
6: k ←i × 2^{m+1} + j
7: (Ak, Ak+2^m) ←(Ak + Ak+2^m , t (Ak − Ak+2^m))
8: **end for**
9: **end for**
10: **end for**
11: **A**←scramble(**A**);
12.return A.

ALGORITHM 3 : INTT ALGORITHM

Let ω be a primitive n-th root of unity in Zp. **a** = (a0, a1, . . . , an − 1) be the coefficient vector of degree n, where ai ∈ Zp, i =0, 1, . . . , n − 1.

Input: a,ω, n, p

Output: A = NT T^n_ω (**a**).

1: **A**← scramble(**a**)
2: **for** m = 0 **to**log2^n − 1 **do**
3: **for** j = 0 **to**2^m − 1 **do**
4: t ← ω$jn/2^{m+1}$
5: **for** i = 0 **to**$n/2^{m+1}$ − 1 **do**
6: k ←i × 2^{m+}1 + j
7: (Ak, Ak+2^m)← (Ak + t Ak+2^m , Ak − t Ak+2^m)
8: **end for**
9: **end for**
10: **end for**
11: **return A.**

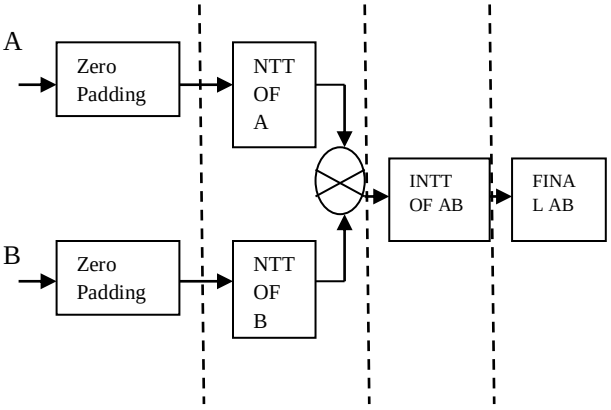

FIG 2 : Proposed multiplication Architecture

Since the scramble function is operation of order two, which means*scramble(scramble(**a**)) = **a**,* ∀ ***a*** ∈ Z*np*. In our proposed work, we use DIF algorithm for forward NTT and DIT algorithm for inverse NTT. Then, reorder operation in state 11 of Algorithm 3 and state 1of Algorithm 2 can be omitted. To the best of our knowledge, this DIF-DIT hybrid approach has been mentioned in as an approach to accelerate FFT. This isthe first time the approach is introduced to accelerate NTT in large integer multiplication.

C.PROPOSED MULTIPICATION

Based on the proposed double modulus NTT method in Section III-A and the hybrid NTT approach in Section III-B, we design a multiplication architecture as Fig. 1 shows. In this architecture, large integer multiplication is achieved through five procedures, which can be presented as follows.

1) Padding and Modulo Procedure: two input multiplicands A and B are zero-padded into N-digit vectors.
2) NTT Procedure: NTT is performed over GF(p1) and GF(p2)simultaneously employing the NTT algorithm.
3) Digitwise Multiplication Procedure: digitwise multiplication is applied on the NTT results over both prime fields.
4) INTT Procedure: inverse NTT is performed over GF(p1) andGF(p2) employing the INTT algorithm.
5) Final Accumulation Procedure: the inverse NTT results over GF(p1) and GF(p2) are Merged. The final multiplication result is obtained by accumulation.

4.VLSI DESIGN

Based on the architecture proposed in Section III-C, we accomplish a VLSI design as Fig. 2 shows. In our design, NTT and INTT in integer multiplication are two-stage pipelined to achieve double the throughput.In the first stage of our design, two 1024k bits integers *A* and *B*are split into 64k pieces of 32-bit words (the first 32k pieces arepadding zeros). Each word of *A* and *B* modulo *p*2 = 216 + 1is computed and the 17-bit result together with the original word(modulo *p*1) are input into two 81×216 bits RAMs: NTT_RAM_Aand NTT_RAM_B, respectively. Then, two pipeline double modulusNTT units are employed to calculated NTT*(A)* and NTT*(B)*. The NTT results are put back into NTT_RAM_A and NTT_RAM_B.In the second stage, the digitwise multiplication resultsof *C*_[*i*] =NTT*(A)*[*i*] ∗ NTT*(B)*[*i*] are calculated and the

results are stored in a 81 × 216 bits RAM (INTT_RAM_C). One pipelinedouble modulus INTT unit is employed to calculated INTT*(C_)* and the results are put back into INTT_RAM_C. Finally, the INTT results are input to a pipeline CRT-accumulation unit to obtain the final multiplication result. Both the NTT stage and INTT stage share the same lookup table: one dual port 81 × 216 bits block ROM (Omegan ROM) to obtain $t \leftarrow \omega \pm jn/2m+1$ in Algorithms 2 and 3.

Also, the two stages share the same state controller. Noticed that the state controller and all the memory interfaces use a clock, which is twice as fast as the clock of the pipeline data path to match the data rate requirement.

5. IMPLEMENTATIONS RESULT COMPARISON

we also synthesis our design on TSMC 90-nm technology and compare our design with work [6]. Work [6] implements a 1152k multiplier employing the same two-point NTT engine as our design. Compared with [6], our design achieves a significant reduction on computing time due to the use of double modulus method. The gatecount is also cut down, because our pipeline memory architecture is less costly than the cache architectureof [6]. In total, the ATP of our design is 55.9 ms × Mgates, which is 70% reduced compared with 206.6 ms × Mgates of work [6].

TABLE : 2

PERFORMANCE	AREA PRODUCT TIME	TIME
EXISTING SYSTEM	206.6msx Mgates	7.74ms
PROPOSED SYSTEM	55.9msx Mgates	2.42ms

6. CONCLUSION

A double modulus number theoretical transform (NTT) method for million-bit integer multiplication is used. In our method, each NTT point is processed simultaneously under two moduli and the final result is generated. The employment of double modulus enlarges the permitted NTT sample size from 24 to 32 bits and thus improves the transform efficiency. Based on the double modulus method, a design of million-bit integer multiplier with the Schönhage–Strassen algorithm is accomplished, which is more area-efficient and reduce the gate levels when compared with the current competitors.

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Application of Raspberry-Pi Environment Monitoring System

V. Swarnalatha, N. Raj and P. John Paul

***Abstract*— The development in embedded system has proved to a reliable solution in monitoring and controlling the environment monitoring system. The project aims at building a system which can be used on universally at any scale to monitor the parameters in a given environment. With the evolution of miniaturized sensor devices coupled with wireless technologies it is possible to remotely monitor the parameters such as temperature, humidity, amount ofco2 in air and many more .We will be using raspberry-pi as our main board and sensors will collect all the real time data from environment and this real time data will be fetched by the web server and display it. User can access this data from anywhere through Internet. Due to unnatural and unpredictable weather farmers now a day face large financial losses due to wrong prediction of weather and incorrect irrigation methods and the amount of pesticides and insecticides used for crops. This system will prove to bean important part in development in agricultural field.**

***Index Terms*— Raspberry-Pi, Sensors, Web server, Weather.**

I. INTRODUCTION

The development in wireless sensor networks can be used in monitoring and con- trolling various parameters in the agriculture field, weather station field. Due to uneven and natural distribution of rain water it is very difficult for farmers to monitor and control the distribution of water to agriculture field in the whole farm or as per the requirement of the crop. There is no ideal and advanced irrigation method for all weather conditions, soil structure and variety of crops cultures. Farmers suffer large financial losses because of wrong prediction of weather and incorrect irrigation methods and the amount of pesticides and insecticides used for crops. In this context, with evolution of miniaturized sensor devices coupled with wireless technologies, it is possible remotely monitor parameters such as temperature and humidity and sun light intensity. Weather monitoring plays an important role in human life, so the collection of information about the temporal dynamics of weather.

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II. INTERNET OF THINGS (IOT)

Internet of Things (IoTs): The Internet of Things (IoTs) can be described as connecting everyday objects like smart-phones, Internet TVs, sensors and actuators to the Internet where the devices are intelligently linked together enabling new forms of communication between things and people, and between things themselves. Building IoTs has advanced significantly in the last couple of years since it has added a new dimension to the world of information and communication technologies. It is expected that the number of devices connected to the Internet will accumulate from 100.4 million in 2011 to 2.1 billion by the year 2021, growing at a rate of 36% per year. In the year 2011, 80% machine to machine (M2M) connections were made over mobile networks such as 2G and 3G and it is predicted that by 2021, this ratio will increase to 93% since the cost related with M2M over mobile networks are generally cheaper than fixed networks. Now anyone, from anytime and anywhere can have connectivity for anything and it is expected that these connections will extend and create an entirely advanced dynamic network of IoTs. The development of the Internet of Things will revolutionize a number of sectors, from automation, transportation, energy, healthcare, financial services to nanotechnology. IoTs technology can also be applied to create a new concept and wide development space for smart homes to provide intelligence, comfort and to improve the quality of life.

A. Motivation

The Motivation of Project is in recent developments in wireless and micro sensor technologies have provided foundation platforms for considering the development of effective modular systems. They offer the prospect of and secure medium of networking. The WSN is built using a coordinator node and several sensor nodes, a workstation and a database. Raw sensor data is collected from multiple nodes.flexibility in use, and network scalability. The Raspberry Pi has proved to be ideal as the core of such a system.

III. SYSTEM DESIGN

Event basis, which means that whenever there is a sudden change in the environment, the sensor data is sent. However, the sensors are always listening, i.e. they wait for changes in environment and report only once a drastic change is detected. These sensors are user-denied and act based on requirement.

The Sensors used are barometric pressure, ambient

temperature, humidity, wind direction, wind speed, and rainfall sensors. Once data from all the nodes are collected, this information is transmitted to a local base station (ATmega 128) through multi-hop transmission. This data is stored in an embedded database SQLite3 and displayed on a web-page using TCP/IP. Ye and Wang extend the WSN to include ZigBee technology as the wireless medium. ZigBee is a wireless standard based on IEEE802.15.4 which is low cost.

WSN Using Raspberry-Pi are many other practical uses for the environment monitor including monitoring of temperature and humidity in a home, outbuilding, greenhouse, or even a museum Although this has been designed for passive monitoring it would be possible to have this used for actively notifying someone of a temperature change, turning on heating. Although the systems mentioned above are active in achieving the purpose of collecting sensor data and storing them, they do have a few limitations that are addressed in this project. For detecting anomalies in sensor networks, creating clusters of data and inserting expected data values and comparing them against received values is a 2. Literature Surveygood way of detecting faulty sensor nodes and replacing them, however, this project uses the in-built features of

Ruchi Mittal and Bhatia propose a system in which they detect irregular patterns of sensory data with respect to time and space. They design a system which continuously queries and monitors sensor data to detect any deviations from the norm. This is essential in detecting a faulty sensor node and ensuring it can be quickly replaced. This system is especially helpful when detec ting environmental activity like forest re. In or- der to achieve desired results. MySQL servers, namely Triggers Delimiters, using these features of MySQL, expected data ranges can be specified in the database table and any deviation from this value will send a trigger to alert the user that either an event has occurred or a node is malfunctioning. This can be checked via the phone app or by logging into the server to check the latest values updated in the database and compare them with past values.

Preprocessing and sensor data clustering is used. In data preprocessing, the sensor data is cleaned by putting in Problem Statement missing values and removing any unwanted data. Mittal and Bhatia analyzed this data cluster by plotting data, comparing them against expected/predicted patterns and detect anomalies. Ye and Wang in have a WSN system which is based on IRIS mote hardware platform which consists of ATmega 128 microprocessor, a RF230 radio chip and external ash memory for over the air.

Design and Implementation of Environment monitoring system using Raspberry-Pi which is interfaced with various sensors (temperature, Humidity, CO2, Vibration). Real time data will be collected by all the sensors and will be fetched by the Webserver. This data can be accessed by the user through web browser. programming. The sensors are programmed to collect and deliver sensor data periodically.

IV. HARDWARE

The averaging/ decimating filter provides optimization controls for lower bandwidth Raspberry-Piapplications. An internal clock drives the data sampling system, which fills the buffer memory for user access. The The Raspberry Pi is a low cost, credit-card sized computer that plugs into a computer monitor or TV, and uses a standard keyboard and mouse.

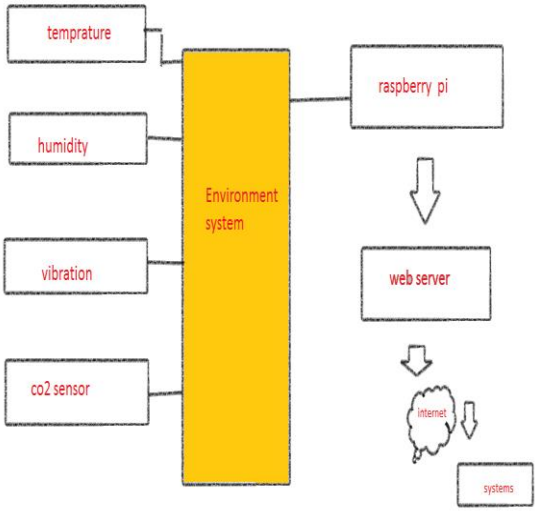

Fig-1:System Architecture

It is a capable little device that enables people of all ages to explore computing, and to learn how to program in languages like Scratch and Python. It's capable of doing everything you'd expect a desktop computer to do, from browsing the internet and playing high-definition video, to making spreadsheets, word-processing, and playing games. data capture function has three different trigger modes. The automatic data collection allows for periodic wake-up and capture, based on a programmable duty cycle. The manual data capture mode allows the user to initiate a data capture, providing power and read-rate optimization. The event capture mode continuously updates the buffers and monitors them for a preset trigger condition. This mode captures pre-event data and post-event data and produces an alarm indicator for driving an interrupt.

A. Sensors

This is a simple-to-use liquefied petroleum gas (LPG) Sensor:The DHT11 is a basic, ultra low-cost digital temperature and humidity sensor. It uses a capacitive humidity sensor and a thermistor to measure the surrounding air, and spits out a digital signal on the data pin (no analog input pins needed).It's fairly simple to use, but requires careful timing to grab data. The only real downside of this sensor is you can only get new data from it once every 2 This sensor includes a resistive-type humidity measure ment component and an NTC temperature measurement component, and connects to a high-performance 8-bit microcontroller, offering excellent quality, fast response, anti-interference ability andsensor, suitable for sensing LPG (composed of mostly propane and butane) concentrations in the air. The MQ-6 can detect gas concentrations anywhere from 200 to 10000ppm. This sensor has a high sensitivity and fast response time. The sensor's output is an analog resistance. This sensor module utilizes an

MQ-6 as the sensitive component and has a protection resistor and an adjustable resistor on board. The MQ-6 gas sensor is highly sensitive to LPG, iso-butane, propane and less sensitive to alcohol, cooking fume and cigarette smoke. It could be used in gas leakage detecting equipment's in family and industry. The resistance of the sensitive component changes as the concentration of the target gas changes.cost-effectiveness. Each DHT11 element is strictly calibrated in the laboratory that is extremely accurate

Technologies:

On humidity calibration. The calibration coefficients are stored as programs in the OTP memory, which are usedby the sensor's internal signal detecting process. The single- wire serial interface makes system integration quick and easy. Its small size, low power consumption and up- to-20 meter signal transmission making it the best choice for various applications, including those most demanding ones. The component is 4-pin single row pin package.

Python: Python is a widely used general-purpose, high- level programming language. Its design philosophy emphasizes code readability, and its syntax allows programmers to express concepts in fewer lines of code than would be possible in languages such as C++ or Java. The language provides constructs intended to enable clear programs on both a small and large scale. Python supports multiple programming paradigms, including object- oriented, imperative and functional programming or ADIS16220 Digital Vibration Sensor: procedural styles .It features a dynamic type system andThe ADIS16220 is a digital vibration sensor that combines industry-leading sensing technology with signalautomatic memory management and has a large and comprehensive standard library.processing, data captures, and a convenient serial peripheral interface (SPI). The SPI and data buffer

Things peak: structure provide convenient access to wide-bandwidth sensor data. The 22 kHz sensor resonance and 100.2 kSPS samplerate provide adequate response for most machine Open source data platform and API for the Internet of Things The Internet of Things provides access to a broad range of embedded devices and web services.

ThingSpeak is an open data platform and API for the Internet of Things that enables you to collect, store, analyze, visualize, and act on data from sensors or actuators, such as Arduino®, Raspberry PiTM, Beagle Bone Black, and other hardware. For example, with ThingSpeak you can create sensor- logging applications, location-tracking applications, and a social network of things with status updates, so that you could have your home thermostat control itself based on your current location.

API KEYS: API keys enable you to write data to a channel or read data from a private channel. API keys are auto-generated when you create a new channel. Hardware and Software Specification FOR COMPUTER: Computer with Internet.for Raspberry-pi

1) SD card of 8GB or 4GB.

2) HDMI/DVI monitor for display.

3) Ethernet cable for internet access or WIFI.

4) Keyboard and Mouse.

5) 5 volt power supply.

6) Sensors.

Software Specification: Languages:Python For Raspberry pi Board: Operating system: NOOBS

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Fig-1:ThingSpeak

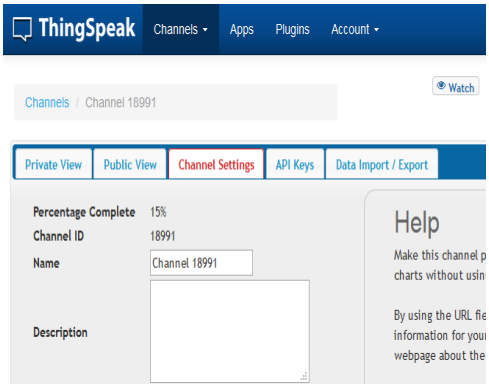
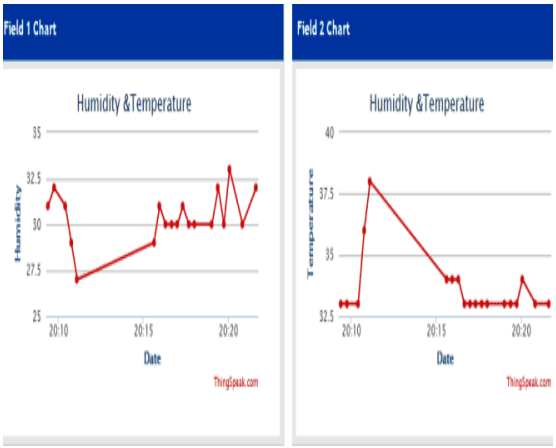


Fig-2: Channel Creation

V. User Interface:

A. *For Temperature and Humidity*



VI. CONCLUSION

The project aims at building a system which can be used on universally at any scale to monitor the parameters in a given environment. With the evolution of miniaturized sensor devices coupled with wireless technologies it is possible to remotely monitor the parameters such as temperature, humidity, amount ofco2 in air and many more .We will be using raspberry-pi as our main board and sensors will collect all the real time data from environment and this real time data will be fetched by the web server and display it. User can access this data from anywhere through Internet.

The future of this system is very wide. Internet of Things is just opening its arms, Same system can be applicable to the variety of applications like Data monitoring ,sending and controlling of data at remote location. In this project I have used sensors with digital input but with suitable A-D convertor we can easily use sensors with analog input. As applications are literally limitless we can send SMS or E-mail through Raspberry Pi. Thus, such a system can be readily implemented using a low cost computer like Raspberry Pi which can function like a complete computer. Using moisture sensor Automatic irrigation control can be done in order to get information about field and accordingly water pump will turn on. Data can be monitored using infrared sensors and pressure sensors in Surveillance system

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A Novel Weighted Scan-Based Test Pattern For Built-In Self-Test

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Abstract- In this paper a new LP BIST method has been proposed using weighted test-enable signal- based pseudorandom test pattern generation and LP deterministic BIST and reseeding. In the existing systems, more power is consumed since all the scan chains are active in both the phases. To overcome this drawback and to design a low power BIST this system is proposed. This new method consists of two separate phases namely, LP weighted pseudorandom pattern generation and LP deterministic BIST with reseeding. The first phase selects weights for test-enable signals of the scan chains in the activated sub circuits. A new procedure has been proposed to select the primitive polynomial and the number of extra inputs injected at the LFSR. A new LP reseeding scheme, which guarantees LP operations for all clock cycles, has been proposed to further reduce test data kept on-chip.

***Index Terms*—Low-power (LP) built-in self-test (BIST), reseeding, scan-based BIST, weighted test-enable signals.**

I. INTRODUCTION

The gap between functional and test power consumption is growing bigger and bigger, with the latter reaching 2X to 5X of the former due to the ever-shrinking functional power and ever-increasing test power . Problems, such as excessive heat that may reduce circuit reliability, formation of hot spots, difficulty in performance verification, reduction of the product yield and lifetime, and so on, have become severe . More details on how to provide more accurate power model can be found from previous paper. A fast simulation approach was proposed for low-power (LP) off-chip interconnect design in [1].An important through silicon via (TSV) modeling/simulation technique for LP 3- D stacked IC design was presented in [12]. Furthermore, the power dissipation of scan-based built-in self-test (BIST) is much higher than power dissipation in deterministic scan testing due to excessive switching important. Weighted pseudorandom testing schemes can effectively improve fault coverage. However, these approaches usually result in much more power consumption due to more frequent transitions at the scan flip flops in many cases. Therefore, we intend to propose an LP scan-based pseudorandom pattern generator (PRPG). This is one of the major motivations of this paper.

Most of the previous deterministic BIST approaches did not include LP concerns. We intend to present a new method that effectively combines an efficient LP PRPG and LP deterministic BIST. In order to reduce test power in deterministic BIST, we will propose a new LP reseeding scheme, since there is no other effective solution in this field. This is another motivation of this paper.

In this paper, we propose a new LP scan-based BIST architecture, which supports LP pseudorandom testing, LP deterministic BIST and LP reseeding. We present the major contributions of this paper in the following.

1) A new LP weighted pseudorandom test pattern generator using weighted test-enable signals is proposed using a new clock disabling scheme. The design - for - testability (DFT) architecture to implement the LP BIST scheme is presented. Our method generates a series of degraded subcircuits. The new LP BIST scheme selects weights for the test-enable signals of all scan chains in each of the degraded subcircuits, which are activated to maximize the testability.
2) A new LP deterministic BIST scheme is proposed to encode the deterministic test patterns for random pattern- resistant faults. Only a part of flip flops are activated in each cycle of the whole process of deterministic BIST. A new procedure is proposed to select a primitive polynomial and the number of extra variables injected into the linear-feedback shift register (LFSR) that encode all deterministic patterns. The new LP reseeding scheme can cover a number of vectors with fewer care bits.

which allows a small part of flip flops to be activated in any clock cycle.

The rest of this paper is organized as follows. The related work is presented in Section II. The new LP weighted pseudorandom test generation approach is described in Section III. The new LP deterministic BIST method with reseeding is presented in Section IV. Experimental results are shown in Section V. This paper is concluded in Section VI.

II. RELATED WORK

Scan flip flops, especially, the ones close to the scan-in pins, are not observable in most of shift cycles. A novel BIST scheme that inserts multiple capture cycles after scan shift cycles during a test cycle. Thus, the fault coverage of the scan-based BIST can be greatly improved. An improved method of the earlier work, presented in [2], selects different numbers of capture cycles after the shift cycles. In this paper, a new LP scan-based BIST technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST.

Weighted pseudorandom testing schemes can effectively improve fault coverage. A weighted test-enable signal-based pseudorandom test pattern generation scheme was proposed for scan-based BIST in [6], according to which the number of shift cycles and the number of capture cycles in a single test cycle are not fixed. A reconfigurable scan architecture was used for the deterministic BIST scheme in using the weighted test-enable signal-based pseudorandom test generation scheme. The proposed a new scan segmentation approach for more effective BIST.

LP BIST approaches were proposed early in a distributed BIST control scheme in order to simplify the BIST execution of complex ICs. The average power was reduced and the temperature was reduced. The methods reduced switching activity during scan shifts by adding extra logic. A new random single-input change test generation scheme in generates LP test patterns that provide a high level of defect coverage during LP BIST of digital circuits. An LP BIST scheme was proposed based on circuit partitioning .

New pseudorandom test generators were proposed to reduce power consumption during testing. A new encoding scheme is proposed in [3], which can be used in conjunction with any LFSR-reseeding scheme to significantly reduce test power and even further reduce test data volume. A new LP PRPG for scan-based BIST using a restricted scan chain reordering method to recover the fault coverage loss. A low-transition test pattern generator in was proposed to reduce the average and peak power of a circuit during test by reducing the transitions among patterns. Transitions are reduced in two dimensions: 1) between consecutive patterns and 2) between consecutive bits. The [1] proposed a PRPG to generate test vectors for test-per-scan BISTs in order to reduce the switching activity while shifting test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented. A new adaptive low shift power pseudorandom test pattern generator was presented to improve the tradeoff between test coverage loss and shift power reduction in logic BIST. This is achieved by applying the information derived from test responses to dynamically adjust the correlation among adjacent test stimulus bits. The proposed LP programmable generators capable of producing pseudorandom test patterns with desired toggling levels.

A new LP BIST technology that reduces shift power by eliminating the specified high frequency parts of vectors and also reduces capture power. A novel approach to reduce peak power and power droop during capture cycles in scan based logic BIST. An efficient BIST architecture was recently presented in [3] for targeting defects in dies and in the interposer interconnects.

A novel low-power BIST technology was proposed in [4] that reduces shift power by eliminating the specified high frequency parts of vectors and also reduces capture power. Multi cycle tests support test compaction by allowing each test to detect more target faults. The ability of multi cycle broadside tests to provide test compaction depends on the ability of primary input sequences to take the circuit between pairs of states that are useful for detecting target faults. This ability can be enhanced by adding DFT logic that allows states to be complemented in [3].

A new DFT scheme for launch-on-shift testing was proposed which ensures that the combinational logic remains undisturbed between the interleaved capture phases, providing computer-aided-design tools with extra search space for minimizing launch-to-capture switching activity through test pattern ordering.

Complete fault coverage can be obtained [9] when the pseudorandom test generator is modified. A combination of a pseudorandom test generator and a

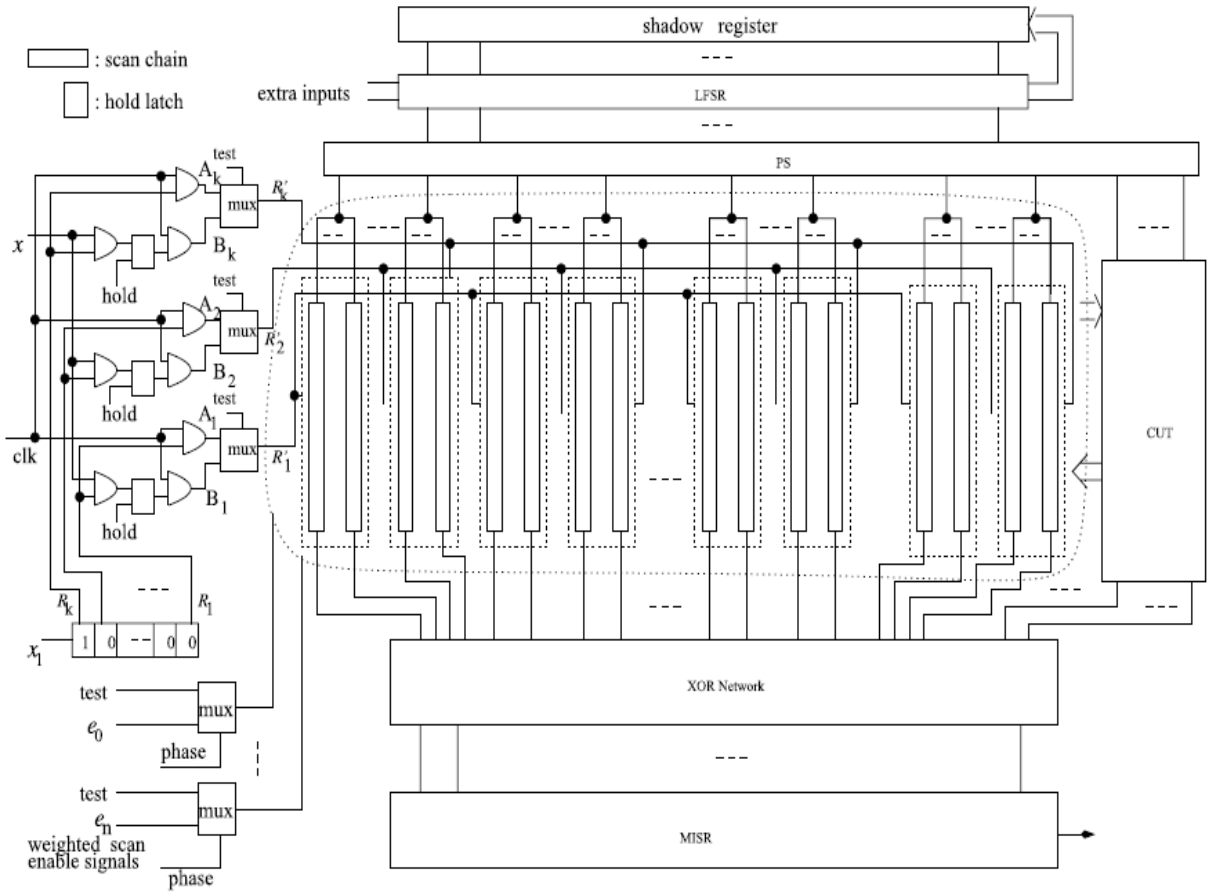


Fig:1. General DFT architecture for LP scan-based BIST.

combinational mapping logic was constructed by produce a given target pattern set of the hard-to-detect faults.

Deterministic vectors can be encoded into LFSR seeds which was proposed the seminal work, which encoded deterministic vectors into seeds. The requirement on the average size of the LFSR can be reduced by using multiple primitive polynomials .Deterministic vectors were encoded by using a folding counter and compressed by a tree architecture in a reconfigurable scan architecture for effective deterministic BIST. LP design was implemented in the new methodology in [2] to increase the encoding efficiency by combining reseeding and bit fixing.

The work is about LP delay testing, whose scan architecture and test application scheme are completely different from the new method. Our method is about scan-based BIST for single stuck-at faults based on a new weighted pseudorandom test generator and an LP deterministic BIST approach. The scan architecture is quite similar to the method in [2]. Both methods do not require test response shift-out operations, which do not cause zero aliasing.

The proposed novel X-filling method by assigning 0 and 1 s to unspecified (X) bits in a test cube obtained during ATPG. This method reduces the circuit switching activity in capture mode and can be easily incorporated into any test generation flow to achieve capture power reduction without any area, timing, or fault coverage impact. A new scan shifting method based on the clock gating of multiple groups was proposed in [45] by reducing the toggle rate of the internal combinational logic. This method prevents cumulative transitions caused by shifting operations of the scan cells, because all scan flip flops are connected to the XOR network for test response compaction.

It is possible to implement LP scan testing in a test compression environment without any increase on test application cost which was proposed a new scan architecture to compress test data and compact test responses for delay testing. An important TSV

modeling/simulation technique for LP 3-D stacked IC design was presented in [4]. The connectivity of TSVs in many important circuits also needs to be tested in an efficient way.

III. NEW LOW-POWER WEIGHTED PSEUDORANDOM PATTERN TEST GENERATOR

We present the DFT architecture to implement the LP BIST method in Section III-A. The process to implement LP pseudorandom pattern generation is presented in Section III-B.

A. DFT Architecture

As shown in Fig. 1, the scan-forest architecture [57] is used for pseudorandom testing in the first phase. Each stage of the phase shifter (PS) drives multiple scan chains, where all scan chains in the same scan tree are driven by the same stage of the PS. Unlike the multiple scan-chain architecture used in the previous methods the scan-forest architecture is adopted to compress test data and reduce the deterministic test data volume. Separate weighted signals e_0 , e_1 , …,e_n are assigned to all scan chains in the weighted pseudo- random testing phase (phase = 0), as shown in Fig. 1, which is replaced by the regular *test* in the deterministic BIST phase (phase = 1). Each scan-in signal drives multiple scan chains, as shown in Fig. 1, where different scan chains are assigned different weights. This technique can also significantly reduce the size of the PS compared with the multiple scan-chain architecture where each stage of the PS drives one scan chain. The compactor connected to the combinational part of the circuit is to reduce the size of the MISR. The shadow register is used for LP deterministic and reseeding, more details of which are described in Section IV-B.

The size of the LFSR needed for deterministic BIST depends on the maximum number of care bits of all deterministic test vectors for most of the previous deterministic BIST methods. In some cases, the size of the LFSR can be very large because of a few vectors with a large number of care bits even when a well-designed PS is adopted. This may significantly increase the test data volume in order to keep the seeds. This problem can be solved by adding a small number of extra variables to the LFSR or ring generator [10] without keeping a big seed for each vector.

We propose a new weighted PRPG for the new LP BIST approach. The new design is significantly different from the ones in [5] and [7]. This is mainly because the proposed LP design uses the gating technique to disable most of the scan chains, where the pseudo primary inputs (PPIs) of the disabled scan chains are set to constant values. As shown in Fig. 1, all scan chains in the same scan tree are selected into the same subset of scan chains, which are driven by the same clock signal. Our method selects weights for each scan chain in the degraded subcircuits. Let the scan chains be partitioned into k subsets, where only one subset of scan chains is activated in any clock cycle. Our method selects optimal weights for all scan chains in the subset of scan chains in each round. It requires k separate rounds to determine optimal weights for all scan chains.

B. Weighted Pseudorandom Test Pattern Generation

Our method generates the degraded subcircuits for all subsets of scan chains in the following way. All PPIs related to the disabled scan chains are randomly assigned specified values (1 and 0). Note that all scan flip flops at the same level of the same scan tree share the same PPI. For any gate, the gate is removed if its output is specified; the input can be removed from a NAND, NOR, AND, and OR gates if the input is assigned a noncontrolling value and it has at least three inputs. For a two-input AND or OR gate, the gate is removed if one of its inputs is assigned a noncontrolling value. For a NOR or NAND gate, the gate degrades to an inverter if one of its inputs is assigned a noncontrolling value.

For an XOR or NXOR gate with more than three inputs, the input is simply removed from the circuit if one of its inputs is assigned value 0; the input is removed if it is assigned value 1, an XOR gate changes to an NXOR gate, and an NXOR gate changes to an XOR gate. For an XOR gate with two inputs, and one of its inputs is assigned value 0, the gate is deleted from the circuit. For a two-input NXOR gate, the gate degrades to an inverter. If one of its inputs is assigned value 1, a two-input XOR gate degrades to an inverter. If one of its inputs is assigned value 1, a two-input NXOR gate can be removed from the circuit. We first propose a new procedure to generate the weights of the test-enable signals for all scan chains in the LP DFT circuit after the degraded subcircuits for each subset of scan chains, which are driven by a single clock signal, have been produced. The i -controllability $C\_i\ (l)$ ($i \in \{0, 1\}$) of a node l is defined as the probability that a randomly selected input vector sets

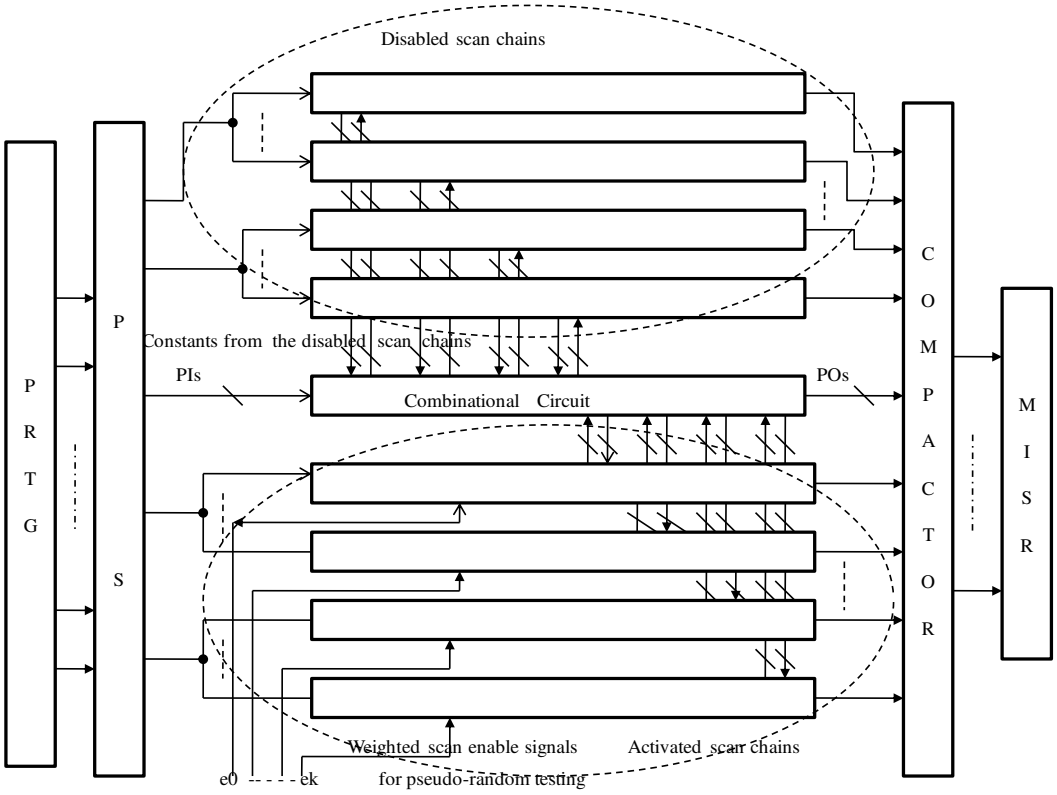


Fig.2. Weighted pseudorandom test generator for scan-tree-based LP BIST.

l to the value *i* . The observability *O_(l)* is defined as the probability that a randomly selected input vector propagates the value of *l* to a primary output. The *signal probability* of a node is defined in the same manner as its 1-controllability measure.

In the scan-based BIST architecture, as shown in Fig. 2, different weights *e*0, *e*1, . . ., and *ek* are assigned to the test-enable signals of the scan chains SC0, SC1, . . ., and SC*k* , respectively, where *e*0, *e*2, . . . , *ek* ∈ {0.5, 0.625, 0.75, 0.875}. Scan flip flops in all disabled scan chains are set to constant values. Our method randomly assigns constant values to all scan flip flops in the disabled scan chains. The circuit is degraded into a smaller sub circuit. All weights on the test enable signals are selected in the degraded subcircuit.

The gating logic is presented in Fig. 1. We do not assign weights less than 0.5 to the test-enable signals, because we do not want to insert more capture cycles than scan shift cycles. We have developed an efficient method to select weights for the test-enable signals of the scan chains. The selection of weights for the test-enable signals is determined by the following testability gain function:

$$G = \sum_{l/i \in F} \frac{|C'_1 - C'_0(l)|}{O'(l)} \quad (1)$$

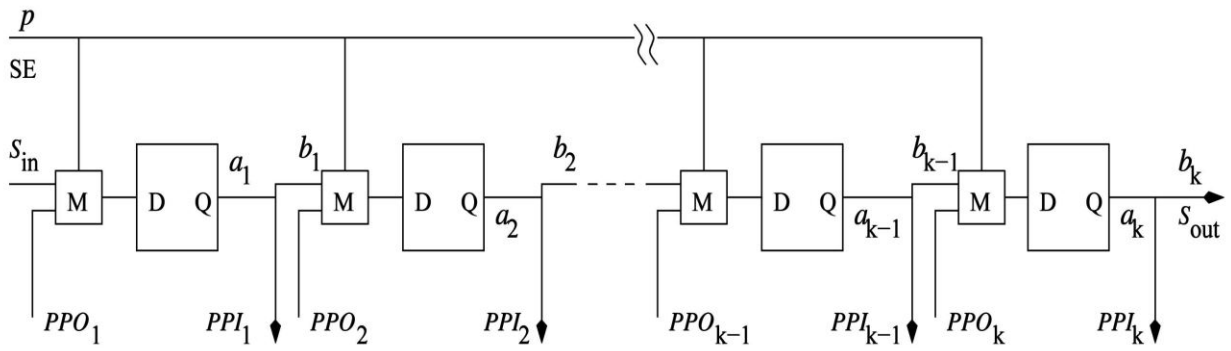


Fig. 3. Scan chain with a weighted test-enable signal.

where *l*/*i* represents the stuck-at *i* (*i* ∈ {0, 1}) fault at line *l*. In (1), *F* is the random-pattern-resistant fault set, defined as the set of faults whose detection probability is no more than ten times that of the hardest fault [6]. We attempt to minimize the testability gain function as given in (1).

Fig. 3 presents a scan chain with a weighted test-enablesignal, where *S*in, *S*out, and test are the scan-in signal, scanout signal, and the test-enable signal of the scan chain, respectively. Initially, all PPIs are assigned signal probability 0.5, and the observability of the pseudoprimary outputs (PPOs) is set to 1*/n*. Let *p* be the selected weight of the test-enable signal, as shown in Fig. 3. Then

$$C'_1(PPI_i) = p.C'_1(a_{i-1}) + (1-p) \,.\, C'_1(PPO_i). \quad (2)$$

The observability of PPO*i* (PPO) can be estimated as follows:

$$O'(PPI_i) = (1-p) \,.\, O'(a_i) \quad (3)$$
$$O'(a_i) = (1-(1-O'(b_i)) \,.\, (1-O'(PPI_i)) \quad (4)$$
$$O'(b_{i-1}) = p.O'(a_i). \quad (5)$$

The observability of the scan-out signal is set to 1. Even though the output of a scan chain is connected to the test response compactor, we can achieve zero aliasing by carefully connecting the scan chains to the XOR gates based on very simple structural analysis. Testability measures of the internal nodes, PPIs, and PPOs can be calculated iteratively using the controllability/observability program (COP) measures [11] and (2)–(5). We find that the testability measures for all nodes in the benchmark circuits converge within a few iterations.

The controllability of the PPI of the *i* th scan flip flop in a scan chain is set to 0.5, and the observability of the PPO of the *i* th scan flip flop is set to 1*/d*, where *d* is the length of the scan chains. Iterative testability estimation is adopted for all nodes based on (2)–(5) and the COP measure. It is found that testability measures for all nodes become stable after a quite few rounds of testability calculation.

Separate weights from the set {0.5, 0.625, 0.75, 0.875} are assigned to the test-enable signals of the scan chains. Algorithm 1 presents the details to select weights for all scan chains that are in the same scan chain subset. The inputs of Algorithm 1 are the scan chain set SC, which are partitioned into subsets {SC0, SC1, . . . , SC*k*−1}. Our method generates *k* degraded subcircuits for each scan chain subset SC*i* ∈ {SC0, SC1, . . . , SC*k*−1}.

Algorithm 1 Select-Weights-for-Test-Enables()

{

1) Assign the same values to the scan enable signals as the regular test-per-scan BIST scheme to all scan segments.
2) While the scan chain set s ≠ 0,do
3) Select a scan chain SC from the scan chain set S = S – {SC}
4) For each weight in {0.5,0.625,0.75,0.875},testability estimation is adopted to evaluate the cost function as presented in equation (1)
5) Select the best weight W Є {0.5,0.625,0.75,0.875} that makes the cost function as presented in equation (1)
6) For each scan chain, if no weight can be selected just leave its scan enable signal as the one in the conventional test-per -scan test scheme

}

Our method selects a weight for the first scan chain testenable signal to minimize the gain function. After the best weight has been selected for the first scan chain, a weight for the test-enable signal of the second scan chain is selected to minimize the cost function in (1). If no weight can be selected for any scan chain, our method sets its test-enable signal to the same value as the one in the conventional *test-per-scan* BIST scheme (the number of shift cycles is equal to the length of the scan chains, and a capture cycle follows). Continue the above process until appropriate weights have been chosen for all test-enable signals of the scan chains in SC*i* .

The proposed DFT architecture, as shown in Fig. 1, has an implicit advantage over other BIST architectures [1]. Each stage of the PS drives a scan tree [5] instead of a single scan chain, while each stage of the PS requires a few number of XOR gates. In any case, flip flops of all disabled scan chains are assigned with specified values. Therefore, no unknown signals are produced to corrupt the compacted test responses kept in the MISR.

Fig. 2 presents a degraded subcircuit based on the proposed LP BIST method. PPIs corresponding to scan flip flops in all disabled scan chains are assigned with randomly selected constant values in the period of weighted pseudorandom test pattern application for the current subset of scan chains. The proposed LP weighted pseudorandom test pattern generation process is as follows. The first subset of scan chains is activated when all the remaining scan chains are disabled. The generated weighted pseudorandom pattern is applied to the degraded subcircuits if a scan chain is set to the capture cycle; otherwise, the scan chain is set to the scan shift mode. Our method turns to the next phase when the second subset of scan chains is activated after the given number of clock cycles. This process continues until all subsets of scan chains have been processed. The first subset of scan chains is again activated, and the above process is executed again. The process continues until the whole given number of clock cycles has run over.

The proposed LP weighted pseudorandom test generator is shown to be able to improve fault coverage compared with the conventional test-per-scan BIST approaches according to the experimental results presented in the experimental result section. The amount of test data to be stored on-chip is also significantly reduced.

IV. LOW-POWER DETERMINISTIC BIST

We use the same LFSR for both pseudorandom pattern generation and deterministic phases. First, we propose a new algorithm to select a proper primitive polynomial; after that the LP deterministic BIST and LP reseeding schemes are presented.

A. Selecting a Primitive Polynomial andthe Extra Variable Number

Some extra variables are injected just like EDT [42]. We propose a new scheme to select the size of the LFSR and the number of extra variables simultaneously in order to minimize the amount of deterministic test data. Usually, a small LFSR constructed by a primitive polynomial is sufficient when a well-designed PS is adopted in the pseudorandom testing phase. In our method, a combination of a small LFSR and the PS from [4] is used to generate test patterns in the pseudorandom testing phase. The weighted test-enable signal-based pseudorandom test generator generates weighted pseudorandom test patterns. The size of the LFSR is not determined by the maximum number of care bits for any deterministic test vector. That is, the same LFSR is used for both phases.

For any degree less than 128, it is computationally feasible to generate enough primitive polynomials in reasonable time, out of which one (whose degree is equal to the maximum number of care bits in the deterministic vectors) can be selected to encode all deterministic test vectors. The tool that we used to generate primitive polynomials can only handle polynomials up to degree 128 of the word-length limit of the computer. However, only very small LFSRs are used for all circuits according to all experimental results (no more than 30). This is mainly because we inject some extra variables to the LFSR. To encode a few deterministic test vectors with a large number of care bits, the injected extra variables and the seed kept in the LFSR are combined just like the EDT tool. Therefore, it is not necessary to provide an LFSR whose size is at least the maximum number of care bits by injecting some extra variables.

A well-designed LFSR is needed in order to encode all deterministic vectors after the pseudorandom testing phase. A new procedure is proposed to select a primitive polynomial with the minimum degree that can encode all deterministic test vectors for the hard faults. An efficient algorithm is used to generate primitive polynomials of any desired degree. For any $i \leq 30$, assume that all primitive polynomials are kept in Q_i. As for $i > 30$, only a number of primitive polynomials are provided in Q_i . The following procedure returns a primitive polynomial with the minimum degree that encodes all deterministic vectors for the randompattern- resistant (hard) faults. Usually, the numbers of care bits of all deterministic test vectors is quite different.Therefore,

it is recommended to use an LFSR whose size is more than the maximum number of care bits S_{max} of all deterministic vectors. Unlike the method in the new method selects a primitive polynomial of relatively low degree when some extra variables are injected into the LFSR. The commercial tool EDT used similar technique to reduce the amount of test data stored in the on-chip ROM or automatic test equipment (ATE).

B. Low-Power Deterministic BIST and Reseeding

An effective seed encoding scheme is used here to reduce the storage requirements for the deterministic test patterns of the random-pattern-resistant faults. The encoded seed is shifted into the LFSR first. A deterministic test vector is shifted into the scan trees that are activated by the gating logic, where each scan-in signal drives a number of scan trees, and only one of the scan trees driven by the same scan-in signal is activated. The extra variables are injected into the LFSR when the seed is shifted into the activated scan trees. The gating logic, as shown in Fig. 1, partitions scan trees into multiple groups.

The first group of scan trees is disabled after they have received the test data. The second group of scan trees is activated simultaneously, and all other scan trees are disabled. The seed can be stored in an extra shadow register, which is reloaded to the LFSR in a single clock cycle. The scan shift operations are repeated when the extra variables are injected into the LFSR. This process continues until all scan trees have received test data.

Let us describe the details about constructing the scan forest. Assume that the number of scan flip flops at each level in the same scan tree is l and the depth of the scan forest is d. For a given scan-in pin, l scan flip flops are selected among all scan flip flops for the first level of the scan tree. The routing overhead is minimized when constructing the scan trees, which can be easily estimated using tools, such as *Astro* from synopsys [4]. Experimental results reported in this paper were obtained using the *Astro* tool. All scan flip flops at the same level in the same scan tree meet the following condition. Each pair of scan flip flops has no combinational successor in the circuit . Each scan flip flop p at the first level of the scan tree is connected to a scan flip flop f at the second level that has the minimum distance from p among all scan flip flops that can be placed at the second level of the scan tree, where all scan flip flops at the second level of the same scan tree have no common combinational successor. Repeat the above process until the scan trees have been constructed.

We propose an LP deterministic BIST scheme with reseeding. The deterministic test vectors for the random-pattern resistant faults are ordered according to the number of care bits. Our method partitions all scan chains into multiple subsets, while only one subset of scan trees is activated at any clock cycle. The gating logic controls the whole test application process. The first deterministic test vector is shifted into all scan trees as follows. The seed is first shifted into the LFSR. The extra variables with calculated values are injected into the LFSR when the seed is applied to the first subset of activated scan trees. The same values on the extra inputs are delivered after the same seed is loaded to the LFSR again for the second subset of activated scan trees. This process continues until all scan trees have received the test vector.

Our method turns to the reseeding process. The final values in the LFSR remain unchanged. The activated subset of scan trees performs d shift cycles when the extra variables with the same values are injected. The second subset of activated scan trees performs d shift cycles when the same values of the extra variables are injected. This process continues until the values of the extra variables have been shifted into all scan trees. Our method begins to check the values of the scan trees to see whether they are compatible with any remaining deterministic test vector. If so, the test vector is deleted from the ordered test sequence, and another LP capture period is applied as stated earlier from this state.

If the values kept in the scan chains are compatible with a deterministic vector, our method continues the responses capturing process. Assume that the initial values kept in the LFSR are stored in the shadow register. The first subset of scan trees is activated, which captures the test responses. The values kept in the shadow register are reloaded to the LFSR. The values of the extra variables are injected again when activated scan trees are filled. The above process continues until all scan trees have captured test responses.

If the values kept in the scan flip flops are incompatible with any other deterministic test vector, our method starts another LP shift-in period when injecting the extra variables that are stated earlier. The reseeding process continues until the given number of reseeding processes has been completed. In each round of the reseeding processes, the states of the scan trees are checked to see whether they are compatible with any deterministic test vector. If so, the deterministic vector is deleted. Our method copes with the second deterministic vector after the reseeding processes have been completed.

TABLE- 1

FAULT COVERAGE COMPARISON OF THE LP WEIGHTED PSEUDORANDOM TEST GENERATOR

-	The Proposed Method				[10]			
circuits	FC	FC(10)	FC(20)	FC(30)	FC	FC(10)	FC(20)	FC(30)
s38417	99.165	99.053	99.077	99.107	97.879	97.365	97.561	97.613
b19	84.832	84.332	84.645	84.679	83.237	82.859	82.883	82.994
wb_conmax	93.527	93.266	93.437	93.471	91.793	91.412	91.486	91.506
usb_funct	92.811	92.742	92.787	92.798	92.016	91.621	91.795	91.814
pci_bridge	95.447	95.003	95.224	95.287	94.841	94.597	94.772	94.768
des_perf	96.901	96.887	96.889	96.892	95.396	95.013	95.175	95.223
ethernet	96.318	96.089	96.117	96.226	95.904	95.457	95.682	95.726
vga_lcd	92.031	91.683	91.778	91.859	91.303	90.768	90.917	91.162
netcard	95.194	93.982	94.337	94.756	94.546	93.349	93.651	94.173

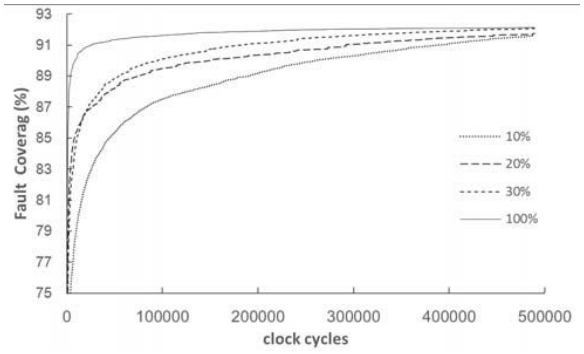
V. EXPERIMENTAL RESULTS

The proposed method has been implemented and evaluated on a Dell Precision 7810 workstation. The pseudorandom testing phase was used with the scan-forest scan architecture, and separate weighted test-enable signals were assigned to the scan chains. A very small number of scan-in pins were used, making the size of the PS very small. That is, the area overhead can be reduced significantly.

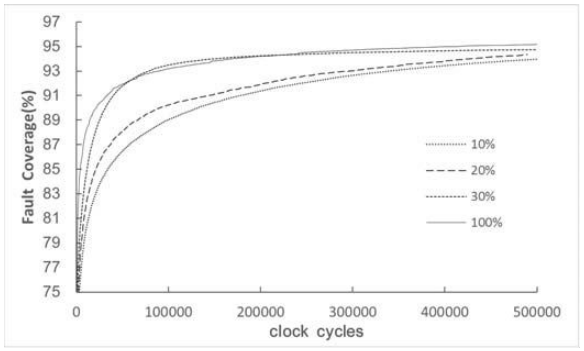
Performance comparison for the proposed LP BIST scheme and the one in [10] is presented in Table I on the fault coverage of the pseudorandom test generators. The column FC shows the fault coverage of the original weighted pseudorandom test generator. The columns FC(10), FC(20), and FC(30) present the fault coverages of the proposed LP BIST method after 500k clock cycles, where the number given in the bracket shows the percentages of the activated scan flip flops for the proposed LP BIST method and the one presented in [10].

As for the circuit netcard, both LP BIST methods reach 93.98% and 93.35% fault coverage when only 10% scan chains are activated. The numbers of the deterministic test vectors for both methods are 173 and 192, respectively, and the final amount of on-chip data for the seeds is reduced approximately 26.8 times. It is shown that the number of maximum care bits of the deterministic vectors for both methods are 379 and 9873, respectively, which makes the amount of seeds to be kept on-chip completely different.

Fig. 3 presents the performance of the proposed LP PRPG for circuits netcard and vga when different percentages (10%, 20%, 30%, and 100%) of scan chains are activated. It is shown that the fault coverage is less when fewer scan chains are activated. Finally, the fault coverages for all four cases are quite close after 500 000 clock cycles. In a few cases, the fault coverage with 30% activated scan chains is slightly more than that with 100% activated scan chains for the circuit netcard. This anomaly also occurs for the circuit vga, as shown in Fig. 3.



(a)



(b)

Fig. 5. Fault coverage with different toggle rates. (a) vga_lcd. (b) Netcard

TABLE II

POWER REDUCTION

-	low-power deterministic BIST			low-power PRPG		
circuits	peak(mW, before)	lp peak(mW, after)	rate(%)	peak(mW, before)	lp peak(mW, after)	rate(%)
s38417	6724	643	9.6	7695	704	9.1
b19	41933	5660	13.4	45334	5779	12.7
wb_conmax	10299	1111	10.8	11197	1255	11.2
usb_funct	6261	610	9.7	6342	639	10.1
pci_bridge	8119	984	12.1	8783	1014	11.5
des_perf	22771	2181	9.5	25552	2398	9.4
ethernet	28865	3746	12.9	29331	3823	13
vga_lcd	46372	4775	10.2	47432	4396	9.3
netcard	95165	9426	9.9	103676	9970	9.6

Table II presents the performance of the proposed LP deterministic BIST scheme on peak power (milli-Watt, mW) reduction when 10% scan chains are activated. The supply voltage and frequency are set to 1.5 V and 200 MHz, respectively. The column's peak (mW, before) and lp peak (mW, after) show the peak power for the original deterministic BIST and weighted test-enable-based PRPG, and the proposed LP BIST method. The column rate(%) shows the percentage of peak power for the proposed method compared with the one without the LP design for both the weighted pseudorandom test generation phase and the deterministic BIST phase. Experimental results in Table II show that the proposed LP PRPG phase reduces the peak power to less than 13% for all circuits, and the LP deterministic BIST scheme reduces the peak power to less than 14% in all cases. Experimental results show that the peak power for the PRPG phase is a little more than that for the deterministic BIST phase for the all circuits except s38417 before the LP design is included. This is mainly because only 10% flip flops are activated in any case during the LP weighted pseudorandom testing and the LP deterministic BIST phases, as shown in Fig. 1.

VI. CONCLUSION

A new low-power (LP) scan-based built-in self-test (BIST) technique is proposed based on the weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed in this paper, which supports both the pseudorandom testing and deterministic BIST. During pseudorandom testing phase, an LP weighted random test pattern generation scheme is proposed by disabling a part of scan chains. During the deterministic BIST phase, the design-for testability architecture is modified slightly while the linear-feedback shift register is kept short. In both the cases, only a small number of scan chains are activated in a single cycle thus low power scan based BIST technique is designed.

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Reversible Adder/Subtractor Circuits: A Study

T. Melina, N. Raj and P. John Paul

***Abstract*— The Reversible logic is a unconventional form of computing where the computational process is reversible. The study of this technology is to implement reversible computing where they offer what is predicted to be the only potential way to improve the energy efficiency of computers beyond von Neumann- Lindauer limit. This is new and emerging area in the field of computing that taught us to think physically about computation. Quantum Computing will bring a total change in how the computer will operate and function. The reversible arithmetic circuits are efficient in terms of number of reversible gates, garbage output and quantum cost. Study of Reversible Binary Adder Subtractor- Mux, Adder- Subtracter - TR Gate., Adder-Subtractor- Hybrid is studied in this paper. In all the three design approaches, the Adder and Subtractor are realized in a single unit as compared to only full adder/subtractor in the existing design.**

***Index Terms*— Reversible gates, Fredkin gate, Feynman gate, Toffoli Gate, Peres gate**

I. Introduction

REVERSIBLE logic is generally used in Nanotechnology, quantum computing, Low power CMOS, Optical computing and DNA computing, etc. Quantum computation generally uses reversible logic. Basically, reversible gates are used to perform reversible computations. These circuits do not lose information and reversible computation in a system that can be performed only when system comprises of reversible gates. The gates that are used in digital design are not reversible (i.e) AND, OR and EXOR gates does not perform reversible operation.

A reversible gate can generate a unique output from each input vector, and vice versa, hence one to one mapping between the input and output vectors are obtained. Among all the gates only the NOT gate is reversible. Loss of energy is important criteria in digital design. The energy dissipation is related to non ideality of switches and materials. Two reversible gates are generally used to design a reversible circuit. Reversible gates acts as building blocks for reversible circuits.

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The following are the characteristics of Reversible gates.

- A reversible gate has input and output with a one to one correspondence. i.e. the inputs of a reversible gate is uniquely determined from there outputs.
- The number of inputs and outputs should be equal in reversible logic gate.
- The fan out of every signal including primary inputs in a reversible gate must be one.

In design of reversible logic circuit, the Classical logic synthesis methods cannot be applied directly.

II. Reversible Gates

Reversible logic types:

- The basic reversible gate is NOT gate and is a 1x1 gate, Controlled NOT (CNOT) gate is a 2x2 gate.
- Fredkin gate, Toffoli gate, Peres gate and TR gate are all 3x3 reversible gates.
- Each reversible gate has a cost associated with it called quantum cost. The quantum cost of 1x1 reversible gates is '0', and quantum cost of 2x2 reversible gates is '1'.
- Reversible gates is identified by using 1x1 NOT gates and 2x2 reversible gates, i.e. V and V+ [where V is square root of NOT gate and V+ is its Hermitian] and Feynman gate (CNOT gate).

The property of V and V+ gate is :

$V \times V = NOT$

$V \times V^{+} = V^{+} \times V = I$

$V^{+} \times V^{+} = NOT$

The quantum cost of a reversible gate is calculated by counting the number V, V+ and CNOT gates used in implementing it except in some cases.

A. *NOT Gate*

Among all the conventional logic gates, **Not gate** is the only reversible gate (1x1 gate). The quantum cost of NOT GATE is zero.

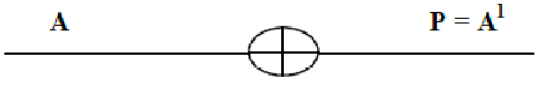

Fig.1 NOT gate

B. *Feynman Gate (CNOT gate):*

This is a 2x2 gate having mapping (A, B) to (P=A, Q=A B)

where A, B are inputs and P, Q are outputs respectively. Feynman gate can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

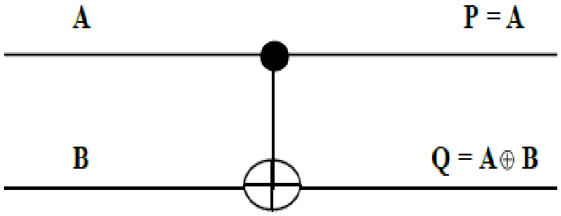

Fig. 2 Feynman or CNOT gate

C. *Toffoli Gate:*

This is a 3x3 reversible gate with two of its outputs are same as inputs with the mapping (A, B, C) to (P=A, Q=B, R= A.B C). Where A, B, C are inputs and P, Q, R outputs respectively. Toffoli gate is most popular reversible gates and has quantum cost of 5. It requires 2V gates, 1 V+ gate and 2 CNOT gates.

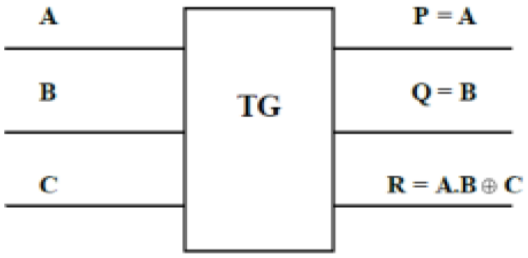

Fig. 3 Toffoli gate

D. *Peres Gate:*

Peres gate is a three input and three output (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q= A B, R= (A.B) C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Peres gate has the quantum cost of 4, since it requires 2 V+ gate, 1 V gate and 1 CNOT gate. Among 3x3 reversible gates, this has the minimum quantnum cost

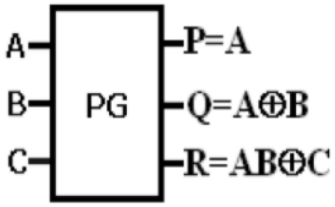

Fig. 4 Peres Gate

E. *Fredkin Gate:*

Fredkin gate is a 3x3 conservative reversible gate. It maps (A, B, C) to (P=A, Q= A' B+AC, R=AB+ A'C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Fredkin gate can be implemented with a quantum cost of 5 and it requires 2 dotted rectangles, 1 V gate and 2 CNOT gates.

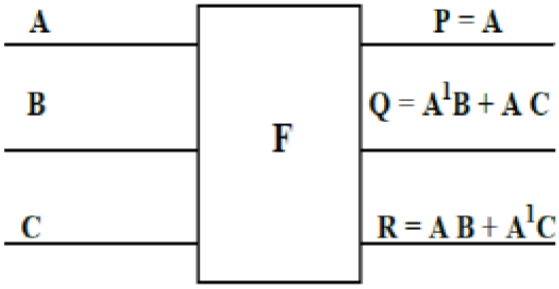

Fig. 5 Fredkin Gate

F. *TR Gate:*

TR gate has 3 inputs and 3 outputs having inputs and outputs mapping as (P = A, Q=A B, R= (A . B') C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. TR gate may also be realized in a different implementation with quantum cost of 6 or lesser than 6. Therefore it is considered that the quantum of TR gate as 6 for the calculation of parallel Subtractor implementing by reversible gate.

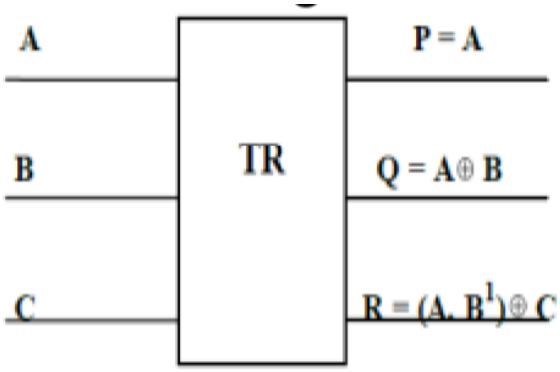

Fig. 6 TR Gate

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Any machine, which can build up arbitrary combinations of logic gates from a universal set is then a universal computer. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. Parameters for determining the complexity and performance of circuits.

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.

- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.
- A 3-input and 3-output reversible logic gate was proposed in. It has inputs a, b, c and outputs x, y and z as shown.
- The truth table of the gate is shown in the Table. It can be verified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined. The gate can be used to invert a signal and also to duplicate a signal.
- The signal duplication function can be obtained by setting input b to 0. The EX-OR function is available at the output x of the gate.
- The AND function is obtained by connecting the input c to 0, the output is obtained at the terminal z. An OR gate is realized by connecting two new reversible gates.
-

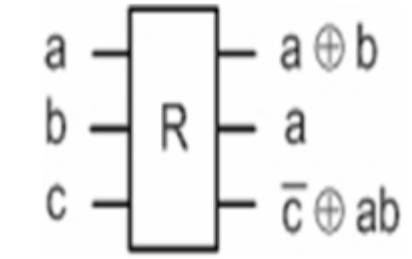

Fig. 7 Reversible gate R

Table: 1 Truth Table for Gate R

a	b	c	x	y	z
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	1	0	1	1

III. REVERSIBLE ADDER/SUBTRACTOR

A. Adder circuits:

Several types of adders are used in computing systems. A ripple carry adder has the simplest structure compared to any another. In a ripple carry adder, full adders connected in series generate the sum and the carry outputs based on the addend bits and the carry input. The disadvantage of a ripple carry adder is that the carry has to propagate through all stages.

B. Ripple carry adders:

Building block of a ripple carry adder is a full adder block. A full adder computes the sum bit Si and the carry output c i+1 based on addend inputs a and b and carry input c.

The output expressions for a ripple carry adder are

(i) Si = a xor b xor c;

(ii) Ci+1 = ab + bc + ca; (i = 0,1, 2,)

A Reversible gate can generate unique output vector from each input vector, and vice versa. Hence the number of outputs in a reversible circuit has the same number of inputs, and commonly use NOT gate as it is the only reversible gate. One of the most important features of a Reversible gate is its garbage output i.e. The input of the gate which is not used with other gate is called garbage output.

A four-bit parallel adder/subtractor is built using the full adder/subtractor and half adder/subtractor units.

Table 2: Truth Table For Full Adder/Subtractor

CTRL	A	B	C	Carry/ Barrow	Sum / Difference
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	1

Half Adder sub:

Subtractor Reversible half adder/subtractor logic is implemented with the four reversible gates i.e. two are Feynman gates and 2 are fredkin gate. Here there are 3 garbage values. Inputs of garbage are '2' and the quantum cost is '12'.. This half adder/subtractor is basically used in implementing four-bit parallel reversible adder/subtractor unit.

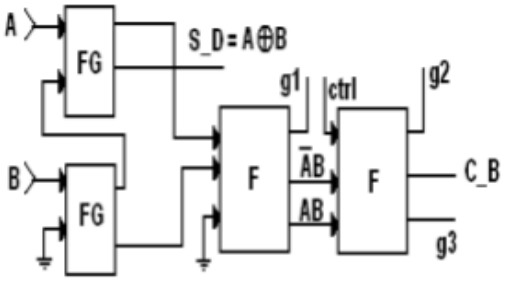

Fig. 8 Implementing reversible Half Adder/ Subtractor.

Table 3: Truth Table For Half Adder/Subtractor

CTRL	A	B	Carry/ Barrow	Sum / Difference
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	0	0
1	0	0	0	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

Full Adder-Subtractor-Mux :

This design is mainly based on the usage of reversible gates for each function i.e. Peres gate for adder function, TR gate for subtractor function and Fredkin gate for multiplexing the Carry and Borrow line into single line output. For creating signal multiplication of each signal 3 Feynman gates are used . For this kind of design 8 reversible gates, 3 Feynman gates, 2 Peres gates, 2 TR gates and one Fredkin gate are used. The table shows that among 7 garbage outputs 5 garbage (constant) inputs and the total quantum cost is 28.

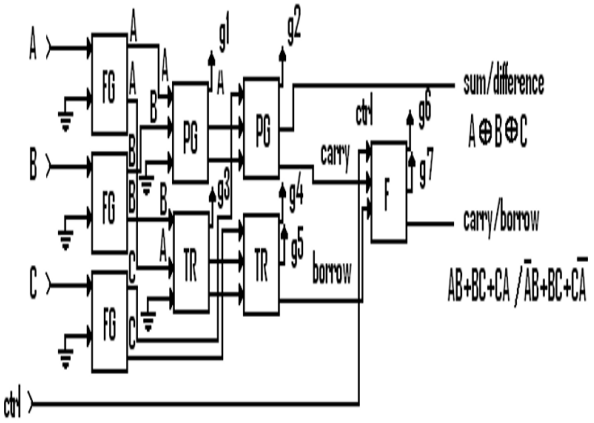

Fig. 9 Implementing reversible full Adder/Subtractor

- This is implemented by using VHDL code and simulated by using Modelism simulator.
- The functionality of individual gates is implemented using Behavioural style of modelling and the overall logic is implemented using structural style of modeling.

Full Adder-Subtractor-TR gate:

The main function of addition and substraction is realized by using TR gates.. The design includes 3 TR gates and 6 Feynman gates. Feynman gates are used for input signal buffering. The garbage output in this design is 7 and the garbage inputs are 5. The quantum cost is 24. If one additional Feynman gate (C-NOT Gate) is used in this design, a quantum cost advantage of 4 is obtained. This quantum cost advantage is mainly due to the realization of arithmetic blocks of adder and subtractor is realized with 3 TR gates as against the 5 numbers of 3x3 reversible gates for Adder-Subtractor- Mux design.

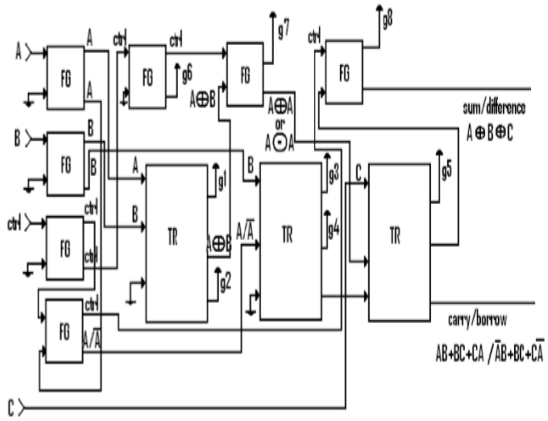

Fig. 10 Implementing reversible Full Adder-Subtractor-TR gate

- This is implemented by VHDL code and simulated using Modelsim simulator.
- The individual gates functions are implemented by using Behavioral style of modeling .

Full Adder-Subtractor- Hybrid:

It is an optimized implementation of adder-substractor function. In this case two Feynman gates are used to realize sum/difference output.. Two Fredkin gates and a TR gate are used to realize carry borrow line. This design utilizes 8 gates including the C-NOT gates for input signal multiplication. The garbage output is 5 and garbage input in this design is 3. The quantum cost is 21. By optimal utilization of gates the optimization of the garbage input, garbage output and quantum cost in this case is obtained. By two CNOT gates, the sum/difference function in this case is realized. Hence it is essential to have a design approach where, the required functionality may be realized with simplest gates as much as possible.

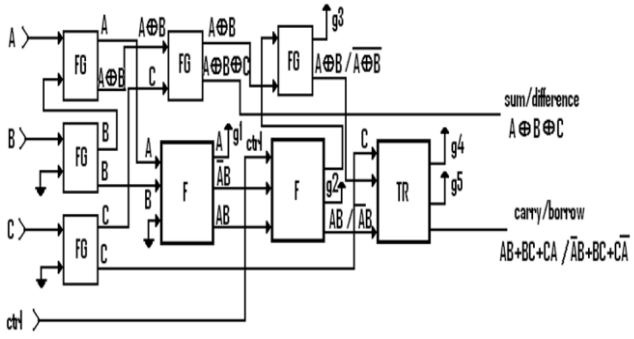

Fig. 11: Implementing reversible Full Adder-Subtractor-Hybrid

IV. CONCLUSION

The Reversible logic is breakthrough for energy efficiency of computers beyond von Neumann- Lindauer limit. The study performed in this paper detailed about Reversible Binary Adder Subtractor- Mux, Adder- Subtracter - TR Gate., Adder-Subtractor- Hybrid. In all the three design approaches, the Adder and Subtractor has been realized in a single unit as compared to only full adder/subtractor in the existing design.

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NOVEL ENERGY EFFICIENT CARRY SKIP ADDER BASED ON DUAL MODE LOGIC DESIGN

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ABSTRACT

The recently proposed dual mode logic (DML) gates family enables a very high level of energy-delay optimization flexibility at the gate level. In this paper, this flexibility is utilized to improve energy efficiency and performance of combinatorial circuits by manipulating their critical and noncritical paths. An approach that locates the design's critical paths and operates these paths in the boosted performance mode is proposed. The noncritical paths are operated in the low energy DML mode, which does not affect the performance of the design, but allows significant energy consumption reduction. The proposed approach is analyzed on a 128 bit carry skip adder.

Keywords:

Dual Mode Logic, energy efficiency, high performance, critical paths, energy-delay optimization.

I. INTRODUCTION

The DML logic gates family was proposed in order to provide a very high level of energy-delay (E-D) optimization flexibility. DML allows an on-the fly change between two operational modes at the gate level: static mode and dynamic mode. In the static mode, DML gates consume very low energy, with some performance degradation, as compared to standard CMOS gates. Alternatively, dynamic DML gates operation obtains very high performance at the expense of increased energy dissipation. A DML basic gate is based on a static logic family gate, e.g., a conventional CMOS gate, and an additional transistor. While DML gates have very simple and intuitive structure, they require an unconventional sizing scheme to achieve the desired behavior .Performance of most digital circuits and systems is determined by the delay of critical paths (CP). Even though standard synthesis tools attempt to design logic blocks without CP (*i*:*e*: equalized path delay), the slack from the targeted *Clk* (Clock) frequency always exists and should be repaired by designers.

Many methods have been proposed to address these slacks. These methods include adaptive voltage scaling with a CP emulator circuit, multi oxide thickness driven threshold-voltages, multi-channel lengths for energy reduction in the non-CPs and performance boost in the CPs. *Meijer et al.* and *Liu et al.* applied a body bias on a non-CP to improve energy consumption and increase performance of the CPs, respectively. While the aforementioned methods solve the critical path slack problem, in most cases they also result in a significant increase of energy consumption. In addition to these gate level approaches higher-level approaches were presented such as multi-mode logics, parameterized logic. In this paper, we issue both the gate and

higher architectural levels. This paper proposes to meet the delay requirements of CPs along with lowering the over-all energy consumption of the design by utilizing the powerful modularity of DML. We propose and analyze a new approach, which locates the design's CPs and utilizes the on-the-fly modularity of DML to operate these paths in the boosted (dynamic) performance mode. The non-critical paths are operated in the low energy static DML mode, which does not affect the performance of the design. Since in most cases the majority of gates in the design are not on the CPs, the increase in energy consumption of the critical paths will be negligible in comparison to the general circuit consumption. Moreover, DML static gates dissipate less power than their CMOS counterparts, resulting in reduced power dissipation of the whole design .The proposed approaches have been analyzed on a 16 bit Carry Skip Adder (CSA) benchmark. Simulations carried out in a standard 180nm CMOS process.

II. DML BASICS

A. DML OVERVIEW

A basic DML gate architecture is composed of an un-clocked static gate, *e*:*g*: CMOS, and an additional transistor *M1*,whose gate is connected to a global clock signal. In this paper we focus on DML gates where the static gate implementation is based on conventional CMOS. A DML gate implementation can be one of two: ``*Type A''* and ``*Type B''*, as shown in Figure 1(a-b) and Figure 1(c-d), accordingly. In the static DML mode of operation (Static mode), the M1 transistor is cut-off by applying the high *Clk* signal for ``*Type A''* and low *Clk_bar* for ``*Type B''* topology. Therefore, the gates of both topologies operate similarly to the static logic gate, CMOS in this case. For a dynamic operation of the gate (Dynamic mode), the *Clk* is enabled for toggling, providing two separate phases: pre-charge and evaluation. During the pre-charge phase, the output is charged to *VDD* in ``*Type A''* gates and discharged to *GND* in ``*Type B''* gates. During evaluation, the output is evaluated according to the values at the gate inputs, in a similar fashion to NORA/np- CMOS implementations. It was shown that DML gates have presented a very robust operation in both static and dynamic modes under process variations (PVT) and at low supply voltages. Dynamic mode robustness is mainly achieved by the intrinsic active restorer (pull-up in ``*Type A''* and pull-down in ``*Type B''*). This restorer also allows sustaining glitches, charge leakage and charge sharing. Unique sizing of the DML gate transistors is the key factor for achieving low energy consumption in the static DML mode (in which the topology of the gate is identical to the static gate). This sizing is also responsible for reduction of all capacitances of the gate. In a similar way, the unique transistor sizing enables evaluation through a low resistive network achieving fast operation in the dynamic mode. An intuitive visualization of the tradeoff inherently related to DML is shown in Figure 1(e). Energy efficiency is achieved in the static DML mode at the expense of slower operation (Low Energy and Low Performance, left scales). However, the dynamic mode is characterized by high performance, albeit with increased energy consumption (High Energy and High Performance, right scales). These tradeoffs allow a very high level of flexibility at the system level, as will be shown

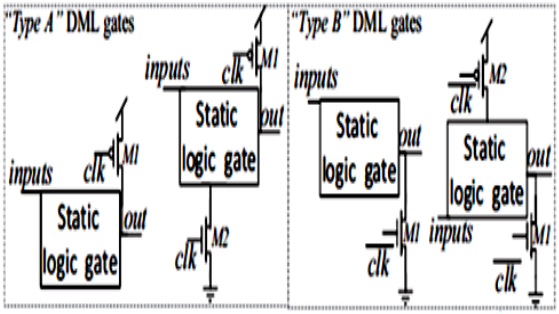


Fig 1 : (a) (b) (c) (d)

in Section III. Figure 1(f) and Figure 1(g) show the sizing of CMOS based DML gates in ``*Type A*" and ``*Type B*", respectively. These are optimized for dynamic operation. Figure 1(h) shows the conventional sizing of a standard CMOS gate where, *WMIN* is a minimal transistor width, β is the PUN to PDN inherent up-sizing factor and *f* is the gate's general up-sizing factor. As can be seen, the in and out capacitances of DML gates are significantly reduced, as compared to CMOS gates, due to the utilization of minimal width transistors in the pull-of``*Type A''* or pull-down of ``*Type B''* networks

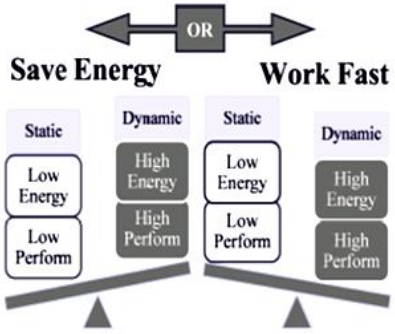


Fig 1: (e)

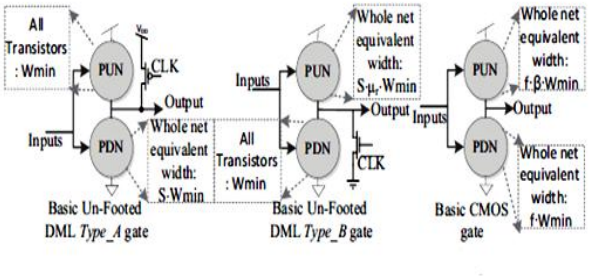


Fig 1: (f) (g) (h)

. The size of the pre-charge transistor is kept equal *S_WMIN* in order to maintain a fast pre-charge period, despite the output load upsized gate, where *S* is the evaluation network upsizing factor. Figure 1(b) and Figure 1(d) show the footed ``*Type A*" and the headed ``*Type B*" DML gates, respectively. It allows successful pre-charge for a cascaded topology of standard Static gates Synchronous devices to a DML logic. Many aspects of DML gates sizing, as well as preferred set of gates for ``*Type A*" and ``*Type B*" topologies, have been analyzed and discussed. Optimization for network up-sizing parameters for load driving was conducted using the Logical Effort (LE) method [3]. The DML key achievement is that while presenting very high performance in the dynamic mode by the proposed sizing, the same topology also enables improved energy efficiency in static mode, as compared to a conventional CMOS.

B. STATIC DML AS A SEMI-ENERGY OPTIMAL CMOS

Design space of a CMOS gate is mainly influenced by *VTH* ,transistor width, *VDD*, channel length, oxide thickness and body voltage. The influence of those parameters on E-D plain-optimization is being explored. For the CMOS family, the symmetry of the gate (*i*:*e*: equal rise and fall times) is highly important. This is due to the fact that in a combinational system there is always some uncertainty regarding the transition type. As a result, the pull-up network (PUN) of CMOS gates, which is constructed by low mobility PMOS devices, is sized up by the β parameter. When optimizing a CMOS gate's energy at the expense of its performance, the transistor's width is the main parameter used for reducing the energy consumption. This is due to several facts:(1) Switching energy is proportionate to the load and quadratic dependent on *VDD*. Under energy optimization, the symmetry of the gates' performance does not constitute a constraint so the transistor's width can be reduced, as well as β This significantly lowers the load capacitances. (2) With circuit's *VDD* lowering and technology scaling, leakage energy has become one of the key factors for static power dissipation. The leakage energy is caused by the numerous leakage currents of a device.

The main leakage currents are the sub-threshold and gate leakage currents. These currents are linearly dependent on the transistor's width And under energy optimization they are considerably reduced. CMOS based DML operated in static mode with transistor sizes optimized for the dynamic mode is *de facto* a semi-energy-optimal CMOS structure with an additional negligible output capacitance for the *Clk* transistors (transistors M1 and M2). Static DML is still highly robust due to its complementary nature and withstands aggressive voltage scaling. This methodology can also be referred to as a stand-alone technique for reducing the energy consumption of digital circuits. The E-D tradeoff space under this approach is very wide and in this paper the discussion is limited only to transistors sizing, as shown in Figure 1(f) and Figure 1(g) for DML gates.

III. CP-DML APPROACHES FOR ENERGY EFFICIENCY AND HIGH PERFORMANCE

This section elaborates the proposed design approaches for energy efficient and high performance design of combinatorial systems. Sub-Section A presents an approach which utilizes DML gates in the dynamic mode on the CPs in order to improve their delays. Sub-Section B elaborates various aspects of energy reduction of all non-CP portions of the design.

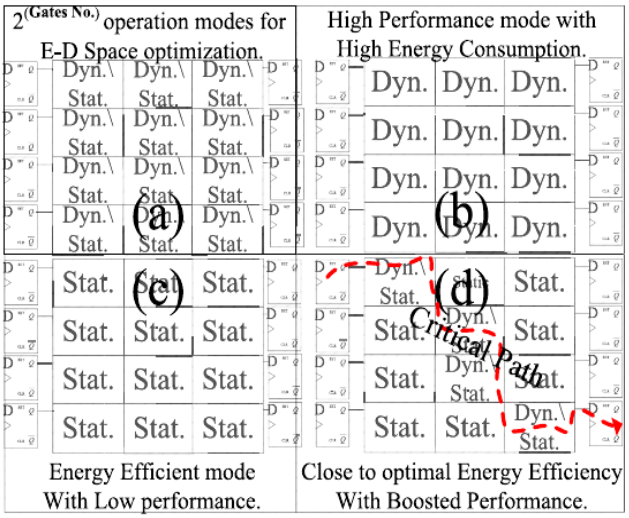


FIGURE 2. (a) DML design optional operation modes (b) DML design degenerated to the dynamic mode (c) DML design degenerated to the static mode (d) DML design where only the CP's are dynamically operated while the rest of the design operate in the low energy static mode.

Where, Dyn. and Stat. stands for Dynamic and Static respectively theoretically, a general DML design can be controlled (input signal-driven control or external signal-driven control) to operate each gate in one of two modes: Static and Dynamic. This means that a general design can be operated in 2(*Gates Number*) different options, each one leading to a different operating point on the E-D space of the design. Figure 2(a) visualizes this modularity. The degenerated approaches for operating all the gates in one of the two modes, similar to a sole gate, are shown in Figures 2(b) and 2(c). Switching between these two modes leads to the distinct tradeoff, meaning that the design optimized either to achieve maximum performance or minimum energy consumption.

A.SOLVING CPs TIMING VIOLATIONS

As discussed in Section I, the CPs of a design are automatically identified using standard design flow tools. By replacing only these paths with DML gates and applying the dynamic mode on these paths, their delay can be reduced. The rest of the design is implemented using standard CMOS static logic. Of course, special design constraints should be enforced in all the intersections between a static path and a dynamic one. In some of these cases, a footer and header should be applied. Figure 2(d) presents a design in which the CPs were located and *only those paths* were given the option to toggle between dynamic and static mode, according to the system requirements. If the system design can withstand slower operation, the CP logic will operate in static mode. If the system is required to

meet the defined *Clk* period for all cycles, the CPs will operate in the dynamic mode. Such application can be a smart phone that operates with two frequencies: slow one for power save/ hibernating mode and a fast one for video streaming. To emphasize, low complexity systems will normally bear only one frequency for operation and therefore the CPs will constantly operate in the dynamic mode. Normally, the amount of gates on the CP is small as compared to the total amount of gates in the design. Therefore, in most cases, the inherent dynamic-operation energy of these CPs will lead to a non-significant increase in total energy consumption of the design.

B. SOLVING THE CPs TIMING VIOLATION WHILE REDUCING THE TOTAL ENERGY CONSUMPTION

As described in the previous Sub-Section, the CPs are mapped and operated in the dynamic DML mode. In Sub-Section A,the rest of the circuit was assumed to keep a standard CMOS logic gates topology. Therefore, the design was proposed to solve the CPs' timing constraints at the expense of a small degradation in energy consumption, as compared to a complete CMOS design. In this Sub-Section, all portions of the design, which are not a part of the CPs, will be mapped to static mode DML gates (similar to semi-energy optimized CMOS gates, described in section II). In most designs, these non-CPs are not time constrained and therefore the asymmetry behavior of their transitions and consequently their performance degradation will withstand the *Clk* period. The use of the static DML mode for the mass majority of gates in the design will lead to a signi ficant reduction in the total dynamic and static energy consumption. Figure 3 visualizes this approach.

IV. MODULAR BENCHMARK

This section, presents the chosen benchmarks. As depicted in Section III we will discuss three designs:

1) A CPs accelerator, as described in Sub-Section III(A), which has 2 operation modes:

_ ``DML Carry Path-Dynamic"- The DML CPs are activated in the dynamic mode.

_ ``DML Carry Path-Static"- The DML CPs are activated in the static mode.

In both of these modes the rest of the non-CPs portions of the system are designed with standard CMOS.

2) A CPs accelerator with low energy consuming non-CPs, as described in Sub-Section III(B), which has 2 operation modes:

_ ``DML Carry Path-Dynamic.With low energy non-CPs-tatic" - The DML CPs are activated in the dynamic mode, while the rest of the system operates in the DML static mode.

_ ``DML Carry Path- Static. With low energy non-CPs- Static" - The DML CPs are activated in the DML static mode, similar to the rest of the system.

3) CMOS equivalent design.

A Carry Skip Adder (CSA, also called carry bypass adder),was chosen as a benchmark to demonstrate and evaluate the proposed concept. The CP of the CSA increases as a function of the number of inputs, making it possible to examine the E-D trends as a function of the CPs lengths. It is important to note that the proposed methods can apply over any combinatorial circuits and a CSA was chosen only due to its modularity and simplicity.

A. CMOS CSA DESIGN

A conventional CSA is composed of a set of Ripple Carry Adder (RCA) blocks. They essentially utilize the carry propagation in order to skip the carry from one RCA to the next RCA block. It is possible to predict the propagation of the carry by a simple XOR gate. Such prediction mechanism can substantially reduce the delay. The CP in CSA occurs when the carry ripples at the first block, and

then skips the rest of the blocks and then ripples again at the last block.This is the longest possible route in the CSA. *Lehman et al.*have researched CSAs with non-uniform sized distributed RCA blocks [20]. *Majerski* has presented a multi-level of carry-skip propagation architecture. *Guyot et al.* and *Oklobdzija et al.* proposed algorithms for choosing optimized block sizes. In this paper, a simple CMOS CSA design with a fixed size of 4-bits blocks was designed, as shown in Figure 4. Clearly, the methods presented in this paper can be generalized to any CSA block size constant or variable and for multi or single level carry path. A general single-bit Full Adder (FA) equations are:

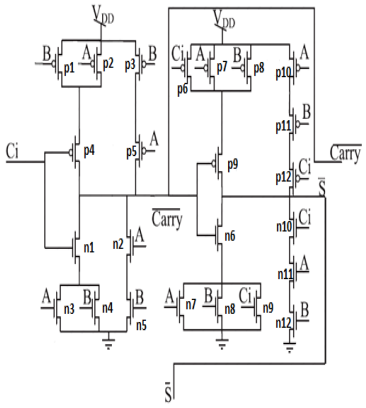


Figure 3. Full Adder

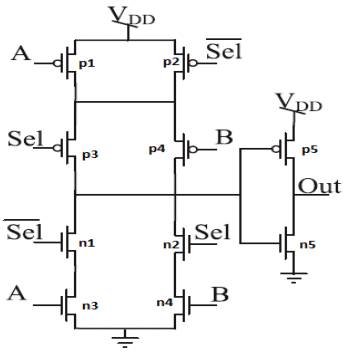


Figure 4. Multiplexer

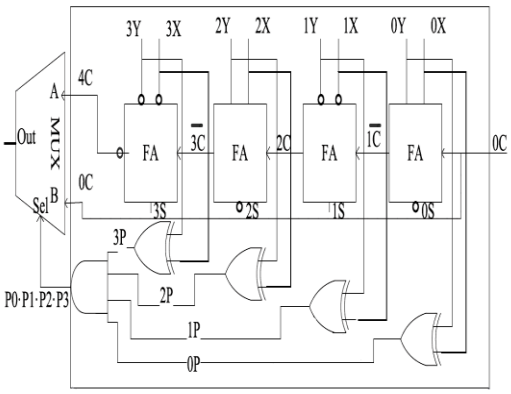


Figure 5. Ripple Carry Adder Block

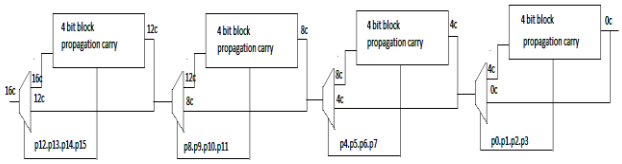


Figure 6. Carry Skip Adder Block

B. DML CRITICAL PATH DESIGN

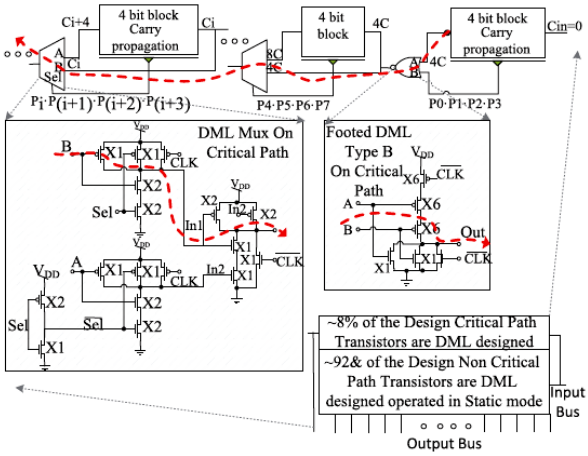


Figure 7. DML Critical Path Design Selected CSA

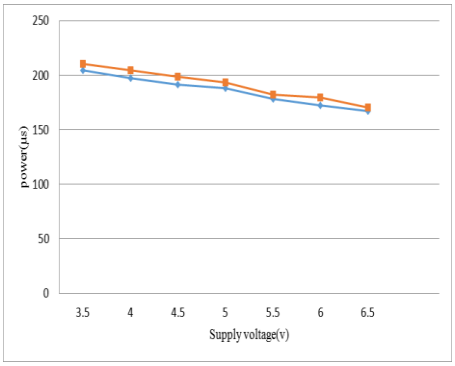
Figure 7 shows the DML implementation of the CSA's CP.The CP _ows through the _rst NOR (assuming that the carry in of the whole design is 0) and through all the MUXs of the design. The gate level implementation of the CP can be constructed with various topologies of DML: DML NOR gates are most efficiently implemented in the ``*Type A*'' topologies and NAND gates in ``*Type B*'',. The Boolean logic does not allow an ef_cient

implementation of a MUX with a NOR following a NAND or vice-versa, which is the preferred topology for DML logic design.Therefore, in the chosen topology, the CP is composed only of NANDs (where one of them is implemented using efficient ``*Type B*'' and the other one has a less optimal ``*Type A*'' structure). The last inverter in each RCA block is a headed ``*Type B*'' inverter, which maintains correct Pre-Charge phase for the CP. The sizes of the transistors in terms of minimal transistor width are shown in Figure 7. In the design, implemented in such way, only 8% of transistors will (optionally) operate dynamically, while the remaining 92% of the transistors are kept at the low energy static mode. This modular design keeps the same complexity and the same dynamic-to-static-gates ratio, as a function of the input vector's length, *N* [bits].

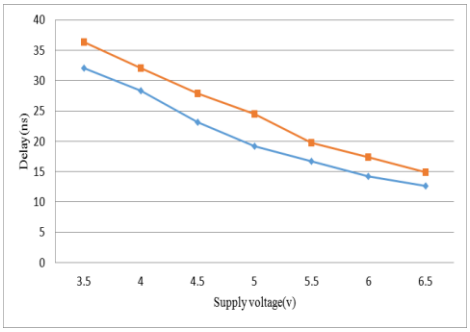
V. SIMULATION RESULTS

The modular benchmarks circuits, described in the previous section were simulated in a standard 180nm CMOS process, using the Mentor Graphics. Implementations of these methods on the benchmark CSAs were mainly examined over the E-D plain and as a function of the operating voltage and the CP's length. Note, the naming convention for the different designs and operating modes is elaborated in the preface of Section III. All energy and delay measurements are per-operation.

POWER COMPARISON AT DIFFERENT APPLIED VOLTAGE



DELAY COMPARISON AT DIFFERENT APPLIED VOLTAGE



VI. CONCLUSION

CP timing violation and energy minimization are important issues in all digital circuits. The invaluable possibilities, inherent to design with DML gates, leverage the flexibility of the design to meet CP timing along with reducing the total energy consumed by the circuit, as shown in this paper. Until now, meeting the CP timing was closely related to a rise in the consumed energy by conventional methods. In this work this paradigm is contradicted - both timing and low energy consumption requirements are met. We showed that the performance of the 180nm CSA benchmark circuit was improved by X2, while also achieving reduction of energy consumption of X2.5. Since the CSA circuit is not optimal for DML implementations, it is expected that these improvements will be even more significant for other designs.

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Recent Trends in Optical Communications

Proceedings of International Conference on Latest Trends in Electronics and Communication - ISBN: 978-93-85100-14-7

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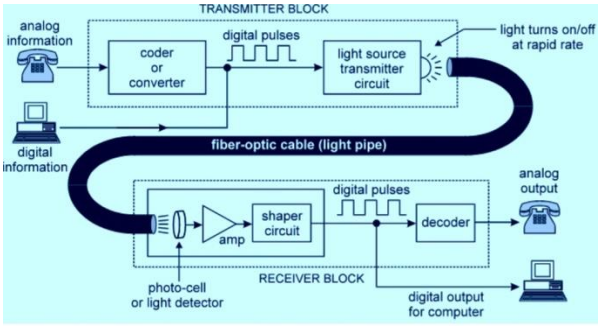
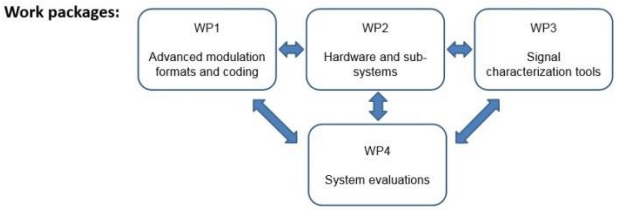
Abstract
The Recent Trends in optical communication are changing very quickly. It is quite interesting to see that the core of every large communication network carries huge traffic, to minimize this optical fiber technology was introduced, which was very unrealistic 3 decades ago. With the changes in the demand and availability of the new technologies are being added to the main optical fiber technologies. Now, there are so many emerging technologies in this list, such as the usage of optical fiber in the Military sector, in Railways, in Space communications, in telecommunications, in marine fields, in medical fields etc. In the future it will be more advanced and diversified with new applications and trends. One day it may be possible that the whole static communication network will be purely optical.

Introduction:`
Optical communication[1] is any type of communication in which light is used to carry the signal to the remote end, instead of electrical current. Optical communication relies on optical fibers to carry signals to their destinations. A modulator/demodulator, a transmitter/receiver, a light signal and a transparent channel are the building blocks of the optical communications system.
Communication systems[4] that carry information through a guided fiber called fiber optic systems.



Block Diagram: Optical Communication System
Because of its numerous advantages over electrical transmission, optical fibers have largely replaced copper wire communications in core networks in the developed world. Because, when metal wires transmit information, they create a small amount of heat. This heat causes damage to the wires over time. They often need to be replaced. For fiber optics, the data is transmitted through the use of light, which does not affect the integrity of the wire, therefore there is a much lower chance of needing to replace them

Future plans :



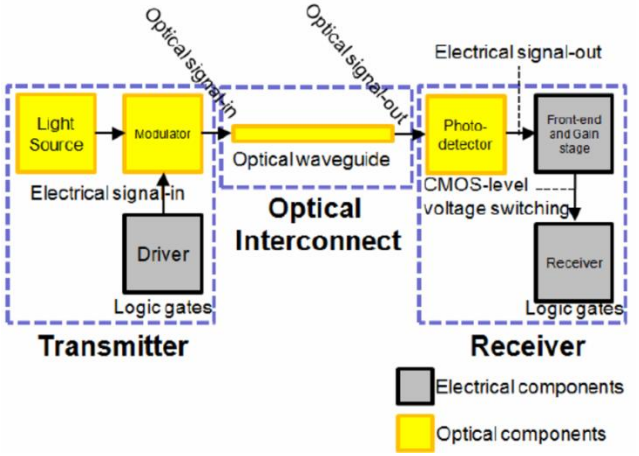
WP1: Advanced modulation and coding Coded modulation optimized for more realistic fiber transmission systems Estimation methods based on training sequences for phase/polarization tracking & timing recovery

WP2: Hardware and subsystems Novel modulation formats, e.g. pulse-position modulation combined with PS-QPSK Novel concepts for dispersion and nonlinearity mitigation, e.g. so-called factor graphs

WP3: Signal characterization tools Quantify DSP-based carrier recovery performance (coherence, noise) by benchmarking with self-homodyne method Parallelized real-time optical sampling for high bandwidth signal characterization

WP4: System evaluations Evaluation of ultralow noise, phase-sensitive amplifiers in real transmission links Adaptive optical networks; Channel estimation & optical performance monitoring

Trends in Optical Communications:
Fiber Optic Interconnects
Interconnections[3] are one of the largest and most widely used areas for fiber optic cables and assemblies. An interconnect is defined as the physical connection of two or more fixtures through which communication is possible. Interconnects range from simple, simplex patch cords to multi-channel distribution and backbone cables and virtually everything in between. Most interconnects are used for smaller, localized network or system structures, linking similar machines, complimentary devices, and/or data communications from one system to another, please see below ref [4]



Typical interconnect products are centered on a variety of industry standard cable assemblies that move, relay, or distribute data from point-to-point. Often this link, or connection, is very short for applications like switch-to-switch, switch-to-patch panel, and server-to-server. However, interconnects can also be rather long, linking two network or telecommunications closets on an inter-building campus.

Fiber Optic Networking

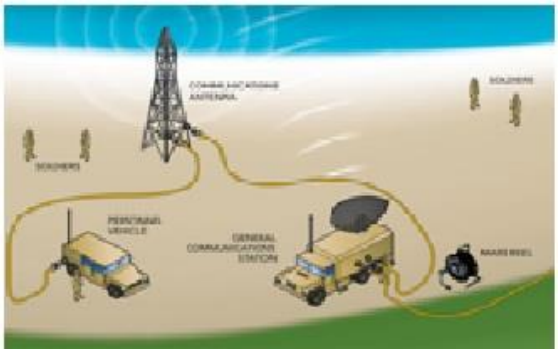
Networking is a wide ranging and loosely defined area in the industry. With all broadband and MSO applications using a network structure to deliver its signal, networking applications have a significant contribution in virtually every area. The defining difference is networking focused on the conduit and method of delivering a signal or content, rather than creation, switching, or termination.

With the increasing bandwidth requirements associated with broadband services, service providers and network operators are expanding and extending fiber optics further down line to accommodate present and future requirements. This network extension and expansion requires multiple fiber optic connectivity products in a myriad of forms. Trunk cables, distribution cables, high-density interconnect cables, and standard patch cords are just a few of the many types of products.

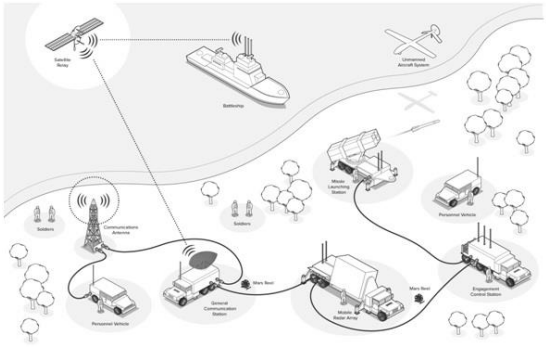
Military Fiber Optics

fiber optic products are used in a variety of military applications requiring rigorous testing and harsh environment certification to ensure reliability and performance in the field

The U.S. military uses fiber optic technology for a wide variety of air, sea, ground, and space applications. fiber optic technology has already been implemented in the Fiber. STAR project for Lockheed Martin's LM-STAR avionics test equipment module. The LM-STAR is used in the ground support system for the F-35 Joint Strike Fighter (JSF).



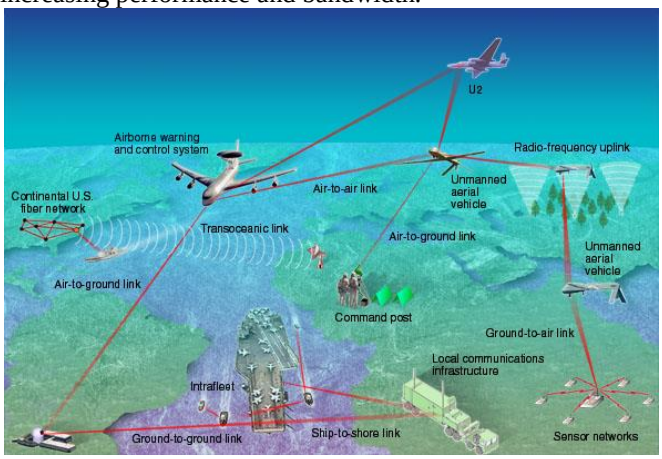
high-reliability fiber optic connectors in its military fiber optics to produce precision alignment of optical fibers. Connectors with polarization keys and key ways are manufactured to exacting tolerances to reduce radial misalignment and insertion loss. military specific MIL-DTL-38999 connectors also incorporate a bottoming surface to ensure reliable shell-to-shell connection.

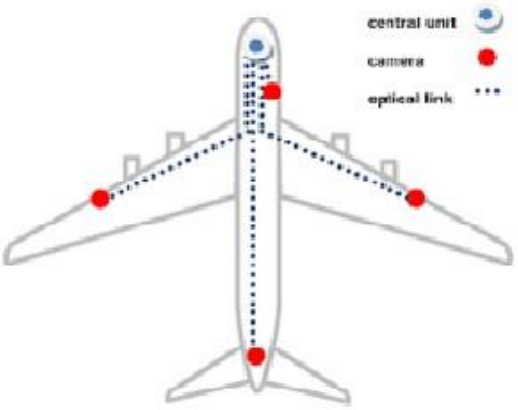


Military fiber optic applications are highly specialized, often with very specific project and scope requirements

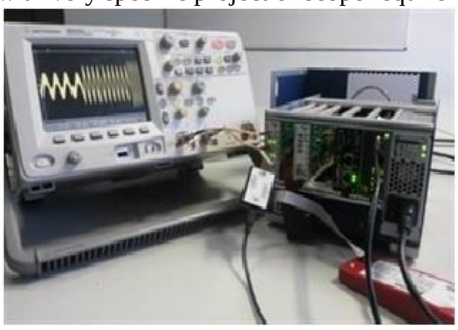
Fiber Optics for Aerospace and Avionics

Aerospace and avionics products are designed to provide maximum performance and durability in the harsh conditions and demanding environments found in most aerospace and avionic applications. The recent adoption of fiber optic technology in aerospace and avionics applications has enabled systems designers to make great strides in integrated and support-level systems by leveraging the natural characteristics of fiber, thus reducing size and weight requirements, while increasing performance and bandwidth.





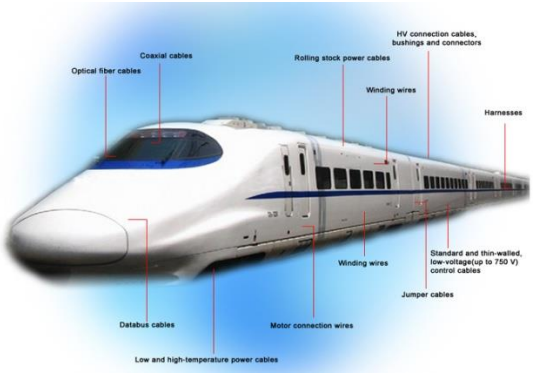
As with many military or defense type applications, most aerospace and avionics applications are highly specialized, with very specific project or scope requirements.



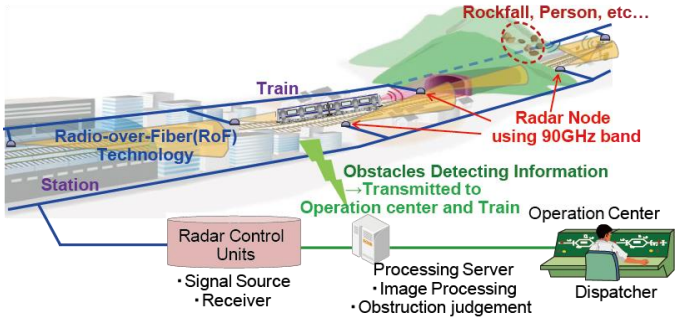
While specific requirements generally yield a more suitable finished product, it's rare to find a standard product to fit those requirements without some customization.

Fiber Optics in Railways:

To ensure safe and cost-effective train operations in the transportation industry, it is essential to monitor both traffic levels and the condition of railways. Effective railway maintenance and inspection techniques must provide information about defects in rails and wheels



In the field of railway monitoring, optical fiber sensors are receiving increasing attention. These sensors use optical fibers either as the sensing element itself, or to relay signals from a remote sensor to the signal processing electronics.



Optical fiber sensors are immune to electromagnetic interference and have low invasiveness, i.e., because they are very thin (0.9mm outer diameter), the optical fiber sensors do not cause any extra load or modifications to the structures they are attached to.

Photograph of the optical fiber laid out on the railway track for the monitoring tests

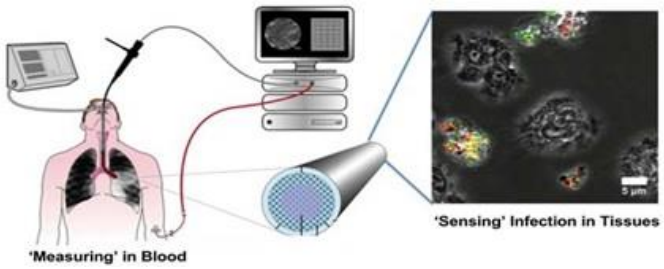
We have used a distributed optical fiber sensor to identify trains and measure dynamic loads on a rail. These trains are composed of a four-axle motor car and a four-axle trailer car, which are permanently connected. For our tests, we attached about 60m of single-mode standard optical fiber along the rail using a fast-curing epoxy adhesive

Fiber Optics for Diagnostics and Troubleshooting

Fiber optics for diagnostics and troubleshooting are used in varying capacities to test, measure, analyze, transmit, distribute, and/or simulate an optical signal with which the technician can perform procedures and processes associated with maintenance, problem solving, and calibration of equipment and/or networks.

Generally in these applications, fiber optic products are used to create loop tests or transmit signals from point-to-point (either single-point to single-point, or single-point to multiple-points).

For loop testing, commonly referred to as loopback testing, a signal is sent from a piece of equipment through a loopback or cable and returned to the source, simulating a complete network connection. This type of test allows technicians to perform function tests and internal diagnostic processes without the equipment being physically tied to an active network. This type of setup provides technicians with the advantage of easily isolating individual components for faster, more comprehensive analysis.



With signal transmission applications, technicians generally use cables (multiple types for different applications) to connect one or more pieces of equipment in a specific order or sequence to perform function testing and analysis. While many of these test and analysis processes are specific to a piece or multiple pieces of equipment, the fiber optic products used are generally based on industry standards.

wide range of diagnostic and troubleshooting products designed to provide optimal performance and flexibility for a variety of applications. From certified test cables to the Armadillo loopback and network simulation modules, Fiber optic products work very well for troubleshooting network issues for a number of reasons:

Low cost, high-bandwidth solution

Large network simulation capabilities

Pure optical signal testing allows for more precise results as opposed to optical to electrical back to optical testing

Ability to test main backbones of the network without signal conversion to electrical

Fiber Optics for Network Equipment

Fiber optics are used for a wide variety of applications in the network equipment market. Typically, fiber optics are used as internal components or interconnects associated with the finished product.

With the ever increasing bandwidth requirements of FTTx and broadband services, more and more network equipment manufacturing companies are using all-fiber transport internally and externally for switch, router, director, SAN, and NAS applications. These all-fiber systems offer a very versatile connection medium to other commonly used devices at the end user premise.

Generally, these applications use fiber cabling and interconnects designed around industry standards. However, some equipment and/or applications require fiber cabling products to be customized to ensure optimal performance or to meet space or physical constraint limitations.

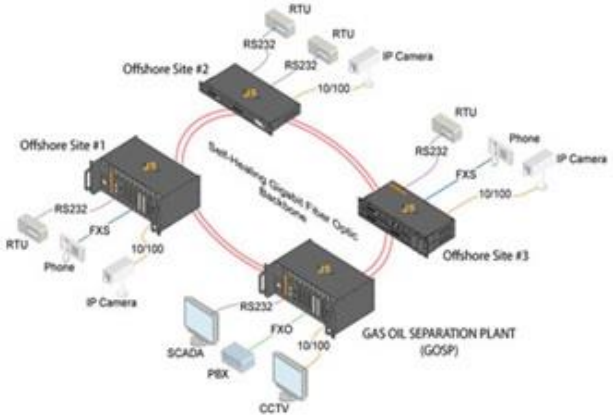
Broadcast Fiber Optics

Broadcast media utilizes outside plant, ruggedized, and harsh environment fiber optic products to support a variety of connectivity and communication requirements. These broadcast fiber optics are designed to provide multiple channel, high-bandwidth links and, in some cases, power (electrical) connections to and from cameras, trucks, and satellite links.

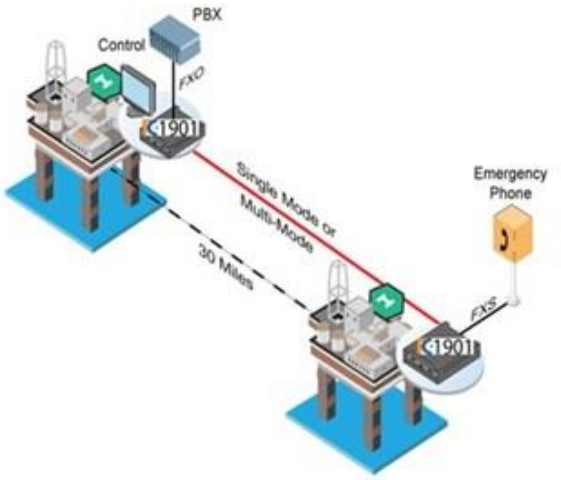
With the increasing demand for HDTV programming, broadcasters are implementing more fiber to support HDTV signal capture and transport at live sports, music, and entertainment events. Fiber is also rapidly becoming the data transmission method of choice for stadiums, arenas, and venues allowing these facilities to supply high-definition content for HDTV, video-on-demand, and broadband networks.

Fiber Optics for Oil & Gas

Fiber optics are used for a number of applications in the oil and gas markets. These markets require very specific cabling and connectivity requirements to ensure the utmost in safety, productivity, and harsh environment durability.



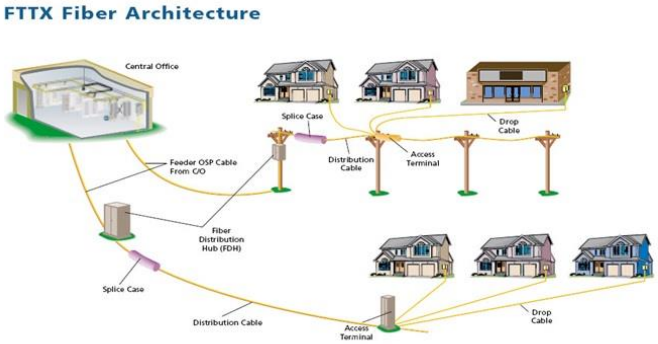
As producers of one of the most widely used consumables, oil and gas companies are rapidly expanding operations to support the increasing global demand for petroleum products. As part of this deployment, these companies are installing fiber optics to leverage the advantages offered by fiber, improving the overall performance and accuracy of their operations.



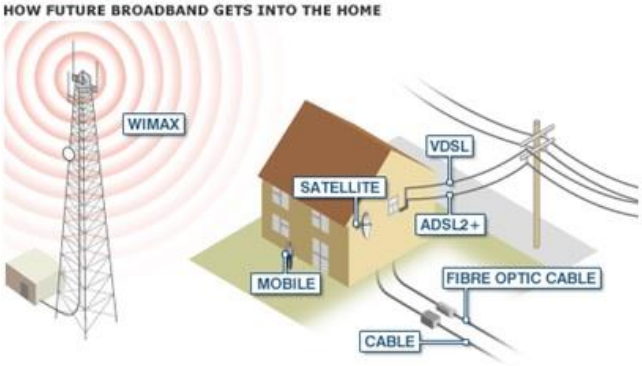
Generally, fiber optics for oil and gas are used as a communications conduit or as a sensor communication/control link. For communications, fiber optics offer a large amount of bandwidth in a compact package, saving space, weight, and install time. With sensor applications, fiber optics can provide a wide range of data about environmental conditions, oil reserve levels, and equipment performance or status.

FTTx

FTTx (Fiber To The X), most commonly covers FTTh (Fiber To The Home), FTTc (Fiber To The curb), FTTp (Fiber To The Premises), and FTTd (Fiber To The Desk) applications running from the central office or head-end to business, residential, or multi-unit dwellings.



FTTh indicates fiber network connections running from the central office to a residence, or very small multi-unit dwelling.



FTTc indicate fiber network connections to a network enclosure located at, or near, a property street/curb location, from which copper based networks generally connect to the end user

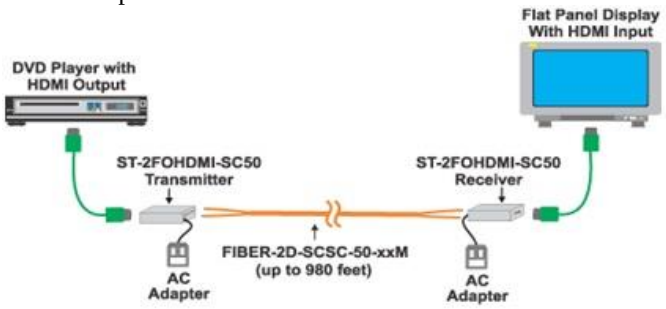
FTTp is used for business, commercial, and institutional applications where fiber network connection(s) are distributed to a campus, set of structures, or high density building with a centrally located network operations center.

FTTd indicates applications where a fiber optic connections are distributed from the central office to individual work stations or computers inside a structure, dwelling, or building.

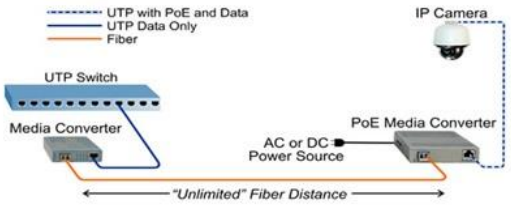
FTTx applications require a wide range of products from multi-fiber trunk cables to standard simplex cable assemblies, and most everything in between.

HDTV

HDTV (high definition television) is the broadcasting of a higher resolution format than possible with traditional analog television broadcasting. A form of digital television, HDTV is a very bandwidth intensive application requiring maximum allowable speed and data volume transfer.



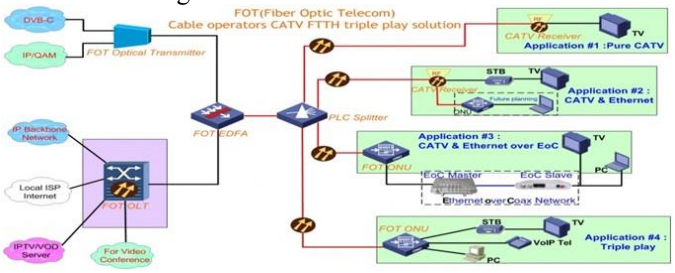
Originating with HD camera and video capture/processing equipment, television networks, service providers, and production companies are utilizing fiber optics as the support and distribution structure all the way to the subscriber premises.



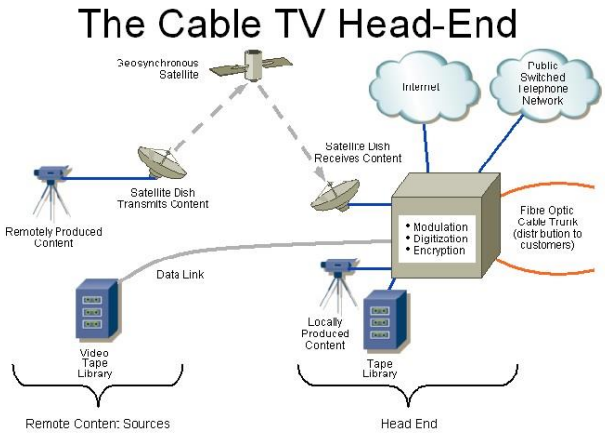
fiber optics for HDTV provide precision design, high quality manufacturing, and superior performance for a myriad of applications. From tactical fiber cables for HD camera connections to integrated premise cabling solutions.

CATV Fiber Optics

CATV (cable television) systems support multiple services including broadcast television, on-demand entertainment (video), and high speed internet access. These services are supplied via a fiber optic network to an optical node, which converts and distributes the electrical signal to subscribers via a coaxial cable connection.[4]



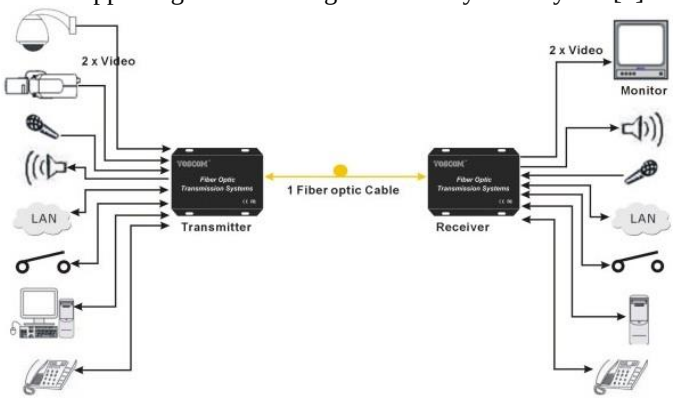
Most CATV applications will utilize both single mode and multimode signals within different areas of the network. Single Mode fiber is used to distribute signal from the central office to optical nodes, where it can be converted to multimode.[4]



CATV products include single mode and multimode distribution cables, cassette modules, coupler and splitters, ruggedized cable assemblies, and loopback test fixtures.

Data Transmission Fiber Optics

Data transmission fiber optics, simply put, is the sending and receiving of data from point-to-point via a network, thus the fundamental function of all fiber systems from small to large. Data transmission requirements range from very simple cables connecting servers or storage arrays inside a network or telecommunications system, to large multi-fiber distribution cables supporting intra-building connectivity and beyond.[4]



For smaller, localized data transmission applications, a multitude of products are available to move data from place to place. Primarily multimode, these applications use single fibers to move multiple signals over distances, usually less than 300 meters. Depending on the particular application or system requirement, data transmission cabling can take many forms from basic simplex (SX) or duplex (DX) cable assemblies to ribbon fiber distribution cables, and various combinations of customized products.

In larger data transmission applications, data transmission can be multimode, single mode, or a combination of the two, depending on bandwidth and transmission distance requirements. These applications generally use a higher volume or longer lengths of cabling, or in some case both, supporting data centers, building-to-building, campuses, and carrier network communications.

Fiber Optic Imaging

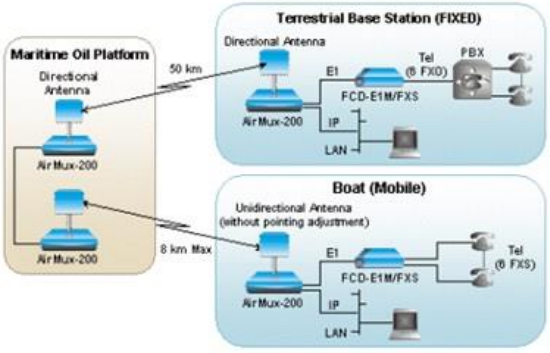
Fiber optic imaging[3] is used for a myriad of applications across several different industries. The concept of fiber optic imaging uses the optical transmission properties of fiber to transmit an image from end to end. To accomplish this, most imaging applications use an image guide or coherent bundle to collect an image of the target or subject area, then relays that information to the view end for interpretation. Imaging products are designed and fabricated to very strict tolerance, ensuring each image guide will meet or exceed your requirements. Imaging applications require individual fibers to be aligned, fused, and bundled to function correctly as an image guide. Bundling is necessary as a single fiber optic cable is only capable of reproducing a single color of varying intensity, based on what it received from the source or subject area. By bundling several, in some cases thousands of identical individual fibers, an image guide or coherent bundle relies on each fiber to focus on reproducing a single color, but collectively the bundle reproduces the target subject exactly.

Fiber optic imaging is used in a wide variety of industries including the semiconductor and medical industries. Imaging is also used for measurement and has enabled advancements in science and manufacturing previously not possible with older technologies.

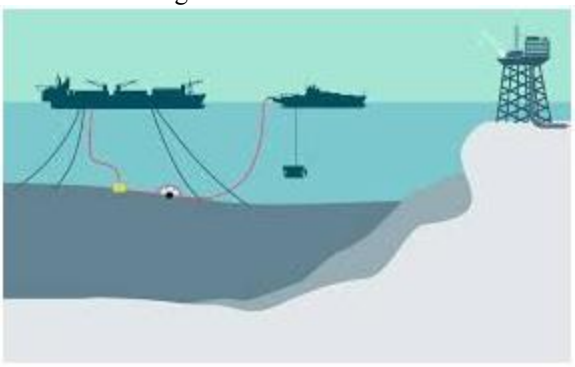
Fiber Optics for Ship to Shore Connectivity

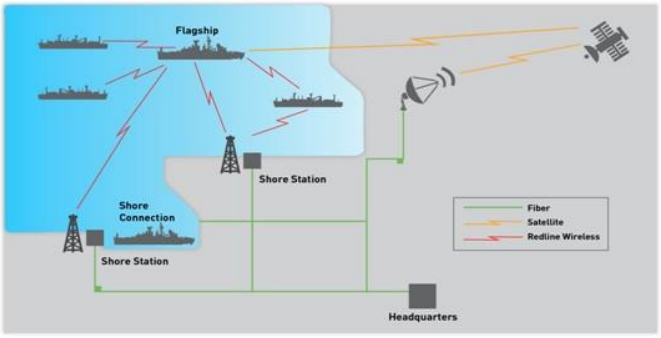
Fiber optics[2] for ship to shore applications are designed to provide data, phone, and other services to docked ships via umbilical cable to landline connection.

These connections allow high speed, high bandwidth communications to and from the vessel, without using shipboard wireless transmit/receive systems[4]



For this application, fiber optics offer some distinct advantages with size, weight, performance, and durability. These cables are typically small, light, and flexible, making it an easy product to work with while providing the performance to support present and future communications requirements.

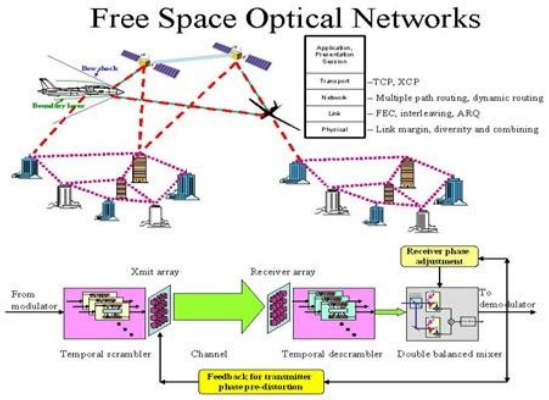




ship to shore products are designed and manufactured to withstand the rigors of daily use while performing to your specifications.

Fiber Optics for Space

Over the last several years[1], fiber optics have become increasingly popular in space environments as a medium of choice for a variety of applications. Fiber offers some distinct advantages over other mediums including:



FSO involves the optical transmission of voice, video, and data using air as the medium of transmission as opposed to fiber optic cable. Transmission using FSO technology is relatively simple. It involves two systems each consisting of an optical transceiver which consists of a laser transmitter and a receiver to provide full duplex (bi-directional) capability. Each FSO system uses a high-power optical source (e.g., laser) plus a telescope that transmits light through the atmosphere to another telescope that receives the information. At that point, the receiving telescope connects to a high-sensitivity receiver through an optical fiber. Unlike radio frequencies, the technology requires no spectrum licenses. It is easily upgradeable, and its open interfaces support equipment from a variety of vendors, which helps carriers protect the investment in their embedded infrastructures.

Conclusion

Future is uncertain, we knew the traffic is increasing, ie., we need a faster and more sophisticated infrastructure to support the demand. The age of optical communications is an era. In several ways fiber optics is a pivotal break through, and it has revolutionized the field of communication now a days, We have looked at what is optical communication, how a communication occurs and how fibers plays a vital role in various fields like telecommunications, military, medical, space and marine etc, all these are achieved because of high security, higher signal strength, immunity to interface and cross talk, lower transmission loss compared to wires or any other technology, because here the carrier used was light which has the ability to travel at higher speed with a higher signal strength and has the electric isolation, due to this the transmission rate and data transfer will be higher over miles. Though the cost of initialization was huge but the cost of maintenance was very low compared to other communications and its secure because the hacking cannot be easily performed as we can monitor the light ray to check any data loss while transmission.

A huge amount of development can be made by making further research and work on fiber optics. The trend is expected to continue in the future leading to a new generation in Fiber optical communication

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G.Sridhar received the Ph.d degree in electronics and instrumentation engineering from the SR university, India, in 2015, the M.E. degree in Control and Instrumentation from Anna University, Chennai, India, in 2012. He is currently working as a Professor in Department of ECE, Malla Reddy College of Engineering, Hyderabad. His research interests include communication and networks, wireless communication networks, Control systems, Fuzzy logic and Networks, AI, Sensor Networks.

Reversible Gates for Digital Design

D. Reddy, N. Raj and G. Ahmed

***Abstract*— Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nanotechnology and optical computing. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. The purpose of this paper is to give a frame of reference, understanding and overview of reversible gates. In this paper various logic gates and its applicability on logic design have been discussed. Also a brief framework of comparisons between various reversible circuits is presented on the basis of various parameters.**

***Index Terms*—Reversible, Quantum cost, logic, optical computing, garbage**

I. Introduction

Reversible computing is a model of computing where the computational process to some extent is reversible, *i.e.*, time-invertible. In a model of computation that uses deterministic transitions from one state of the abstract machine to another, a necessary condition for reversibility is that the relation of the mapping from (nonzero-probability) states to their successors must be one-to-one. Reversible computing is a form of unconventional computing. The other method of computational process is conventional computing in which we use logical gates.

The disadvantage of unconventional computing is physical architecture is not present. In conventional computing we can go through transistor level. In conventional computing we cannot reverse the circuits but in unconventional it is possible and number of gates used is less.

II. Reversible circuits

The Reversible Logic The n-input and k-output Boolean function f(x1, x2, x3… xn) (referred to as (n, k) function) is called reversible if:

1) The number of outputs is equal to the number of inputs

2) Each input pattern maps to unique output patterns

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A. Reversible Logic Gate

Reversible Gates are circuits in which number of outputs is equal to the number of inputs .And there is a one to one mapping between the vector of inputs and outputs. It helps to determine the outputs from the inputs as well as helps to uniquely recover the inputs from the outputs.

B. Ancilla inputs/Constant inputs

This can be defined as the number of inputs that are to be maintain constant at either 0 or 1 in order to synthesize the given logical function.

C. Garbage Output

Additional inputs or outputs can be added so as to make the number of inputs and outputs equal whenever required. This also indicates the number of outputs which are not used in the synthesis of a given function. In certain cases these become mandatory to attain reversibility. Therefore garbage is the number of outputs added to make an n-input k-output function ((n; k) function) reversible. Constant inputs are used to denote the present value inputs that are added to an (n; k) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs. Input + constant input = output + garbage.

D. Quantum Cost

Quantum cost may be defined as the cost of the circuit in terms of the cost of a primitive gate. It is calculated by the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1.

III. Reversible gates

Some of the important reversible logic gates are:

A. NOT Gate

The simplest Reversible gate is NOT gate and is a 1*1 gate. The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Fig. 1.

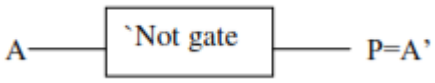

Fig. 1: NOT Gate

B. Feynman Gate

The Feynman gate which is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out purposes.

The inputs (A, B) and outputs P=A, Q= A XOR B. It has quantum cost one.

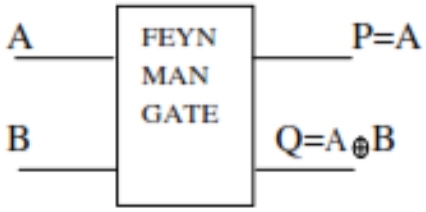

Fig. 2: Feyman Gate

The Equations are:
P=A
Q=A⊕B

Table 3: Truth table of Feyman Gate

Inputs		Outputs	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

C. Toffoli Gate

Fig 3 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are Fig 3 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB ⊕C. Quantum cost of a Toffoli gate is 5.

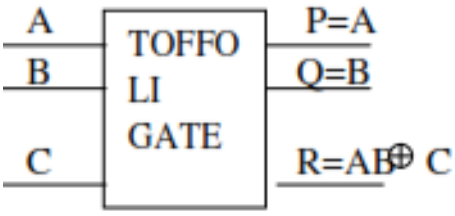

Fig. 3: Toffoli Gate

Table 3: Truth table of Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

D. Fredkin Gate

Fig 4 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5.

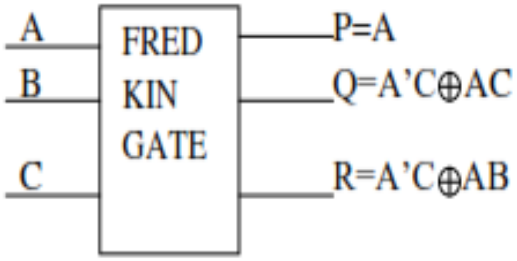

Fig. 4: Fredkin Gate

Table 4: Truth table of Fredkin Gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	0	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

E. Peres Gate

Fig 5 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4.

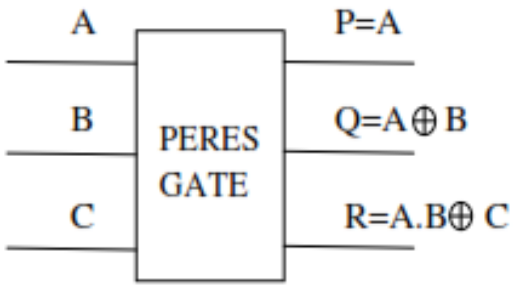

Fig. 5: Peres Gate

Table 5: Truth table of Peres Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

IV. COMPARATIVE STUDY

To Various reversible gates and different circuits associated with these gates are discussed here. And also comparisons have been made among the existing circuit in terms of various parameters such as quantum cost, garbage output, constant input, gate count and delay. Comparison between existing reversible gates is shown in Table 6.

Table 5: Comparison between Reversible Gates

Reversible gates	Quantum cost	Types
Feynman gate	1	2*2
Toffoli gate	5	3*3
Fredkin gate	5	3*3
Peres gate	4	3*3
TR gate	6	3*3

V. APPLICATIONS OF REVERSIBLE GATES

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance.

It include the area like

- Low power CMOS.
- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.
- Design of low power arithmetic and data path for digital signal processing (DSP).
- Field Programmable Gate Arrays (FPGAs) in CMOS technology.

The potential application areas of reversible computing include the following

- Nano computing
- Bio Molecular Computations
- Laptop/Handheld/Wearable Computers
- Spacecraft
- Implanted Medical Devices
- Wallet “smart cards”
- “Smart tags” on inventory

Prominent application of reversible logic lies in quantum computers. Quantum gates perform an elementary unitary operation on one, two or more two–state quantum systems called qubits. Any unitary operation is reversible and hence quantum networks also.

Quantum networks effecting elementary arithmetic operations cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible). Thus, Quantum computers must be built from reversible logical components.

VI. CONCLUSION

The reversible circuits form the basic building block of quantum computers. This paper presents the primitive reversible gates which are gathered from literature and this paper helps researchers/designers in designing higher complex computing circuits using reversible gates. The paper can further be extended towards the digital design development using reversible logic circuits which are helpful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics.

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Analyze on Path Loss Models of Spectrum Sensing in Cognitive Radio Networks

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***Abstract*—Cognitive Radio networks provide advancement to thewireless generations. Due to the fixed spectrum allocation policy, a wider portion of the spectrum is underutilized in many areas. Spectrum sensing adds intelligence to Cognitive Radios that dynamically identifies the spectrum holes. Many spectrum sensing algorithms are proposed in literature to sense the spectrum holes in a noisy environment. But, there are several challenges that are to be considered in simulating the algorithms in a real-time channel. In this paper, a review of various issues of spectrum sensing is discussed**

Keywords—Co-operative spectrum sensing, path loss, fading, noise uncertainty.

I INTRODUCTION

The concept of cognitive radio was first introduced by Joseph Mitola III and Gerald Q. Maguire, Jr in 1999. The radio frequency spectrum contains electromagnetic radiation with frequencies between 3000 Hz and 300 GHz. The fixed spectrum allocation prevents frequencies that are rarely used by unlicensed users, even when their transmissions would not interfere at all with primary user's usage. Cognitive radio is the most intelligent means of facilitating effective usage of spectrum holes. This communication system senses its surrounding environment, and adapts itself to changes in the incoming RF stimuli by making suitable changes in carrier frequency, transmission power and other parameters.

Spectrum sensing is the primary function of Cognitive Radio [1]. This technique identifies the spectrum holes. The CR then performs spectrum management to select the most appropriate channel meeting with the secondary user requirements. The CR then calculates the spectrum mobility to predict how long the spectrum holes are likely to remain available for use to the secondary users. Finally, spectrum sharing is done
to distribute the spectrum holes fairly among the secondary users in accordance with usage cost.A preemptory challenge in spectrum sensing is to sense in very low SNR regions. Several sensing techniques have been proposed in literature for enhanced utilization of the spectrum band.In paper [2] [3] and [4] some of the spectrum sensing techniques are- Energy detection technique, Matched filter Cyclo-stationary techniques. Energy detection technique [1] is a simple blind detection technique. It does not consider the structure of the signal. But its performance is susceptible to uncertainty in noise power.

Matched filtering [1] requires shorter detection time compared to Energy detection technique. It gives best results when secondary user has a prior knowledge of primary user signal. It maximizes output SNR for a given signal. But it fails in the scenario where the information from the primary user is unknown. Cyclo-stationary detection [1] is a method which utilizes the cyclic features of the signal. Cyclo-stationary signals exhibit the features of periodic statistics and spectral correlation, a characteristic which is not found in stationary noise and interference. Thus, cyclo-stationary feature detection is robust to noise uncertainties and performs better than energy detection in low SNR regions. But this method uses high number of computations and longer sensing time.

A major drawback of the Energy Detection method is that it requires information on the noise power but experiences noise uncertainty. Covariance detection [5] does not require prior information about the signal and noise power as this detector exploits space-time signal co-relation. The signal and noise generally have different co-variances which can be used to estimate the presence of primary user. However, there is uncertainty in its performance under fading channels.

The presence of primary user can also be formulated with unknown noise levels. Entropy detection [6] is a simple technique in which the entropy of the received signal is compared to a suitable threshold value to determine the presence of a primary user. This method achieves a good performance in low SNR regions.

The other sections of the paper are organized as follows: Section II presents classification of spectrum sensing techniques. Section III emphasizes on challenges faced by Spectrum Sensing and finally section IV closes with conclusions.

II CLASSIFICATION OF SPECTRUM SENSING TECHNIQUES

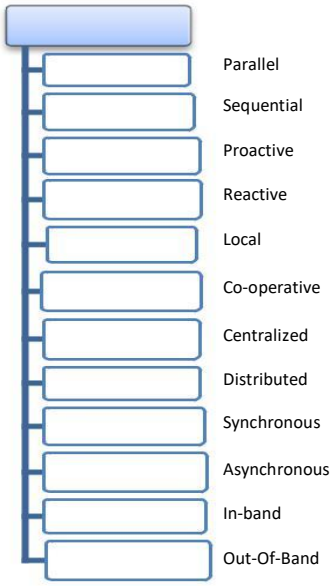

Fig 1: *Classification of Spectrum Sensing Techniques*

Fig 1 depicts the Classification of Spectrum Sensing Techniques

To begin with Parallel Sensing**,** if there are N frequency sensing channels, it senses all the N channels at the same time. It requires N sensing devices. Whereas, sequential sensing senses the N channels, one at a time. It might be difficult in finding an empty channel to carry out sequential sensing.

Another sensing technique is Proactive sensing where the Performs sensing operation even though it does not transmit immediately. In comparison, reactive sensing technique is more energy efficient than proactive sensing. In this technique, CR performs the sensing operation only if it has to perform receive or transmit operation. However, the time taken to find an empty channel is higher than proactive sensing.

In Local Sensing**,** each CR senses on its own and uses its data to make a decision on channel state, whether idle or busy. Butin Cooperative Sensing, CR shares its sensing information with others and utilizes the sensing results of others to make decision. This method is a solution to hidden node or fading channelproblem

Centralized Sensing is a technique where a Central node or Fusion center collects the sensing information and then makes a decision on channel state on whether it is idle or busy. If the Central node fails, the whole system collapses .It is called Single Sensing Point of Failure. On the contrary, Distributed (Decentralized) technique is when each CR makes its own decision on the channel state. This technique is more efficient than Centralized sensing.

On the basis of clock schedule, sensing is divided into synchronous and asynchronous. In Synchronous sensing, all The CR's have a common time schedule to sense the channel. On the other hand, asynchronous sensing is performed when sensing is done to sense all the other channels other than the channel it is at present, to find an available channel in case of presence of a primary signal.

III. CHALLENGES OF SPECTRUM SENSING

The first part of this section elaborates few path loss models which explain the path loss which occurs during the propagation of the signal from the transmitter to the receiver.

The following models being:

- Friis Free Space propagation Model
- Log Distance Path Loss or Log Normal Shadowing Model
- Empirical models- Hata – Okumura Model, COST231 Extension to Hata Model, COST 231-Walfish-Ikegami Model, ErcegModel

The second half emphasizes on signal fading. This phenomenon occurs on an encounter of a transmitted signal with an obstacle. Several important models of fading such as Rayleigh fading model, Rician fading model and Nakagamifading model are highlighted.

PathLoss

Path loss is used to estimate the signal loss between the transmitted and received signal when a clear path lies in-betweenthem. It is also used to measure the attenuation loss due to various environmental factors between the received and transmitted signal. The commonly used models for path loss modeling are:

A. Path Loss Models

Friis Free Space Propagation Model

This model explains path loss in the channel. Propagation loss [7] is the loss which occurs during the transmission of thesignal.

In this model, the received power decreases in the power of 2, when the distance from the transmitting antenna increases.

The received power is given by [7]:

$$P_r \alpha \frac{1}{d^2} \quad (1)$$

$$\text{Pr(d)}=pt\,\frac{GtG\lambda^2}{(4\pi d)^2 2L} \quad (2)$$

p_r(d)=Received signal power in Watts.
p_t= Transmitted signal power in Watts
$G_t G_r$ = Gains of transmitter & receiver antennas with respectto an isotropic antenna.
λ= Wavelength of carrier signal in meters.
L = Losses other than propagation losses like loss at the antenna, transmission line attenuation, filters etc.
This model is applicable only in the far-field of the Transmitting antenna. Propagation loss is the difference between the transmitted and received power of the antenna. Itis given by [7]

$$p_L\text{(db)} = -10\log10\left(\frac{\lambda^2}{4\pi d}\right) = +20\log10\left(\frac{4\pi d}{\lambda}\right) \quad (3)$$

If we substitute lambda =c/f, we see that the propagation lossis more when the frequency is more.

$$\lambda = c/f \quad (4)$$

$$\text{Pr(d)}=pt\,\frac{GtG\lambda c^2}{(4\pi d f)^2 L} \quad (5)$$

It is seen that the received power decreases at the rate of 20Db for every increase in 10 λ.

Log Distance Path Loss or Log Normal Shadowing Model

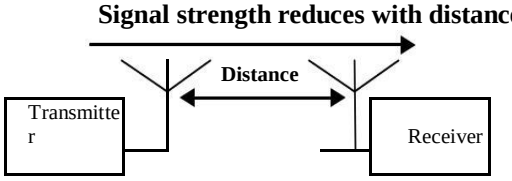

Fig 2 is the log distance path loss model

Fig 2 is the log distance path loss model which explains pathloss and shadowing. Unlike the traditional path loss model which is restricted to a clear path between the transmitter andthe receiver, this model can measure a propagation loss for a widerenvironment [7].The loss in power while moving distance d0 to any distance d is given by [7]:

$$PL_{do} \rightarrow d^{(db)} = \text{PL(do)} + 10n\log\left(\frac{d}{do}\right) + \chi \quad p_f \leq d_o \leq \text{d} \quad (6)$$

PL(d0) = Path Loss in dB at distance d0
PL (d>d0) = Path Loss in dB at a distance d

n = It is called the Path Loss exponent.

χ = A zero-mean Gaussian distributed random variable (in dB) which has the standard deviation – σ. This variable is used only if there is a shadowing effect. The log of this Normal (Gaussian)-variable is known as the "Log-Normal" fading.
If the shadowing effect is neglected, the Path Loss is a straight-linewhen the shadowing effect is added, a standard deviation– σ is also added to the equation
Empirical models

Hata – Okumura Model

The Okumura model is a universally used model. Almost all the propagation models are derived from this model. This model is useful for frequencies up to 3000 MHz.The maximum distance between transmitter and receiver is 100 kmand the receiver height between 3 m and 10 m.
The path loss in Okumura model is given by [8]:
L50(db)=LF + Amu(f, d)- G(the) – G(hre) -G_{area} (7)
In this equation,
L50 is the median value of propagation loss
LF= path loss.
G(hte)- antenna gain factor
G(hre)-receiver gain factor.
hte and hre-heights of base station and the receiver.
Amu(f,d) -median attenuation factor.

COST 231 Extension to Hata Model

This model functions as a radio propagation model. This model is an extension to Hata Model to 2GHz and is as follows [8]:
L = 46.3+33.9log f- 13.82 log hB- a(hR) + [44.9-6.55 log hB]log d+ C (8)
For rural environments
A(hR)= (1.1 log f -0.7) hR – (1.56 log f – 0.8) (9)

$$C=\begin{cases} 3\ db\ for\ rural\ and\ suburban\ areas \\ 0db\ for\ metropolitan\ areas \end{cases}$$

Where,
L(dB) is a measure of median path loss.
F(MHz) is the frequency of transmission signal.
HB(m) is the antenna height in base station.
D(km) is the link distance.
HR(m) is mobile station antenna height.
A(hr) is the antenna height correction factor of mobile station.

COST 231-Walfish-Ikegami Model

This model is obtained from the combination of the models ofJ. Walfisch and F. Ikegami. It was later developed by theCOST 231 model. It is now known as Empirical COSTWalfisch-Ikegami Model. The model takes into consideration, only the buildings in the vertical plane between the transmitter and the receiver. The accuracy of this empirical model is higher in urban environments because of the multiple diffractions over the roof-tops. The main parameters of the
Model are:

- Frequency f= 800-2000 MHz
- Transmitter height (hTX)= 4-50 m
- Receiver height (hRX) =1-3 m
- The Distance between transmitter and receiver d= 20-5000m
- Mean value of all the building heights= hROOF
- Mean value of street width= w
- Mean value of building separations =b

This model considers two situations: LOS-Line of Sight andNLOS-Non Line-Of Sight.
LOS Situation This is similar to the free space loss condition and is given by [9]

$$lp = 42.6 + 26\log\left(\frac{d}{Km}\right) + 20\log\left(\frac{f}{MHz}\right) \quad (10)$$

NLOS Situation the NLOS equations are more complicated.
The loss is given below:
Here,
The free space loss=l0
Multiple screen diffraction loss=lmsd
Rooftop-to-street diffraction loss=lrts:
The free space loss is given by [9]:

$$l0 = 32.44 + 20\log\frac{f}{MHZ} + 20\log\frac{d}{km} \quad (11)$$

The lrts equation determines the loss which occurs on the wave coupling where the receiver is located.

$$I_{rts} = -16.9 - 10\log\frac{w}{m} + 10\log\frac{f}{MHz} + 20\log\frac{h_{roof-h_{RX}}}{m} + I_{ori} \quad (12)$$

With

$$I_{ori} = \begin{cases} -10 + 0.35\frac{\varphi}{deg} & for\ 0 \le \varphi < 35^{\circ} \\ 2.5 + 0.075\left(\frac{\varphi}{deg} - 35\right) & for\ 35^{\circ} \le \varphi < 35^{\circ} \\ 4.0 - 0.114\left(\frac{\varphi}{deg} - 35\right) & for\ 55^{\circ} \le \varphi < 90^{\circ} \end{cases} \quad (12)$$

The orientation loss lori[9] is the correction term determined from the calibration with measurements COST 231 modified this equation for base station antenna heights below the rooftop level given by the following equations[9].
building separation= b

$$I_{msd} = I_{bsh} + K_a + K_d\log\frac{d}{km} + K_f\log\frac{f}{MHz} - 9\log\frac{b}{m} \quad (13)$$

$$K_a \begin{cases} 54 - 0.8\frac{h_{TX-h_{roof}}}{m} & for\ h_{TX} > h_{roof} \\ 54 - 0.8\frac{h_{TX-h_{roof}}}{m}\frac{\frac{d}{km}}{0.5} & for\ d \le 0.5km\ and\ h_{TX} \le h_{roof} \end{cases} \quad (14)$$

$$K_d = \begin{cases} 18 & for\ h_{TX} > h_{roof} \\ 18 - 15\left(\frac{h_{TX-h_{roof}}}{h_{Roof-h_{RX}}}\right) & for\ \ h_{TX} < h_{roof} \end{cases} \quad (15)$$

$$Kf = -4 + \begin{cases} 0.7\left(\frac{\frac{d}{MHZ}}{925} - 1\right) & formedium\ sized\ city\ and\ suburbs \\ 1.5\left(\frac{\frac{d}{MHz}}{925} - 1\right) & for\ metroplitan\ areas \end{cases} \quad (15)$$

The factors $K_d$and K_f balances the relation between the multi-screen diffraction loss vs distance/frequency.

Erceg Model

This model was developed from the results of an experiment conducted by AT&T Wireless services in the United States in95 microcells at 1.9GHz [9]

Here path loss PL is given by [10]:

$$PL_{(db)} = 20\log10\left(\frac{4\pi d_o}{\lambda}\right) + 10\gamma\log10\left(\frac{d}{\lambda d}\right) \text{ for } d > d0 \quad (16)$$

Here,
λ = wavelength in meters
γ= is the path-loss exponent
$\gamma = a - bh_{(b)} + dh_{(b)}$ (17)
h(m)=height of base station
The above model is valid for all frequencies up to 2 GHz and for receiver antenna heights up to 2 m. For

frequencies and antenna heights which lies in the range of 2m to 10m, the following correction terms are as follows in [10]:

PLmodified= PL +ΔPLf +ΔPLh (18)

ΔPLf=6log10(f/2000) (19)

ΔPLh=-10.8log10(h/2) for categories A and B (20)

ΔPLh=-20log10(h/2) for C (21)

ΔPLf = frequency

ΔPLh= the receiver antenna height correction term.

Fading

If the transmitted signal encounters any obstruction in its propagating medium (for eg: buildings), it gets scattered, reflected, diffracted or undergoes absorption. This is called as slow fading/ long term fading.

Multipath Fading and time dispersal

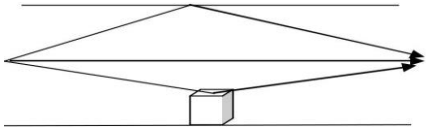

Fig 3: Transmission of signal via multiple paths

Fig 3 represents transmission of signal via multiple paths. in wireless communication networks. Sometimes uncertainties in received signal strength arises due to channel fading which may wrongly deduce that the primary system is located out of the secondary user's interference as the primary signal maybe undergoing a deep fade or might be shadowed by obstacles. Therefore, cognitive radios are supposed to be more sensitive to distinguish a faded or shadowed primary signal from white space. Since noise power is not constant, calculation of noise power is difficult

Noise Uncertainity

One of the important challenges in spectrum sensing is the impact of uncertainty in measurement of channel noise. The inaccurate estimation of noise power is termed as noise uncertainty. The signal to noise ratio gets severelydegraded due to its presence. The detection of spread spectrum signals. By a wideband energy detector becomes far more difficult because the SNR which is required for detection becomes dependent on noise uncertainty but independent of its observation interval. To overcome noise uncertainty, multiple antennas are used [11].Noise uncertainty is given asfollows [12]

$$\gamma_{min} = \frac{p_p L(D+R)}{N} \quad (22)$$

Where

N= Noise power.

Pp=Transmitted power by the primary user.

D= Interference Range

R= Maximum distance between primary transmitter and its

Receiver

B.Fading Models

Rayleigh Fading

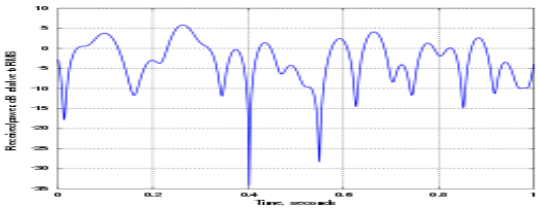

Fig 3: *Rayleigh plot of time Vs Received power in Db*

In Fig 3, deep fading appears in every half a wavelength.Thephenomenon of Rayleigh Fading [13] arises as result of multipath fading. A moving antenna receives a large number ofwaves due to scattering and reflection. Due to wavecancellation effects, the received power as seen from theantenna becomes a variable dependent on the location of theantenna.

Rician Fading

Rician fading model [14] is similar to that for Rayleigh fading.But in Rician fading, a strong dominant component is observed. This dominant component can for example, be the Line-of-sight wave. Refined Rician models are explained asfollows:

- The dominant wave can be considered as a phasorsum of two or more dominant signals, e.g. the line of-sight and a ground

reflectionthe dominant wave can also undergo shadowattenuation. This is a supposition in the modelling ofsatellite channels.In addition to the dominant component, the mobile antennareceives reflected and scattered waves.

Nakagami Fading

Nakagamifading [15] does occur for multipath scattering having large delay-time spreads. In this model, the power density function of signal amplitude which is exposed to mobile fading is demonstrated.

- If the signal is Nakagami distributed, the instantaneous power of the signal is gamma distributed.
- The Nakagami parameter *m* is called the 'shape factor'. If*m* = 1, Rayleigh fading is recovered, the signal having an exponentially distributed instantaneous power
- For *m* > 1, the fluctuations in the strength of thesignal reduce.

IV CONCLUSION

The broad classification of spectrum sensing techniques is presented. The detection performance of the spectrum sensing techniques can be improved by increasing the number of cognitive users in co-operative sensing. Butthere are several issues that are to be considered whilesimulating multi node sensing. The various path lossmodels for transmission between transmitter and receiver are also discussed .Finally, the fading channels and the effect of noise uncertainty are explored.

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AREA-AWARE AND SAFER CARDS

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Abstract— **In this paper, we report on a new approach for improving security and privacy in certain RFID applications whereby location or location-related information (such as speed) can serve as a legitimate access context. Examples of these applications include access cards, toll cards, credit cards, and other payment tokens. We show that location awareness can be used by both tags and back-end servers for defending against unauthorized reading and relay attacks on RFID systems. On the tag side, we design a location-aware selective unlocking mechanism using which tags can selectively respond to reader interrogations rather than doing so promiscuously. On the server side, we design a location-aware secure transaction verification scheme that allows a bank server to decide whether to approve or deny a payment transaction and detect a specific type of relay attack involving malicious readers.**

The premise of our work is a current technological advancement that can enable RFID tags with low-cost location (GPS) sensing capabilities. Unlike prior research on this subject, our defenses do not rely on auxiliary devices or require any explicit user involvement.

Keywords- Context Recognition,RFID, Mobile Payment System, Relay Attacks, Location Sensing.

I. INTRODUCTION

Low cost, small size and the ability of allowing computerized identification of objects make Radio Frequency Identification (RFID) systems increasingly ubiquitous in both public and private domains. Prominent RFID applications supply chain management (inventory control), e-passports, credit cards, driver's licenses, vehicle systems (toll collection or car key), access cards (building, parking or public transport), and medical implants. NFC, or Near Field Communication, is yet another upcoming RFID technology that allows devices, such as smart phones, to have both RFID tag and reader functionality. In particular, the use of NFC-equipped mobile devices as payment tokens (such as Google Wallet) is considered to be the next generation payment system and the latest buzz in the financial industry.

A typical RFID system consists of tags, readers, and/or back-end servers. Tags are miniaturized wireless radio devices that store information about their corresponding subject. Such information is usually sensitive and personally identifiable. For example, a US e-passport stores the name, nationality, date of birth, digital photograph, and (optionally) fingerprint of its owner. Readers broadcast queries to tags in their radio transmission ranges for information contained in tags and tags reply with such information. The queried information is then sent to the server (which may coexist with the reader) for further processing and the processing result is used to perform proper actions (such as updating inventory, opening gate, charging toll or approving payment).

Due to the inherent weaknesses of underlying wireless radio communication, RFID systems are plagued with a wide variety of security and privacy threats. A large number of these threats are due to the tag's promiscuous response to any reader requests. This renders sensitive tag information easily subject to unauthorized reading. Information (might simply be a plain identifier) gleaned from a RFID tag can be used to track the owner of the tag, or be utilized to clone the tag so that an adversary can impersonate the tag's owner.

Promiscuous responses also incite different types of relay attacks. One class of these attacks is referred to as "ghostand-leech". In this attack, an adversary, called a "leech," relays the information surreptitiously read from a legitimate RFID tag to a colluding entity known as a "ghost." The ghost can then relay the received information to a corresponding legitimate reader and vice versa in the other direction. This way a ghost and leech pair can succeed in impersonating a legitimate RFID tag without actually possessing the device.

A more severe form of relay attacks, usually against payment cards, is called "reader-and-ghost"; it involves a malicious reader and an unsuspecting owner intending to make a transaction in this attack, the malicious reader, serving the role of a leech and colluding with the ghost, can fool the owner of the card into approving a transaction which she did not intend to make (e.g., paying for a diamond purchase made by the adversary while the owner only intending to pay for food). We note that addressing this problem requires secure transaction verification, i.e., validation that the tag is indeed authorizing the intended payment amount.

The feasibility of executing relay attacks has been demonstrated on many RFID (or related) deployments, including the Chip-and-PIN credit card system, RFID assisted voting system, and keyless entry and start car key system. With the increasingly ubiquitous deployment of RFID applications, there is a pressing need for the development of security primitives and protocols to defeat unauthorized reading and relay attacks. However, providing security and privacy services for RFID systems presents a unique and formidable set of challenges. The inherent difficulty stems

partially from the constraints of RFID tags in terms of computation, memory and power, and partially from the unusual usability requirements imposed by RFID applications (originally geared for automation). Consequently, solutions designed for RFID systems need to satisfy the requirements of the underlying RFID applications in terms of not only efficiency and security, but also usability.

In this paper, we report on our work on utilizing location information to defend against unauthorized reading and relay attacks in certain applications. We notice that in quite some applications, under normal circumstances, tags only need to communicate with readers at some specific locations or while undergoing a certain speed. For example, an access card to an office building needs to only respond to reader queries when it is near the entrance of the building; a credit card should only work in authorized retail stores; toll cards usually only communicate with toll readers in certain fixed locations (toll booths) or when the car travels at a certain speed.

Hence, location or location-specific information can serve as a good means to establish a legitimate usage context specifically; we present two location-aware defense mechanisms for enhanced RFID security and privacy. First, we show that location information can be used to design selective unlocking mechanisms so that tags can selectively respond to reader interrogations. That is, rather than responding promiscuously to queries from any readers, a tag can utilize location information and will only communicate when it makes sense to do so, and thus, raising the bar even for sophisticated adversaries without affecting the RFID usage model. For example, an office building access card can remain locked unless it is aware that it is near the (fixed) entrance of the building. Similarly, a toll card can remain locked unless the car is at the toll booth and/or it is traveling at a speed range regulated by law.

II. BACKGROUND AND PRIOR WORK

All of these approaches, however, require the users to carry an auxiliary device. In Blocker Tag, a special RFID tag, called "Blocker," is used to disrupt the identification process used by the reader to identify tags in proximity. RFID Enhancer Proxy and RFID Guardian are special RFID-enabled devices that could be implemented in a PDA or cellphone. They are assumed to come with greater computation capability and, thus, can perform more sophisticated interactions with readers, on behalf of tags, for various security purposes. In Vibrate-to-Unlock, a user unlocks his/ her RFID tags by authenticating to these tags through a vibrating phone. However, such an auxiliary device (required by above schemes) may not be available at the time of accessing RFID tags, and users may not be willing to always carry these devices.

Cryptographic protocols: Cryptographic reader -to-tag authentication protocols could also be used to defend against unauthorized reading. However, due to their computational complexity and high-bandwidth requirements, many of these protocols are still unworkable even on high-end tags. There has been a growing interest in the research community to design lightweight cryptographic mechanisms. However, these protocols usually require shared key(s) between tags and readers, which is not an option in some applications.

Distance bounding protocols. These protocols have been used to thwart relay attacks. A distance bounding protocol is a cryptographic challenge-response authentication protocol. Hence, it requires shared key(s) between tags and readers as other cryptographic protocols. Besides authentication, a distance bounding protocol allows the verifier to measure an upper bound of its distance from the prover. (We stress that normal "non-distance-bounding" cryptographic authentication protocols are completely ineffective in defending against relay attacks.) Using this protocol, a valid RFID reader can verify whether the valid tag is within a close proximity thereby detecting ghost-and leech and reader-and-ghost relay attacks. The upper bound calculated by an RF distance bounding protocol, however, is very sensitive to processing delay (the time used to generate the response) at the prover side. This is because a slight delay (of the orders of a few nanoseconds) may result in a significant error in distance bounding. Because of this strict delay requirement, even XOR- or comparison-based distance bounding protocols are not suitable for RF distance bounding since simply signal conversion and modulation can lead to significant delays. By eliminating the necessity for signal conversion and modulation, a very recent protocol, based on signal reflection and channel selection, achieves a processing time of less than 1ns at the prover side. However, it requires specialized hardware at the prover side due to the need for channel selection. This renders existing protocols currently infeasible for even high-end RFID tags.

Context -aware selective unlocking: "Secret Handshakes" is a recently proposed interesting selective unlocking method that is based on context awareness. To unlock an accelerometer-equipped RFID tag using Secret Handshakes, a user must move or shake the tag (or its container) in a particular pattern. For example, the user might be required to move the tag parallel with the surface of the RFID reader's antenna in a circular manner. A number of unlocking patterns were studied and shown to exhibit low error rates. A central drawback to Secret Handshakes, however, is that a specialized movement pattern is required for the tag to be unlocked. This requires subtle changes to the existing RFID usage model. While a standard, insecure RFID setup only requires users to bring their RFID tags within range of a reader, the Secret Handshakes approach requires that users consciously move the tag in a certain pattern.

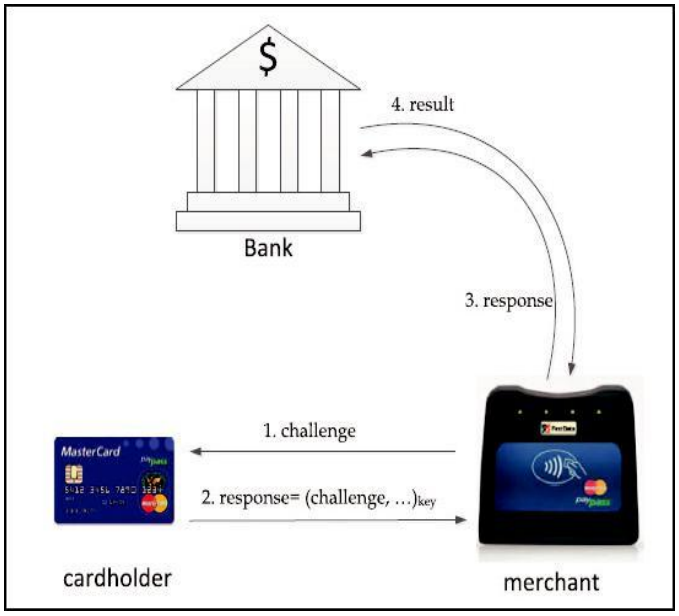

Fig. 1: Online Authorization in a Mobile Payment System.

A. *Advervrsarial models*

Our proposed techniques are meant to defend against unauthorized reading, ghost-and-leech, and reader-and ghost attacks. Adversary models used in the three attack contexts are slightly different. In the following description, we call the tag (reader) under attack as valid tag (reader) and call the tag (reader) controlled by the adversary as malicious tag (reader).

In unauthorized reading, the adversary has direct control over a malicious reader. The malicious reader can be in the communication range of the victim tag without being detected or noticed and, thus, can surreptitiously interrogate the tag. The goal of the adversary is to obtain tag specific information and (later) use such information to compromise user privacy (through inventory checking), clone the tag (and thus impersonate the user), or track the user.

In ghost-and-leech attack, besides the malicious reader (the leech), the adversary has further control over a malicious tag (the ghost), which communicates with a valid reader. The adversary's goal is to use the malicious tag to impersonate the valid tag by letting the malicious tag respond to interrogations from the valid reader with information surreptitiously read from the valid tag by the malicious reader. In reader-and-ghost attack, originally called the "mafia fraud" attack, the adversary controls a malicious reader and tag pair, just like in the ghost-and-leech attack. However, the malicious reader controlled by the reader and- ghost adversary is a legitimate reader or believed by the valid tag as a legitimate reader. Hence, the valid tag (or its owner) is aware of and agree with communications with the malicious reader. That is, the interrogation from the malicious reader to the valid tag is not surreptitious as in unauthorized reading and ghost-and-leech attacks.

In all the attack contexts, we assume the adversary does not have direct access to the valid tag, so tampering or corrupting the tag physically is not possible or can be easily detected. The adversary is also unable to tamper the tag remotely through injected malicious code. We further assume that the adversary is able to spoof the GPS signal around the victim tag but not around the victim reader. This is because the reader is usually installed in a controlled place (toll booth, office building gate, or retail store) and, thus, GPS spoofing around the victim reader can be easily detected. We do not consider loss or theft of tags.

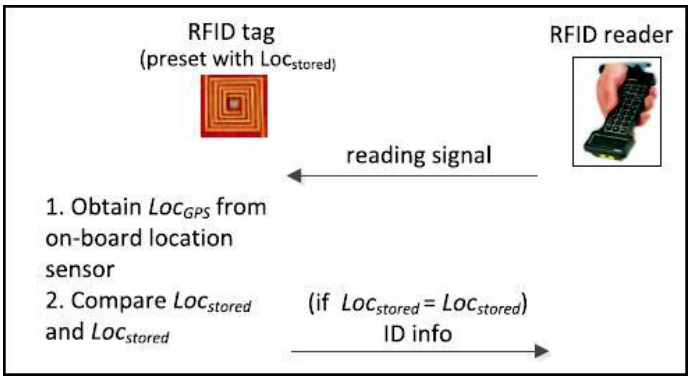

Fig. 2: Location-aware selective unlocking where Locstored is legitimate location (or speed) info stored on the tag side and LocGPS is the location info obtained from on-board GPS upon a reader request.

B. *Location-Aware selective unlocking*

In this section, we present our location-aware selective unlocking mechanism. It can be used to protect against unauthorized reading and ghost- and-leech attacks. Using location-aware selective unlocking, a tag is unlocked only when it is in an appropriate (prespecified) location. This mechanism is suitable for applications where reader location is fixed and well known in advance. One example application is RFID-based building access system. An access card to an office building needs to only respond to reader queries when it is near the entrance of the building.

A prerequisite in a location-aware selective unlocking scheme is that a tag needs to store a list of legitimate locations Locstored beforehand (as depicted in Fig. 2. Upon each interrogation from a reader, the tag obtains its current location information LocGPS from its on-board GPS sensor, and compares it with the list of legitimate locations and decides whether to switch to the unlocked state or not. Due to limited on-board storage (e.g., the WISP has an 8 KB of flash memory) of tags, the list of legitimate locations must be short. Otherwise, testing whether the current location is within the legitimate list may cause unbearable delay and affect the performance of the underlying access system. Moreover, the list of legitimate locations should not change frequently because otherwise users will have to do extra work to securely update the.

List on their tags. Thus, selective unlocking based on pure location information is more suitable for applications where tags only need to talk with one or a few readers, such as building access cards. It may not be suitable for credit card applications, as there is a long list of legitimate retailer stores, and store closing and new store opening occur on a frequent basis.

C. Location-Aware transaction verification

A highly difficult problem arises in situations when the reader, with which the tag (or its user) engages in a transaction, itself is malicious. For example, in the context of an RFID credit card, a malicious reader can fool the user into approving for a transaction whose cost is much more than what she intended to pay. That is, the reader terminal would still display the actual (intended) amount to the user, while the tag will be sent a request for a higher amount. More seriously, such a malicious reader can also collude with a ghost and then succeed in purchasing an item much costlier than what the user intended to buy. As discussed in Section 1, addressing this reader-and-ghost relay attack requires transaction verification, i.e., validation that the tag is indeed authorizing the intended payment amount. Note that selective unlocking is ineffective for this purpose because the tag will anyway be unlocked in the presence of a valid (payment) context.

In this paper, we set out to explore the design of location-aware automated mechanisms for protecting against reader-and-ghost attacks. We note that under such attacks, the valid tag and the valid reader would usually not be in close proximity. This is in contrast to normal circumstances whereby the two entities would be at the same location, physically near to each other. Thus, a difference between the locations of the tag and the reader would imply the presence of such attacks. In other words, both the valid tag (credit card) and valid reader may transmit their locations to a centralized authority (issuer bank). This authority can then compare the information received from both entities and reject the transaction if the two mismatch Measure their location information. Location information generated by both card and reader are then forwarded to the bank. The bank server decides whether to approve the transaction after comparing the location data received from the two ends. Fig.3 illustrates the process of location-based proximity verification inside the current mobile payment infrastructure. The user-side card generates its location information loccard while the merchant-side reader generates its version of location information locmerchant. loccard is protected (e.g., via MAC) with the key shared with the issuer bank before it is sent to the merchant's terminal, which then forwards its own location information locmerchant along with the card credentials to the bank for transaction verification and authorization. Since the integrity of loccard is protected by the shared key between the card and bank, a malicious reader would be unable to change this value.

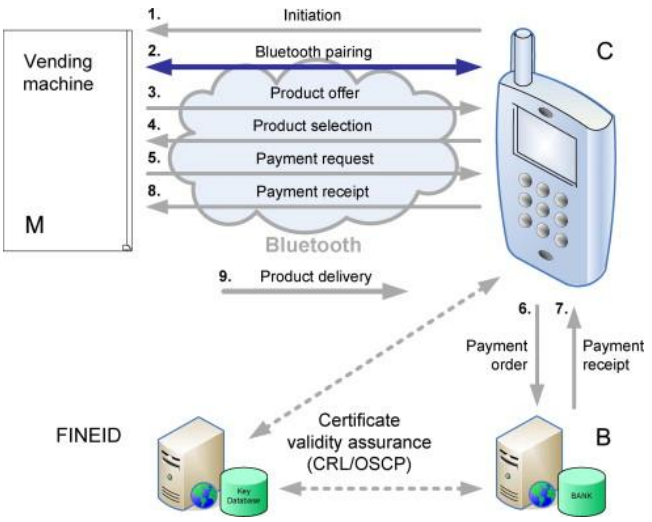

Fig. 3: Online Authorization in a Mobile Payment System Enhanced With Our Proximity Detection Approach.

III. DESIGN AND IMPLEMENTATION

GPS is generally used as the main source of location information and the major enabler for location-based services. It has world-wide availability and an accuracy of a few meters in location estimation—adequate enough for most civilian applications. However, the accuracy of GPS deteriorates inside buildings and in arrow urban canyons. Unlike GPS, WiFi positioning can provide good positioning results (with an accuracy of a few meters just like that of GPS) even indoors. However, it is prone to signal interferences and may not be always available due to the limited coverage of WiFi networks. Cellular network positioning is almost available both outside and indoors. However, it has poorer accuracy (50-100 meters) in location estimation.

Since location is used as a security control parameter in our approach, accuracy of location estimation can affect the security level we can achieve. For example, poor accuracy can cause a high false unlocking rate in selective unlocking and give more space for the adversary to cheat in proximity in server transaction verification. For this reason, the cellular network positioning technology is believed not a good candidate to use to get location information for security purpose.

A GPS receiver derives its location by timing the signals sent by GPS satellites high above the Earth. The receiver uses the messages it receives from the satellites to determine the travel time of each message and computes the distance to respective satellite. These distances along with the satellites' own locations are used with the possible aid of trilateration, to compute the position of the receiver.

we have to store this valid location list on an external memory for the purpose of our selective unlocking mechanism (note that the transaction verification mechanism does not require the tag to store anything). Location sensing and computation. For location sensing, we dynamically obtain the location data from the GPS continuously at the rate of 1 Hz, and compare it with the list of valid locations stored on the tag within a time span.

IV. EXPERIMENTS AND RESULTS

Location tests, in this experiment, we used location information as a selective control to lock/unlock the tag. We took the reading of five locations around the campus and stored them as valid locations where the tag should be in an unlocked state.

Speed tests, we make use of the instantaneous speed of the GPS receiver in our experiments. We found the instantaneous speed from the GPS receiver matches the reading of odometer in the car.

The kit designed was shown in below figure.

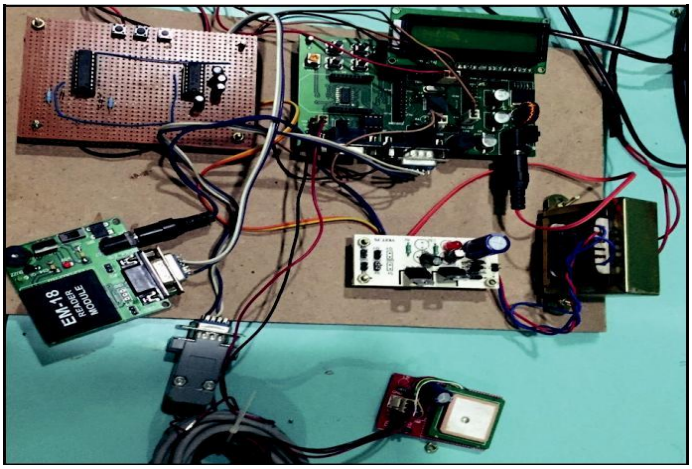

Fig. 4: Overall System.

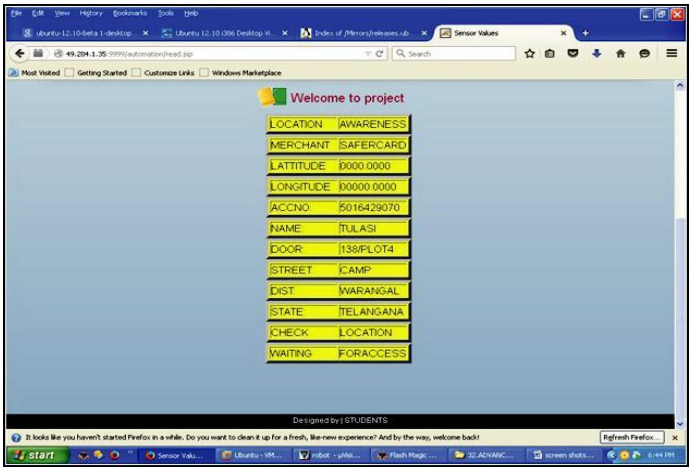

Fig. 5: Output of the System.

V. CONCLUSION

In this paper, we reported a new approach to defend against unauthorized reading and relay attacks in some RFID applications whereby location can be used as a valid context. We argued the feasibility of our approach in terms of both technical and economical aspects. Using location and derived speed information, we designed location aware selective unlocking mechanisms and a location aware transaction verification mechanism. For collecting this information, we made use of the GPS infrastructure. To demonstrate the feasibility of our location-aware defense mechanisms, we integrated a low-cost GPS receiver with a RFID tag (the Intel's WISP) and conducted relevant experiments to acquire location and speed information from GPS readings. Our results show that it is possible to measure location and speed with high accuracies even on a constrained GPS-enabled platform and that our location aware defenses are quite useful in significantly raising the bar against the reader-and-leech attacks.

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Hard Faults Auto Correction using FPGA

H. Machaand and N. Raj

***Abstract*— Multi-core systems have more functional units fabricated in to a single chip and they are more vulnerable to faults. These faults have to be handled efficiently without substantial loss of overall performance. In this paper a self repairing approach for hard faults using Field Programmable Gate Array (FPGA) is proposed. The proposed multi-core system will have a reconfigurable hardware unit and a fault look-up table included to individual cores of the multi-core system. The faulty unit details are updated in the fault look-up table as a result of fault detection phase. The faulty unit details are given as input to the decoder unit along with the usual inputs. Depending on these, the decoder unit will decide to choose either the Arithmetic and Logic Unit (without fault) or the Reconfigurable hardware unit (Faulty unit reconfiguration).**

***Index Terms*— Self Reparing, Hard faults, Field Programmable Gate Arrays, Reliability, Online Fault Repair**

I. Introduction

With the advancements in the VLSI technology, more and more functional units are fabricated in a single chip. With more number of circuits in the chip, the probability of occurrence of faults in the circuit is also high. The faults can be classified in to a) Transient (or soft) errors, [1] caused by environmental disturbances, b) Permanent (or hard) errors[2], caused by latent manufacturing defects as well as aging (wear out phenomena) and c) Verification inefficiencies that allow important design bugs to escape in the system.

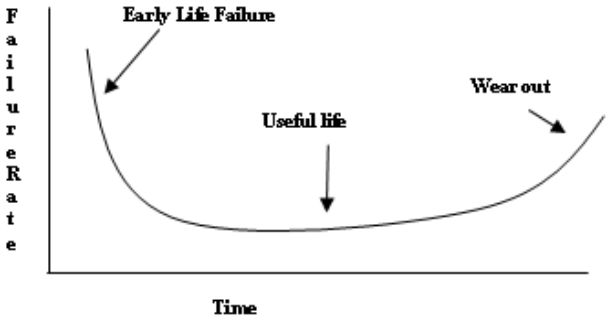

Figure 1. Product reliability [1]

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Any type of fault in the system has to be taken care off, for graceful degradation of the system. The hard faults can occur during any stage of the chip's life cycle. The following figure 1 shows the trend in a chip's failure rate [3]. From the above diagram it is clear that the faults can happen at early life of the product or during its useful period or can wear out after a long time. Early life failures are also called as infant mortalities and they are the faults that escape during design verification process. Ideally, the early life failure should have a brief region in the figure 1. Even with today's advanced design verification and testing tools, early aging in multi-core processors is high because of their high transistor density [4]. For handling hardware failure during the early life or useful life, a post silicon fault repairing technique that can be done on the field is essential. Self-repairing of hardware fault is the capability of the processor to handle the hardware fault by itself. This paper proposes the idea of using FPGA for self-repairing of hardware faults in an ASIC design. The following section explains the existing post silicon self-repairing techniques.

II. Problem Formulation

Self-repairing is an emerging field that will have a major impact on increasing the reliability of the system. The importance of failure prediction is emphasized in [5]. Circuit failure prediction in [5] predicts the occurrence of hard faults even before it surfaces on the system's state or data. This prediction is made possible by collecting information about various system parameters over time and comparing them with the fault free signatures. Other available self-testing techniques includes Built In Self-Test(BIST) for failure prediction[6], Concurrent self-test[7] for failure prediction and Genetic algorithm based BIST [8].

After a fault has been detected in the system, it has to be repaired effectively. The use of Triple Modular Redundancy (TMR) for self-repair of transient faults is described in [14]. The use of TMR also does not guarantee fault repair on all the three systems involved. For repairing faults in any of the three system involved in the TMR using FPGA is proposed in [11]. FPGA is the most suitable for self-repairing and lots of work has already been proposed to heal a FPGA. The use of an autonomous self-healing architecture proposed in [15] uses FPGA. Fault tolerant FPGA processor architecture proposed in [17] considers a FPGA architecture on which faults are handled efficiently by reconfiguration. Software based self-repair discussed in [10] uses software based micro architecture self-configuration. Another method of Self repair using FPGA

is to include a spare core [9] to the processor architecture and use the spare core for any permanent fault. Using a spare core for fault handling provides dynamic fault recovery in the field. When fault repair is done through a spare FPGA core in a multi-core environment, there is a complication of inter processor communication involved. So it will be better to have a within core mechanism to repair hard faults. This paper proposes the idea of using FPGA as a unit inside each core of the multi-core processor architecture for self-repairing of permanent fault.

III. Problem Solution

Multi-core processor can be shared or distributed. In any type of multi-core architecture, including a FPGA hardware unit inside the core will enable self-repairing of hard faults. The proposed system includes a reconfigurable hardware in every core of a multi-core system. The reconfigurable hardware will be handling the hardware faults occurring in that particular core. A self-detection technique based on software [2] can be incorporated to detect a fault before it surfaces on the system state. After the fault is detected, the FPGA is configured to perform the functionality of the unit on which fault has occurred. The permanent faults can be maintained in a table so that any future reference to that unit may be handled by the reconfigurable hardware. By providing self-repairing like this will enable reduced space and time for fault recovery. For explaining the details about the implementation of the above concepts, OpenSPARC T1 [18] architecture is considered. OpenSPARC T1 is the open source code of SPARC architecture provided by SUN Micro systems. OpenSPARC T1 architecture has 8 CPU cores, with 4 threads per core, for a total of 32 threads. The cores are connected by a cache cross bar. Each core has 132 Gbytes of level 1 instruction cache and 8 Kbytes of level 1 data cache. The execution unit of OpenSPARC T1 has an ALU, a multiplier circuit, a divider circuit and shifter circuit. There is a Execution Control Logic (ECL) that generates the necessary select signals that control the multiplexers, keeps track of the thread, and reads each instruction and implements the bypass logic. The bypass logic does the operand bypass E,M, W stages to the D stage. The ALU consists of an adder and logic operations such as ADD, SUB, AND, NAND, OR, NOR, XNOR, NOT. The ALU is also used for branch address or virtual address calculation. The method proposed in this paper for the self-repairing of hard faults on the ALU can also be extended to other units.

A. Model Proposed

The overall system of the SPARC core along with Reconfigurable Hardware Unit (RHU) and Fault Lookup Table (FLT) is shown in the following figure.1. In the figure 1, the FLT and RHU are represented using dotted boxes as in

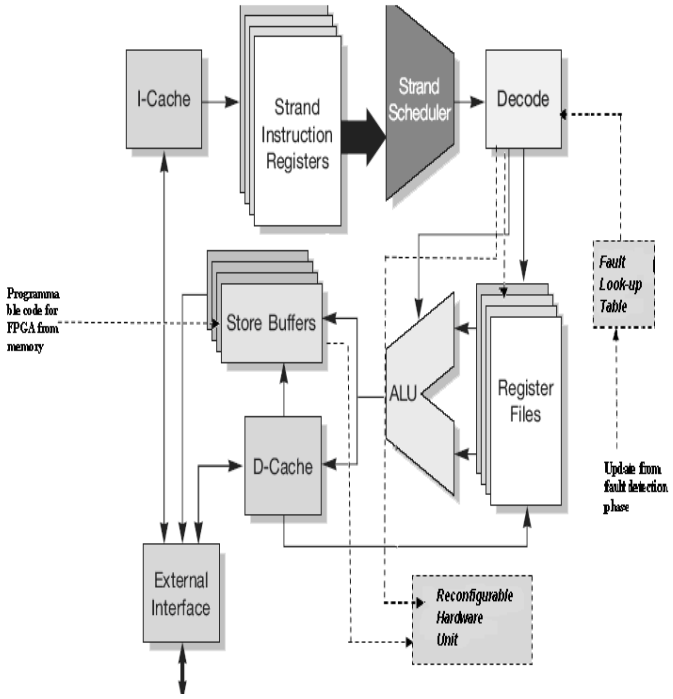

Figure 2. OpenSPARC Core with RHU and FLT

The reconfigurable hardware is a FPGA unit that will reconfigured to work as the faulty unit. The FLT will store the details of the faulty functional unit that has been obtained as a result of fault detection.

If a fault occurs in the system, the fault can be predicted by using one of the methods proposed in [6]-[8]. The faults predicted will be loaded on to the FLT. Every time the system is switched off the details of the (FLT) are updated in a secondary memory file. So when a future reference to the faulty unit occurs, the details of the faulty unit are seen by the decoder and hence the necessary functionality will be initiated on the Reconfigurable hardware. A similar proposed solution in [17] for fault recovery had complex control logic. But in this proposed method, the control logic of this test and recovery units are made much simpler. The faulty unit is captured in a table and it will be given to the decoder unit which will in-turn initiate the necessary reconfiguration.

B. Working Principle of the Proposed System

The detailed communication between the fault lookup table, the instruction decoder and the reconfigurable hardware is explained in the following figure 3. The fault lookup table is an on chip table to store the list of the permanent faults happened in the system and their diagnosis details. This will aid in the repair of the faulty circuit online. The decoder takes input from the thread selection mux which has details about the instruction to be executed and also the fault lookup table. If the instruction requires the usage of the faulty unit listed in the fault lookup table then instead of sending control signals to the faulty unit, they are sent to the reconfigurable hardware.

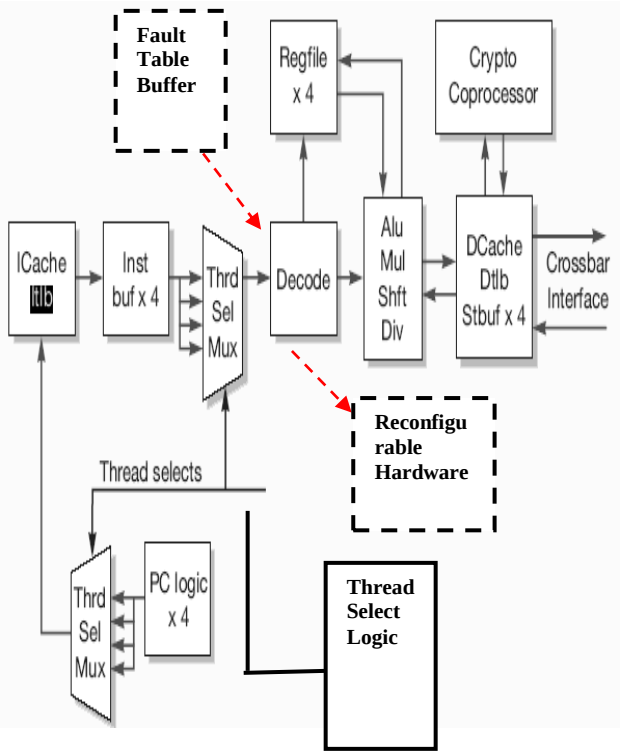

Figure 3. OpenSPARC Pipeline logic with RHU and FLT

The code for configuration of the FPGA stored off the cache is loaded on to the FPGA via the DCache buffer. The architecture proposed is a hybrid that uses FPGA to augment an ASIC design [16]. The main concern in such a design is that, ASIC's are fine-grained whereas FPGA's are medium grained or coarse-grained. However for fault repair considering coarse-grained reconfiguration will not harm the system. Because of the above reason, in the proposed system, we have used library based FPGA mapping.

The FPGA considered here consists of Programmable logic blocks and Programmable interconnects. The structure of the programmable logic block is given in the following figure 4.

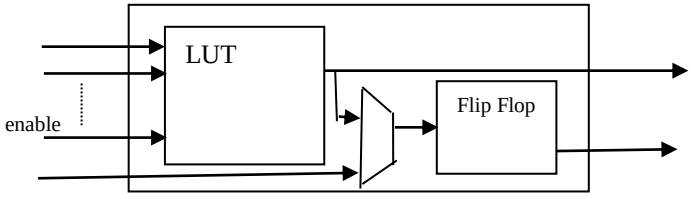

Figure 4. FPGA Cell Structure

The FPGA and the ASIC hybrid architecture can be a parallel one with ASIC processor being the master and the FPGA being the slave. The faults detected by [6][7][8] are keyed in the FLT . The FLT can also be a FPGA so that dynamically the table size can be varied. Unique identification numbers can be given for all the units under test. Look up tables are usually arrays or associative arrays often used for indexing. The indexing here points to the memory space where the program for reconfiguration for that particular unit lies.

C. Analysis

The gate counts for basic circuits are given in the following table.

Table.1 Gate Counts for common functions

Function	**Gates**
2-input NAND	1
2 to 1 mux	4
3 input XOR	6
4 input XOR	9
2 bit carry full adder	9
D flip flop	6
D flip flop with set and reset	8
D flipflop with reset and enable	12

By using hashing function for the look up table, the searching for a particular unit in the table will be O(1). Even with multiple faults searching the lookup table for all the instruction will take O(1) for each instruction. For a program with 'n' instructions there will be 'n' reference to the table.

Reconfiguration time of the FPGA is an important criterion on runtime reconfigurable architectures. For example the full time reconfiguration time of Spartran3. The reconfiguration of FPGA takes milliseconds and hence the fault repair using FPGA will increase the overhead by milliseconds. There some algorithms [17]-[21] already proposed to reduce the reconfiguration time. Using one of them, the reconfiguration time cane is reduced by 40%. The reconfiguration time for the FPGA can be given from the following equation.

TbitLoad=((BitStreamLength)/(ClockFrequency* ConfigurationPortBandwidth))

The OpenSPARC T1 has an ALU unit with a gate count of 1968. For this the bits stream size will be with the above table the reconfigurable hardware proposed can be made from a bit stream size of 48.07KBytes. With an 8 bit parallel port and clock frequency of 5GHZ, the Tbit load time can be calculated as 119.91 microseconds [24]. If the number of faults and the frequency of its reference is increased then we get a curve C1 given in the following figure 4. If number of faults increases but the references remains constant, curve C2 will be obtained. When the number of faults is not increased, then there will be no change in the performance degradation. From the figure it could be seen that if the number of faults and the reference to it is increased to a higher value, the system degrades. But the degradation is graceful. The proposed system is a model which will be implemented with synchronous fault repair using XILINX Virtex FPGA board.

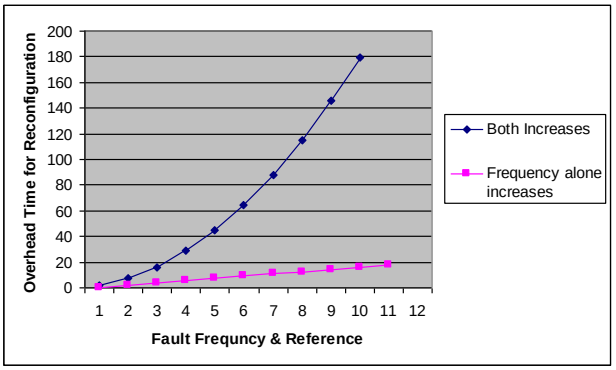

Figure 5. Fault frequency versus overhead time

IV. CONCLUSION

Faults (or) permanent faults occurring during the early or working lifetime of the processor should be avoided. But the probability of early life permanent faults has increased with multi-core processors where the chip density per square area is high. This has made online permanent fault repair on the field a necessity. In this paper such a method is proposed for handling hard faults on the field by using reconfigurable arrays. As discussed in the previous section, there will be some overhead to perform the fault repair. This overhead time is proportional to the fault occurrence. Since the multiple fault occurrences will not be very high during the initial or working lifetime of the processor , the overhead will not affect much of the system's performance. Thus with the aging of the processor, the proposed technique guarantees graceful degradation. In future the proposed technique can be refined to have minimum overhead.

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Inexact Computing in digital systems with Transmission Gate-based Approximate Adders

K. Swapna and N. Raj

***Abstract*— The low power and high speed architecture is the major concern in the adder circuit design. To achieve compactness and low power consumption, we need to reduce the number of transistors. Power dissipation has become a significant concern for integrated circuit design in nanometric CMOS technology. To reduce power consumption, approximate implementations of a circuit have been considered as a potential solution for applications in which strict exactness is not required. In inexact computing, power reduction is achieved through the relaxation of the often demanding requirement of accuracy. In this paper, new approximate adders are proposed for low-power imprecise applications by using logic reduction at the gate level as an approach to relaxing numerical accuracy. Adders are the basic elements which are widely used in digital systems. The power consumption of a conventional full adder circuit is reduced by using transmission gate at the place of pass transistor logic (NMOS or PMOS). Transmission gates are utilized in the designs of two approximate full adders with reduced complexity. The approximate adders show advantages in terms of power dissipation over accurate and recently proposed approximate adders. An image processing application is presented using the proposed approximate adders to evaluate the efficiency in power and delay at application level.**

***Index Terms*— Approximate adder, inexact computing, error distance.**

I. Introduction

Today there is an escalating number of portable applications with limited power availability, requiring small area, low-power and high throughput circuitry. Therefore circuits which consume low power become the major concern factor for design of microprocessors and system components. The research effort in low power microelectronics has been intensified and low power VLSI systems have emerged as exceedingly in demand. In highly integrated nano-scale designs, reliability issues resulting from PVT (process, voltage and temperature) variations, aging effects and soft errors have become major impediments for leveraging the benefits of a lower device scaling; moreover, leakage and static power are significant concerns for the high power consumption encountered at such high density. A potential solution to lower power dissipation is to employ approximate circuit designs.

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Commonly used multimedia applications rely on digital signal processing blocks as core components. Most of these DSP blocks implement algorithms, by which an output is produced as either an image, or a video for human perception and analysis. However, the limited perception of human senses allows the output of these algorithms to be numerically approximate rather than accurate [1]. The relaxation on numerical exactness allows performing imprecise or approximate computation. The development of imprecise and simplified arithmetic units provides an additional layer of power saving over conventional low-power design techniques. Adders have been investigated for approximate implementations [2]. Speculative approximate adders are proposed in [3, 4] to achieve better performance in terms of area, power and delay over accurate adders. The basic principle of these designs is to truncate the long carry chain of a multiple bit adder by using several sub-adders to calculate the sum. OR gates are used in [5] for the addition of each less significant bit (LSB), while more significant bits (MSBs) use accurate adders to preserve accuracy. Logic reduction is considered in [6] by removing transistors from a mirror adder (AMA) to simplify its design. In [7], pass transistors are used in XOR/XNOR-based approximate adders. However, these designs suffer from a severe signal distortion or degradation when passing a '0' for PMOS and passing a '1' for NMOS transistors. This paper discusses two new multiplexer-based approximate adder designs. In contrast to [7], transmission gates (TGs) are used as alternative circuit components in the proposed designs. TG is a promising replacement for pass transistors and is commonly used in implementing look up tables (LUTs) of field programmable gate arrays (FPGAs) [8]. Hence, TG-based multiplexers are utilized due to their lower power dissipation than conventional CMOS multiplexers [9] [10].

In this paper, the approximate adders are designed for reducing circuit complexity (in the number of transistors) at the gate level by removing some of the gates from the original full adder. Additionally, the node capacitances and thus the dynamic power are also reduced in the proposed circuits. Delay, power, area and power-delay product are measured and the proposed designs are compared to a truncated adder. The metrics of error distance (ED) and mean error distance (MED) [11] are used to compare the proposed designs with other approximate adders in terms of accuracy. Extensive simulation results are provided to show the effectiveness of the proposed designs.

II. LITERATURE

In this section, accuracy metrics are introduced for error analysis with a brief review of transmission gates (TGs) and TG-based multiplexers.

A. Metrics

The error distance (ED) and mean error distance (MED) are proposed in [11] to characterize the accuracy of approximate arithmetic circuits. The ED is defined as the absolute difference between the accurate and approximate output values, i.e.,

$$ED = |R' - R|,$$

where R'(R) denotes the output value of an approximate (accurate) circuit. The MED is defined as the average of EDs for a set of input values, i.e.,

$$MED = E[ED] = \sum ED_i P(ED_i),$$

where P(ED*i*) is the probability to produce a particular value of ED, EDiin this case. The error rate (ER) is defined as the percentage of incorrect output values among all outputs. Similarly, the pass rate (PR) is defined as 1-ER. Other metrics such as power and delay are mostly related to circuit- level features and are also utilized.

A. Transmission Gate based Multiplexer

A PMOS or an NMOS transistor can be used as an imperfect switch; this structure is commonly referred to as a pass transistor (Fig. 1). The pass transistor suffers from signal strength loss due to the threshold hold voltage drop [12]. The degradation determines the closeness of the output signal to an ideal voltage source. The PMOS generates a degraded 0, while the NMOS generates a degraded 1. However, this degradation could be very severe to potentially violate the noise margin of the next stage [12]. A transmission gate consists of an NMOS and a PMOS transistor in parallel with the gates controlled by complementary signals (Fig. 2).

NMOS Pass Transistor- Logic '1' transfer; Logic '0' transfer:

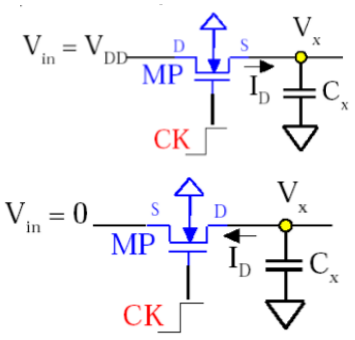

Fig.1. NMOS pass transistor

A transmission gate passes both 0 and 1 gracefully. Hence, the transmission gate is often used as an alternative approach to implement a multiplexer. A gate level multiplexer requires rather complex circuitry, thus a transmission gate based multiplexer is a better option for reducing both power and delay.

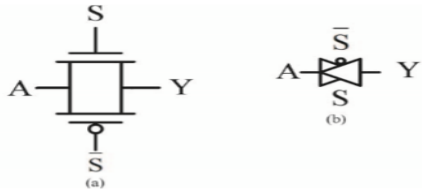

Fig. 2. (a) A transmission gate (TG) and (b) symbol for TG.

The implementation of a transmission gate-based multiplexer is shown in Fig. 3. The signal *sel*is inverted as the complementary signal for selecting the two transmission gates (using an additional inverter).

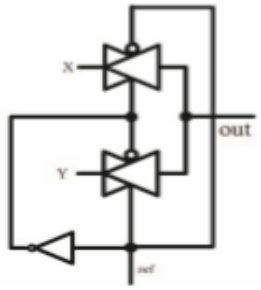

Fig 3. A transmission gate based multiplexer

The implementations of TG based XOR and XNOR gates are shown in Fig. 4. Compared with Fig. 3, the TG based XOR/XNOR gate is a special case for a multiplexer in which the inputs have complementary signal values.

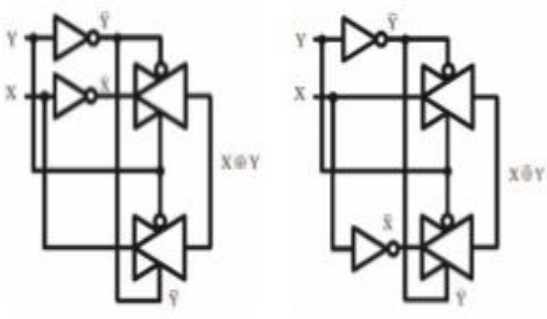

Fig. 4. Transmission gate based (a) XOR (b) XNOR gates.

III. APPROXIMATE ADDERS

In this section, two approximate adders are proposed. It is shown in [13] that a transmission gate based full adder exhibits good power and delay performance with a rather simple circuit. Fig. 5 shows a transmission gate-based full adder.

The adder consists of three modules (as enclosed in the red, blue and brown blocks in Fig. 5).The first module is an XOR gate with inputs X and Y. The second module is an XOR gate for generating Sum. The last module is a MUX for generating Cout. This implementation is based on transmission gates and several inverters. Table I shows the truth table of an accurate adder (CS denotes C*out*and Sum).

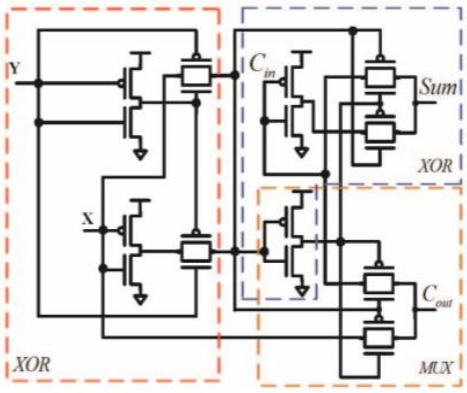

Fig. 5. Transmission gate based accurate full adder [13].

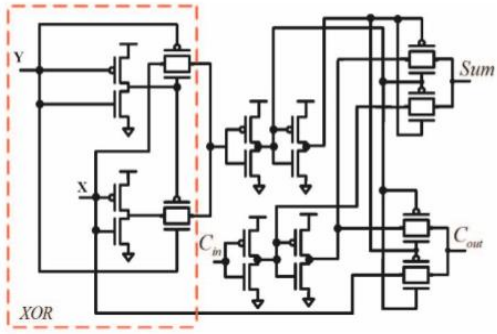

Fig. 6. Transmission gate based full adder by inserting inverters.

Table 1. Truth table for an accurate full adder

	*CS	XY 00	01	11	10
C_{in}	0	00	01	10	01
	1	01	10	11	10

*CS=Cout&Sum

However, the utilization of more than two transmission gates in series increases the delay unless buffers are added [12]. Hence, buffers (using two inverters) are added in Fig. 7 instead of using the full adder based on transmission gates connected in series (Fig. 6). The simpler structure of a transmission gate based multiplexer allows achieving complex logic functions. The proposed approximate adders are designed either by removing some transistors or changing some of the signals for Sum or C*out*.

Figs. 8 and 9 show the proposed approximate adders using transmission gates (denoted as TGA1 and TGA2). The feature common to both TGAs is that the first module is implemented by an XOR gate to reduce the node capacitance, thus lowering power dissipation. Moreover, the first stage just uses an XOR gate for reductions in both delay and power.

A. *TGA1- Approximate Adder*

In Table I, there are six cases when C*out*is equal to Y, thus a simpler design can be obtained if Y is directly connected to C*out*. Moreover, the carry propagation path is reduced (C*in*to C*out)* by connecting an input to C*out*. The Sum signal is also modified. In Fig. 5, an additional inverter is utilized to invert C*in* and generate Sum. This is simplified in TGA1 by removing this inverter, while connecting input X directly to the transmission gate based multiplexer (Fig. 7). This generates two incorrect results out of eight; therefore, the ER is two out of eight for CS. Table II is the truth table for TGA1; below equations show the logic functions of TGA1.

$$Sum = (X \overline{\oplus} Y)C_{in} + X\overline{Y}$$

$$C_{out} = Y$$

Table 2. Truth table for TGA1

	CS	XY 00	01	11	10
C_{in}	0	00	**10**	10	01
	1	01	10	11	**01**

B. *TGA2- Approximate Adder*

In Table I, if either X or Y is “1", then there are four out of six cases where C*out*is “1"; thus an approximate adder can use only an OR gate to generate C*out*. In this case, only two incorrect C*out*values are generated (shown in bold in Table III). When the input combination is “010" or “100", the accurate adder generates C*out*as “0" while it is “1" for TGA2. The error rate is two out of eight for CS. Similarly, the generation of C*out*only depends on X and Y, thus there is no carry propagation for TGA2, resulting in a reduction of the delay. For Sum, compared with TGA1, the input for the transmission gate is connected to Gnd. This results in two incorrect output values. Fig. 8 shows TGA2, while below equations show its output functions.

$$Sum = (X \overline{\oplus} Y)C_{in}$$

$$Cout = X+Y$$

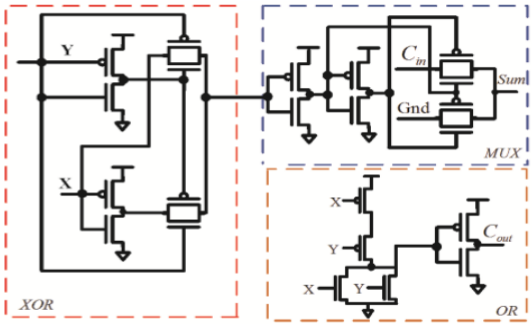

Fig 8.Transmission gate based approximate adder 2(TGA2).

Table 3. Truth table for TGA2

	CS	XY 00	01	11	10
C_{in}	0	00	**10**	10	**10**
	1	01	10	11	10

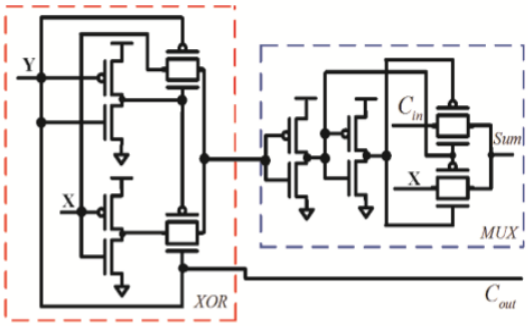

Fig. 7. Transmission gate based approximate adder 1 (TGA1).

IV. Comparison Result

This section the designs of the two proposed approximate adder are evaluated comparison with respect to power and delay as well as accuracy is presented for each design. The approximated mirror adders (AMAS) are considered for comparison purposes AMA1-4 are obtained by removing transistors from the accurate mirror full adder. In our simulation 8 and 16 bit adders are compared by replacing the less significant half in an RCA, accurate mirror adders and the TG based full adder (fig.6) are applied for AMA and TGA based multipliers respectively. The lower part OR adder (LOA) [5] is also compared with the accurate mirror adders as the MSB part.

A truncation based adder is considered as a baseline when assessing the approximate designs. For this adder the sum outputs of the truncated section are connected to ground. While the sum of the truncated part is zero, the carry in the higher section of a truncated adder is connected to one of the most significant inputs to the truncated part. However, the number of bits that are truncated must be carefully selected for a fair comparison. The power dissipation is chosen as a baseline for a fair comparison of accuracy and delay, i.e., the same power is chosen for each considered adder with value similar to that of the TGA1 based approximate adder. Hence under this condition, the truncated bits are given by 3 and 6 for the 8 bit and 16 bit adders with a power consumption of 2.03Uw and 4.69uW. Power and delay are measured by using the cadence ultraism SPICE simulator at a clock frequency of 100MHz.Accuracy comparison in terms of MED and PR is also assessed. A comprehensive comparison by considering both accuracy and power/delay is presented to show significant savings with an acceptable for the TGAs.

A. Accuracy

Table IV summarizes the comparison results including accuracy in terms of MED and PR, and circuit characteristics. The exhaustive input combinations are applied for analysis of an 8-bit RCA; one million randomly generated inputs are used for evaluation of a 16-bit RCA.

- For the 8-bit RCA, TGA1 and TGA2 have a significantly higher PR (i.e., 1YER) and lower MED than AMA1-4 and the truncated adder.
- TGA2 has the lowest MED and the largest PR (same as AMA1) for both 8 and 16 bit RCAs; thus, TGA2 is the most accurate design in terms of MED and ER.
- AMA2 and the truncated adder have the lowest PR for 8 and 16 bit RCAs respectively, while AMA3 has the largest MED for both 8 and 16 bit RCAs

B. Power

The power consumption is found by using the Cadence Ultraism simulator with STM 65nm CMOS standard cell library. For an 8(16) bit RCA, 5k (25k) randomly generated inputs are used for evaluating the power. A fanout of 4 standard sized inverters is applied as load as shown in table IV, TGA1 has the lowest power dissipation for both the 8-bitand16-bit approximate adders. AMA1has the largest power dissipation compared to the other approximate adder designs.

C. Delay

The delay for designs including TGAs, AMAs and LOA is also measured by using the simulator Ultrasim with an STM 65nm standard cell library. The delay is reported in Table IV for both 8 and 16 bit RCAs. Four standard-sized inverters are utilized as load for the output. These results yield the following conclusions.

- TGA1/TGA2 and AMA4 have the shortest delay for 8-bit and 16-bit RCAs respectively; meanwhile AMA2 has the largest delay for both cases.
- The delay of AMA2 is nearly twice the delay of AMA4, because the critical path of AMA4 is about half of that of the accurate mirror full adder (i.e., n/2, where n is the length of the RCA), whereas the critical path delay of AMA2 is nearly the same as the n-bit mirror adder, because the carry propagation path for AMA2 is the same as the accurate mirror full adder.
- AMA4 has a shorter delay than AMA2 for the 16-bit RCA; however, it is larger than the delays of TGA1 and the TGA2 for the 8-bit RCA.

In summary, TGA1 and TGA2 have the best performance in terms of delay than AMAs (except AMA4 as a 16-bit adder).

Table 4: Comparison of 8 bit (8b) and 16 bit (16b) RCAs with approximate adders

	Power (uW)		Delay (ns)		PDP (10^{-15}J)		MED		PR (%)	
	8b	16b	8b	16b	8b	16b	8b	16b	8b	16b
Truncation	**2.03**	**4.69**	**0.463**	**0.975**	**0.94**	**4.57**	**3.61**	**33.92**	**7.69**	**0.81**
TGA1	1.97	4.30	0.445	0.934	0.88	4.02	2.94	44.71	20.77	10
TGA2	2.28	4.95	0.447	0.937	1.02	4.63	2.67	32.31	23.08	14.1
AMA1	2.79	6.22	0.778	1.597	2.17	9.60	3.04	34.63	15.38	14.1
AMA2	2.74	5.92	0.809	1.601	2.22	9.48	3.68	59.65	3.46	10.1
AMA3	2.55	5.49	0.768	1.562	1.96	8.58	4.57	71.27	8.08	2.44
AMA4	2.53	5.72	0.471	0.895	1.23	5.12	4.36	66.29	10	2.42
LOA	2.05	4.59	0.499	0.923	1.02	4.24	2.83	47.81	31.15	9.98

D. Power-Delay Product (PDP)

As shown in Table IV, the proposed designs have lower PDPs compared to AMAs while TGA1 has the lowest PDP among all designs. Moreover, LOA has a better performance than AMAs (i.e. lower PDP) due to the shorter delay and lower power. Therefore, TGA1 has the best performance than the other designs while LOA has a smaller PDP than TGA2 and AMAs.

V. Image Processing Application

Using the proposed approximate adders, an image sharpening algorithm is implemented in Matlab with an Intel Core i5 processor and 4GB RAM. The sharpened image quality is measured by the peak signal noise ratio (PSNR). The PSNR is usually used to measure the quality of a reconstructive process involving information loss and is based on the mean square error. For an accurate image I and an image K generated by an approximate process (I and K are monochrome images with mxn pixels), the MSE is defined as

$$MSE = \frac{1}{mn}\sum_{i=0}^{m-1}\sum_{j=0}^{n-1}[I(i,j)-K(i,j)]^2 \cdot$$

The PSNR is given by

$$PSNR = 20\log_{10}(\frac{MAX_I}{\sqrt{MSE}})$$

.

The term MAX*I* is the maximum possible pixel value of the image; for example, when a pixel is encoded by 8 bits, its maximum value is 255. In the image sharpening algorithm [14, 15], multiplication is performed by using carry save adders (CSAs) followed by a ripple carry adder (RCA). The subtraction is also performed in 2's complement addition, i.e. an RCA is used as a subtractor and as an adder for multiplication. In this image processing application TGAs and AMAs are compared by replacing the lower bits of the CSAs and RCAs. An 8 by 6 multiplier is used for multiplication, with the lower 7 LSBs replaced by approximate adders for CSAs and the RCA. The multiplication results in 25 terms that are added using a 16-bit RCA with the lower 8 bits replaced by approximate adders. For the subtractor, a 9 bit RCA is used with the lower 5 bits approximated. Fig. 9 shows the images processed by approximate adders (with corresponding PSNR values). It can be seen that the images processed by TGAs have better image qualities (i.e., with higher PSNR values) than the AMAs and only slight quality degradation for the images.

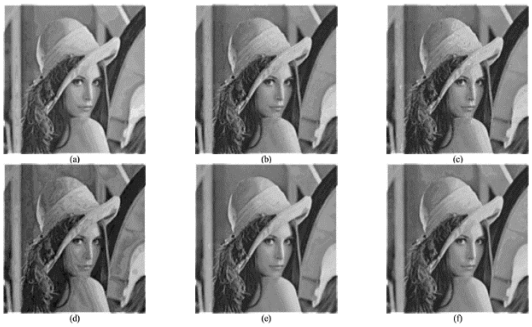

Fig. 9. Images processed by: (a) AMA1 with PSNR=27.81; (b) AMA2 with PSNR=29.91; (c) AMA3 with PSNR=28.27; (d) AMA4 with PSNR 23.19; (e) TGA1 with PSNR=32.89; (f) TGA2 with PSNR=30.56

VI. Conclusion

The proposed approximate adder designs show significant savings in power and delay. At the same time, they generate results that incur only a marginal degradation of accuracy. While TGA2 exhibits the best accuracy in terms of error rate and mean error distance, an image sharpening application shows that TGA1 provides excellent performance in terms of PSNR compared with other approximate adders using logic reduction techniques. Approximate computing probably has a great future ahead of it. There's been some impressive work on using analog for approximate computing - and the startup, isocline, is talking about 100x better power consumption, and 10x price reduction, with others talking about even better results. As for possible applications - there are probably many, in signal and image processing(for ex. GPS and image compression/decompression, computer vision), in optimization , in some areas of scientific computing where they can mitigate the inaccuracies, in neural inspired computing and various machines learning algo's, and probably other fields.

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A Study on Communication Infrastructures in 5G Cellular Networks

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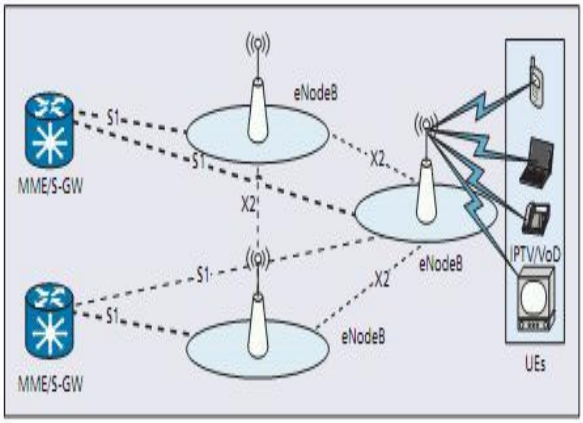
ABSTRACT- Device-to-device (D2D) communication commonly refers to a type of technology that enable devices to communicate directly with each other without communication infrastructures such as access points (APs) or base stations (BSs). Bluetooth and WiFi-Direct are the two most popularD2D techniques, both working in the unlicensed industrial, scientific and medical(ISM) bands. Cellular networks, on the other hand, do not support direct over-the-air communications between users and devices. However, with the emergence of context-aware applications and the accelerating growth of Machine-to-Machine (M2M) applications, D2D communication plays an increasingly important role. It facilitates the discovery of geographically close devices, and enables direct communications between these proximate devices, which improves communication capability and reduces communication delay and power consumption. To embrace the emerging market that requires D2D communications, mobile operators and vendors are accepting D2D as a part of the fourth generation (4G) Long Term Evolution (LTE)-Advanced standard in 3rd Generation Partnership Project (3GPP) Release 12.

1. INTRODUCTION

As LTE systems are reaching maturity and have been deployed, the future fifth generation (5G) cellular networks have drawn great attention from researchers and engineers around the world. 5G cellular networks are envisioned to attain 1,000 times higher mobile data volume per unit area, 10-100 times higher number of connecting devices and user data rate, 10 times longer battery life, and five times reduced latency. Although it is still too early to give an exact definition of 5G, current research trends have shown that the above ambitious goals can potentially be achieved by a multi-tier and heterogeneous network architecture along with the aggregation of several key technologies, such as spatial modulation, millimeter wave (mmWave), visible light communication (VLC), and massive MIMO. Among these potential technologies, D2D communication is considered as one of the pieces of the 5G jigsaw puzzle. Apart from the research issues that need to be addressed before D2D is completely standardized in LTE Advanced, there will be new challenges to support D2D in 5G. In the following, we discuss two challenges in developing D2D communication technology in 5G cellular networks.



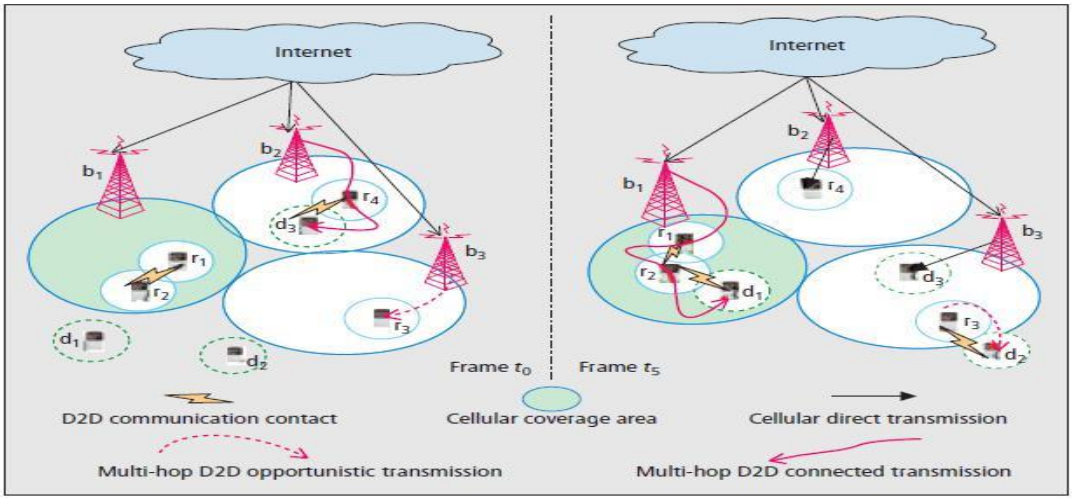
2. D2D IN MMWAVE NETWORKS

mmWave communication is a promising technology for future 5G cellular networks to provide very high data rate (multi-Gbps) for mobile devices, since it operates over a large frequency band from 30 GHz to 300 GHz. However, it also has several unique propagation features different from those of the microwave band, which lead to challenges to achieve seamless coverage and reliability. First, the propagation loss is much higher since the received signal power is proportional to the square of carrier frequency. Therefore, high-gain directional antennas are favored to compensate for the tremendous propagation loss and reduce shadowing

effect. Second, the short wavelengths of mmWave bands result in difficulties in diffracting around obstacles. Line-of-sight (LOS) transmissions can be easily blocked by obstacles, which results in link outage. Third, it is difficult for mmWave signals to penetrate through solid materials, which confines outdoor mmWave signals to streets and other outdoor structures, although some signal power might reach inside the buildings through glass windows and wood doors.

2.1 Opportunities & Advantages in enabling D2D Communication

The above propagation features provide opportunities and advantages in enabling D2D communications over directional mmWave networks. First, mmWave can be applied to D2D-enabled wireless devices for direct short range communications between users or machines in close proximity. Moreover, D2D communication can also establish a path between two wireless devices and between wireless devices and mmWave BSs by relay if LOS links between them are blocked. Second, in contrast with 4G cellular . straightforward but extremely networks where communications between BSs are perform via fiber links, mmWave communication with highly directional antennas provides wireless connections with a high data rate for BS to BS (B2B) communications. Third, interference management is one of the most important challenges to harvest the performance gain in D2D communications. Due to the directional antennas and large propagation loss, mmWave communication has relatively low multi-user interference (MUI), which can support simultaneous communications over the same radio spectrum. By allowing multiple concurrent D2D links, the network capacity and spectrum efficiency can be greatly improved. Therefore, new network architectures and resource sharing schemes accounting for the directional interference sources are necessary in mmWave 5G cellular networks to fully exploit the advantages of both technologies. effective way to increase the network capacity over several cellular generations. This is mainly due to the higher reuse of spectrum across a geographic area and the ensuing reduction in the number of users competing for resources at each BS.



3. D2D-ENABLED ULTRA- DENSE DEPLOYMENT WITH SMALL CELLS

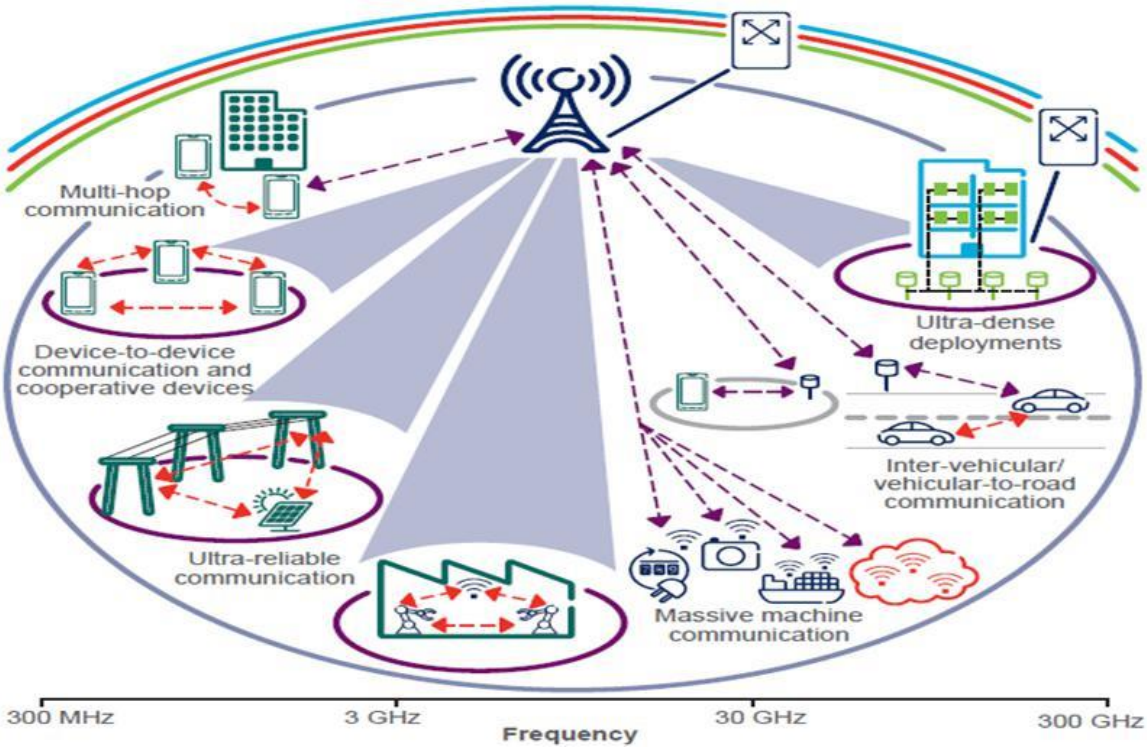
One of the main drivers behind 5G is the need to increase the capacity to cope with the mobile data traffic explosion. Ultra-densification, which means deploying more active nodes per unit area and Hz, is one of the “big three” 5G technologies along with mmWave and massive MIMO. In fact, making the cells smaller has been demonstrated as a

In 4G LTE Advanced networks, the term “small cells” refers to several quite different technologies, all of which have low-power short-range operator-owned nodes integrated in the cellular infrastructure to enhance its coverage and/or capacity. Such communication nodes go under names such as femto, pico- or micro-enhanced Node Bs (eNBs).Both D2D and small cells can be used to offload traffic from the macro-eNBs. However, D2D focuses on offloading the proximity services,

while small cells are more suitable for offloading hot-spot traffic. Therefore, integrating these two technologies to provide D2D-enabled ultra-dense deployment with small cells in 5G is an appealing solution for localized data transfers as well as general purpose downloading. However, it also poses several challenges and risks, which are

D2D pair can be from different cells, which further complicates interference control. Therefore, it is necessary to investigate how to achieve efficient interference management and develop practical inter-node

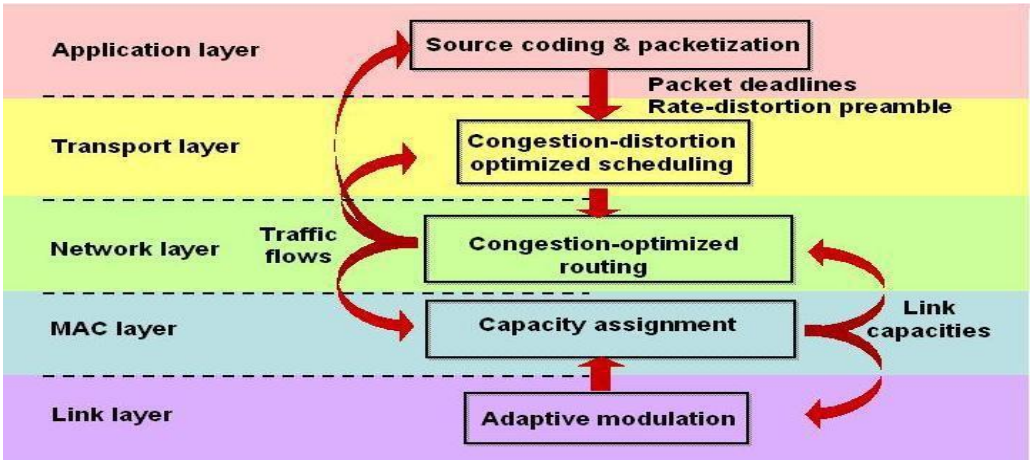
Signaling mechanisms



4. CROSS- LAYER RESOURCE CONTROL, UNDER BURSTY DATA TRAFFIC

Resource management for D2D communications in cellular networks mainly includes three function blocks: mode selection, power control, and resource allocation. Compared with the resource management in traditional cellular networks, there are more degrees of freedom in D2D communications. First, a pair of D2D centered on complex interference scenarios. When frequency reuse is applied to improve resource utilization, the interference among macro-cell cellular links, small-cell cellular links, and D2D links all should be considered and efficiently managed. Moreover, a terminals can either communicate directly over-the-air, or communicate via a BS. Moreover, the direct over-the-air link or D2D link may reuse radio resources with other cellular or D2D links. Finally, as signaling can be exchanged directly between a pair of D2D terminals due to their proximity, some of the resource management actions can be performed in a distributive way and offloaded to the D2D terminals from the BS. Such flexibility provides both opportunities and challenges in designing optimal resource control policies. Related works in the literature usually assume that theD2D and cellular terminals are saturated with infinite backlogs, and focus on optimizing the PHY layer performance metrics (such as sum throughput and

power consumption).However, the data arrival process at each terminal is dynamic and bursty in real-life applications. Moreover, latency and reliability are critical performance measures in 5G, which need to be quantified and evaluated in terms of delay and packet dropping rate under a bursty



5. CONCLUSION AND FUTURE PERSPECTIVES

Resource management for D2D communications in cellular networks mainly includes three function blocks: mode selection, power control, and resource allocation. Compared with the resource management in traditional cellular networks, there are more degrees of freedom in D2D communications. First, a pair of D2D terminals can either communicate directly over-the-air, or communicate via a BS. Moreover, the direct over-the-air link or D2D link may reuse radio resources with other cellular or D2D links. Finally, as signaling can be exchanged directly between a pair of D2D terminals due to their proximity, some of the resource management actions can be performed in a distributive way and offloaded to the D2D terminals from the BS. Such flexibility provides both opportunities and challenges in designing optimal resource control policies. Related traffic model. To derive the optimal resource allocation policies for bursty data traffic, cross-layer design and stochastic optimization, which take advantage of both the channel state information (CSI) and the queue state information (QSI), should be applied. Although cross-layer performance evaluation and resource optimization in conventional cellular networks and wireless multihop networks have been well studied, these research issues in D2D communications require further research.

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much larger and more diverse set of devices and applications. Although there have been intense research activities on D2D communications in recent years, there are still many challenging issues to be addressed, especially in terms of network architectures, physical layer features, and performance requirements in 5G. I hope that you enjoy reading this Editor's Note and find it interesting and helpful.

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RFID Based Door Locking System Using finger print

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ABSTRACT

Security has been assuming a key part in a large number of our places like workplaces, establishments, libraries, research facilities and so forth with a specific end goal to keep our information secretly so no other unapproved individual could have an entrance on them. These days, at each purpose of time, we require security frameworks for assurance of significant information and even cash. This paper shows a unique mark based entryway opening framework which gives security which can be utilized for some, banks, foundations and different associations etc..,. There are different techniques for checking confirmation through secret key, RFID however this strategy is most effective and solid. To give idealize security to the bank lockers and to make the work less demanding, this undertaking is taking help of two distinct innovations viz. Implanted SYSTEMS and BIOMETRICS. Unapproved get to is restricted by outlining a bolt that stores the fingerprints of at least one approved clients. Unique mark is detected by sensor and is approved for verification. In the event that the unique finger impression coordinates, the entryway will be opened naturally generally the signal associated with a sound intensifier will be initiated so the general population close to the environment will get a caution.

Keywords: Biometrics, Fingerprint, Authentication, Alarm, Security.

INTRODUCTION

Security is of primary concern and in this busy, competitive world, human cannot find ways to provide security to his confidential belongings manually. Instead, he finds an alternative which can provide a full fledged security as well as atomized. In the ubiquitous network society, where individuals can easily access their information anytime and anywhere, people are also faced with the risk that others can easily access the same information anytime and anywhere. Because of this risk, personal identification technology, which can distinguish between registered legitimate users and imposters, is now generating interest. Generally passwords, identification cards and PIN verification techniques are being used but the disadvantage is that the passwords could be hacked and a card may be stolen or lost. The most secured system is fingerprint recognition because a fingerprint of one person never matches the other. Biometrics studies commonly include fingerprint, face, iris, voice, signature, and hand geometry recognition and verification. Many other modalities are in various stages of development and assessment. Among these available biometric traits fingerprint proves to be one of the best traits providing good mismatch ratio, high accurate in terms of security and also reliable.

BACKGROUND

Various attempts are made for providing security for all domiciles. Up to date, complete security is not discovered.

i. Lock and Key System:

First step towards security was Lock and key system. Security protocol followed in this system was “Single key for a single lock”. Initially, this system was considered to provide atmost security. But this belief was soon proved wrong by the fact that multiple keys can be easily made for a single lock. Hence this system is an outdated system to provide security.

ii. Password Authentication:

Next level of Security used password as an authenticating tool. This system stores password of authenticated users for the purpose of validation. System using password authentication provides considerable security to the users as it acts as a secret of authorized users. This system also have a pitfall that password can be acquired by unauthorized user by continuously trying all the possible combinations. This is also one among the hundreds of attempt made for providing security.

iii. Authentication by RFID card:

Next level of technological development for providing security was authentication by RFID card. This system enriched the level of security. Access is granted only for the user whose RFID code matches with the authorized code. This system also have disadvantage of duplication of RFID card and anyone who possess this card can unlock the door.

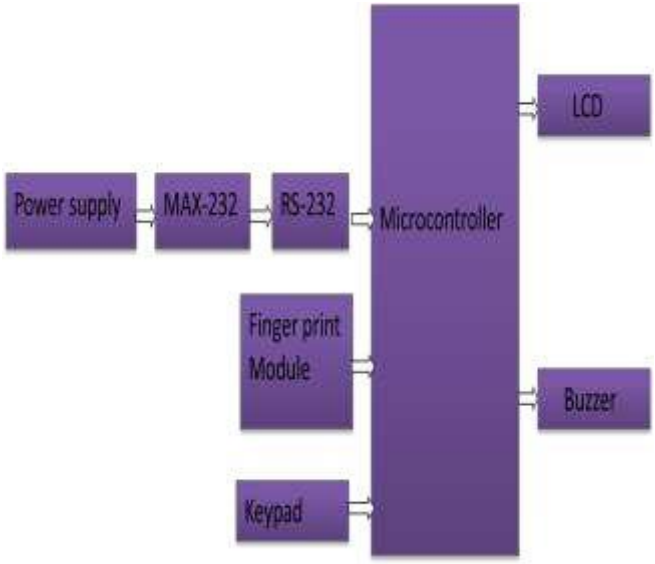
SCOPE OF RESEARCH

In future, alarm will be introduced. When intruder tries to break the door, the vibration is sensed by sensor which makes an alarm. This will inform the neighbors about intruders and this will help to take further action to prevent intruder from entering.

PROPOSED METHODOLOGY

Our proposed system overcomes all the security problems in existing system and provides high security and efficiency. This is a perfect/optimal solution for saving/protecting one from the hassle of stolen/lost key or an unauthorized entry. Fingerprint is a boon solution for these problems which provides high level of recognition accuracy. The skin on our palms and soles exhibits a flow like pattern of ridges called friction ridges. The pattern of friction ridges on each finger is unique and immutable. This makes fingerprint a unique identification for everyone. Fingerprint door lock incorporates the proven technology. Fingerprint scanner scans the fingerprints of users and used for ensuring authentication. Fingerprint scanning is more accurate and cost effective method and duplication is virtually impossible. A Fingerprint recognition system can easily perform verification. In verification, the system compares an input fingerprint to the enrolled fingerprint of a specific user to determine if they are from the same finger. Now the security of our home/office is literally in our hands or rather on our fingertips.

PROPOSED MODEL OF THE SYSTEM



RELATED DISCUSSION

When fingerprint module is interfaced to the microcontroller, it will be in user mode. In this mode, stored images will be verified with the scanned images. When coming to our application the images of the person's fingerprint that are authorized to open the locker door will be stored in the module with a unique id. To prove that the persons are authorized to open the locker door they need to scan their fingerprint images. The scanner is interfaced to 8051 microcontroller; this controller will be controlling the scanning process. After the scanning has been completed, user has to

enter the password to open his locker with the help of a keypad. Immediately the locker will be opened. After the work has been completed if key is pressed again with help of keypad the locker door will be closed again. If an unauthorized person tries to scan his fingerprint image then an indication will be given by a
buzzer which is interfaced to the controller and also if wrong password is entered by the user again indication will be given by the buzzer. The current user instead of him/her can make a new person as the user of the same locker by new registration process and the old user's fingerprint image will be deleted. Option for changing the password is also available.

EXPERIMENTAL RESULTS

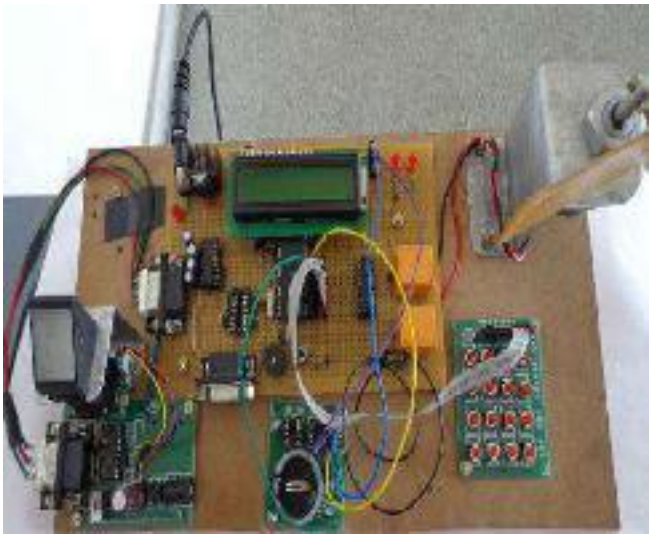


Figure 1. Hardware part

Figure2. Initial display on LCD when power is turned on.

Figure3. Indication to scan the finger.

Figure 4.Scanning the finger.

Step 1: When power is supplied to the board, the initial displays on the LCD are as shown below.
Step 2: When the fingerprint is mismatched.
Step 3: When the persons fingerprint matches, display on LCD.
Step 4: We need to enter the valid password.
Step 5: When invalid password is entered display on LCD.
Step 6: When the password is matched, it displays two options.
Step 7: When option 1 is selected, displays on LCD.
Step 8: After work has been completed, we have to press key 3 for closing the locker door and it goes back to step 1.
Step 9: After step 5 when option 2 is selected, it displays four options. Select required option, for

The main advantages of using this system are:

1. Easy to use and requires no special training or equipment.
2. Fingerprint is unique for every person it cannot be imitated or fabricated .It is not same in the case of twins also.
3. High accuracy in terms of security.
4. No manual errors.
5. No false intrusions

CONCLUSIONS

A step by step approach in designing the microcontroller based system for securing the transactions of the user and providing the security for the locker system and even more for the PASSPORT verification using a finger print scanner has been followed. The result obtained in providing the security is quite reliable in all the three modes. The system has successfully overcome some of the aspects existing with the present technologies, by the use of finger print Biometric as the authentication Technology.

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Implementation of Wideband Spectrum Sensing For Performance Improvement of Cognitive Radio

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***Abstract*— Cognitive radio has emerged as one of the most promising candidate solutions to improve spectrum utilization in next generation cellular networks. A crucial requirement for future cognitive radio networks is wideband spectrum sensing: secondary users reliably detect spectral opportunities across a wide frequency range. In this article, various wideband spectrum sensing algorithms are presented, together with a discussion of the pros and cons of each algorithm and the challenging issues. Special attention is paid to the use of sub-Nyquist techniques, including compressive sensing and multi-channel sub-Nyquist sampling techniques.**

***Index Terms*— Cellular network, cognitive radio, compressive sensing, spectrum sensing, sub-Nyquist sampling, wideband spectrum sensing.**

I. INTRODUCTION

Radio frequency (RF) spectrum is a valuable but tightly regulated resource due to its unique and important role in wireless communications. With the proliferation of wireless services, the demands for the RF spectrum are constantly increasing, leading to scarce spectrum resources. On the other hand, it has been reported that localized temporal and geographic spectrum utilization is extremely low [1]. Currently, new spectrum policies are being developed by the Federal Communications Commission (FCC) that will allow secondary users to opportunistically access a licensed band, when the primary user (PU) is absent. Cognitive radio [2], [3] has become a promising solution to solve the spectrum scarcity problem in the next generation cellular networks by exploiting opportunities in time, frequency, and space domains.

Cognitive radio is an advanced software-defined radio that automatically detects its surrounding RF stimuli and intelligently adapts its operating parameters to network infrastructure while meeting user demands. Since cognitive radios are considered as secondary users for using the licensed spectrum, a crucial requirement of cognitive radio networks is that they must efficiently exploit under-utilized spectrum (denoted as spectral opportunities) without causing harmful interference to the PUs. Furthermore, PUs have no obligation to share and change their operating parameters for sharing spectrum with cognitive radio networks. Hence, cognitive radios should be able to independently detect spectral opportunities without any assistance from PUs; this ability is called spectrum sensing, which is considered as one of the most critical components in cognitive radio networks.

Many narrowband spectrum sensing algorithms have been studied in the literature [4] and references therein, including matched-filtering, energy detection [5], and cyclostationary feature detection. While present narrowband spectrum sensing algorithms have focused on exploiting spectral opportunities over narrow frequency range, cognitive radio networks will eventually be required to exploit spectral opportunities over wide frequency range from hundreds of megahertz (MHz) to several gigahertz (GHz) for achieving higher opportunistic throughput. This is driven by the famous Shannon's formula that, under certain conditions, the maximum theoretically achievable bit rate is directly proportional to the spectral bandwidth. Hence, different from narrowband spectrum sensing, wideband spectrum sensing aims to find more spectral opportunities over wide frequency range and achieve higher opportunistic aggregate throughput in cognitive radio networks. However, conventional wideband spectrum sensing techniques based on standard analog-to-digital converter (ADC) could lead to unaffordably high sampling rate or implementation complexity; thus, revolutionary wideband spectrum sensing techniques become increasingly important.

In the remainder of this article, we first briefly introduce the traditional spectrum sensing algorithms for narrowband sensing in Section II. Some challenges for realizing wideband spectrum sensing are then discussed in Section III. In addition, we categorize the existing wideband spectrum sensing algorithms based on their implementation types, and review the state-of-the-art techniques for each category. Future research challenges for implementing wideband spectrum sensing are subsequently identified in Section IV, after which concluding remarks are given in Section V.

II. NARROWBAND SPECTRUM SENSING

The most efficient way to sense spectral opportunities is to detect active primary transceivers in the vicinity of cognitive radios. However, as primary receivers may be passive, such as TVs, some receivers are difficult to detect in practice. An alternative is to detect the primary transmitters by using

traditional narrowband sensing algorithms, including matched-filtering, energy detection, and cyclostationary feature detection as shown in Fig. 1. Here, the term "narrowband" implies that the frequency range is sufficiently narrow such that the channel frequency response can be considered flat. In other words, the bandwidth of our interest is less than the coherence bandwidth of the channel. The implementation of these narrowband algorithms requires different conditions, and their detection performance are correspondingly distinguished. The advantages and disadvantages of these algorithms are summarized in Table I.

The matched-filtering method is an optimal approach for spectrum sensing since it maximizes the signal-to-noise ratio (SNR) in the presence of additive noise. This advantage is achieved by correlating the received signal with a template for detecting the presence of a known signal in the received signal. However, it relies on prior knowledge of the PUs and requires cognitive radios to be equipped with carrier synchronization and timing devices, leading to increased implementation complexity. Energy detection [5] is a non-coherent detection method that avoids the need for prior knowledge of the PUs and the complicated receivers required by a matched filter. Both the implementation and the computational complexity are relatively low. A major drawback is that it has poor detection performance under low SNR scenarios and cannot differentiate between the signals from PUs and the interference from other cognitive radios. Cyclostationary feature detection method detects and distinguishes between different types of primary signals by exploiting their cyclostationary features. However, the computational cost of such an approach is relatively high, because it requires to calculate a two-dimensional function dependent on both frequency and cyclic frequency.

III. WIDEBAND SPECTRUM SENSING

Against narrowband techniques as mentioned above, wideband spectrum sensing techniques aim to sense a frequency bandwidth that exceeds the coherence bandwidth of the channel. For example, for exploiting spectral opportunities in the whole ultra-high frequency (UHF) TV band (between 300 MHz and 3 GHz), wideband spectrum sensing techniques should be employed. We note that narrowband sensing techniques cannot be directly used for performing wideband spectrum sensing, because they make a single binary decision for the whole spectrum and thus cannot identify individual spectral opportunities that lie within the wideband spectrum. As shown in Table II, wideband spectrum sensing can be broadly categorized into two types: Nyquist wideband sensing and sub-Nyquist wideband sensing. The former type processes digital signals taken at or above the Nyquist rate, whereas the latter type acquires signals using sampling rate lower than the Nyquist rate. In the rest of this article, we will provide an overview of the state-of-the-art wideband spectrum sensing algorithms and discuss the pros and cons of each algorithm.

A. Nyquist Wideband Sensing

A simple approach of wideband spectrum sensing is to directly acquire the wideband signal using a standard ADC and then use digital signal processing techniques to detect spectral opportunities. For example, Quan et al. [6] proposed a multi-band joint detection algorithm that can sense the primary signal over multiple frequency bands. As shown in Fig. 2(a), the wideband signal x(t) was firstly sampled by a high sampling rate ADC, after which a serial to parallel conversion circuit (S/P) was used to divide sampled data into parallel data streams. Fast Fourier transform (FFT) was used to convert the wideband signals to the frequency domain. The wideband spectrum X(f) was then divided into a series of narrowband spectra X1(f), · · · , Xv(f). Finally, spectral opportunities were detected using binary hypotheses tests, where H0 denotes the absence of PUs and H1 denotes the presence of PUs. The optimal detection threshold was jointly chosen by using optimization techniques. Such an algorithm can achieve better performance than the single band sensing case.

Furthermore, by also using a standard ADC, Tian and Giannakis proposed a wavelet-based spectrum sensing algorithm in [7]. In this algorithm, the power spectral density (PSD) of the wideband spectrum (denoted as S(f)) was modeled as a train of consecutive frequency subbands, where the PSD is smooth within each subband but exhibits discontinuities and irregularities on the border of two neighboring subbands. The wavelet transform was then used to locate the singularities of the wideband PSD, and the wideband spectrum sensing was formulated as a spectral edge detection problem as shown in Fig. 2(b).

However, special attention should be paid to the signal sampling procedure. In these algorithms, sampling signals should follow Shannon's celebrated theorem: the sampling rate must be at least twice the maximum frequency present in the signal (known as Nyquist rate) in order to avoid spectral aliasing. Suppose that the wideband signal has frequency range 0 ∼ 10 GHz, it should be uniformly sampled by a standard ADC at or above the Nyquist rate 20 GHz which will be unaffordable for next generation cellular networks. Therefore, sensing wideband spectrum presents significant challenges on building sampling hardware that operates at a sufficiently high rate, and designing high-speed signal processing algorithms. With current hardware technologies, high-rate ADCs with high resolution and reasonable power consumption (e.g., 20 GHz sampling rate with 16 bits resolution) are difficult to implement. Even if it comes true, the real-time digital signal processing of sampled data could be very expensive.

One naive approach that could relax the high sampling rate requirement is to use superheterodyne (frequency mixing) techniques that "sweep" across the frequency range of interest as shown in Fig. 2(c). A local oscillator (LO) produces a sine wave that mixes with the wideband signal and down-converts it to a lower frequency. The down-converted signal is then filtered by a bandpass filter (BPF), after which existing narrowband spectrum sensing techniques in Section II can be

applied. This sweep-tune approach can be realized by using either a tunable BPF or a tunable LO. However, this approach is often slow and inflexible due to the sweep-tune operation. Another solution would be the filter bank algorithm presented by Farhang-Boroujeny [8] as shown in Fig. 2(d). A bank of prototype filters (with different shifted central frequencies) was used to process the wideband signal. The base-band can be directly estimated by using a prototype filter, and other bands can be obtained through modulating the prototype filter. In each band, the corresponding portion of the spectrum for the wideband signal was down-converted to base-band and then low-pass filtered. This algorithm can therefore capture the dynamic nature of wideband spectrum by using low sampling rates. Unfortunately, due to the parallel structure of the filter bank, the implementation of this algorithm requires a large number of RF components.

B. Sub-Nyquist Wideband Sensing

Due to the drawbacks of high sampling rate or high implementation complexity in Nyquist systems, sub-Nyquist approaches are drawing more and more attention in both academia and industry. Sub-Nyquist wideband sensing refers to the procedure of acquiring wideband signals using sampling rates lower than the Nyquist rate and detecting spectral opportunities using these partial measurements. Two important types of sub-Nyquist wideband sensing are compressive sensing-based wideband sensing and multi-channel sub-Nyquist wideband sensing. In the subsequent paragraphs, we give some discussions and comparisons regarding these sub-Nyquist wideband sensing algorithms.

1) Compressive Sensing-based Wideband Sensing: Compressive sensing is a technique that can efficiently acquire a signal using relatively few measurements, by which unique representation of the signal can be found based on the signal's sparseness or compressibility in some domain. As the wideband spectrum is inherently sparse due to its low spectrum utilization, compressive sensing becomes a promising candidate to realize wideband spectrum sensing by using subNyquist sampling rates. Tian and Giannakis firstly introduced compressive sensing theory to sense wideband spectrum in [9]. This technique used fewer samples closer to the information rate, rather than the inverse of the bandwidth, to perform wideband spectrum sensing. After reconstruction of the wideband spectrum, wavelet-based edge detection was used to detect spectral opportunities across wideband spectrum.

Furthermore, to improve the robustness against noise uncertainty, Tian et al. [10] studied a cyclic feature detection-based compressive sensing algorithm for wideband spectrum sensing. It can successfully extract second-order statistics of wideband signals from digital samples taken at sub-Nyquist rates. The 2-D cyclic spectrum (spectral correlation function) of a wideband signal can be directly reconstructed from the compressive measurements. In addition, such an algorithm is also valid for reconstructing the power spectrum of wideband signal, which is useful if the energy detection algorithm is used for detecting spectral opportunities.

For further reducing the data acquisition cost, Zeng et al. [11] proposed a distributed compressive sensing-based wideband sensing algorithm for cooperative multi-hop cognitive radio networks. By enforcing consensus among local spectral estimates, such a collaborative approach can benefit from spatial diversity to mitigate the effects of wireless fading. In addition, decentralized consensus optimization algorithm was proposed that aims to achieve high sensing performance at a reasonable computational cost.

However, compressive sensing has concentrated on finite-length and discrete-time signals. Thus, innovative technologies are required to extend the compressive sensing to continuoustime signal acquisition, i.e., implementing compressive sensing in analog domain. To realize the analog compressive sensing, Tropp et al. [12] proposed an analog-to-information converter (AIC), which could be a good basis for the above-mentioned algorithms. As shown in Fig. 3(a), the AIC-based model consists of a pseudo-random number generator, a mixer, an accumulator, and a low-rate sampler. The pseudo-random number generator produces a discrete-time sequence that demodulates the signal x(t) by a mixer. The accumulator is used to sum the demodulated signal for 1/w seconds, while its output signal is sampled using a low sampling rate. After that, the sparse signal can be directly reconstructed from partial measurements using compressive sensing algorithms. Unfortunately, it has been identified that the performance of AIC model can be easily affected by design imperfections or model mismatches.

2) *Multi-channel Sub-Nyquist Wideband Sensing*: To circumvent model mismatches, Mishali and Eldar proposed a modulated wideband converter (MWC) model in [13] by modifying the AIC model. The main difference between MWC and AIC is that MWC has multiple sampling channels, with the accumulator in each channel replaced by a general low-pass filter. One significant benefit of introducing parallel channel structure in Fig. 3(b) is that it provides robustness against the noise and model mismatches. In addition, the dimension of the measurement matrix is reduced, making the spectral reconstruction more computationally efficient. An alternative multi-channel sub-Nyquist sampling approach is the multi-coset sampling as shown in Fig. 3(c). The multi-coset sampling is equivalent to choosing some samples from a uniform grid, which can be obtained using a sampling rate fs higher than the Nyquist rate. The uniform grid is then divided into blocks of m consecutive samples, and in each block v($v < m$) samples are retained while the rest of samples are skipped. Thus, the multi-coset sampling is often implemented by using v sampling channels with sampling rate of fs m , with different sampling channels having different time offsets. To obtain a unique solution for the wideband spectrum from these partial measurements, the sampling pattern should be carefully designed. In [14], some sampling patterns were proved to be

valid for unique signal reconstruction. The advantage of multi-coset approach is that the sampling rate in each channel is m times lower than the Nyquist rate. Moreover, the number of measurements is only v-mth of that in the Nyquist sampling case. One drawback of the multi-coset approach is that the channel synchronization should be met such that accurate time offsets between sampling channels are required to satisfy a specific sampling pattern for a robust spectral reconstruction.

To relax the multi-channel synchronization requirement, asynchronous multi-rate wideband sensing approach was studied in [15]. In this approach, sub-Nyquist sampling was induced in each sampling channel to wrap the sparse spectrum occupancy map onto itself; the sampling rate can therefore be significantly reduced. By using different sampling rates in different sampling channels as shown in Fig. 3(d), the performance of wideband spectrum sensing can be improved. Specifically, in the same observation time, the numbers of samples in multiple sampling channels are chosen as different consecutive prime numbers. Furthermore, as only the magnitudes of subNyquist spectra are of interest, such a multi-rate wideband sensing approach does not require perfect synchronization between multiple sampling channels, leading to easier implementation.

IV. RESEARCH CHALLENGES

In this section, we identify the following research challenges that need to be addressed for implementing a feasible wideband spectrum sensing device for future cognitive radio networks.

A. Sparse Basis Selection

Nearly all sub-Nyquist wideband sensing techniques require that the wideband signal should be sparse in a suitable basis. Given the low spectrum utilization, most of existing wideband sensing techniques assumed that the wideband signal is sparse in the frequency domain, i.e., the sparsity basis is a Fourier matrix. However, as the spectrum utilization improves, e.g., due to the use of cognitive radio techniques in future cellular networks, the wideband signal may not be sparse in the frequency domain any more. Thus, a significant challenge in future cognitive radio networks is how to perform wideband sensing using partial measurements, if the wideband signal is not sparse in the frequency domain. It will be essential to study appropriate wideband sensing techniques that are capable of exploiting sparsity in any known sparsity basis. Furthermore, in practice, it may be difficult to acquire sufficient knowledge about the sparsity basis in cognitive radio networks, e.g., when we cannot obtain enough prior knowledge about the primary signals. Hence, future cognitive radio networks will be required to perform wideband sensing when the sparsity basis is not known. In this context, a challenging issue is to study “blind” sub-Nyquist wideband sensing algorithms, where we do not require prior knowledge about the sparsity basis for the sub-Nyquist sampling or the spectral reconstruction.

B. Adaptive Wideband Sensing

In most of sub-Nyquist wideband sensing systems, the required number of measurements will proportionally change when the sparsity level of wideband signal varies. Therefore, sparsity level estimation is often required for choosing an appropriate number of measurements in cognitive radio networks. However, in practice, the sparsity level of wideband signal is often time-varying and difficult to estimate, because of either the dynamic activities of PUs or the timevarying fading channels between PUs and cognitive radios. Due to this sparsity level uncertainty, most of sub-Nyquist wideband sensing systems should pessimistically choose the number of measurements, leading to more energy consumption in cellular networks. As shown in Fig. 4, more measurements (i.e., 0.38N rather than 0.25N measurements for achieving the success recovery rate 0.9) are required for the sparsity uncertainty between 10 and 20, which does not fully exploit the advantages of using sub-Nyquist sampling technologies. Hence, future cognitive radio networks should be capable of performing wideband sensing, given the unknown or timevarying sparsity level. In such a scenario, it is very challenging to develop adaptive wideband sensing techniques that can intelligently/quickly choose an appropriate number of compressive measurements without the prior knowledge of the sparsity level.

C. Cooperative Wideband Sensing

In a multipath or shadow fading environment, the primary signal as received at cognitive radios may be severely degraded, leading to unreliable wideband sensing results in each cognitive radio. In this situation, future cognitive radio networks should employ cooperative strategies for improving the reliability of wideband sensing by exploiting spatial diversity. Actually, in a cluster-based cognitive radio network, the wideband spectra as observed by different cognitive radios could share some common spectral components, while each cognitive radio may observe some innovative spectral components. Thus, it is possible to fuse compressive measurements from different nodes and exploit the spectral correlations among cognitive radios in order to save the total number of measurements and thus the energy consumption in cellular networks. Such a data fusion-based cooperative technique, however, will lead to heavy data transmission burden in the common control channels. It is therefore challenging to develop data fusion-based cooperative wideband sensing techniques subject to relaxed data transmission burden. An alternative is to develop decision fusion-based wideband sensing techniques, if each cognitive radio is able to detect wideband spectrum independently. Due to the limited computational resource in cellular networks, the challenge that remains in the decision fusion-based cooperative approach is how to appropriately combine information in real time.

V. CONCLUSION

In this article, we first addressed the challenges in the design and implementation of wideband spectrum sensing algorithms for the cognitive radio-based next generation cellular networks. Then, we categorized the existing wideband spectrum sensing algorithms based on their sampling types and discussed the pros and cons of each category. Moreover, motivated by the fact that wideband spectrum sensing is critical for reliably finding spectral opportunities and achieving opportunistic spectrum access for next generation cellular networks, we made a brief survey of the state-of-the-art wideband spectrum sensing algorithms. Finally, we presented several open research issues for implementing wideband spectrum sensing.

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Low Power High speed CSLA

P. Gupta, N. Raj and P. John Paul

***Abstract*— This paper presents a modified design of Area-Efficient Low power Carry Select Adder (CSLA) Circuit. In digital adders, the speed of addition is limited by the time required to transmit a carry through the adder. Carry select adder processors and systems. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries.**

***Index Terms*— Area-efficient, Low power, CSLA, Binary to excess one converter, Multiplexer.**

I. Introduction

CONVENTIONAL carry select adder (CLSA) performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder to excess-1 code converters (BEC) to improve the speed of addition.

This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure. The basic idea of the proposed work is by using n-bit binary to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

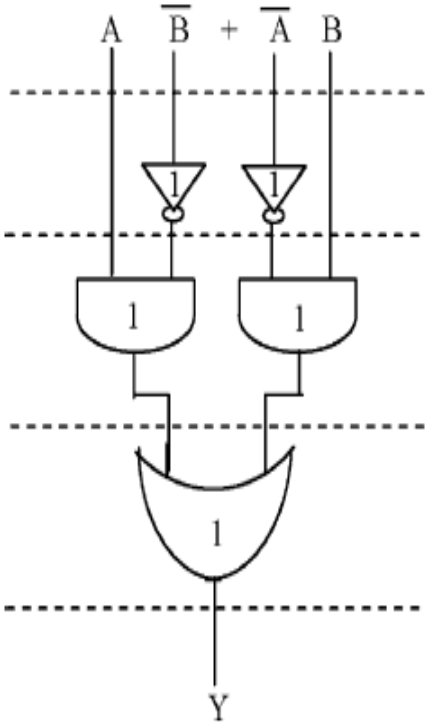

Figure 1: Delay and Area evaluation of an XOR gate

Table 1
Delay and Area Evaluation of the Basic Blocks of CSLA

Basic Blocks	Delay	Area
XOR	3	5
2:1 MUX	3	4
Half Adder	3	6
Full Adder	6	13

II. BASIC STRUCTURE OF BEC LOGIC

Conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path. However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder area and power consumption

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of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-bit BEC are shown in Figure.2 and Table 2, respectively.

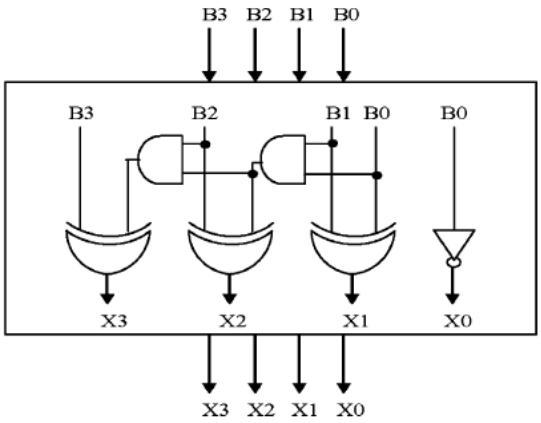


Figure 2: 4-Bit BEC

The Boolean expressions of the 4-bit BEC are

X0 = ~B0 (1)

X1 = B0^B1 (2)

X2 = B2^ (B0 & B1) (3)

X3 = B3^ (B0 & B1 & B2) (4)

Table.2 Function table of the 4-bit BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
|	|
	|
|	|
1110	|
1111	1111
	0000

III. BASIC STRUCTURE OF REGULAR 16-BIT CSLA

The structure of the 16-b regular SQRT CS conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder

{c6, sum [6:4]} = c3 [t=10] +mux (5)

{c10, sum [10:7]} = c6 [t=13] +mux (6)

{Cout, sum [15:11]}=c10 [t=16] +mux. (7)

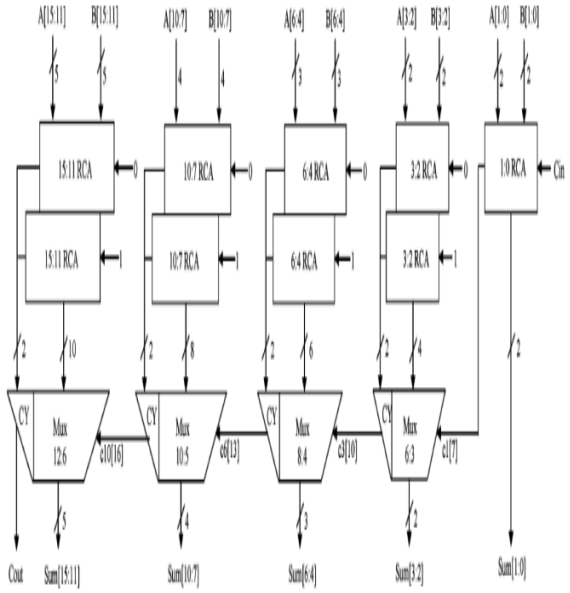


Figure 3: Regular CSLA circuit

The one set of 2-b RCA in group2 has 2 FA for Cin=1 and the other set has 1 FA and 1 HA for Cin=0.

Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:

Gate Count = 57 (FA+HA+MUX) (8)

FA=39(3*13) (9)

HA=6(1*6) (10)

MUX=12(3*4) (11)

Table 3

Group	Delay	Area
2	11	57
3	13	87
4	16	117
5	19	147

Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in Table 3.

IV. DELAY AND AREA EVALUATION OF CSLA USING BEC CONVERTER

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with Cin=1 to optimize the area and power is shown in Fig. 4. We again split the structure into five groups. The steps leading to the conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder) are depending on s3and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

The area count of group2 is determined as follows:

Gate count =43(FA+HA+MUX+BEC) (12)

FA= 13(1*13) (13)

HA=6(1*6) (14)

AND=NOT=1 (15)

XOR=10(2*5) (16)

MUX=12(3*4) (17)

Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table 4.

Table 4

Group	Delay	Area
2	13	43
3	16	61
4	19	84
5	22	107

Comparing Tables 3and 4, it is clear that the proposed modified CSLA saves 113 gate areas than the regular CSLA, with only 11 increases in gate delays.

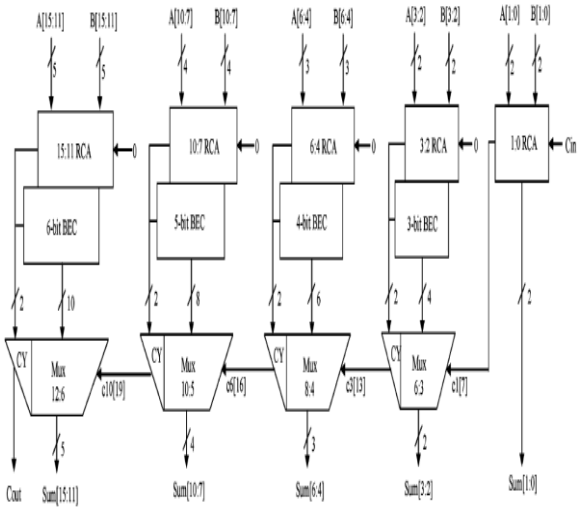
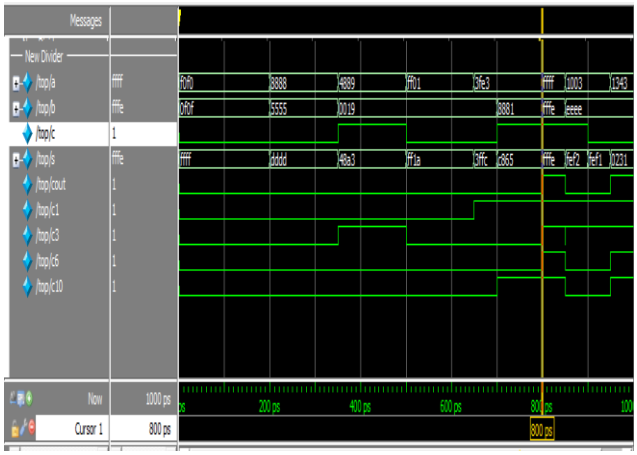


Figure 4: CSLA circuit using BEC Converter

V. SIMULATIONS AND EXPERIMENTAL RESULTS

The proposed solutions have been designed using Xilinx. The area-efficient carry select adder can also achieve an outstanding performance in power consumption. Power consumption can be greatly saved in our proposed area-efficient carry select adder because we only need one XOR gate and one INV gate in each summation operation as well as



one AND gate and one OR gate in each carry-out operation after logic simplification and sharing partial circuit. Because of hardware sharing, we can also significantly reduce the occurring chance of glitch. Besides, the improvement of power consumption can be more obvious as the input bit number increases.

Figure 5: Simulated Results

The conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path. However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder design; the delay increment of the proposed design is similar to that in the conventional design as the input bit number increases. We also simulated the delay performance in the proposed area-efficient adder and

conventional carry select adder with 4, 8, 16, and 32-bit respectively.

VI. CONCLUSION

The BEC logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure.is therefore, low area, low power, simple and efficient for VLSI hardware implementation.

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An Overview of 5G Technology

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Abstract: 5G (5th generation mobile networks) stand for the next major phase of mobile telecommunications standards beyond the current 4G/IMT - Advanced standards. 5G has speeds further what the present 4G can provide. From generation 1G to 2.5G and from 3G to 5G this world of telecommunication has seen a number of advancement along with improved performance with every passing day. This fast change in mobile computing gives us change our day to day life that is way we work, interact, learn etc. This paper also highlight on all preceding generations of mobile communication along with fifth generation technology. The development of 5 G technologies i s a c o r n e r s t o n e f o r realizing breakthroughs in the transformation of ICT network infrastructure. Ultra-broadband and intelligent-pipe network features that achieve near- instantaneous, "zero distance" connectivity between people and connected machines – no matter where they are – are just the first step. In this paper also we discuss architecture, waveform concept, requirements etc.

Keywords—5 G, zero distance, speed, performance.

I. INTRODUCTION

A new mobile generation has came approximately every 10 years since the first 1G system, Telephone, was introduced in 1982. The first 2G system was commercially came in 1992, and the first 3G system came in 2001. 4G systems fully compliant with IMT Advanced were first standardized in 2012. The development of the 2G (GSM) and 3G (IMT-2000 and UMTS) standards took about 10 years from the official start of the R&D projects, and development of 4G systems began in 2001 or 2002. In April 2008, NASA assists with Machine-to-Machine Intelligence (M2Mi) Corp to develop 5G communication technology.

As the different generations of cellular telecommunications have evolved, each one has brought its own improvement. The same will be true of 5G technology.

- First generation, 1G: These phones were analogue and were the first mobile or cellular phones to be used. Although revolutionary in their time they provide very low levels of spectrum efficiency and security.
- Second generation, 2G: These were based around digital technology and provide much better spectrum efficiency, security and new features such as text messages and low data rate communications.
- Third generation, 3G: The main goal of this technology was to provide high speed data. The original technology was enhanced to allow data up to 14Mbps and more.
- Fourth generation, 4G: This was an all-IP based technology capable of providing data rates up to 1Gbps.

Any new 5th generation, 5G cellular technology needs to provide significant benefits over previous systems to give an enough business case for mobile operators to invest in any new system. Facilities that might be seen with 5G technology include far better levels of connectivity and coverage. The term World Wide Wireless Web or WWWW is being coined for this. For 5G technology to be able to achieve this, new methods of connecting will be required as one of the main drawbacks with previous generations is lack of coverage, dropped calls and low performance at cell edges. 5G technology will need to address this.

A) 5G specifications

Although the standards bodies have not yet defined the parameters needed to meet a 5G performance level yet,

other organizations have set their own aims that may eventually influence the final specifications.

Typical parameters for a 5G standard may include:

SUGGESTED 5G WIRELESS PERFORMANCE	
PARAMETER	SUGGESTED PERFORMANCE
Network capacity	10 000 times capacity of current network
Peak data rate	10 Gbps
Cell edge data rate	100 Mbps
Latency	< 1 ms

These are some of the ideas being put forwards for a 5G standard, but they are not accepted by any official bodies yet.

II. 5G Mobile Network Architecture

Figure 1 shows network architecture for 5G mobile systems. Architecture of 5G is highly advanced; its network elements and various terminals are characteristically improved to allow a new situation. Likewise, service providers can implement the advance technology to accept the value-added services easily. It is all-IP based model for wireless and mobile networks interoperability. The IP technology is designed exclusively to ensure sufficient control data for appropriate routing of IP packets associated to a certain application connections i.e. sessions between client applications and servers somewhere on the Internet. The system resides of a user terminal (which has a crucial role in the new architecture) and a number of free, autonomous radio access technologies. Within each of the terminals, each of the radio access technologies is examine as the IP link to the outside Internet world. However, there should be different radio interface for each Radio
Access Technology (RAT) in the mobile terminal. For an example, if we want to have access to four different RATs, we require to have four different accesses - specific interfaces in the mobile terminal, and to have all of them effective at the same time, with aim to have this architecture to be functional.

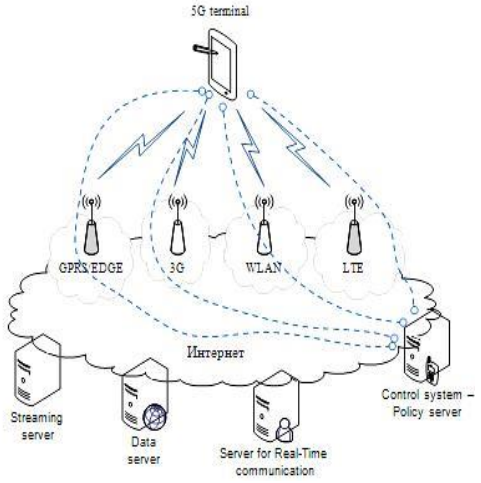

Figure 1 Functional Architecture for 5G Mobile Networks

III. 5G waveform background

Orthogonal frequency division multiplexing has been an excellent waveform choice for 4G. It provides superior spectrum efficiency, it can be processed and controlled with the processing levels achievable in current mobile handsets, and it operates better with high data rate stream covering wide bandwidths. It performs well in situations where there is selective fading.

However with the advances in to achieve a result of capabilities that will be available by 2020 when 5G is wanted to have its first cast means that other waveforms can be considered.

There are several advantages to the use of new waveforms for 5G. OFDM wants the use of a cyclic prefix and this occupies space within the data streams.

There are also other benefits that can be introduced by using one of a variety of new waveforms for 5G.

One of the key requirements is the opportunity of processing power. Although Moore's Law in its basic form is running to the limits of device feature sizes and further advances in miniaturization are unlikely for a while, other techniques are being developed that mean the energy of Moore's Law is able to continue and processing capability will increase. As such new 5G waveforms that need additional processing power, but are able to provide additional advantages are still viable.

A) 5G waveform requirements

The potential applications for 5G containing high speed video downloads, gaming, car-to-car / car-to-infrastructure communications, general cellular communications, IoT / M2M communications and the like, all place requirements on the form of 5G waveform scheme that can support the required performance.

Some of the key requirements that need to be provided by the modulation scheme and overall waveform include:

- Capable of handling high data rate wide bandwidth signals
- Capable to provide low latency transmissions for long and short data bursts, i.e. very short Transmission Tine Intervals, TTIs, are required.
- It give fast switching between uplink and downlink for TDD systems that are likely to be used.
- Allow the possibility of energy efficient communications by minimizing the on-times for low data rate devices.

These are a few of the necessity that are needed for 5G waveforms to support the facilities that are needed.

IV. Other 5G concepts

There are many new concepts that are being examined and developed for the new 5th generation mobile system. Some of these involve:

- **Pervasive networks*:*** This technique being considered for 5G cellular systems is where a user can together be connected to several wireless access technologies and seamlessly moves between them.
- **Group co-operative relay*:*** This is a technology that is being considered to make the high data rates available over a wider area of the cell. Currently data rates decreasing towards the cell edge where interference levels are higher and signal levels lower.
- **Cognitive radio technology*:*** In case cognitive radio technology was used for 5th generation, 5G cellular systems, then it would allow the user equipment / handset to see at the radio landscape in which it is located and choose the best radio access network, modulation scheme and other specification to configure itself to gain the best connection best performance.
- **Wireless mesh networking and dynamic ad-hoc networking:** With the variety of different approach schemes it will be possible to link to others adjoining to provide ad-hoc wireless networks for much speedier data flows.
- ***Smart antennas:*** Next major element of any 5G cellular system will be that of smart antennas. Using these it will be available to alter the beam direction to allow more direct communications and limit interference and increase overall cell capacity.

V. 5G technology requirements

In current years there have been several aspects about the ultimate form that 5G wireless technology should take. There have been two aspect of what 5G wireless technology should be:

- **Hyper connected view*:*** This view of the requirements for 5G wireless systems goals to take the existing technologies including 2G, 3G, 4G, Wi-Fi and other relevant wireless systems to serve higher coverage and availability, along with more dense networks. Apart from having requirements to give traditional services, a key differentiator would be to enable new services like Machine to Machine, M2M applications along with added Internet of Things, IoT applications. This set of 5G requirements could require a new radio technology to allow low power, low throughput field devices with long battery lifetimes of ten years or more.

- **Next generation radio-access technology:**
  This aspect of the 5G requirements takes the more technology driven view and sets specifications for data rates, latency and other key specification. These requirements for 5G would enable a clear demarcation to be made between 4G or other services and the new 5G wireless system.

In order to meet the industry and user wants, it is necessary to accommodate all requirements within the definition process, ensuring that the final definition meets the majority of users wants without becoming so demanding that any system cannot succeed.

A) 5G requirements summary

By accounting for the majority of wants, the following set of 5G requirements is gaining industry acceptance.

- 1-10Gbps connections to deadline points in the field (i.e. not theoretical maximum)
- 1 millisecond end-to-end round trip delay - latency
- 1000 x bandwidth per unit area
- 10-100 x number of connected devices
- Perception of) 99.999% availability
- Perception of 100% coverage
- 90% decrease in network energy usage
- Up to ten year battery life for low power, machine-type devices

One of the key concerns with the 5G requirements is that there are many different interested parties involved, each wanting their own requirements to be met by the new 5G wireless system. This leads to the fact that not all the requirements form a consistent list. None of the technology is going to be able to meet all the needs together.

As a result of these widely varying necessities for 5G, many anticipate that the new wireless system will be a umbrella that authorize a number of different radio access networks to work together, each meeting a set of needs. As very high data download and ultra low latency concerns do not easily sit with low data rate and long battery life times, it is likely that different radio access networks will be want for each of these requirements.

Accordingly it is likely that various mixtures of a subset of the overall list of requirements will be supported when and where it matters for the 5G wireless system.

B) WHY NEED OF 5G?

- It provides a very high speed, high capacity, and low cost per bit.
- It supports interactive multimedia, voice, video, Internet and other broadband services, greater effective and more attractive, and has Bi-directional, accurate traffic statistics.
- It is supporting large broadcasting capacity up to Gigabit which supporting almost 65,000 connections at a time.
- 5G technology offers remote management that user can get better and fast solution.
- 5G technology offers Global access and service portability
- It provides the high quality services due to high error tolerance.
- 5G technologies provide high resolution for crazy cell phone user and bi-directional large bandwidth shaping.
- The uploading and downloading speed of 5G technology is very high.
- 5G technologies provide transporter class gateway with unparalleled consiste

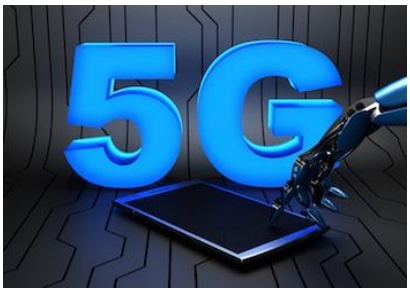

Fig.2: 5G Mobile

V. conclusion:

5G will give the foundational infrastructure for building smart cities, which will push mobile network performance and capability requirements to their extremes. It supports interactive multimedia, voice, video Internet and other broadband services, greater effective and more attractive, and has Bi- directional, accurate traffic statistics. It will give unbelievably fast broadband speeds, but more importantly it will have enough capacity wherever you go to achieve each function you want it to without a decrease in speed or connection, no matter how many people are connected at the same time.

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A REVIEW ON TRENDS AND CHALLENGES OF GRID-CONNECTED PHOTOVOLTAIC SYSTEMS

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Abstract:

This paper presents a literature review of the recent developments and trends pertaining to Grid-Connected Photovoltaic Systems (GCPVS). In countries with high penetration of Distributed Generation (DG) resources, GCPVS have been shown to cause inadvertent stress on the electrical grid. A review of the existing and future standards that addresses the technical challenges associated with the growing number of GCPVS is presented. Maximum Power Point Tracking (MPPT), Solar Tracking (ST) and the use of transformer-less inverters can all lead to high efficiency gains of Photovoltaic (PV) systems while ensuring minimal interference with the grid. Inverters that support ancillary services like reactive power control, frequency regulation and energy storage are critical for mitigating the challenges caused by the growing adoption of GCPVS.

II.INTRODUCTION

It is generally accepted in the scientific community that human activity is affecting climate change and that a majority of this impact comes from fossil fuel combustion caused by the electric utility industry [3]. Conventional fossil-fuel generating facilities have in past met the majority of global electrical energy demands. However, environmental and climate change implications of fossil fuel-based generation present serious challenges to society and the environment [1]. Distributed Generation (DG), particularly Photovoltaic (PV) systems, provides a means of mitigating these challenges by generating electricity directly from sunlight.

Unlike off-grid PV systems, Grid-Connected Photovoltaic Systems operate in parallel with the electric utility grid and as a result they require no storage systems. Since GCPVS supply power back to the grid when producing excess electricity (i.e., when generated power is greater than the local load demand), GCPVS help offset greenhouse gas emissions by displacing the power needed by the connected (local) load and providing additional electricity to the grid. As such, during peak solar hours (maximum solar irradiance), fewer conventional generation plants are needed. In addition, GCPVS reduce Transmission and Distribution (T&D) losses. Although average T&D losses amounted to 5.7% in the U.S. in 2010, losses during peak hours are higher [2]. For example, the estimated T&D losses for Southern California Edison and Pacific Gas & Electric exceeded 10% in 2010 [4]. Locating DG assets close to loads can help to partially mitigate these losses.

This paper is organized as follows: section II summarizes the current state and trends of the PV market. Section III discusses regulatory standards governing the reliable and safe operations of GCPVS. In section IV we discuss the technical challenges caused by GCPVS. Since there are a number of approaches for increasing the output power of PV systems, i.e., Maximum Power point tracking (MPPT), Solar Tracking (ST), a combination of both [5] or by using transformless inverters, section V examines each method

independently. We present evidence that these methods can indeed help improve the efficiency of GCPVS. In section VI, we explore recent developments in inverter technology and conclude with the changing role of GCPVS inverters in section VII.

II.Standards and requirements for safe operation of Grid-Connected PV Systems

The increase in the number of DG resources has introduced several technical challenges that have necessitated the development of applicable standards. These standards are intended to foster, rather than hinder the reliability, safe operation and further proliferation of grid-tied DG resources. Connecting large numbers of PV systems to the electrical grid without the appropriate regulatory standards and requirements poses a significant threat to the integrity and stability of the grid. A number of industry professionals, organizations and researchers have been working on defining and addressing the potential impacts of the mass adoption of GCPVS on existing electrical infrastructure and how to better prepare for and respond to the upcoming challenges. These organizations have had several technical sessions between 2013 and 2015 and some are close to completing their findings.

A. IEEE 1547

IEEE standard 1547 (Standard for Interconnecting Distributed Resources with Electric Power Systems) is the technical guide[6]. This standard provides the guidance requirements for the design, construction, installation, safe operational performance and maintenance of these resources by ensuring compliance with local, regional and national codes. In addition, IEEE 1547 specifies the power factor, frequency and voltage tolerances, fault detection and anti-islanding characteristics that dictate the conditions with which a DG may remain connected to a utility. Inverters are required to detect unintentional islanding and disconnect from the grid such that there is no back-feeding onto a utility line that has been isolated for maintenance.

B. IEEE 929

While IEEE 1547 applies to all distributed resources under 10 MVA, IEEE standard 929 (Recommended Practice for Utility Interface of PV Systems) applies to GCPVS and several other inverter-based technologies that operate in parallel with the electric utility and that are 10 KVA or less.

IEEE 929 requires the inverter to continuously monitor the grid. It defines the behavior of the GCPVS when any utility abnormalities are present. For example, responses to abnormal conditions like loss of synchronization between the GCPVS and the utility, fault monitoring, PV system protection, isolation mechanisms and the maximum allowable trip time in cycles are specified when there is an abnormal voltage condition on the grid.

General	Safety and protection	Power quality
Voltage regulation	Voltage disturbance	Harmonics mitigation
System frequency	Frequency disturbance	Direct current injection
Synchronization	Isolation device	Flicker
Monitoring provisions	Disconnect for faults	Power factor
Grounding	Reconnection	
Voltage unbalance	Anti-islanding	
Immunity	Surge capability	

Table 1

Standards and Requirements for grid-connected distributed generators (GCPVS included)

III. Challenges caused by Grid-Connected PV Systems

As the overall costs of installing and owning GCPVS systems are declining, residential, commercial and utility scale adoption of this

technology is on the rise. Although there are many benefits of GCPVS, such as its long working life (25–30 years), low operations and maintenance costs and obvious environmental advantages over fossil-fuel power plants, however, GCPVS have their own set of challenges. Due to their volatility, Hossain and Ali referred to the interoperability of GCPVS with the grid as a major concern [7]. According to Omran et al., due to the high penetration of GCPVs and its unpredictable output power, in the near future, several utilities and independent system operators will begin to enforce more stringent regulations regarding the inter-connection of GCPVS to the grid[8].

At the root of these claims is the inherent functional nature of GCPVS, primarily because their output generation decreases as the sun goes down. Consequently, they are unable to adequately contribute to the grid when demand increases in the hours following sunset (when demand for electricity is greatest). The California Independent System Operator (CAISO) created the duck curve (Fig.1.) to show the impact of GCPVS on the electric grid'soperations based on CAISO's real-time analysis and forecast of electricity net demand from 2012 to 2020. The net demand load represents the amount of conventional generation plants (excluding renewables) that will need to be on-line during different times of the day.

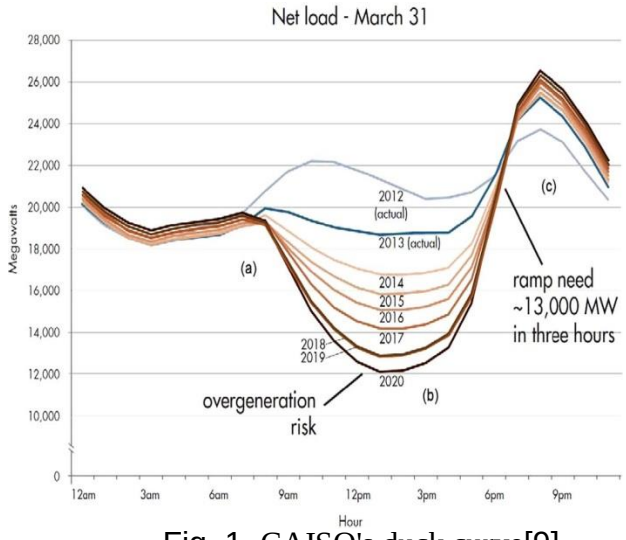

Fig. 1. CAISO's duck curve[9].

A.Optimizing the efficiency of Grid-Connected PV Systems

As discussed in the preceding section, the inherent nature of how PV systems operate makes it difficult to predict the power delivered to the load. However, GCPVS with higher efficiency tends to have less interference with the electric grid and the loads they are serving. By increasing system efficiency, it is possible to maximize output power during times of low solar irradiance and high unpredictability. Three methods of improving system efficiency are presented below.

B. Using MPPT to improve output performance

While several studies have been conducted on making GCPVS economically attractive [10-12], other research has focused on maximizing output power under varying temperature, lighting (irradiance) and load (current) conditions. In general, PV systems have low solar-to-electric conversion efficiencies that mostly depend on the amount of available unobstructed sunlight in the sky[14].

Secondly, the nonlinearity of the current/voltage curve and the power/voltage relationship exhibited by solar PV panels impacts the ability of PV systems to obtain higher efficiency rates [13]. Depending on the irradiance level and temperature, at any given time, PV cells operate at a fixed point.

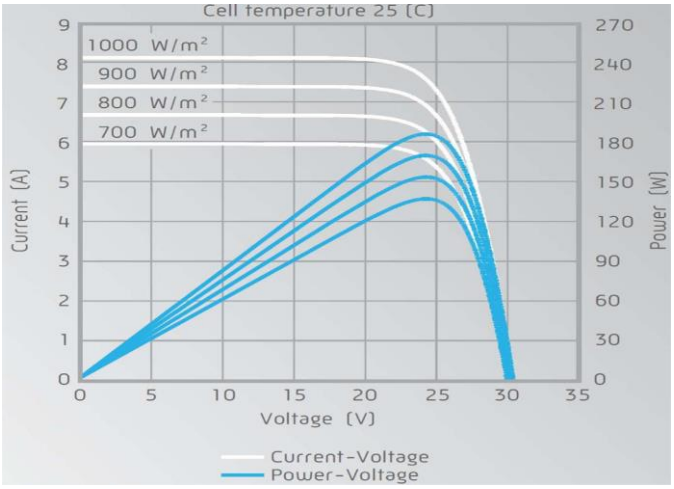

Fig. 5. The effect of irradiance on theI–Vcharacteristics of a PV solar module[13].

C. Effects of solar tracking

Solar trackers, unlike inverter based maximum power point trackers, are mechanical rotors that guide the PV panels in such a way that the panels are constantly position at an angle that allows them to receive the most sunlight. Stationary positioning of panels limits the surface area with direct exposure to the sun [15]. There are a number of interesting investigations that have been devoted to correctly determining the position of the sun.

Transformless inverters

The power available on the grid and for use by end utility customers is Alternating Current (AC) and as such, the Direct Current (DC) power provided by the output of Solar PV modules will need to be converted to AC in order for it to become useful. An inverter is needed to convert DC power into AC. In many inverter designs, transformers are added to provide galvanic isolation between the DC and AC components – for safety and to prevent damage to the sensitive electronic devices on the DC side of the inverter. Galvanic isolation ensures that there is no physical connection (or wires) between the primary and secondary sides of the transformer.

IV. Conclusion

Although the solar PV market has experienced astronomical levels of growth and cost reductions in recent years, there are many technical challenges and economic realities that need to be reconciled in order for DG resources like GCPVS to be at parity with conventional generation. For successful mass adoption ofGCPVs, new technologies must be developed that will allow the inverter to do more than just provide DC/AC conversions. Modern grid-interactive inverters will need to provide Volt/VAr control (power factor and voltage stabilization), frequency regulation, enable storage and utilize modern communications protocols, all at a reasonable cost. This new generation of inverters has been rightly termed “smart inverters” [16-18].

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Optimization of LUTfor Memory-Based Computation Using APC&OMS Techniques

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***Abstract*— Recently, we have proposed the antisymmetric item coding (APC) and odd-multiple storage (OMS) methods for query table (LUT) outline for memory-based multipliers to be utilized as a part of advanced flag preparing applications. Each of these systems brings about the decrease of the LUT measure by a factor of two. In this short, we show an alternate type of APC and a changed OMS conspire, keeping in mind the end goal to join them for proficient memory-based augmentation. The proposed joined approach gives a lessening in LUT size to one-fourth of the customary LUT. We have likewise recommended a basic system for particular sign inversion to be utilized as a part of the proposed plan. It is demonstrated that the proposed LUT outline for little information sizes can be utilized for productive execution of high-exactness augmentation by input operand decay. It is discovered that the proposed LUT-based multiplier includes practically identical range and time many-sided quality for a word size of 8 bits, however for higher word sizes, it includes altogether less territory and less augmentation time than the sanctioned marked digit (CSD)- based multipliers. For 16-and 32-bit word sizes, individually, it offers over 30% and half of sparing in area– defer item finished the comparing CSD multipliers.**

Index Terms*—*Digital signal processing (DSP) chip, lookuptable (LUT)-based computing, memory-based computing.

I. INTRODUCTION

Digital signal processing algorithms typically require a large number of mathematical operations to be performed quickly and repetitively on a set of data. Signals are constantly converted from analog to digital, manipulated digitally, and then converted again to analog form, as diagrammed below. Many DSP applications have constraints on latency; that is, for the system to work, the DSP operation must be completed within some fixed time, and deferred processing is not viable. Digital signal processing:

In-order to reach a certain criteria memory based computation plays a vital role in dsp (digital signal processing) application.

1. FILTER DESIGNING :

Finite impulse response (FIR) digital filter is widely used as a basic tool in various signal processing and image processing applications. The order of an FIR filter primarily determines the width of the transition-band, such that the higher the filter order, the sharper is the transition between a pass-band and adjacent stop-band. Many applications in digital Communication (channel equalization, frequency channelization), speech processing (adaptive noise cancelation), seismic signal processing (noise elimination), and several other areas of signal processing require large order FIR filters. Since the number of multiply-accumulate (MAC) operations required per filter output increases linearly with the filter order, real-time implementation of these filters of large orders is a challenging task. Several attempts have, therefore, been made and continued to develop low-complexity dedicated VLSI systems for these filters.

As the scaling in silicon devices has progressed over the last four decades, semiconductor memory has become cheaper, faster and more power-efficient. According to the projections of the international technology roadmap for semiconductors (ITRS) , embedded memories will continue to have dominating presence in the system-on-chip (SoC), which may exceed 90% of total SoC content. It has also been found thatthe transistor packing density of SRAM is not only high, but also increasing much faster than the transistor density of logic devices .

1.1 BINARY MULTIPLICATION:

Multiplication in binary is similar to its decimal counterpart. Two numbers A and B can be multiplied by partial products: for each digit in B, the product of that digit in A is calculated and written on a new line, shifted leftward so that its rightmost digit lines up with the digit in B that was used. The sum of all these partial products gives the final result.

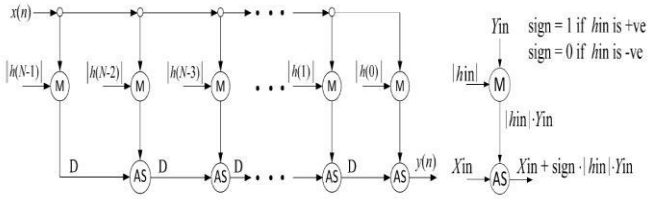
1.2 MEMORY BASED MULTIPLICATION :

The input-output relationship of an N-tap FIR filter in time-domain is given by

$$y(n) = h(0) \cdot x(n) + h(1) \cdot x(n-1) + h(2) \cdot x(n-2) + \cdots h(N-1) \cdot x(n-N+1)$$

where h(n), for n = 0,1,2,--------N-1, represent the filter coefficients x(n-i), while for i== 0,1,2,--------N-1, for x(n) , represent recent input samples y(n), and represents the current output sample. Memory-based multipliers can be implemented for signed as well as unsigned operands

1.3 FIR FILTER ARCHITECTURE



The objectives of this work are:

- Multiplying two binary numbers one number is fixed X[4:0] and another variable _A‘
- Using APC–OMS combined LUT design for the

multiplication of W-bit fixed coefficient A with 5-bit input X.

- Number of calculations reduced and memory required is less to perform multiplication.

For 16- and 32-bit word sizes, respectively, it offers more than 30% and 50% of saving in area–delay product over the corresponding CSD multipliers.

1.4 ANTI -SYMMETRIC PRODUCT CODING:

Anti symmetric product coding is the technique used to process the multiplication based on LUT multiplication which reduces the size of conventional lut by 50 % .

The anti symmetric product coding is based on the antisymmetric coding i.e the 2‘s complement phenomenon which is used to reduce the LUT size by half.

For simplicity of presentation, we assume both X and A to be positive integers.2 The product words for different values of X for L = 5 are shown in Table I. It may be observed in this table that the input word X on the first column of each row is the two‘s complement of that on the third column of the same row. In addition, the sum of product values corresponding to these two input values on the same row is 32A. Let the product values on the second and fourth columns of a row be u and v, respectively.

Since one can write

u = [(u + v)/2 − (v − u)/2] and

v = [(u + v)/2 + (v − u)/2], for (u + v) = 32A, we can have

TABLE I
APC WORDS FOR DIFFERENT INPUT VALUES FOR $L = 5$

Input, X	product values	Input, X	product values	address $x_3'x_2'x_1'x_0'$	APC words
0 0 0 0 1	A	1 1 1 1 1	$31A$	1 1 1 1	$15A$
0 0 0 1 0	$2A$	1 1 1 1 0	$30A$	1 1 1 0	$14A$
0 0 0 1 1	$3A$	1 1 1 0 1	$29A$	1 1 0 1	$13A$
0 0 1 0 0	$4A$	1 1 1 0 0	$28A$	1 1 0 0	$12A$
0 0 1 0 1	$5A$	1 1 0 1 1	$27A$	1 0 1 1	$11A$
0 0 1 1 0	$6A$	1 1 0 1 0	$26A$	1 0 1 0	$10A$
0 0 1 1 1	$7A$	1 1 0 0 1	$25A$	1 0 0 1	$9A$
0 1 0 0 0	$8A$	1 1 0 0 0	$24A$	1 0 0 0	$8A$
0 1 0 0 1	$9A$	1 0 1 1 1	$23A$	0 1 1 1	$7A$
0 1 0 1 0	$10A$	1 0 1 1 0	$22A$	0 1 1 0	$6A$
0 1 0 1 1	$11A$	1 0 1 0 1	$21A$	0 1 0 1	$5A$
0 1 1 0 0	$12A$	1 0 1 0 0	$20A$	0 1 0 0	$4A$
0 1 1 0 1	$13A$	1 0 0 1 1	$19A$	0 0 1 1	$3A$
0 1 1 1 0	$14A$	1 0 0 1 0	$18A$	0 0 1 0	$2A$
0 1 1 1 1	$15A$	1 0 0 0 1	$17A$	0 0 0 1	A
1 0 0 0 0	$16A$	1 0 0 0 0	$16A$	0 0 0 0	0

For $X = (0\ 0\ 0\ 0\ 0)$, the encoded word to be stored is $16A$.

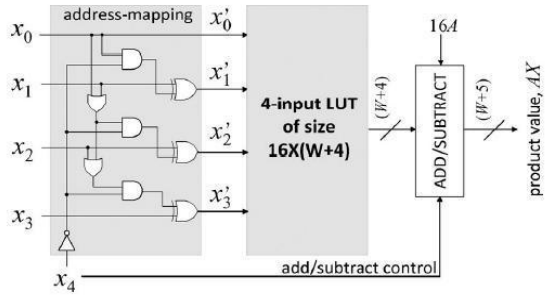
The product values on the second and fourth columns of Table I therefore have a negative mirror symmetry. This behavior of the product words can be used to reduce the LUT size,where, instead of storing u and v, only [(v − u)/2] is stored for a pair of input on a given row. The 4-bit LUT addresses and corresponding coded words are listed on the fifth and sixth columns of the table, respectively. Since the representation of the product is derived from the anti-symmetric behavior of the products, we can name it as anti-symmetric product code.

The 4-bit address X‘= x3‘x2‘x1‘x0‘ of the APC word is given by

X‘ = XL, if x4 = 1

=X‘L , if x4 = 0

where XL = (x3x2x1x0) is the four less significant bits of X, and XL‘ is the two‘s complement of XL.



1.5 LUT –BASED MULTIPLICATION USING APC – OMS MODIFIED OPTIMIZATION TECHNIQUE

The APC approach, although providing a reduction in LUT size by a factor of two, incorporates substantial overhead of area and time to perform the two‘s complement operation of LUT output for sign modification and that of the input operand for input mapping. However, we find that when the APC approach is combined with the OMS technique, the two‘s complement operations could be very much simplified since the input address and LUT output could always be transformed into odd integers.

1.6 LUT COMBINED APC-OMS BASED MULTIPLICAT-ION TECHNIQUE

TABLE II
OMS-BASED DESIGN OF THE LUT OF APC WORDS FOR $L = 5$

input X' $x_3'x_2'x_1'x_0'$	product value	# of shifts	shifted input, X''	stored APC word	address $d_3d_2d_1d_0$
0 0 0 1	A	0	0 0 0 1	$P0 = A$	0 0 0 0
0 0 1 0	$2 \times A$	1			
0 1 0 0	$4 \times A$	2			
1 0 0 0	$8 \times A$	3			
0 0 1 1	$3A$	0	0 0 1 1	$P1 = 3A$	0 0 0 1
0 1 1 0	$2 \times 3A$	1			
1 1 0 0	$4 \times 3A$	2			
0 1 0 1	$5A$	0	0 1 0 1	$P2 = 5A$	0 0 1 0
1 0 1 0	$2 \times 5A$	1			
0 1 1 1	$7A$	0	0 1 1 1	$P3 = 7A$	0 0 1 1
1 1 1 0	$2 \times 7A$	1			
1 0 0 1	$9A$	0	1 0 0 1	$P4 = 9A$	0 1 0 0
1 0 1 1	$11A$	0	1 0 1 1	$P5 = 11A$	0 1 0 1
1 1 0 1	$13A$	0	1 1 0 1	$P6 = 13A$	0 1 1 0
1 1 1 1	$15A$	0	1 1 1 1	$P7 = 15A$	0 1 1 1

The proposed APC–OMS combined design of the LUT for L = 5 and for any coefficient width W is shown in Fig. 2.4. It consists of an LUT of nine words of (W + 4)-bit width, a four-to-nine-line address decoder, a barrel shifter, an address generation circuit, and a control circuit for generating the RESET signal and control word (s1s0) for the barrel shifter. The recomputed values of A × (2i + 1) are stored as Pi, for

i = 0, 1, 2, . . . , 7, at the eight consecutive locations of the memory array, as specified in Table II, while 2A is stored for input X = (00000) at LUT address ―1000,‖ as specified in Table III. The decoder takes the 4-bit address from the address generator and generates nine word-select signals, i.e., {wi, for $0 \le i \le 8$}, to select the referenced word from the

LUT. The 4-to-9-line decoder is a simple modification of 3-to-8-line decoder.

The control bits s0 and s1 to be used by the barrel shifter to produce the desired number of shifts of the LUT output are generated by the control circuit, according to the relations.

Here a simple design for sign modification of the LUT output.

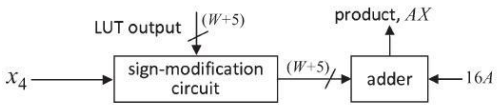
TABLE -3

input X $x_4x_3x_2x_1x_0$	product values	encoded word	stored values	# of shifts	address $d_3d_2d_1d_0$
1 0 0 0 0	$16A$	0	− − −	−−	− − −
0 0 0 0 0	0	$16A$	$2A$	3	1 0 0 0

The product values and encoded words for input words X = (00000) and (10000) are separately shown in Table III. For X = (00000), the desired encoded word 16A is derived

by 3-bit left shifts of 2A [stored at address (1000)]. For X = (10000), the APC word ―0‖ is derived by resetting the LUT output, by an active-high RESET signal given by

ADDER/SUBSTRACTOR (ANTISYMMETRY GENERATION CIRCUIT)



The adder /sub circuit is also called as an ant symmetryl generation circuit

Based on the sign of x4,the circuit generates the anti symmetry based on the msb of x input.

$$\text{Product word} = 16A + (\text{sign value}) \times (\text{APC word})$$

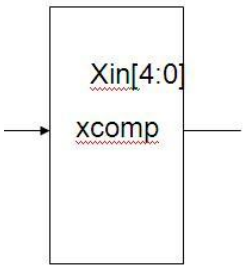
2. LUT OPTIMATION

2.1 Basic Components of LUT Optimization :

The modules contributed for combined APC-OMS based LUT optimization technique are

1 .Xin generation module (based on antisymmetric process)
2. Address generation module
3. line decoder
4. 9*(w+4) LUT
> line selector module
> multiplier result module
> resultant multiplier module
5. Barrel Shifter
6. Add/Substractor (Sign Determination) module

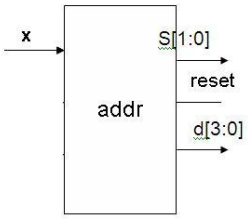
Xin generation module (based on antisymmetric process): A input of 5-bit length is given as input to this module. It used to generate antisymetric of last 4-bits (Xin(3 to 0)) when the msb of Xin i.e Xin(4) is _0‘ and and process the same input when the msb of Xin is _1‘ hence only 16 combinations will be achived for 5-bit of input as in table 1.



Block diagram

If (xin(4) = _0‘) then
Xcomps = Xin(4) & 2‘scomplement of(Xin(3 to 0));
Else
Xcomps = Xin

2.2 Address Generation Unit :



The address generation unit generats the 4-bit address for the input given by Xin generation module the 4-bit address is named as d.

The reset output will be set when the input combination Xin = ―10000‖;

Inorder to make the output of the barrel shifter to _0‘ .

$$\text{RESET} = \overline{(x_0 + x_1 + x_2 + x_3)} \cdot x_4.$$

The oupt s[1:0] are used to get the shift terminology in barrel shifter maximum of 3 shifts .

$$s_0 = \overline{x_0 + \overline{(x_1 + \overline{x_2})}}$$
$$s_1 = \overline{(x_0 + x_1)}.$$

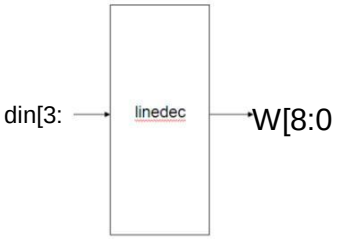
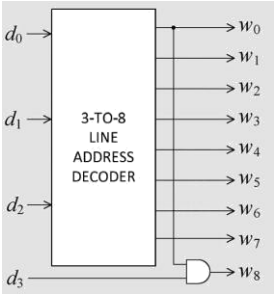


Figure: 4 to 9 Line decoder

The 4 input lines _din‘ is converted into 9 output lines _w‘ which is used to calculate the LUT output .

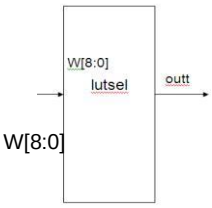
A decoder is a device which does the reverse of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decoder.



Decoding is necessary in applications such as data multiplexing, 7 segment display and memory address decoding.

A simple CPU with 8 registers may use 3-to-8 logic decoders inside the instruction decoder to select two source registers of the register file to feed into the ALU as well as the destination register to accept the output of the ALU. A typical CPU instruction decoder also includes several other things.

LUT selector:



LUT selector is used to generate PVN (product value number) which is used to calculate the corresponding product value i.e (PVN X A)

The PVN is calculated depending on the W input corresponding bit set in order to generate the stored APC word i.e

The possible PVN values are

When w = 000000001 then PVN = 1

When w = 000000010 then PVN = 3

When w = 000000100 then PVN = 5

When w = 000001000 then PVN = 7

MULTIPLIER RESULT:

Multiplier result module is used to calculate multiplication of individual bits of operand and get the individual multiplication results .

Ex: 1 0 1 1 (A)

× 1 0 1 0 (B)

---

0 0 0 0 ← ress0 i.e B(0) X A

\+ 1 0 1 1 ← ress1 i.e B(1) X A

\+ 0 0 0 0 ← ress2 i.e B(2) X A

\+ 1 0 1 1 ← ress3 i.e B(3) X A

BARREL SHIFTER :

Barrel Shifter is an combinational logic circuit which is used to do any no. of shift‘s for one clock cycle. Depending upon the _s‘ the no of shift‘s is decided and output _outp‘ is given .

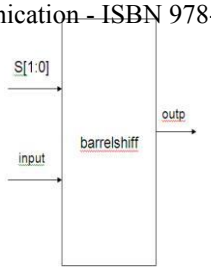


Fig:Block diagram:

For example, take a 4-bit barrel shifter, with inputs A, B, C and D. The shifter can cycle the order of the bits ABCD as DABC, CDAB, or BCDA; in this case, no bits are lost. That is, it can shift all of the outputs up to three positions to the right (and thus make any cyclic combination of A, B, C and D). The barrel shifter has a variety of applications, including being a useful component in microprocessors (alongside the ALU).

Implementation:

A barrel shifter is often implemented as a cascade of parallel 2×1 multiplexers. For a 4-bit barrel shifter, an intermediate signal is used which shifts by two bits, or passes the same data, based on the value of S[1]. This signal is then shifted by another multiplexer, which is controlled by S[0]:

im = IN, if S[1] == 0

= IN << 2, if S[1] ==

1 OUT = im, if S[0] == 0

= im << 1, if S[0] == 1

It is used to add the intermediate results to 16A to get the final output .It may make output 0 when _clr‘ is high.

u = [(u + v)/2 − (v − u)/2] and

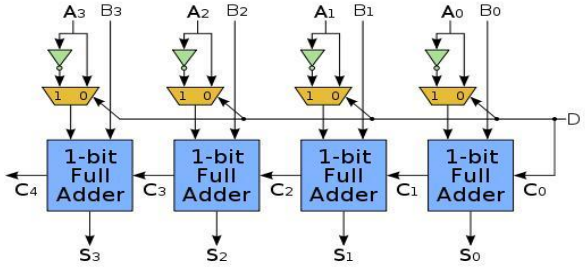
v = [(u + v)/2 + (v − u)/2], for (u + v) = 32A,

$$u = 16A - \left[\frac{v-u}{2}\right] \quad v = 16A + \left[\frac{v-u}{2}\right].$$

$$\text{Product word} = 16A + (\text{sign value}) \times (\text{APC word})$$

When xin(4) = _1‘ then sign value = 1

When xin(4) = _0‘ then sign value = 0.



4-bit_ripple_carry_adder-subtracter.svg

In digital circuits, an adder-subtractor is a circuit that is capable of adding or subtracting numbers.

This works because when D = 1 the A input to the adder is really $\overline{A}$ and the carry in is 1. Adding Bto $\overline{A}$ and 1 yields the desired subtraction of B − A.

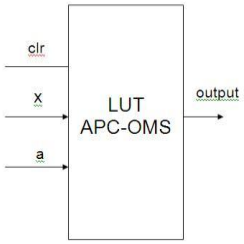
The adder-subtractor above could easily be extended to include more functions. For example, a 2-to-1 multiplexer could be introduced on each Bi that would switch between zero and Bi; this could be used (in conjunction with D = 1) to yield the two's complement of A since $-A = \overline{A} + 1$.

A further step would be to change the 2-to-1 mux on A to a 4-to-1 with the third input being zero, then replicating this on Bi thus yielding the following output functions:

0 (with the both Ai and Bi input set to zero and D = 0)
1 (with the both Ai and Bi input set to zero and D = 1)
A (with the Bi input set to zero)
B (with the Ai input set to zero)
A + 1 (with the Bi input set to zero and D = 1)
B + 1 (with the Ai input set to zero and D = 1)
A + B
A − B
B − A
$\overline{A}$ (with Ai set to invert; Bi set to zero; and D = 0)
− A (with Ai set to invert; Bi set to zero; and D = 1)
$\overline{B}$ (with Bi set to invert; Ai set to zero; and D = 0)
− B (with Bi set to invert; Ai set to zero; and D = 1)

By adding more logic in front of the adder, a single adder can be converted into much more than just an adder — an ALU.

LUT APC – OMS Optimization Top Model



The APC approach, although providing a reduction in LUT size by a factor of two, incorporates substantial overhead of area and time to perform the two‘s complement operation of LUT output for sign modification and that of the input operand for input mapping.

The proposed APC–OMS combined design of the LUT for L = 5 and for any coefficient width W is shown in Fig. 2.4. It consists of an LUT of nine words of (W + 4)-bit width, a four-to-nine-line address decoder, a barrel shifter, an address generation circuit, and a control circuit for generating the RESET signal and control word (s1s0) for the barrel shifter.

The recomputed values of A × (2i + 1) are stored as Pi, for i = 0, 1, 2, . . . , 7, at the eight consecutive locations of the memory array, as specified in Table II, while 2A is stored for input X = (00000) at LUT address ―1000,‖ as specified in Table III. The decoder takes the 4-bit address from the address generator and generates nine word-select signals, i.e., {wi, for $0 \le i \le 8$}, to select the referenced word from the LUT.

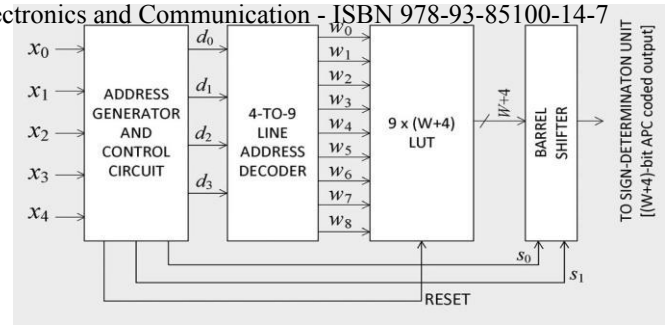
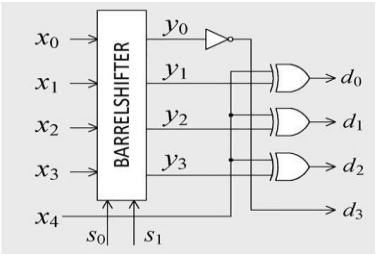


fig 2.4 lut combined apc-oms based multiplication technique



Here we observe that they will Antisymmetry in the address for the LSB 4 bits. We will get all the address from 0 to 15 for 0 to 31.Thus we reduce the memory locations required to store coefficients by half. Then we will store only odd coefficients in the look up table .

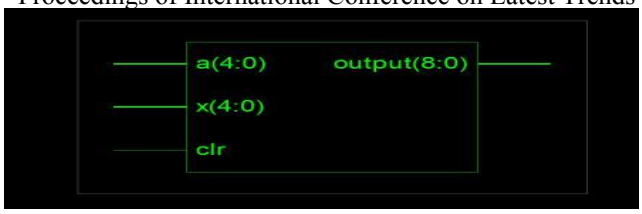
Thus we reduce the number of coefficients by half again.
On total we have reduced the number coefficients by quarter.

RESULTS AND CONCLUSION:

The proposed LUT multipliers for word measure L = W = 8, 16, and 32 bits are coded in VHDL and integrated by Synopsys Design Compiler utilizing the TSMC 90-nm library, where the LUTs are actualized as varieties of constants, and increases are executed by the Wallace tree and swell convey exhibit. The CSD-based multipliers having a similar expansion plans are additionally integrated with a similar innovation library. The territory and defer complexities of the multipliers evaluated from the combination comes about are recorded in Table IV. It is discovered that the proposed LUT configuration includes similar region and time complexities for a word size of 8 bits, yet for higher word sizes, it includes fundamentally less region and less augmentation time than the CSD-based multiplier. For L = W = 16, and 32 bits, separately, it offers over 30% and half of sparing in area– postpone item (ADP) over the CSD multiplier.

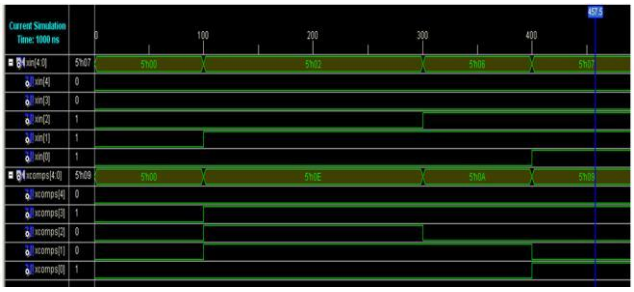
In this short, we have demonstrated the likelihood of utilizing LUT based multipliers to actualize the steady duplication for DSP applications. The full points of interest of proposed LUT based plan, be that as it may, could be determined if the LUTs are actualized as NAND or NOR read-just recollections and the number juggling shifts are executed by a cluster barrel shifter utilizing metal– oxide–semiconductor transistors [11]. Additionally work should at present be possible to infer OMS– APC-based LUTs for higher info sizes with various types of deteriorations and parallel and pipelined option plans for reasonable area– postpone tradeoffs.

RTL SCHEMATIC:

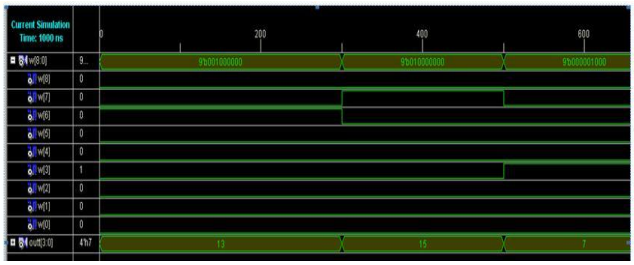


SIMULATION RESULTS:

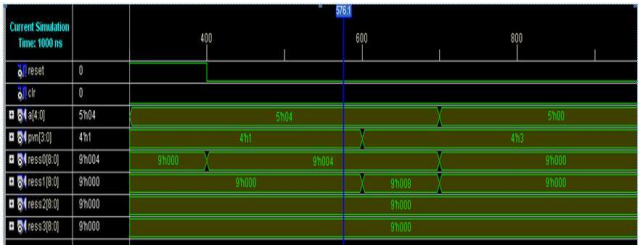
Xin Generation Module:



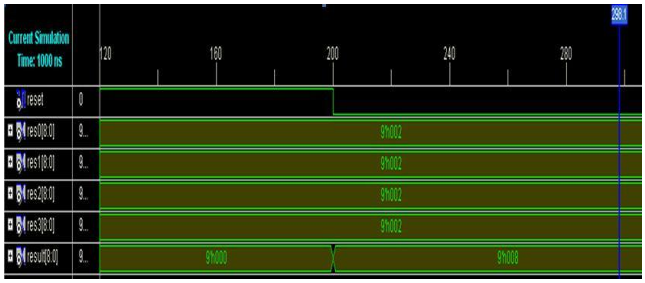
LINE SELECTOR:



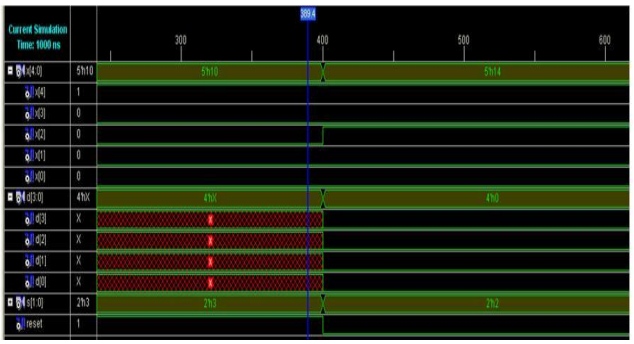
MULTIPLIER RESULT MODULE:



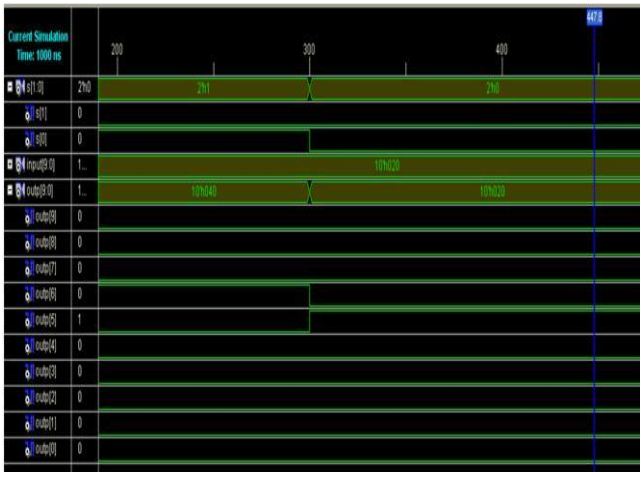
RESULTANT MULTIPLICATION MODULE:



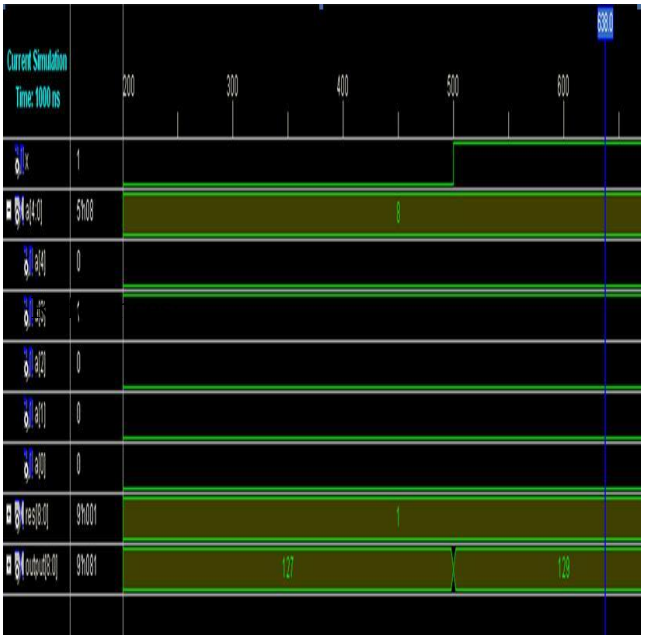
ADDRESS GENERATION MODULE:



BARREL SHIFTER :



ADDER/SUBSTRACTOR (sign determination module)



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SST with EMG based Noise Reduction System

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Abstract-the Silent sound technology (SST) is a completely new technology which can prove to be a solution for those who have lost their voice but wish to speak over phone. It can be used as part of a communications system operating in silence-required or high-background- noise environments. This article outlines the history associated with the technology followed by presenting two most preferred techniques viz. Electromyography and Ultrasound SSI. The concluding Section compares and contrasts these two techniques and put forth the future prospects of this technology.

Index Terms - Articulators , Electromyography, Ultrasound SSI, Vocoder, Linear Predictive Coding.

I.INTRODUCTION

Each one of us at some point or the other in our lives must have faced a situation of talking aloud on the cell phone in the midst of the disturbance while travelling in trains or buses or in a movie theatre. One of the technologies that can eliminate this problem is the 'Silent Sound' technology.Silent sound technology is a technique that helps one to transmit information without using vocal cords which was developed at the Karlsruhe Institute of Technology[1]. It enables speech communication to take place when an audible acoustic signal is unavailable. The main goal of Silent Sound technology is to notice every movement of the lips and internally transform the electrical pulses into sounds by neglecting all the surrounding noise, which could help people who lose voices to speak, and allow people to make silent calls without bothering others. Rather than making any sounds, the handset would decipher the movements made by one's mouth by measuring muscle activity, then convert this into speech that the person on the other end of the call can hear[2].

The technology opens up a host of applications, from helping people who have lost their voice due to illness or accident to telling a trusted friend your PIN number over the phone without anyone eavesdropping assuming no lip-readers are around. It can be used used in Military for communicating secret or confidential matters to others Also, given the numbers of cell phones in use today, the market for this technology could potentially become very important if such a concept gained public acceptance. Silent Sound Technology is implemented using two methods. They are

- Electromyography (EMG)
- Ultrasound SSI

Electromyography involves monitoring tiny muscular movements that occur when we speak and converting them
into electrical pulses that can then be turned into speech, without a sound being uttered. Ultrasound imagery is a non-invasive and clinically safe procedure which makes possible the real-time visualization of the tongue by using an ultrasound transducer.

II. HISTORICAL FRAMEWORK

The idea of interpreting silent speech with a computer has been around for a long time, and came to public attention in the 1968 Stanley Kubrick science-fiction film 2001,A Space Odyssey, where a HAL 9000 computer was able to lip-read the conversations of astronauts who were plotting it's destruction. Automatic visual lip-reading was proposed as an enhancement to speech recognition in noisy environments [3], and patents for lip-reading equipment able to interpret simple spoken commands began to be registered in the mid 1980's [4].The first true SSI system which deployed 3 electromyographic sensors mounted on speaker's face and interpreted the speech with an accuracy of 71%, originated in Japan. [5]A few years later, an imaging- based system, which extracted the tongue and lip features from the video of speaker's face, returned 91% recognition[6]. A major focal point was the DARPA Advanced Speech Encoding Program (ASE) of the early 2000's, which funded research on low bit rate speech synthesis with acceptable intelligibility, quality, and aural speaker recognizability in acoustically harsh environments, thus spurring developments in speech processing using a variety of mechanical and electromagnetic glottal activity sensors [7]. The first SSI research papers explicitly mentioning cellphone privacy as a goal also began to appear around this 2004[8].

III. SILENT SOUND TECHNOLOGIES

This section illustrates two fundamental techniques that are put to use in interpretation of speech in noisy

environments in the absence of intelligible acoustic signals. These techniques are:

- Electromyography
- Ultrasound SSI

Electromyography involves monitoring tiny muscular movements that occur when we speak and converting them into electrical pulses that can then be turned into speech, without a sound being uttered. Ultrasound imagery is a non-invasive and clinically safe procedure which makes possible the real-time visualization of the tongue by using an ultrasound transducer.

IV. ELECTROMYOGRAPHY

Electromyography (EMG) is a technique for evaluating and recording the electrical activity produced by skeletal muscles[9].An electromyograph detects the electrical potential generated by muscle cells when these cells are electrically or neurologically activated. The signals can be analysed to detect medical abnormalities, activation level, or to analyse the biomechanics of human or animal movement.Fig1 shows the basic mechanism of Electromyography where the muscle activity is analysed by the Electromyograph to generate an Electromyogram.

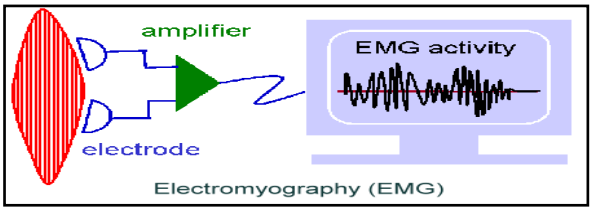

FIG 1. ELECTRMYOGRAPHY

V. ELECTRICAL CHARACTERISTICS

The electrical source is the muscle membrane potential of about -90 mV. Measured EMG potentials range between less than 50 μV and up to 20 to 30 mV, depending on the muscle under observation. Fig 2 shows EMG sensors connected on the face of a speaker.Typical repetition rate of muscle motor unit firing is

about 7–20 Hz, depending on the

size of the muscle. In interfacing we use four different kind of transducers -

- Vibration sensors
- Pressure sensor
- Electromagnetic sensor
- Motion sensor

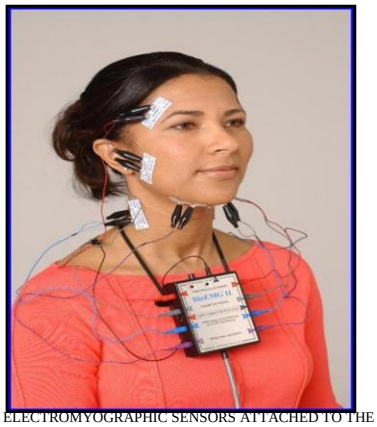

FIG 2: ELECTROMYOGRAPHIC SENSORS ATTACHED TO THE FACE

VI. TYPES OF EMG

There are two kinds of EMG in widespread use: surface EMG and intramuscular (needle and fine-wire) EMG. To perform intramuscular EMG, a needle electrode or a needle containing two fine-wire electrodes is inserted through the skin into the muscle tissue. A trained professional (such as a neurologist, physiatrist, chiropractor, or physical therapist) observes the electrical activity while inserting the electrode. Certain places limit the performance of needle EMG by non-physicians. A recent case ruling in the state of New Jersey declared that it cannot be delegated to a physician's assistant. The insertional activity provides valuable information about the state of the muscle and its innervating nerve. Normal muscles at rest make certain, normal electrical signals when the needle is inserted into them. Then the electrical activity when the muscle is at rest is studied. Abnormal spontaneous activity might indicate some nerve and/or muscle damage. Then the patient is asked to contract the muscle smoothly. The shape, size, and frequency of the resulting electrical signals are judged. Then the electrode is retracted a few millimeters, and again the activity is analyzed until at least 10–20 motor units have been collected. Each electrode track gives only a very local picture of the activity of the whole muscle. Because skeletal muscles differ in the inner structure, the electrode has to be placed at various locations to obtain an accurate study.

Intramuscular EMG may be considered too invasive or unnecessary in some cases. Instead, a surface electrode may be used to monitor the general picture of muscle activation, as opposed to the activity of only a few fibers as observed using an intramuscular EMG. This technique is used in a number of settings; for example, in the physiotherapy clinic, muscle activation is monitored using surface EMG and patients have an auditory or visual stimulus to help them know when they are activating the muscle. The technique primarily

used for this purpose is surface electromyography. Surface Electromyography (sEMG) is the process of recording electrical muscle activity captured by surface (i.e., non-implanted) electrodes. When a muscle fiber is activated by the central nervous system, small electrical currents in the form of ion flows are generated. These electrical currents move through the body tissue, whose resistance creates potential differences which can be measured between different regions on the body surface, for example on the skin. Amplified electrical signals obtained from measuring these voltages over time can be fed into electronic devices for further processing.As speech is produced by the activity of human articulatory muscles, the resulting myoelectric signal patterns measured at these muscles provides a means of recovering the speech corresponding to it. Since sEMG relies on muscle activity alone, speech can be recognized even if produced silently, i.e., without any vocal effort, and the signal furthermore cannot be corrupted or masked by ambient noise transmitted through air. As a result, sEMGbased speech recognition overcomes the major shortcomings of traditional speech recognition, namely preserving privacy of (silently) spoken conversations in public places, avoiding the disturbance of bystanders, and ensuring robust speech signal transmission in adverse environmental conditions.This technique could enable silent speech interfaces, as EMG signals are generated even when people pantomime speech without producing sound. Having effective silent speech interfaces would enable a number of compelling applications, allowing people to communicate in areas where they would not want to be overheard or where the background noise is so prevalent that they could not be heard. In order to use EMG signals in speech interfaces, however, there must be a relatively accurate method to map the signals to speech.[12]

Recent research studies aim to overcome the major limitations of today‘s sEMG-based speech recognition systems and applications, to, for example:

- remove the restriction of words or commands spoken in isolation and evolve toward a less limited, more user-friendly continuous speaking style
- allow for acoustic units smaller than words or phrases, enabling large vocabulary recognition systems
- implement alternative modeling schemes such as articulatory phonetic features to enhance phoneme models
- study the effects of electrode re-positioning and more robust signal preprocessing
- examine the impact of speaker dependencies on the myoelectric signal
- investigate real-life applicability,by augmenting conventional speech recognition systems and addressing size, attachment, and mobility of the capturing devices.

The applicability of EMG-based speech recognition in acoustically harsh environments, such as first responder tasks where sirens, engines, and firefighters breathing apparatus may interfere with reliable communication, has been investigated at NASA. For example, Jorgensen and colleagues (Betts et al., 2006) achieved 74% accuracy on a15-word classification task, in a real-time system which was applied to subjects exposed to a 95 dB noise level.[13] Electromyography thus captures electrical stimuli from the articulator muscles or the larynx, which can subsequently be exploited in speech processing applications. One may also imagine, however, capturing viable speech bio signals directly from the brain, using electroencephalography (EEG) or implanted cortical electrodes. These possibilities are discussed in the following two sections. Although considerably further off in terms of commercial application, these Brain Computer Interface (BCI) approache very much in vogue today – are fascinating, and hold enormous promise for speech, as well as for other types of applications.

VII. ULTRASOUND SSI

Another way to obtain direct information on the vocal tract configuration is via imaging techniques. Ultrasound imagery is a non-invasive and clinically safe procedure which makes possible the real-time visualization of one of the most important articulators of the speech production system the tongue. An ultrasound transducer, placed beneath the chin, can provide a partial view of the tongue surface. Ultrasound device which is coupled with a standard optical camera as shown in Fig 3 is used to capture tongue and lip movements. Because of its non-invasive property, clinical safety and good resolution, ultrasound is well adapted to vocal tract imaging and analysis. Furthermore, since laptops with high performance ultrasound imaging systems are available, a portable real-time SSI system with an ultrasound transducer and camera, can be feasible.

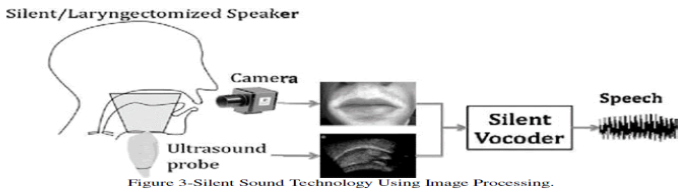

FIG 3: SCHEMATIC OF ULTRASOUND SILENT SOUND INTERFACE

The speech synthesis from the analysis of articulator motion is usually done by the use of a two- or three-dimensional articulator model of the vocal tract However, the state of the art in high quality speech synthesis uses a segmental approach(or HMM-based methods, as discussed later), in which the speech waveform is obtained by concatenating acoustic speech segments. This technique uses visual observations of articulators to drive a Segmental Vocoder. The terms visual Information and visual observations are taken to refer both to the ultrasound and optical images. This approach integrates a phone recognition stage with a corpus-based synthesis system. As the first (off-line)step, an audiovisuall dictionary is built from a training set containing units which associate the acoustic and visual realizations of each phone; this dictionary will later be used in the synthesis step.Given a test sequence of visual information only, the vocoder generates the speech waveform in three
stages as shown in figure 4:

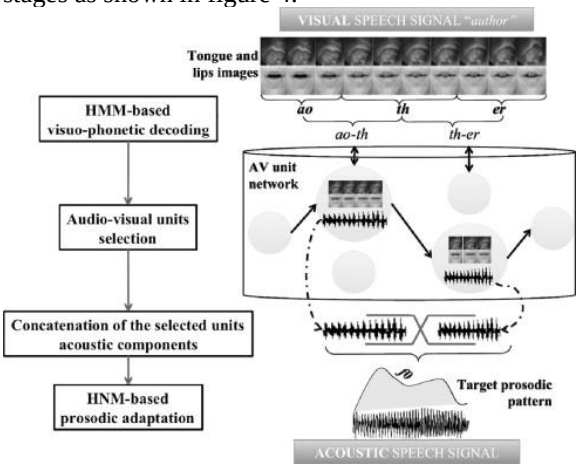

FIG4:OVERVIEW OF THE SEGMENTAL APPROACH FOR A SILENT VOCODER DRIVEN BY VIDEO-ONLY SPEECH DATA.

VIII. DATA ACQUISITION

As shown in figure 5, the hardware component of the system is based on:

- The Terason T3000 ultrasound system which is based on a laptop running Microsoft Windows XP and provides 640x480 pixels resolution images
- 140° microconvex transducer with 128 elements (8MC4)
- An industrial USB color camera able to provide 60 fps with a 640x480 pixels resolution (USB 2.0, WDM compliant)
- An external microphone connected to the built-in soundcard of the T3000

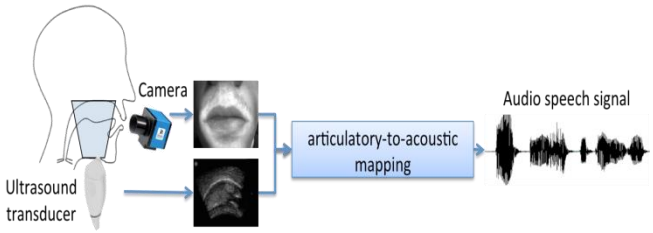

FIG 5: SHOWS A TYPICAL ULTRASOUND SSI SYSTEM

In the context of a silent speech interface based on tongue and lip imaging, the desired acquisition system should be able to record synchronously ultrasound data and video data at their respective maximum frame rate together with the acoustic speech signal. In order to have a compact, transportable, and easy-to-use system, a PC-based hardware architecture coupled with a single control program has been adopted. In the described system, data streams are recorded, processed and stored digitally on a single PC using our stand-alone software Ultraspeech.

IX. COMPARISON OF TECHNOLOGIES

The research article titled "Silent Sound Interfaces"[15] contrasts these two technologies based on the following parameters:

- Works in silence – Can the device be operated silently?
- Works in noise – Is the operation of the device affected by background noise?
- Works for laryngectomy – Can the device be used by post-laryngectomy patients? It may be useful for other pathologies as well, but laryngectomy is used as a baseline.
- Non-invasive –Can the device be used in a natural fashion, without uncomfortable or unsightly wires, electrodes, etc.?
- Ready for market – Is the device close to being marketed commercially? This axis also takes into the account in a natural way the current technological advancement of the technique, responding, in essence, to the question, How well is this technology working as of today?.
- Low cost – Can the final product be low cost? The answer will depend, among other factors, on whether any exotic technologies or procedures are required to make the device function.The article discusses the results(Scores out of 5) as follows:

A)Electromyography

Works in silence: 5 – Silent articulation is possible. Works in noise: 5 – Background noise does not affect

the operation. Works for laryngectomy: 5 – No glottal activity is required. Non-invasive: 4 – A facemask-like implementation should eventually be possible, thus eliminating unsightly glued electrodes. Ready for market: 3 – EMG sensors and their associated electronics are already widely available. Low cost: 4 – The sensors and the data processing system are relatively manageable.

B)Ultrasound Ssi

Works in silence: 5 Silent articulation is possible. Works in noise: 5 – Background noise does not affect the operation. Works for laryngectomy: 5 No glottal activity is required. Non-invasive: 4 Miniaturisation of ultrasound and camera and gel-free coupling should eventually lead to a relatively portable and unobtrusive device. Ready for market: 3 Recognition results suggest a useful, limited vocabulary device should not be far off, but instrumental developments are still necessary. Low cost: 3 – Although costs much below those of medical ultrasound devices should eventually be possible, ultrasound remains a non-trivial technology.

X. FUTURE PROSPECTS

As already discussed, Electromyography interprets the speech merely by analysing the signals generated by monitoring the muscle activities in the vocal tract. Nanobots can be injected into the blood stream. These bots, attached with RNA strands, adhere to skeletal muscles of vocal tract and transmit information about vocal activity. Instead of employing chords to measure electric signals, these signals can be monitored through special sensors attached to mobile or portable devices and help transmit information wirelessly.

TERC band is interfaced with cellular phone: Transmission of the acoustic signal is managed via an application. The TERC band transmits the vibration signal developed due to glottis movements.

Computer brain interface: Brain signals are sensed by sensors and then they are processed and compared with the patterns stored in database and accordingly the speech is converted. Image Processing Techniques like Image Segmentation and Histogram Equalisation can be used to compare the images of tongue and lips obtained with the database. There has been a revolution as far as techniques for image comparison are considered.

XI. CONCLUSION

As we can see from the survey results mentioned in Section 3, both the technologies can work in noisy environments to produce desired results. These technologies are non invasive and safe on medicinal grounds. With the advent of nanotechnology, nanobots can be assigned the task to retrieve the signals of vocal activity, giving away with the chords required to monitor. Also the entire system can be turned wireless by sending the monitored signals wirelessly for analysis. Speech Synthesis techniques have come a long way since LPC method. Also, Mobile manufacturing companies can have a large chunk of profits if they embed these technologies in the cell phones. These advantages are indicative of the fact that Silent Sound Technology has it all for it to be embedded in our daily lives.

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Multi-core Fiber for High-Capacity Long-Haul Spatially-Multiplexed Transmission

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Data traffic is growing exponentially due to the emergence of various network services. Although the transmission capacity of optical fibers has dramatically increased thanks to advanced communication technologies such as wavelength-division multiplexing and multi-level modulation, the capacity is rapidly approaching its fundamental limit as the amplification bandwidth has been used up and drastic improvements of the signal-to-noise ratio cannot be expected any further. To overcome this problem, space-division multiplexing has come to attract lots of attention, and we have conducted research and development on multi-core fiber (MCF), achieving positive results. This paper reviews the major achievements of our MCF research and development.

Keywords: optical fiber communication, space-division multiplexing, spatial multiplexing, multi-core fiber, inter-core crosstalk

1. Introduction

Data traffic is growing exponentially due to the emergence of various network services such as video streaming and smartphones. The transmission capacity of the optical fiber has also been increasing exponentially due to the roll-outs of technologies such as wavelength-division multiplexing (WDM)*1 and the multi-level modulation*2; however, the capacity is rapidly approaching its fundamental limit due to the depletion of the amplification bandwidth*3 and the limit of signal-to-noise ratio (SNR) from nonlinear noise*4 (1),(2). Under these circumstances, space-division mul-tiplexing (SDM) has come to attract a lot of attention(2),(3). For further increasing fiber capacity, various research groups have been investigating SDM-related technologies.

For overcoming the capacity limit, we have been promoting research and development on multi-core fiber (MCF) toward practical use. Since the MCF includes the plurality of cores as shown in **Fig. 1**, characteristics degradations specific to the MCF structure, which were not observed in the conventional single-core fiber (SCF), are concerns for the actualization of this technology. The inter-core crosstalk (XT) is one of the most important parameters in the MCF, and suppression of the XT is crucial for transmitting signals independently on individual cores. We

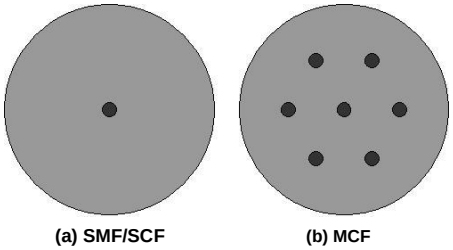

Fig. 1. Schematic cross sections of optical fibers (Darker color represents higher refractive index)

proposed and experimentally validated a theoretical model that can predict the crosstalk and its statistical characteristics of actual MCFs(4)-(7), demonstrated that low loss and ultra-low XT—necessary for long-haul transmission—can be achieved in the fabricated MCF(6)-(8), theoretically revealed the behavior of the XT as a noise(8)-(10), and enhanced the SNR of each core of the MCF based on considering the XT as a noise(11),(12), each for the first time. This paper reviews these major achievements of our research and development on the MCF.

2. Behavior of Inter-core Crosstalk

2-1 Theoretical prediction in earlier studies

Earlier studies(13)-(15) reported that the XT of the MCF can be suppressed by inducing a slight difference in the ef-fective refractive indices (n_{eff} s) between cores, based on theoretical considerations. According to these studies, the XT from Core m to Core n can be expressed by using the coupled-mode equation(16):

$$\frac{dA_n}{dz} = -j\kappa_{nm} \exp\left[j\left(\beta_n - \beta_m\right)z\right] A_m , \quad \text{..... (1)}$$

where A_n is the complex amplitude of the electric field of Core n, κ_{nm} is the mode-coupling coefficient from Core m to Core n, $\beta_n = (2\pi/\lambda)n_{\mathrm{eff},n}$ is the propagation constant of Core n, and z is the longitudinal position along the fiber. When only Core m is excited [$A_m(0) = 1$], the power of Core n can be derived as(16):

$$|A_n|^2 = F \sin^2 qz , \quad (2)$$

$$F = \left[1 + \left(\frac{\beta_n - \beta_m}{2\kappa_{nm}}\right)^2\right]^{-1}, \quad q = \sqrt{\kappa_{nm}^2 + \left(\frac{\beta_n - \beta_m}{2}\right)^2} . \quad \text{..... (3)}$$

Thus, a slight difference in n_{eff} can remarkably suppress the maximum power transfer ratio F, as shown in **Fig. 2**. This

is because the slight difference in n_{eff} can induce a large difference in β in conditions of $\lambda \sim 10^{-6}$, and the large vari-ation of the phase difference along the MCF—the phase mismatch— inhibits efficient mode couplings.

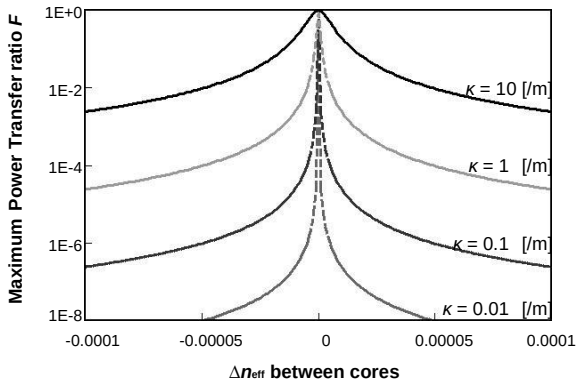

Fig. 2. The relationship between the inter-core refractive index mismatch and the power conversion efficiency F at 1550 nm

2-2 Effect of fiber bend on the crosstalk

However, the above discussion is based on the simple coupled-mode theory that assumes ideal conditions where the cores are not longitudinally perturbed, and thus was anticipated to be inapplicable to actual MCFs, which are longitudinally perturbed by various internal and external factors. We speculated that the fiber bend should have a particularly large effect on the XT, and therefore investi-gated the effect theoretically and experimentally[4].

Based on the equivalent index model[17], which has been widely used in loss analysis of bent waveguides, a bent fiber can be described as a corresponding straight fiber which has an equivalent refractive-index profile

$$n_{eq} \approx n_{mat}\left(1+\frac{r\cos\theta}{R_b}\right), \quad \text{..... (4)}$$

where n_{mat} is the intrinsic refractive index of the material, R_b is the bend radius, and (r, θ) is the local polar coordinate on the fiber cross-section (see **Fig. 3**). The equivalent effec-tive index of the Core n of an MCF can be expressed as

$$n_{eff,eq,n} \approx n_{eff,n}\left(1+\frac{r_n\cos\theta_n}{R_b}\right). \quad \text{..... (5)}$$

Equation (5) may be intuitively understood as such that the change of the optical path length due to the bend is simply translated into the change of the refractive index, although it is not a rigorous interpretation. By assuming, for expla-nation simplicity, that Core m is the center core and the distance between the centers of Core m and Core n is D_{nm}, a slight difference in n_{eff} between the cores can be nagated, as shown in **Fig. 3,** by the fiber bend when the bend radius is no more than the threshold bend radius R_{pk}:

$$R_{pk} = \frac{n_{eff,n}}{|n_{eff,m} - n_{eff,n}|} D_{nm}, \quad \text{..... (6)}$$

and the XT is considered to be largely degraded.

In order to quantify the effect of the bend on the XT, we theoretically and experimentally investigated the de-pendence of the XT on the bend radius. If the propagation constants are variable along propagation distance z, the coupled-mode equation can be expressed as

$$\frac{dA_n}{dz} = -j\kappa_{nm}\exp\left[j\int_0^z(\beta_{eq,n}-\beta_{eq,m})dz'\right]A_m \quad \text{..... (7)}$$

where $\beta_{eq,n} = (2\pi/\lambda)n_{eff,eq,n}$ is the equivalent propagation constant. **Figure 4** shows an example of longitudinal evo-lutions of XT—to be precise, coupled power, or $|A_n|^2$ cal-culated using **Eq. (7)** — and equivalent effective indices

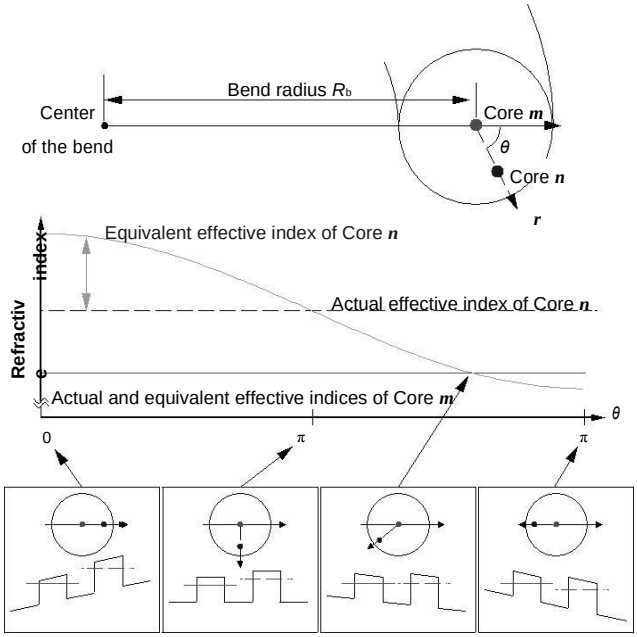

Fig. 3. Variation of the equivalent refractive index due to the fiber bend

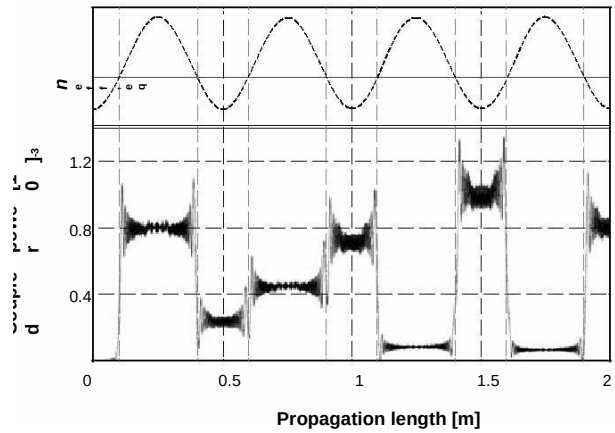

Fig. 4. Example of longitudinal evolutions of a calculated coupled power and equivalent effective indices between the two cores, in the case where the MCF is bent at a constant bend radius ($R_b < R_{pk}$) and twisted at the constant rate of 2 turns/m

between the two cores, in the case where the MCF is bent at a constant bend radius ($R_b < R_{pk}$) and twisted at the constant rate of 2 turns/m. In contrast with the simple oscillation shown in **Eqs. (2) and (3)**, the XT changed dominantly at every phase-matching point where the equivalent effective indices are equal, and the changes appear random. Only little oscillations occurred in XT at positions other than the phase-matching points.

The reason why the dominant XT changes appear random is because the phase differences between the cores are different for each phase-matching point. In the calculation, these random changes are deterministic; however, they are considered to be stochastic in practice because the phase differences can be easily fluctuated in practice by slight variations in the bending radius, twist rate of fiber, and so on. Therefore, to deal with such randomness of the XT, we conducted a Monte Carlo simulation by introduc-ing random phase shifts to **Eq. (7)**, and investigated the relationship between the bend radius and statistical mean of the simulated XT. In addition, we evaluated a fabricated MCF, and validated the above consideration and simulation method. Comparisons between the measured and the simulated XT are shown in **Fig. 5**. Points represent the averages of ten measurements under the same conditions, and the MCF was rewound before each of the ten measure-ments. The error bars indicate the maximum and the min-imum of the measured values at each bend radius. The solid line represents the average of the simulated XT for 600 instances. The measured and the simulated XT are in a good agreement. From these results, we revealed that the measured XT can be predicted by the theoretical model. Fiber designs considering the effect of the bend are neces-sary for the XT suppression in MCFs[4].

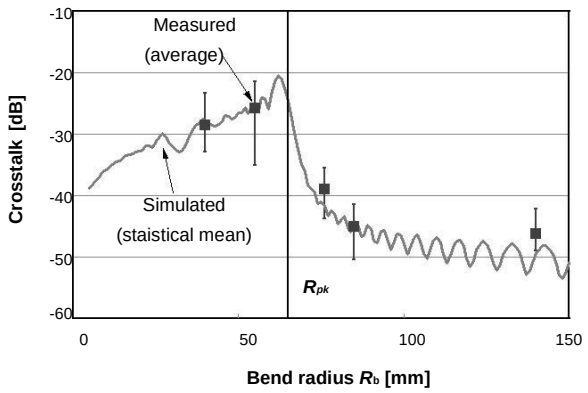

Fig. 5. Example of the dependence of the crosstalk on the bend radius

2-3 The crosstalk of the homogeneous MCF

Based on the previous section, it was found that the XT can be suppressed if R_b is adequately larger than R_{pk}, and large differences in the optical properties between the cores are required to shorten R_{pk}. On the other hand, it is unfavorable to pack different types of cores into an MCF because the characteristics of every core of the MCF trans-mission lines need to be managed. Therefore, we pro-posed a low-XT homogeneous MCF, where all the cores are identical, by utilizing the bend for inducing the phase mismatch[5]-[8].

In this section, we review the derivation and validation of the analytical expressions of the statistical characteristics of the XT of the homogeneous MCF, with which we can easily design homogeneous MCFs.

If the bend perturbation is dominant, the XT discretely changes at every phase-matching point, as shown in **Fig. 4**. These XT changes can be approximated as discrete and random mode coupling:

$$A_{n,N} = A_{n,N-1} - jK_{nm,N} \exp(j\varphi_{\mathrm{rnd},N})\, A_{m,N-1}, \quad \cdots\cdots\cdots\cdots (8)$$

where $A_{n,N}$ is the A_n after N-th phase-matching point, $\varphi_{\mathrm{rnd},N}$ the phase difference between the cores at N-th phase-matching point, and $K_{nm,N}$ the *coupling coefficient* from Core m to Core n for the discrete change. The phase dif-ference $\varphi_{\mathrm{rnd},N}$ is a random number as we mentioned above. If only Core m is excited ($A_{m,0} = 1$, $A_{n,0} = 0$), by assuming adequately low XT, the approximations of $|A_{n,N}| << 1$ and $A_{m,N} \approx A_{m,0} = 1$ hold, and the XT value X can be approximated as $|A_{n,N}|^2$. Thus, **Eq. (8)** can be approximated as

$$A_{n,N} \approx -j\sum_{l=1}^{N} K_{nm,l} \exp(j\varphi_{\mathrm{rnd},l}). \quad \cdots\cdots\cdots\cdots (9)$$

The probability density functions (PDFs) of $\Re[K_{nm} \exp(j\varphi_{\mathrm{rnd}})]$ and $\Im[K_{nm} \exp(j\varphi_{\mathrm{rnd}})]$ are not normally distributed; how-ever, based on the central limit theorem, the PDFs of $\Re[A_{n,N}]$ and $\Im[A_{n,N}]$ can converge to a normal distribution if N is large enough. With some assumptions, the variance of $\Re[A_{n,N}]$s and $\Im[A_{n,N}]$s of the two polarization modes can be analytically derived as[7]:

$$\sigma_{4\mathrm{df}}^2 \approx \frac{1}{2}\kappa_{nm}^2 \frac{\lambda R_b}{2\pi n_{\mathrm{eff},n} D_{nm}} L, \quad \cdots\cdots\cdots\cdots (10)$$

where L is the fiber length. Since the sum of powers of l random numbers—whose PDFs are the standard normal distribution— has the PDF of the chi-square distribution with l degrees of freedom (df), the PDF of X ($\approx |A_{n,N}|^2 = \{\Re[A_{n,N}]\}^2 + \{\Im[A_{n,N}]\}^2$) can be expressed as[7]

$$f(X) = \frac{X}{4\sigma_{4\mathrm{df}}^4} \exp\left(-\frac{X}{2\sigma_{4\mathrm{df}}^2}\right), \quad \cdots\cdots\cdots\cdots (11)$$

and the mean value (mean XT) of X can be expressed as

$$\mu_{X,nm} \approx 4\sigma_{4\mathrm{df}}^2 \approx \kappa_{nm}^2 \frac{\lambda R_b}{\pi n_{\mathrm{eff},n} D_{nm}} L. \quad \cdots\cdots\cdots\cdots (12)$$

It can be found, from **Eq. (12)**, that the XT can be suppressed by shortening the bend radius R_b. In decibels, 99.99 percent of the XT distribution is μ_X + ~7.7 dB—the XT distribution on the decibel scale has the constant shape independent of μ_X.

The XT distribution expressed by **Eq. (11)** can be measured with the wavelength scanning method[8]. The XT value X can be adequately dispersed by the randomization of the phase difference between cores, thanks to the wave-length dependence of the propagation constant. A measured XT spectrum is shown in **Fig. 6**, and the XT distribution ob-

tained from the data of **Fig. 6** is shown in **Fig. 7**. It can be observed that X heavily varied with wavelength and that the actual XT distribution is well fitted by **Eq. (11)**.

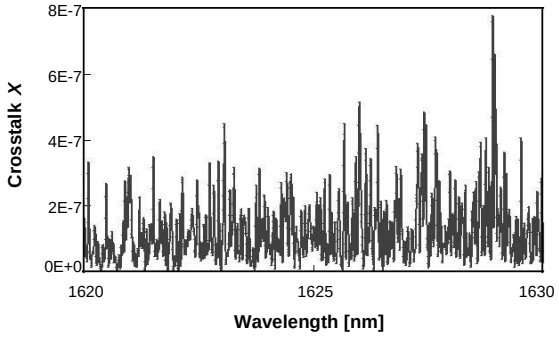

Fig. 6. Example of the XT spectrum

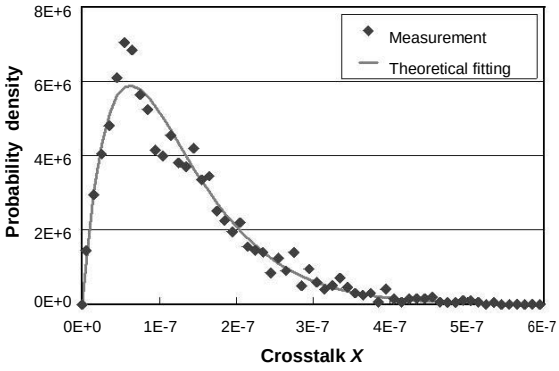

Fig. 7. Example of the XT distribution

3. Demonstration of Ultra-Low-Crosstalk Homogeneous MCF Feasible to Long-Haul Transmission

We designed and fabricated a low-XT homogeneous MCF (MCF-A) by using **Eqs. (11) and (12)**[(5)-(8)].

Figure 8 shows a cross section of the fabricated MCF-A. The core pitch, the cladding diameter, and the coating diameter of MCF-A were 45 μm, 150 μm, and 256 μm, respectively. **Table 1** shows the optical properties of each MCF-A core. The transmission loss was 0.175–0.181 dB/km (avg. 0.178 dB/km) at 1550 nm, and no more than 0.192–0.202 dB/km in C+L band (1530–1625 nm), owing to the pure sil-ica core technology. Furthermore, no loss degradations were observed in the outer cores. Including other optical prop-erties, the fabricated MCF was suitable for C+L band trans-mission that is necessary for long-haul transmission.

Figure 9 shows the mean XT between neighboring cores of MCF-A, measured using the wavelength scanning method[(8)]. The measurement results were in good agreement with **Eq. (12)**. The averages of the mean XT μ_X were

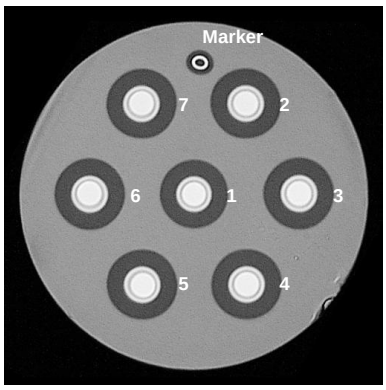

Fig. 8. A cross section of MCF-A

Table 1. Optical properties of cores of MCF-A

	Transmission loss [dB/km]		λ_{cc} [nm]	MFD [μm]	A_{eff} [μm^2]	Disp. [ps/(nm·km)]	D. slope [ps/(nm^2·km)]
λ [nm]	1550	1625		1550	1550	1550	1550
Avg.	0.178	0.198	1497	9.8	79.9	22.2	0.062
Min.	0.175	0.192	1483	9.7	78.2	22.1	0.062
Max.	0.181	0.202	1509	9.9	81.3	22.2	0.062

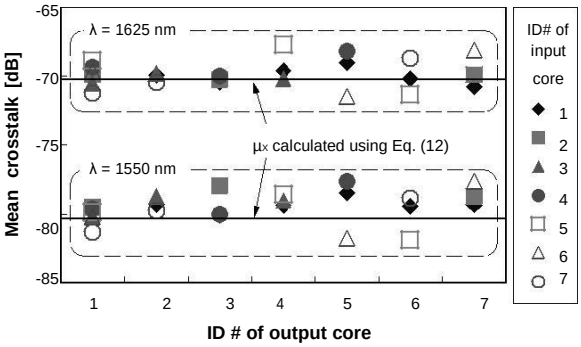

Fig. 9. Mean crosstalk between neighboring cores of MCF-A after 17.4-km propagation

as low as −79.5 dB at 1550 nm, and −69.7 dB at 1625 nm. Even μ_X from 6 outer cores to the center core (center-core μ_X) was −72.3 dB at 1550 nm, and −62.1 dB at 1625 nm.

By using **Eq. (12)**, the dependence of μ_X on the propagation length L and the bend radius R_b can be estimated, though the length and the bend radius of MCF-A was 17.4 km and 140 mm, respectively. **Figure 10** shows the relationship between the propagation length, the bend radius, and the center-core μ_X of MCF-A at 1550 nm. The center-core μ_X and the 99.99 percent of the XT can be less than −30 dB, even after 10,000 km when R_b is less than ~4 m and ~0.7 m respectively, and it was demonstrated for the first time that the XT of the MCF can be suppressed enough for ultra-long-haul transmission.

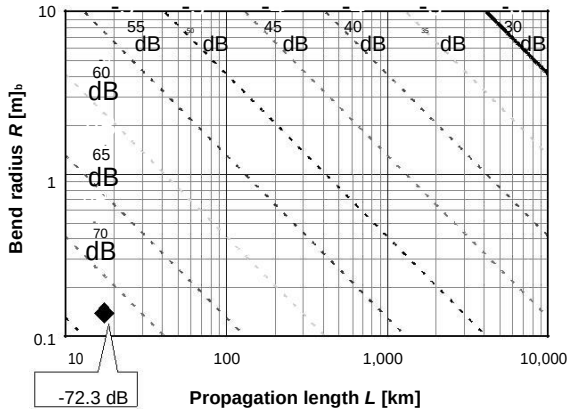

Fig. 10. The relationship between the propagation length, the bend radius, and the mean XT μ_X to the center core of MCF-A at 1550 nm. Dia-mond: R_b and L where μ_X was measured. Contour lines represent μ_X to the center core, estimated from the measurement values and Eq. (12).

With this MCF, a transmission capacity of more than 100 Tb/s per fiber was achieved, for the first time, in the transmission experiment conducted by The National Insti-tute of Information and Communications Technology, among others[18), (19)].

4. Effect of the Crosstalk on the Transmission Quality

In the previous section, the target level of the XT was set such that the 0.9999-quantile of the statistical distribution should be less than −30 dB, after an earlier study[15)], which set the target of the XT between neighboring cores as less than −30 dB. However, it was not necessarily based on theoretical groundings, which should include the consideration of the behavior of the XT as a noise. Therefore, we considered the effect of the XT on the transmission quality[9),10)], based on the stochastic behavior of the XT, which are described in the previous section.

Based on Section 2, the XT of the MCF stochastically changes with the time/wavelength variation of the phase difference between the cores, and the I- and Q-components[*5] of the two polarization modes of coupled light (XT light) are normally distributed with the variance of $\mu_X/4$. Like amplified spontaneous emission (ASE) noise[21)] and nonlinear interference noise[22)], XT can be regarded as a virtual additive white Gaussian noise when the band-width of the signal light is adequately broad, since the XT changes rapidly in the wavelength.

The Q -factor—that is, the most commonly used figure of the transmission quality— can be defined as[22)]:

$$Q = \frac{|\mu_1 - \mu_2|}{\sigma_1 + \sigma_2} \quad \text{..... (13)}$$

where μ_i and σ_i are the means and the standard deviations, respectively, of the neighboring constellation points.

The decibel value of the Q -factor can be expressed as

$$Q_{\mathrm{dB}} = 20\log_{10} Q = 10\log_{10} Q^2 . \quad \text{..... (14)}$$

Therefore, hereinafter, we will discuss the Q^2-factor instead of the Q -factor. If we assume $\sigma_n = \sigma_1 = \sigma_2$, and let $S = |\mu_1 - \mu_2|$, the nearest distance between the constellation symbols, the Q^2-factor, can be expressed as

$$Q_n^2 = \frac{S^2}{4\sigma_n} . \quad \text{..... (15)}$$

When we consider the total mean XT $\mu_{X,\mathrm{total}}$ from other cores, where the mean XT is defined as the average power of the XT light divided by that of the signal power P_s, the variance σ_x^2 of the XT light on the I–Q planes can be ex-pressed as

$$\sigma_x^2 = P_s \frac{\mu_{X,\mathrm{total}}}{4} . \quad \text{..... (16)}$$

Since the variance of a sum of statistically independent vari-ables equals to the sum of the variances of the statistically independent variables, the Q^2-factor affected by the XT can be expressed as

$$Q_x^2 = \frac{S^2}{4(\sigma_n^2 + \sigma_x^2)} . \quad \text{..... (17)}$$

From **Eqs. (15)–(17)**, XT-induced Q^2-penalty (Q_n^2/Q_x^2) can be expressed as

$$\frac{Q_n^2}{Q_x^2} = 1 + Q_n^2 \mu_{X,\mathrm{total}} \frac{P_s}{S^2} = \left(1 - Q_x^2 \mu_{X,\mathrm{total}} \frac{P_s}{S^2}\right)^{-1} , \quad \text{..... (18)}$$

where P_s/S^2 is the value determined by the modulation format. Values of P_s/S^2 for typical ideal modulation formats are shown in **Table 2**. **Figure 11** shows the XT-induced Q^2-penalty at Q_x^2 = 9.8 dB (bit-error rate BER = 1 × 10^{-3}), which was calculated using **Eq. (18)**. The XT-induced Q^2-penalty (Q_n^2/Q_x^2) can be suppressed to be less than 1 dB at Q_x^2 = 9.8 dB if $\mu_{X,\mathrm{total}}$ can be suppressed to be less than −16.7 dB for PDM-QPSK, −23.7 dB for PDM-16QAM, and −29.9 dB for PDM-64QAM.

This result revealed that signals modulated with a high-order modulation with a spectral efficiency (SE) of 10 bit/s/Hz or more can be transmitted with no significant penalty if $\mu_{X,\mathrm{total}}$ is less than about −30 dB after the propagation of the total MCF link, and that MCF-A can transmit the high-SE signals over ultra-long-haul (> 10,000 km) links in terms of the XT.

Table 2. Values of P_s/S^2 for the typical modulation format

Modulation format	P_s/S^2
PDM-QPSK	1
PDM-8PSK	$2^{1/2} / (2^{1/2}-1)$
PDM-16QAM	5
PDM-32QAM	10
PDM-64QAM	21
PDM-128QAM	41

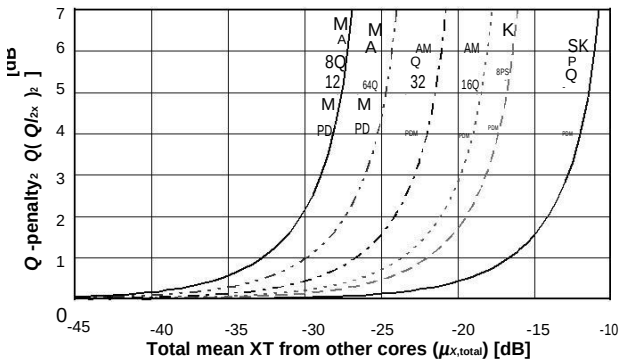

Fig. 11. XT-induced Q^2-penalty at $Q_{w/XT}^2$ = 9.8 dB

5. Enhancement of SNR in MCF

Though the XT of MCF-A was confirmed to be extremely low, the suppression of noises other than the XT is also very important for long-haul transmission.

Recently, owing to the actualization of digital coherent detection, the phase information of light can be received, and linear distortions—such as the chromatic dispersion— can be compensated by digital signal processing. There-fore, the suppression of the ASE noise and the nonlinear interference (NLI) noise has become one of the most im-portant issues for the SCF for high-capacity transmission(2), and a recent high-capacity transmission experiment has employed an SCF that has low loss for ASE noise suppres-sion and large effective area A_{eff} for NLI noise suppres-sion(23).

The XT of MCF-A was suppressed to an extremely low level; however, the transmission loss was higher than that of typical pure-silica-core SCF (≤ 0.17 dB/km)—though it was lower than that of the standard SMF (SSMF) and the lowest in reported MCFs, and A_{eff} was not improved from SSMF. Therefore, we proposed an MCF that can suppress the ASE and NLI noises by lowering loss and enlarging A_{eff} and can *properly* suppress the XT simultaneously(11),(12).

5-1 Effect of crosstalk on SNR

For the single-core dispersion-uncompensated Nyquist WDM*6 transmission system, SNR can be estimated using closed-form equations(21), and the maximum SNR achievable in the system (SNR_{SC}: the SNR includes ASE and NLI noises but does not include XT) can be derived.

As described in Section 4, when the bandwidth of the signal light is adequately broad, XT can be regarded as a virtual additive white Gaussian noise, similar to ASE and NLI noises. Accordingly, the maximum SNR achievable in the multi-core system (SNR_{MC}: the SNR includes ASE, NLI, and XT noises) can be derived(11),(12), by expanding the equations in Ref. (21). From the derived expressions, it was found that the XT-induced SNR penalty (SNR_{SC}/SNR_{MC}) is dependent on the noise figure F of optical amplifiers, the whole bandwidth B_{WDM} of WDM, and the span length (interval of the amplifiers), but independent of the num-ber of spans, or (the length of transmission link) = (the span length) × (the number of spans). This is because F, B_{WDM}, and the span length affect the ratio of ASE/NLI noise increase per unit length to the XT increase per unit length, but the number of spans does not affect the ratio.

Figure 12 shows the XT-induced SNR penalty in the MCF with SSMF cores (loss ~ 0.19 dB/km, A_{eff} ~ 80 μm^2) at a wavelength of 1550 nm in the condition at the span length of 80 km. It was found that the SNR penalty begins to drastically degrade when $\mu_{x,total}$ per one 80-km span ex-ceeds 10^{-4} (−40 dB), and that the effect of over suppression of the XT is limited.

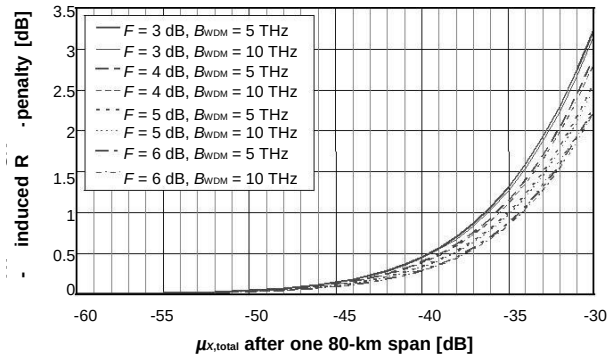

Fig. 12. XT-induced SNR penalty in the MCF with SSMF cores (A_{eff} ~ 80 μm^2). (F : the noise figure of optical amplifier, B_{WDM}: the whole bandwidth of WDM)

5-2 Fabrication of the low-loss large-A_{eff} low-XT MCF

$\mu_{x,total}$ of MCF-A was about −66 dB at 1550 nm after 80-km propagation, and it can be noted that the $\mu_{x,total}$ was suppressed *too much* in terms of the suppression of the XT-induced SNR penalty. Thus, by relaxing the target of $\mu_{x,total}$ such as less than −40 dB after 80-km propagation and lever-aging the relaxed margin for enlarging A_{eff} of each core, we designed and fabricated an MCF (MCF-B) that can si-multaneously achieve low loss, large A_{eff}, and low XT.

Figure 13 shows a cross-section of the fabricated MCF-

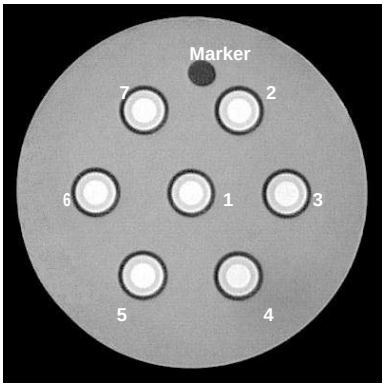

Fig. 13. A cross-section of MCF-B

B. Measured optical properties of MCF-B are shown in **Table 3** and in **Figs. 14 and 15**. The transmission loss we achieved was 0.163–0.172 dB/km (average: 0.168 dB/km) at 1550 nm, and no more than 0.183–0.194 dB/km over the whole C+L band, which are the lowest values among the reported MCFs. The A_{eff}s were 121–127 μm^2 (average: 124.1 μm^2). The core pitch and the cladding diameter of MCF-B were 51 μm and 188 μm. The μ_X between the neigh-boring cores were from −62.8 dB to −59.2 dB (average: −61.3 dB) for L = 6.99 km and R_b = 140 mm at λ = 1550 nm, and the center-core μ_X was −53.1 dB. Accordingly, the center-core μ_X was estimated to be −42.5 dB after 80-km propagation.

Table 3. Optical properties of cores of MCF-B

	Transmission loss [dB/km]	λ_{cc} [nm]	MFD [μm]	A_{eff} [μm^2]	Disp. [ps/(nm·km)]	D. slope [ps/(nm^2·km)]
λ [nm]	1550 1625		1550	1550	1550	1550
Avg.	0.168 0.188	1462	12.2	124.1	21.7	0.063
Min.	0.163 0.183	1457	12.1	121.3	21.7	0.062
Max.	0.172 0.194	1470	12.4	126.9	21.7	0.063

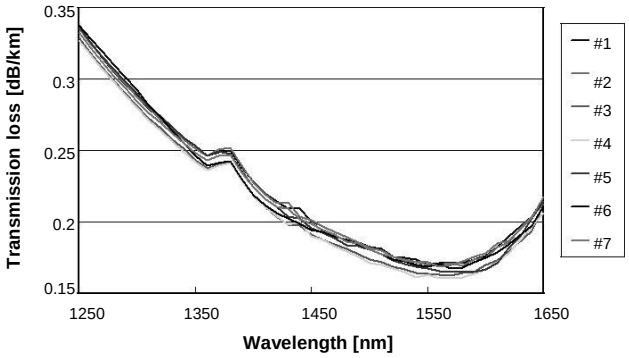

Fig. 14. Attenuation spectra of cores of MCF-B

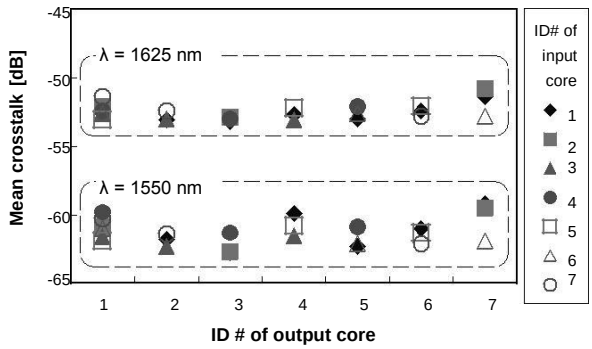

Fig. 15. Mean crosstalk between neighboring cores of MCF-B after 6.99-km propagation

5-3 SNR improvements of the fabricated MCFs from standard SMF

Figure 16 shows the calculated results how the XT-induced SNR penalty (SNR_{SC}/SNR_{MC}, shown as dash-dotted lines) and the SNR improvement (SNR_{MC}, shown as solid curves) from the standard SMF depend on SNR_{SC} and $\mu_{X,total}$ after one span, for MCF-A and MCF-B (see Ref. (12) for the details of the calculations). The calculation assumed a whole WDM bandwidth of 10 THz, noise figure of ampli-fiers of 4 dB, and a span length of 80 km. The SNR improve-ment and penalty, represented by the contour lines, are independent of the number of spans, as mentioned above. It can be seen that the SNR improvement by ASE/NLI noise suppression is cancelled if $\mu_{X,total}$ is larger than around −40 dB after 80-km propagation. It was confirmed that the SNR in each core was successfully improved in MCF-B by the design change from MCF-A to MCF-B, which leveraged the margin of the over suppressed XT of MCF-A for enlarg-ing A_{eff} (and by lowering loss). Thus, it was revealed that balanced improvements of A_{eff}, transmission loss, and XT are important. The balance of A_{eff} and XT is especially im-portant because A_{eff} enlargement weaken the power con-finements into cores.

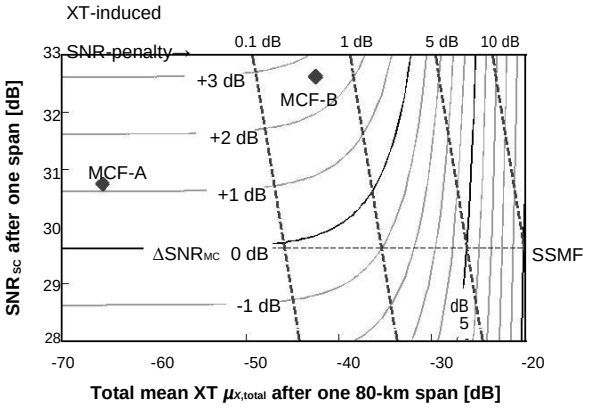

Fig. 16. SNR improvements of the fabricated MCFs compared with the standard SMF

6. Conclusion

We reviewed the major achievements of our research and development on the MCF. By investigating the behav-ior of the inter-core crosstalk (XT)—which does not occur in the conventional single-core fiber— in detail, we pro-posed and validated the simulation model that can predict the XT of actual MCFs, demonstrated the low-loss ultra-low-XT MCF feasible for ultra-long-haul high-capacity transmission by trial fabrication—the first > 100-Tb/s/fiber transmission experiment was conducted using the fabri-cated MCF. We also theoretically revealed the behavior of the XT as a noise, and improved the SNR of each core of the MCF even under the existence of the XT.

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Industrial Automation Control Using Li-Fi Technology

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Abstract: Light Fidelity (Li-Fi) could be a new technology for wireless communication. during this paper we will survey on industrial automation management victimization, Li-Fi technology is going to be analyzed in details. Its applications, challenges, and limitations are going to be mentioned. Li-Fi is going to be compared with wireless local area network (Wi-Fi). In industrial automation systems, production method ought to be quickly and safely. not like Wi-Fi, high-speed web association is provided victimization Li-Fi technology. Therefore, the pertinence of commercial automation systems of Li-Fi technology is going to be examined. The parameters that may be tracked square measure temperature, candlepower, and water level. The hardware style is finished with the surface mount devices on a double-layered computer circuit board to cut back the scale and improve the ability potency.

Keywords: light-weight Fidelity (Li-Fi), wireless local area network (Wi-Fi), industrial automation system, light communication, Windows, Linux, PCB

I. INTRODUCTION

Wireless communication system has become an indispensable part of everyday lives with the help of the technological devices (e.g. smartphones, tablets). NCR corporation/AT&T invented Wireless Fidelity (Wi-Fi) in 1991 [1]. Wi-Fi technology, which enables to exchange data between two or more devices, utilizes radio waves to send data without using wires or cables [1]. Thus, the Internet access can easily be provided in both private and public places. Radio signals, router and antenna are fundamental elements in wireless communications. Antennas and routers transmit data using radio waves and Wi-Fi receivers collect that signals [2]. Nowadays, four different types of Wi-Fi access technologies, which are Wi-Fi-802.11 a/b/g/n, are used in local area [3].

The amount of data that send through wireless network usage rises 10-fold within four years according to estimation [4]. However, Radio Frequency (RF) bandwidth is narrow and limited to allocate. In near future, a potential spectrum crisis is expected according to The US Federal Communication Commission due to limited RF spectrum range [5].

A variety of wireless solutions have been recommended to provide more data traffic [6]. In 2011, Harald Haas announced a new wireless technology that is called Light Fidelity (Li-Fi) [7]. Although Wi-Fi uses radio waves, Li-Fi uses visible light spectrum. The radiofrequency spectrum is 10,000 times shorter than the visible light spectrum as shown in Fig. 1 [5], [7].

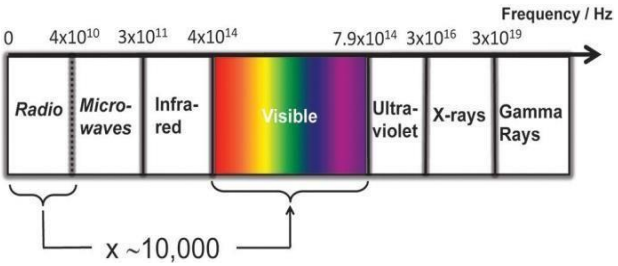

Figure 1. The electromagnetic spectrum [5]

Infrared rays can be used only low power due to eye safety regulation. Gama rays and ultraviolet light can be dangerous for human body. However, visible rays are safe for human body. Therefore, visible light is used for Li-Fi technology.

Although Wi-Fi uses modems, Li-Fi uses transceiver- fitted LED lamps that can transmit and receive information. Li-Fi can transmit more data in a very short amount of time than Wi- Fi seeing as a higher aggregate data rate is possible.

II. THE OPERATION PRINCIPLE OF LI-FI

In data transmission, Li-Fi utilizes light waves instead of radio waves so visible light spectrum is used Li-Fi technology. As mentioned previously, visible light spectrum is 10,000 times larger than radio spectrum. Therefore, Li-Fi technology offers unlimited capacity in wireless network system [8]. Although the transmission speed of fluorescents light source is 10Mb/s, LED (light emitter diode) light transmission speed is 500Mb/s. Therefore, LED light source is preferred in Li-Fi systems [9]. Essentially, Li-Fi is a Visible Light Communication system (VLC) that uses high brightness white LED lights to transmit data without wires. In other words, not only Li-Fi transfers data wirelessly but it also receives data wirelessly [7], [9].

In principle, LED lamps can be turn on and off very quickly and this situation cannot be realized in human eye. If light is on state, a digital 1 is transmitted. If light is off state, a digital 0 is transmitted. LED can be switched on

and off within nanoseconds, which gives good possibility for transmitting data [9]. A photo detector, which is p-i-n photodiode or avalanche photodiode, receives transmitted data from the light source and decodes the data [5], [9]. Parallel data transmission can be produced using LED arrays so data transmission speed is increased.

The operation principle of Li-Fi is similar with TV remote system. These two systems are shown in Fig. 2 [10].

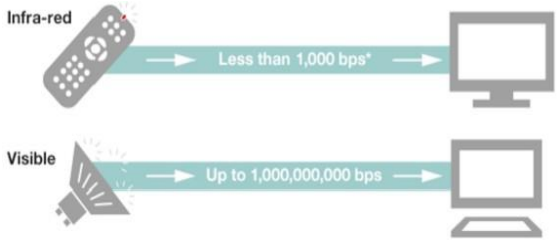

Figure 2. The operation principle of Li-Fi and TV remote control system [10] (*bits per second)

Intensity modulation and direct detection is used to encode data because LED light generates incoherent light, which is oscillating different directions. Therefore, data communication cannot use the signal phase as used in laser diodes [5].

A block diagram of the Li-Fi system is shown in Fig. 3. Power supply produces constant power for lamp driver. Lamp driver connect to the internet connection. Switch and LED lamp is connected lamp driver with fibre optics cables. LED lamp acts as a communication source. Microchip, which is located in LED lamp, converts the data into light. High-speed data is transmitted using light beam from LED lamp to photo detector. Receiver detects changing in intensity of the light beam and converts the data into electrical signal [9]. These converted data are transmitted to the technological devices [8], [9].

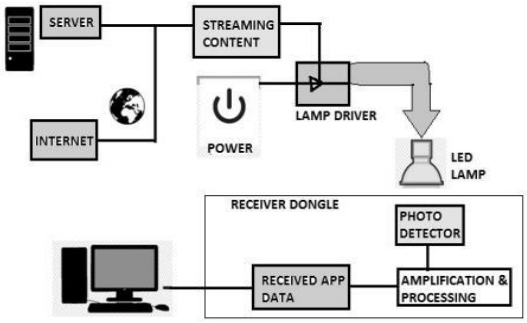

Figure 3. A block diagram of Li-Fi system [9]

Li-Fi has a variety of applications due to providing fast speed Internet access and using visible light. Wi-Fi uses radio waves for communication. However, Wi-Fi connection cannot permit in some places (hospitals, airplanes, etc.) because of radiation concerns and interfering with other radio signals [7]. Unlike Wi-Fi, signals of monitoring equipment cannot be blocked using visible light. Thus, Li-Fi can be used in hospitals to access Internet and control the medical equipment. Additionally, it may be used for robotic surgery in near future [11].

Li-Fi can provide cheaper and high speed Internet in airplane using every light source [7], [12]. In addition, Li- Fi can be used for location specific information services which are navigation and advertising. Stores use LED lights to brighten their showcases. At the same time, they can advertise their products using Li-Fi technology [12]. Museums and art galleries use specific light to illuminate exhibits. Li-Fi technology can be used to get further information about the object using that specific light.

RF that cannot use in intrinsically safe environments such as petrochemical plants and mine generate antenna sparks but Li- Fi can be used due to safer than radiofrequency communication [12]. Petrochemical plants need fast interconnected data systems to monitoring core temperature and grid integrity. Li-Fi technology provides cheap and fast internet connection to data transmission [7], [12].

Strong signals are absorbed in water so Wi-Fi fails in underwater communication.

However, light can pass through water so Li-Fi can be used in underwater communication [12].

In outdoor environment, between two radios base station distance is about 200-250 meters. In current communication system, radio base station should be positioned in every 250 meters. However, streetlights can be utilized as free access point for high speed Internet along the street using Li-Fi technology [7]. Thus, street lights provide fast and cheap internet connection along the street. Another application is vehicle-to-vehicle or vehicle-to-roadside communication using Li-Fi technology [7] [11]. Traffic lights, street lights and car lights are LED-based. Cars not only can communicate each other but also can communicate traffic light using Li-Fi technology as shown in Fig. 4. Roadside infrastructures, location, direction of travel and each vehicle's speed can be exchanged using Li-Fi [7], [12]. Thus, traffic can be managed and accidents can be reduced.

Figure 4. Vehicle-to-Vehicle communication [13]

Li-Fi technology is used different usage models. Li-Fi consortium defined Giga-speed technologies for different usage purpose. Giga Docks, Giga-Shower, Giga-Beam, Giga-MIMO and Giga-Spot models are different type of Giga-speed technologies [14]. These models address various user scenarios for wireless indoor-like and indoor data transfer. Giga-Docks models including wireless charging for technological devices, which aresmartphones, notebooks or tablets, with speed up 10Gb/s [14]. Unidirectional data services are provided using Giga-Shower. This model enables several channels to multiple users gigabit-class communication speed [14]. Giga-Beam models are used a point-to-point data link for applications or portable-to-portable data exchanges. That means, full HDTV movie can be transferred one device to another device within seconds. Giga-MIMO is an optical wireless multi-channel hot-spot solution which offers bidirectional gigabit-class communication in room [14]. Giga- Spot is an optical single-channel hot-spotsolution.

III. COMPARISON OF LI-FI WITH WI-FI

Current wireless technology, which is called Wi-Fi, has various problems. These problems can be divided into three main groups that are capacity, efficiency and security [8]. Radiofrequency spectrum is narrow so Wi-Fi technology offers limited bandwidth. In addition, 3G and 4G technologies run out of this limited radio spectrum [15]. However, visible light spectrum is 10,000 times wider than radiofrequency spectrum so Li-Fi technology offers unlimited capacity for communication systems. According to Haas, Li-Fi technology is ready for IoT and 5G [15].

On the one hand, Wi-Fi technology uses base station or cellular radio masts to transmit data using radio waves.

1.4 million base stations consume remarkable energy especially to cooling stations. The efficiency of these stations is only at about 5% [15]. On the other hand, Li-Fi uses light waves to transmit data using LEDs. LEDs consume less energy as compared base stations. It can be seen clearly, wireless communication can be cheaper and more efficient using Li-Fi technology.

Energy efficiency graph is shown in Fig. 5. In this graph, Li-Fi and Wi-Fi technology is compared. Energy efficiency of Wi-Fi network declines rapidly while users increasing. However, the energy efficiency of Li-Fi network remains constant along a large number of users. The green curve represents the ratio between Li-Fi and Wi-Fi. As can be seen in this graph, Li-Fi is more energy efficient network technology than Wi-Fi.

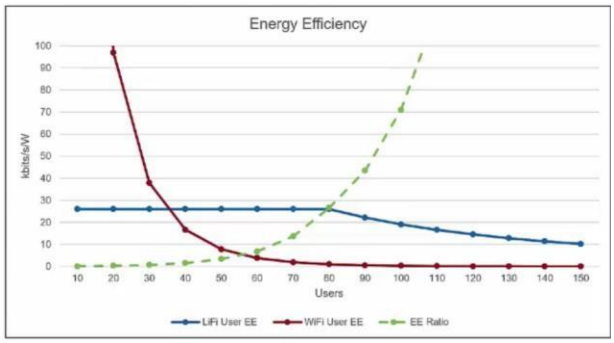

Figure 5. Energy efficiency of wireless technologies [15]

Radio waves can pass through walls and any objects in environment so private networks can be used by someone else [7]. This situation increases security problem in Wi- Fi communication. Light cannot pass through any objects and walls so private network cannot be used someone else for any negative purpose. Therefore, Li-Fi provides secure and private environment. Radio frequencies penetrate human body and can cause cell mutation but light are not harmful for human body. Unlike Wi-Fi, Li- Fi offers safe and green communication environment [7].

Another issue is speed of Internet that is around 11 Mb/s for Wi-Fi connection is 1Gb/s for Li-Fi connection. It can be clearly seen that Li-Fi is a high-speed wireless technology [15]. Data transmission rate of different LEDs is shown in Fig. 6. Different type of LED light source can affect data transmission rate as shown in below graph. 100Gb/s transmission rate are achieved in laboratory environment using laser LEDs [16].

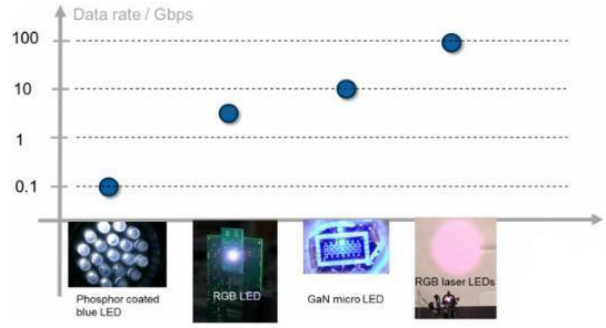

Figure 6. Different LED light transmission rates [16]

Wi-Fi Internet connection area is around 100 meters. However, Li-Fi Internet connection area is based on LED lights. That means Internet connection area can be widening using LED lamps as shown in Fig. 7. This characteristic feature is a great advantage for places that need large Internet access area (e.g. factories, industrial places).

Figure 7. Widening Li-Fi internet connection using LEDs

All these differences are shown in below Table I.

TABLE I. COMPARISON TABLE OF LI-FI WITH WI-FI

Li-Fi has limitation and challenges despite all these advantages. Light cannot pass through walls and solid objects. On the one hand, this situation provides more secure communication environment. On the other hand, solid objects on light pathways can affect data transmission. Researchers try to solve line-of-sight problems for Li-Fi technology. In these days, they work on hybrid model. Hybrid model will include both Wi-Fi and Li-Fi technology. The working principle of hybrid system will be simple. When Li-Fi connection is interrupted for some

reasons, Wi-Fi connection will be activated. Therefore, Internet connection will continue without any interruption. However, hybrid model has not been implemented yet.

Sunlight, natural light and electric light are different light sources. These different light sources can affect data transmission speed. In Li-Fi technology, receiver and light source should be placed a perfect position to reach high-speed transmission rate [7]. Li-Fi has a high installation cost because it is a new technology.

IV. Applicability of Industrial Automation Systems of Li-Fi Technology

In industrial manufacturing process, it is extremely important that process should be completed fast and safely besides product quality. Therefore, the communications between units are developing day by day in nowadays- industrial automation systems. These developments that mostly depending on usage of protocol are shown data transmission rate and security.

In industrial applications, while monitoring and control are being done in real time benefiting various network topologies. The efficiency of network is an important factor while this topology is chosen. However, it will be useful to take into consideration; the using network topology is used to recognize devices besides data transmission speed may vary depending on the distance between units. Under these criteria, many industrial automation companies are trying to provide with different communication protocols. It offers significant advantages in terms of both cost and speed if data transmission is done wirelessly. Wireless monitoring and control systems are provided a major contribution to the development of the SCADA systems. Wireless communication systems, especially applications are made with web-based or smartphones, has been used successfully. As compared with Wi-Fi, Li-Fi technologies should be preferred because of having high-speed data transmission rate and more secure in wireless communication systems.

In current wireless communication system have a security gap because radio waves can pass through the walls. Security gap is a big disadvantage for industrial automation systems that are working in higher-up security level. Light waves cannot pass through the walls. Therefore, these industrial automation systems are protected using Li-Fi technology.

As mentioned previous chapter, line-of-sight is a big challenge for Li-Fi systems. Some people claim that Wi- Fi is an over light based communication technologies and is not much affected from line-of-sight problem as compared with Li-Fi in a factory environment that includes lots of moving obstacles. Therefore, Wi-Fi systems are more useful than Li-Fi for industrial areas. However, when considering a factory, Wi- Fi connection receivers are positioned in specific locations. The internet connection is delivered to the robotic arms via Ethernet cables. When Wi-Fi systems are replaced with Li-Fi, still receivers are positioned in specific locations and nothing can interrupt light. Therefore, internet connection can be provided without any interruption to the robotic arms or any other devices. Thus, line-of-sight problem are solved. In addition, it can be clearly seen that production process will be faster with using Li-Fi, which is provided high- speed data transmission rate. This system model is shown in Fig. 8.

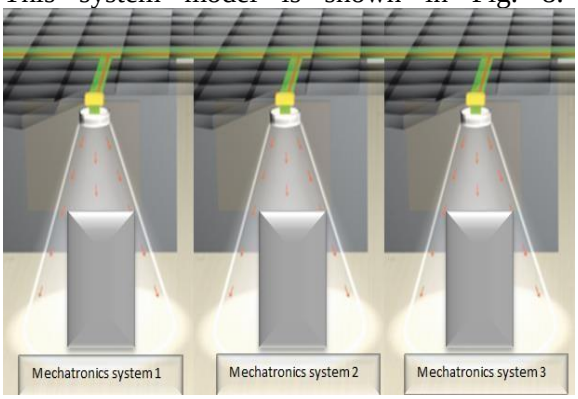

Figure 8. Li-Fi connection system in a factory

V. RESULTS AND DISCUSSION

This system is very useful in all types of industries which acquire large area and having a large production.

The system includes very high degree of automation in it. The system includes very high degree of automation in it and also it is very cost effective. The system is also useful in green house automation, chemical industries, food industries and many more. The additional slaves can be added for measures various other parameters. Also controlling action can be set for some predefined cases in the master module which enables the automatic operation at certain cases.

VI. Conclusion and Future Work

In this article, the new wireless communication technology, that is termed Li-Fi, was examined in details. Li-Fi netaffiliation space will be extendible mistreatment LEDs, that is found consecutive.
In different words, net affiliationwill be provided for giant areas while not disconnection.
In industrial automation systems, safe and high-speed net affiliation is a very important 2 factors for production method. Considering the very fact that a Li-Fi affiliation is proscribed with the realm of semiconductor diode lights, the surfacereach to the network isn't potential. That results in a really secure affiliation. Thus, the Li-Fi technology brings safety affiliation. This reality may result in additional application fields for future work. as an example, the Li-Fi will beemployed in military networking systems. The management of military devices through Li-Fi is also investigated in future studies. in addition, the finance departments of firms or banks could use Li-Fi so as to get safer networks.
In addition, all of those, if hybrid model is enforced for world, this model are going to be additional appropriate for industrial automation systems to incorporate Li-Fi and Wi-Fi systems' blessings.

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The Comparison of Non-Cooperative Spectrum Sensing Techniques for performance improvement of Cognitive Radio

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Abstract: The Cognitive radio is the emerging wireless communication system. In the fundamental wireless communication system, the static allocation of spectrum is used and that directed to the problem called spectrum scarcity. The concept of cognitive radio was suggested by the Mitola in 1998. Spectrum sensing is an important and motivating issue in Cognitive radio. Spectrum sensing is the technique to find the primary user transmission in the assigned licensed spectrum band. The numerous non-cooperative spectrum sensing techniques and their comparisons given in this paper.

Index terms: *Cognitive Radio, Primary User, Secondary User, Spectrum Sensing, Match Filter Detection, Energy Detection, Cyclostationary Detection.*

I. INTRODUCTION:

In cognitive radio(CR), the users that have been given the utmost priority on the use of the particular spectrum are known as Primary Users(PU) and the users with the lower priority on the use of spectrum are called Secondary Users(SU). Our main motive is to make spectrum usable for the secondary users without affecting interference to the PUs. This can be done if the SUs sense the PUs transmission before its own transmission. The secondary users check whether there is any active receiver within the range of the secondary user. If there is a presence of the active primary user then secondary user cannot transmit the signal because it will cause the interfering to the primary user. So to avoid the interference problem to the primary user it is necessary to continuously check the presence of any active primary receiver.

The secondary users need to continuously check the activities of the primary users to find the spectrum holes. Spectrum holes are distinct as the spectrum bands that can be used by the secondary user without producing interference to the primary users. This process of finding the spectrum holes is called the spectrum sensing. A cognitive radio may be furnished with different forms of cognitive capabilities i.e. a CR may sense the ON/OFF status of the PUs, or can measure the interference power level at primary receiver. Since a CR may be organized with different cognitive capabilities, it can access the radio spectrum in different ways. There are two cognitive spectrum access models we have [1]: 1) the opportunistically access model and 2) the concurrent spectrum access model. The first model is shown in Fig. 1. Here a CR user senses the spectrum to detect spectrum holes. As it detects the one or multiple spectrum holes, it reconfigures the transmission parameters (Ex., carrier frequency, bandwidth, and modulation scheme).

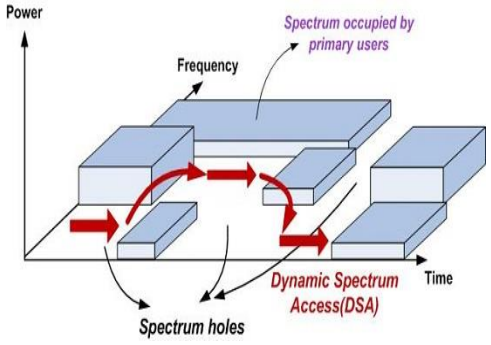

Fig.1. CR users opportunistically access the spectrum hole

The second model is shown in Fig. 2, in which both the CR user and an active PU can exist together till the interference caused by the CR transmitter to the primary receiver is below a tolerable limit. In this

model, the CR transmitter should have the knowledge of interference power level at a particular location. CR users coexist with active PUs under the interference power constraint

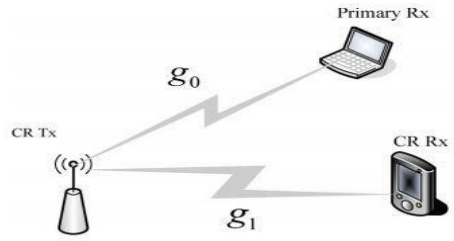

Fig.2. Concurrent spectrum access model:

II. SPECTRUM SENSING TECHNIQUES:

To detect the presence or absence of the active primary users there are different spectrum sensing techniques such as energy detection, feature detection and matched filter detection etc. have been used. Nevertheless their performance is restricted by noise uncertainty, multipath fading and shadowing, which are fundamental characteristics of the wireless channels [3-5].

Principle of spectrum sensing [1]:

the principle of the spectrum sensing shows in fig. 3. Here to guard the PU transmission, the CR Tx is required to perform spectrum sensing to check whether there is any active PU receiver in the coverage of the CR Tx. If there is any primary user transmission in the coverage of CR Tx, then CR Tx cannot transmit at that time because it will cause interference to the primary user transmission.

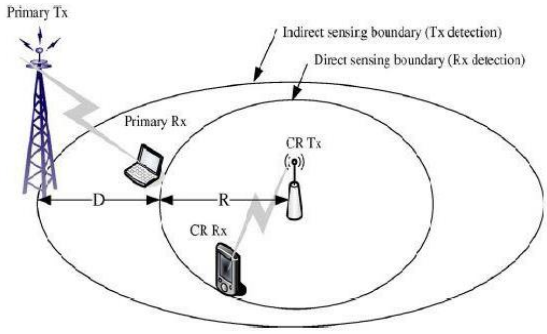

Fig.3. Principle of spectrum sensing

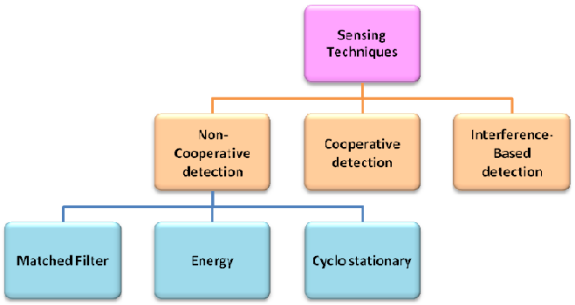

Fig.4. Spectrum sensing techniques

The above figure shows different Spectrum sensing techniques.

Non-cooperative Spectrum Sensing

Since it is difficult to sense the status of the primary receiver, so to detect the primary user transmission it is necessary to detect the signals sent by the primary transmitter. This kind of spectrum sensing is also called primary transmitter detection.

Energy Detection

If CR users have no information about the primary signals then energy detection can be used for spectrum sensing. ED is optimal detector if noise power is known to the CR user [2]. Energy detection is very simple and easy to implement. It is the most common spectrum sensing technique. In energy detection, the presence of the signal is detected by measuring the signal over an observation time.

The block diagram of the energy detection is shown in the figure. The received signal is

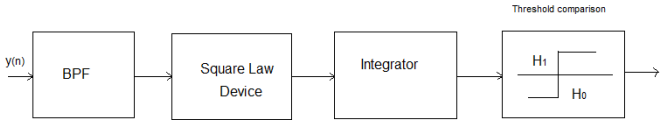

Fig.5. Block diagram of Energy Detection

passed through the band pass filter and then through a square law device to calculate its energy. The average energy of the signal is calculated by integrating it over an observation time interval through an integrator. The integrator gives the final energy output. It is compared with a predefined threshold to detect whether there is presence of primary signal or not i.e. binary decision is made. The threshold can be made fix or variable depending upon the channel condition. Energy detection is also called the BLIND DETECTION TECHNIQUE [9] because it doesn't count the structure of the signal.

Let Y be the energy output from the integrator over the N samples. The decision of the ED is made by comparing the Y with a threshold λ i.e.

$$H_0 : y(t) = w(t)$$
$$H_1 : y(t) = h.x(t) + w(t)$$

where H0 is the hypothesis corresponding to "no signal transmitted", and H1 is to "signal transmitted", y(t) is received signal, x(t) is transmitted signal, w(t) is an Additive White Gaussian Noise (AWGN) with zero mean and variance σ_n^2 and *h* amplitude of channel gain[10].

Advantages:

- Simple and less complex than other techniques
- No prior knowledge of the primary signal required
- Easy to implement

Disadvantages:

- High sensing time required to achieve the desired probability of detection using ED, it is not easy to distinguish primary signal from noise signal.
- Detection performance is limited by noise uncertainty
- Spread spectrum signals cannot be detected by ED

Matched Filter Detection

In this detection SNR of the received signal is maximized. The CR user needs to have the priori knowledge of the primary signal transmitted by the primary user. This is the basic requirement for the matched filter detection. Matched filter detection defines a correlation in which unknown signal is convolved with the filter whose impulse response is the mirror and time shifted versions of a reference signal [6].

Block diagram of matched filter detection is shown below.

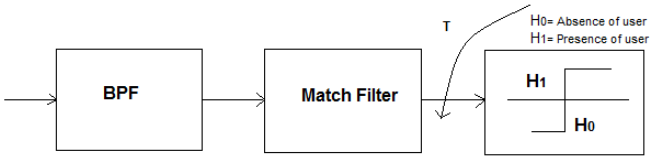

Fig.6 Block Diagram of Matched Filter Detection

Advantages:

It needs less detection time.

When information of the primary user signal is known to the CR user then Matched Filter Detector is optimal detector in stationary Gaussian noise [3].

Disadvantages:

- It needs priori knowledge of the received signal.
- High Complexity

Cyclostationary Feature Detection:

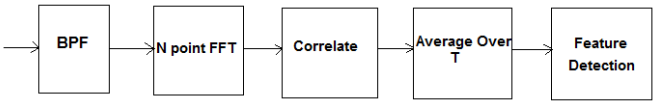

Fig.7 Block diagram of Cyclostationary Feature Detection

The modulated signals are generally cyclostationary in nature and this kind of feature of these signals can be used in this technique to detect the signal. The cyclostationary signals are having the statistical properties that vary periodically with time [7]. It is used to detect the presence or absence of primary users.

Advantages:

- Well performance at low SNR regions.
- No synchronization is required
- Robust to noise uncertainties
- Improves the overall CR throughput

Disadvantages:

- Highly complex method
- Long sensing time

The comparison of various non-cooperative spectrum sensing detections shown in bellow.

Characteristics	**Energy Detection**	**Matched Filter Detection**	**Cyclostationary Detection**
Sensing Time	High Sensing Time	Less Sensing Time	Long Sensing Time
Complexity	Less Complex	Very Complex	Highly Complex
Priori Knowledge	Not Required	Required	Not Required
Cost	Low Cost	Very High Cost	High Cost
Synchronization	Not Required	Required	Not required

Table1: Comparison of different non cooperative spectrum sensing detections

III. CONCLUSION:

The Radio spectrum is a very valuable resource for wireless communication. The use of wireless communication should be very powerfully. Cognitive radio system tells us the way how it can be used as per necessity. Through spectrum sensing, the radio spectrum can be used very efficiently. For this, the spectrum sensing should be fast and trustworthy. The basic three non-cooperative spectrum sensing can be valued for spectrum sensing and compared in this paper. Based on the comparison made, we can see that energy detection technique is most prevalent and most appropriate technique because it has low complexity, easy implementation, low cost and no priori knowledge requirement.

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Automated Irrigation System Using Microcontroller

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Abstract: Irrigation systems are as old as man itself since agriculture is the foremost occupation of civilized humanity. To irrigate large areas of plants is an onerous job. In order to overcome this problem many irrigation scheduling techniques have been developed which are mainly based on monitoring the soil, crop and weather conditions. Irrigation scheduling engrosses when to irrigate and how much water to be applied. Currently most of the irrigation scheduling systems and their corresponding automated hardware are fixed rate. Variable rate irrigation is very essential not only for the improvement of irrigation system but also to reduce the irrigation cost and to increase crop yield. The heart of automatic irrigation system (fixed rate or variable rate) is its control unit: as it controls irrigation time and water flow. Intelligent control based irrigation is necessitated to maximize the efficiency and production. Existing technologies varies from water balance or check book method to sophisticated sensor-based systems [1].Most of the irrigation systems use ON/OFF controllers. These controllers can not give optimal results for varying time delays and varying system parameters. This paper presents Artificial Neural Network (ANN) based intelligent control system for effective irrigation scheduling. The proposed Artificial Neural Network (ANN) based controller is prototyped using MATLAB. The input parameters like air temperature, soil moisture, radiations and humidity are modeled. Then using appropriate method, ecological conditions, evapotranspiration and type of crop, the amount of water needed for irrigation is estimated and then associated results are simulated.

Key words: Artificial Neural Network, Automated hardware, Irrigation scheduling, Evapotranspiration.

1. Introduction

Agriculture has, throughout History, played a major role in human societies endeavors to be self sufficient in food[2].Irrigation is an essential component of crop production in many areas of the world. In cotton for example, recent studies have shown that proper timing of irrigation is an important production factor and that delaying irrigation can result in losses of between USD 62/ha and USD 300/ha [3]. Irrigation water use represents a substantial opportunity for residential water savings. Automation of irrigation system has the potential to provide maximum water use efficiency by monitoring soil moistures at optimum level[4].The control unit is the pivotal block of entire irrigation system. It controls the flow of water and therefore enables the grower to acquire optimized results.

1.1 Types of Controllers [5,6,7,8,10,15]

Irrigation process can be controlled by two types of controllers.

1.1.1Open loop controller:

This are also called non-feedback controllers. This type of controller is designed on following principles:

- It just takes input and computes output for the system accordingly.
- It does not have any feed-back to determine whether the desired output or goal is achieved or not.

This is most simple form of controller in which basic parameters and instructions are pre-defined such as:

- When to start watering/a task
- When to end watering /a task
- Time delay intervals

During execution of above set of instructions using open loop-controller no measures are taken to check whether right amount of water is supplied or not.

These controllers may have less cost, but they are not very good and they do not provide optimal (or a good) solution to irrigation problems.

1.1.2 Closed loop controller:

They are based on pre-defined control concept and utilizing feedback from controlled object/system in some manner. In this type of controller feedback of a necessary parameter is required to check right amount of water needed for irrigation.

There are several parameters which (play important role in order to make an optimal decision. Some of these parameters remains fix through out the process. Such as:

- Kind of soil
- Kind of plants
- Leaf coverage
- Stage of growth etc.

Whereas some of them varies with time and should be measured during irrigation process.
They are physical parameters such as:

- Soil humidity
- Air humidity
- Radiation in the ground
- Temperature

Whole irrigation process is mainly based upon above specified physical parameters. Since these parameters are physical and changes with time; consequently amount of water being used for irrigation also changes.

The irrigation system explicated in this paper exploit closed loop control. The control unit continuously receives feed back from different sensors placed in the field. It enables control unit to update its data about important system parameters. The control unit decides how much water tap to open, in accordance with the data collected from sensors and predefined parameters(depending upon the crop, weather conditions etc.)

The major parameters that determine the irrigation process are:

- type of growth;
- status of the growth (height, depth of roots);
- leaf coverage;
- kind of soil and saltiness;
- water budget (economy or normal irrigation).

Therefore, the input parameters that are used by the system are:

- soil (ground) humidity;
- temperature;
- radiation;
- wind speed;
- air humidity;
- salinity (amount of salt in the ground).

The output parameters are:

- opening/closing the valves for water and/or fertilizer, and adjusting their amounts in combination;
- Turning energy systems on/off (lights, heating, ventilation);
- Opening/closing walls and roofs of hothouses[9].

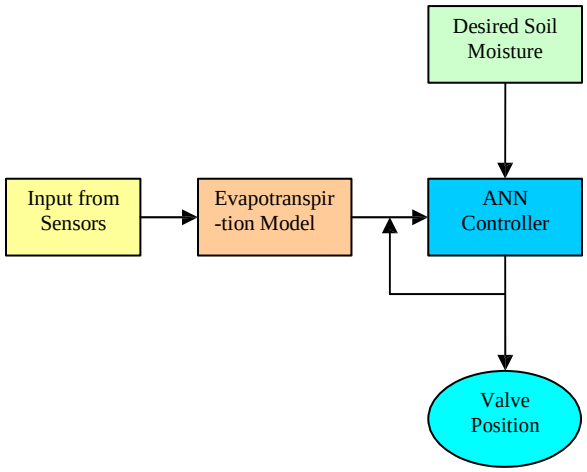

Figure1:Irrigation Control System block diagram

2.Design of ANN based Irrigation Controller

Figure 1 exhibits the block diagram of Complete Irrigation System ingrained with ANN Controller. It is seen that control system consists of four interconnected stages.

- Input from Sensors: In this stage different parameters like temperature, air humidity ,soil moisture, wind speed and radiation ,are collected. Then these parameters are passed to next stage as input.
- Evapotranspiration Model: This block converts four input parameters into actual soil moisture(details in next Section)
- Required Soil Moisture: This block provides information about the amount of water required for proper growth of plants.
- ANN Controller: This stage compares the required soil moisture with actual soil moisture and decision is made dynamically.

2.1.Modeling of System Parameters

We use the modeling of input parameters from [10];

2.1.1. Inputs Parameters: There are four factors (Temperature, air humidity, wind speed and radiation) by which evapotranspiration is influenced.
2.1.2 Temperature: This variable should be defined as a continuous signal (normally as a sine wave which simulated the day and night temperature changes), but may show sharp changes in special places like deserts and so on therefore:

- A sine wave with amplitude of 5 ºC;
- A frequency of 0.2618 rad/h. This frequency is
- measured according to a time period of 24 h: 0.2168 rad/h = 2pi/*T*=2pi/24.
- A constant bias(offset) of 30 ºC;

Figure2: Input Parameters of Evapotranspiration model-Graphical representation.

This stimulus generates a wave which at its maximum can reach 35°C (midday) and at its minimum can reach +25°C (midnight). In this way, the temperature on any given day can be simulated by changing the bias that is attached to the variable. This diversion is obtained by uniform number generation(Yellow graph in figure 2).

2.1.3 Air humidity: It is modeled as:

- A sine wave with amplitude of 10%;
- Bias of 60% (constant);
- A frequency of 0.2618 rad/h (Orange graph in Fig. 2).

2.1.4 Wind speed :

- A sine wave with amplitude of 1 Km/h;
- Bias of 3.5 Km/h (constant);
- A frequency of 0.2618 rad/h (Light Blue graph in Fig. 2) [10].

2.1.5 Radiation: It is modeled as maximum possible radiation at earth's surface (Rmax). (Light Pink graph in figure 2

- A sine wave with amplitude of 2MJ/m^2
- Bias of 112MJ/m;
- A frequency of 0.2618 rad/h.

2.2 Required Soil Moisture: It is solely dependent on the kind of plant ,type of growth ,type of land and type of soil. The required soil moisture is calculated according to the above mentioned factors. An assumed graph is shown in figure3:

2.3.Evapotranpiration Model[10,11,12,13]:

Penman-Monteith equation is a combination equation that

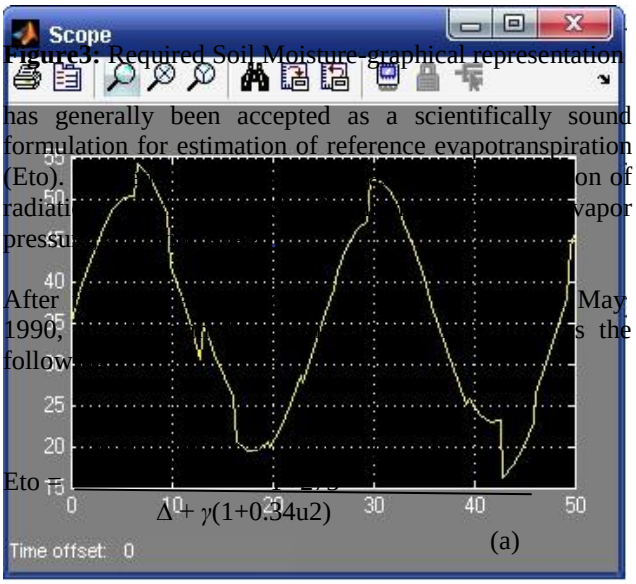

Figure3: Required Soil Moisture-graphical representation

has generally been accepted as a scientifically sound formulation for estimation of reference evapotranspiration (Eto). on of radiati vapor pressu

After May 1990, s the follow

Eto =

$$\frac{\Delta + \gamma(1+0.34u2)}{} \quad \text{(a)}$$

$$\Delta = \frac{4098eo(T)}{(T+273.3)^2} \quad \text{(b)}$$

$$e^o(T)=0.6108 \exp\left(\frac{17.27T}{T+273.3}\right) \quad \text{(c)}$$

$$\gamma = \frac{C_p P}{\varepsilon \lambda} \bullet 10^{-3} = 0.001628 \bullet P/\lambda \quad \text{(d)}$$

Where:

ET0 = Reference evapotranspiration [mm day-1],
Rn = Net radiation at the crop surface [MJ m-2 day1],
G = Soil heat flux density [MJ m-2 day-1],
T = Mean daily air temperature at 2 m height [°C],
U_2 = Wind speed at 2 m height [m s 1],
e_s = Saturation vapor pressure[kPa],
e_a = Actual vapor pressure [kPa],
e_s-e_a = $e^o(T)$= Saturation vapor pressure deficit [kPa],

D = Slope vapor pressure curve [kPa °C-1],
g = Psychrometric constant [kPa °C 1].
P = Atmospheric pressure [kPa],
z = Elevation above sea level [m],

e°(T) = Saturation vapour pressure at the air temperature T [kPa],
λ = Latent heat of vaporization, 2.45 [MJ kg-1],
Cp = Specific heat at constant pressure, 1.013 10-3 [MJ kg-1 °C-1],
ε = Ratio molecular weight of water vapour/dry air = 0.622.

2.4.Control Unit: The control unit consists of Artificial Neural Network based controller. This controller interfaces the required soil moisture and measured soil moisture. The main function of this stage is to keep the actual soil moisture close to the required soil moisture. As a result the output of this stage is control input for valve which supervises the amount of water which should be supplied in order to optimized the whole system. The block diagram of ANN based control system is shown in figure 4.

In the proposed method Dynamic Artificial Neural Network is used. Dynamic Networks are more powerful than static networks because dynamic networks have memory ,they can be trained to learn sequential and time varying patterns[14].

The controller has two inputs i.e. required soil moisture and calculated soil moisture from evapotranspiration model, and there is only one out put of controller also called control input for Valve position. It makes the system configuration very simple and straight forward.

3.ANN Controller Architecture:
ANN Controller is implemented using the following;

- **Topology:** Distributed Time Delay Neural Network is used ;
- **Training Function:** Bayesian Regulation function is used for training.
- **Performance:** Sum squared error is taken as performance measure.
- **Goal:** The set goal is 0.0001.
- **Learning Rate:** The learning rate is set to 0.05.(Figure 6).

The block diagram of ON/OFF controller is shown in figure 5. In this configuration the valve is opened when the required soil moisture exceeds the measured soil moisture and it remains closed otherwise.

Figure 7: Simulation Results of ON/OFF control based System

4.Simulation Results
(Performance Analysis)

Once the neural network is trained, it can be used as direct controller in cascade with the Evapotranspiration model. The control target is to bring the actual soil moisture as close as possible to required soil moisture and to optimize the resources like water and energy.

Keeping the aforementioned requirement in mind behavior of ANN controller is noted for reference (Required) Soil moisture. The Response of ANN controller is compared with ON/OFF controller implemented with the same evapotranspiration model. This is shown in figure 7-8.The important facts that can be extracted from the simulations are:

4.1 ON/OFF Controller

The legend of figure7 is:

- Yellow signal – Required Soil moisture
- Blue Signal-actual soil moisture.
- Light Red signal – valve out put.

1. In ON/OFF control based system ,the actual soil moisture tracks the required soil moisture but there are continuous oscillations around the required soil moisture.
2. The Continuous oscillation at the output shows that the ON/OFF control based system is not stable.

In ON/OFF controller the valve is opened and closed continuously at the extreme points(0 and 10).Due to this lot of energy and water is consumed which is undesirable.

4.2 ANN Controller:

The legend of figure 8 is:

- Yellow signal-Required Soil moisture
- Light Red signal-Actual Soil moisture
- Green-Valve output.

The actual soil moisture tracks the required soil moisture without any oscillations.

1. The error(difference between required and actual soil moisture)is steady and reasonable (less than 2%)
2. In ANN controller the ON/OFF of the valve and energy system is very low and hence lot of energy and water can be saved.

The main goal of designing the cost-effective and result oriented Irrigation Control System has been achieved by using ANN Controller.

5.Conclusions and future work

This paper has described a simple approach to Irrigation control problem using Artificial Neural Network Controller. The proposed system is compared with ON/OFF controller and it is shown that ON/OFF Controller based System fails miserably because of its limitations. On the other hand ANN based approach has resulted in possible implementation of better and more efficient control. These controllers do not require a prior knowledge of system and have inherent ability to adapt to

the changing conditions unlike conventional methods. It is noteworthy that ANN based systems can save lot of resources(energy and water)and can provide optimized results to all type of agriculture areas.

In future we plan to remove some idealizations used in this paper (such as input parameters), and will make use of real data. We also plan for hardware implementation of current work.

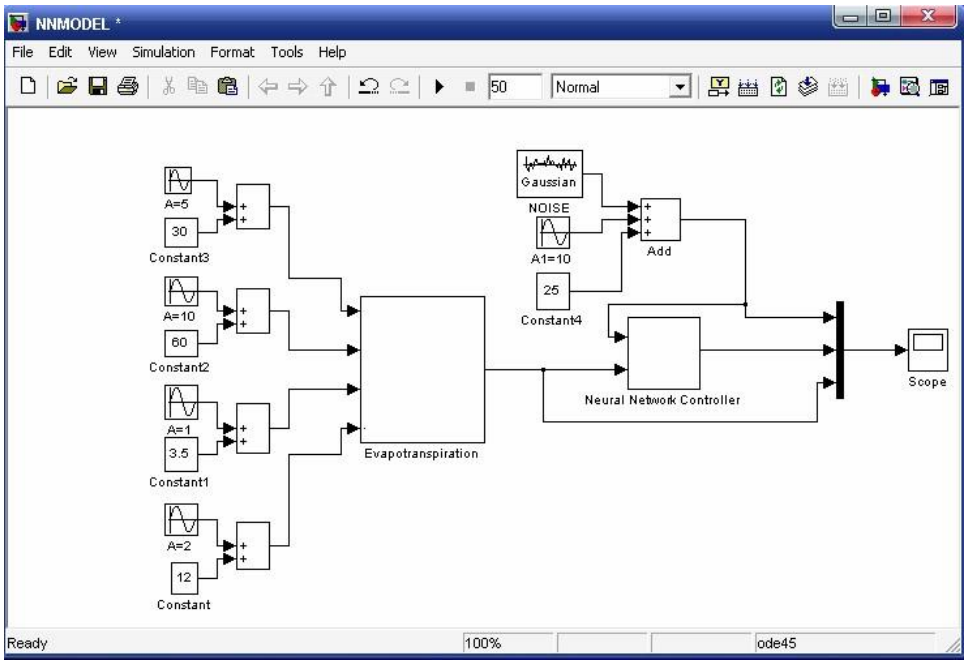

Figure4: ANN based Control System with Evapotranspiration model

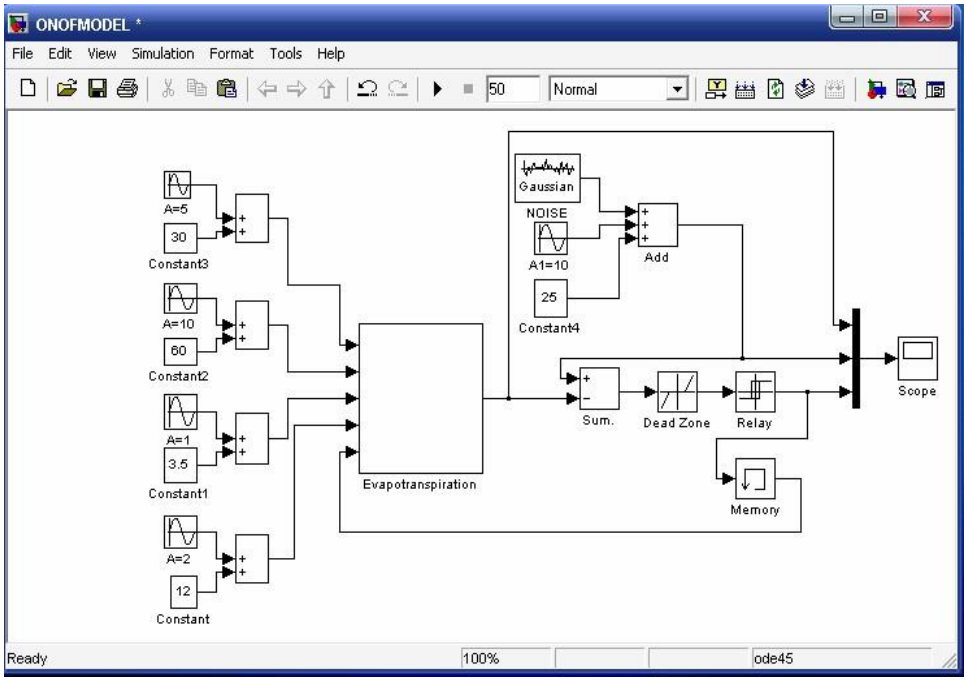

Figure5:ON/OFF based Control System with Evapotranspiration model

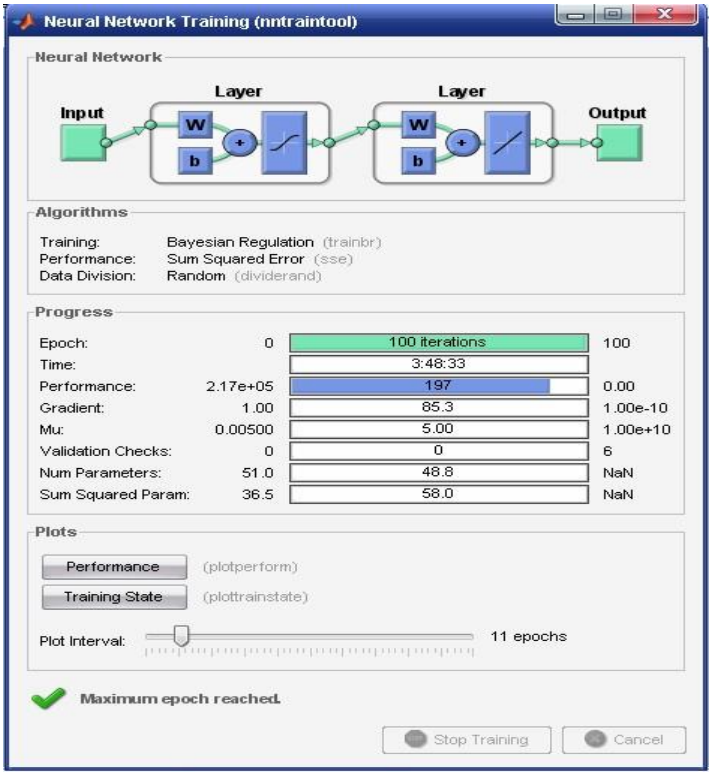

Figure 6: Neural Network Training

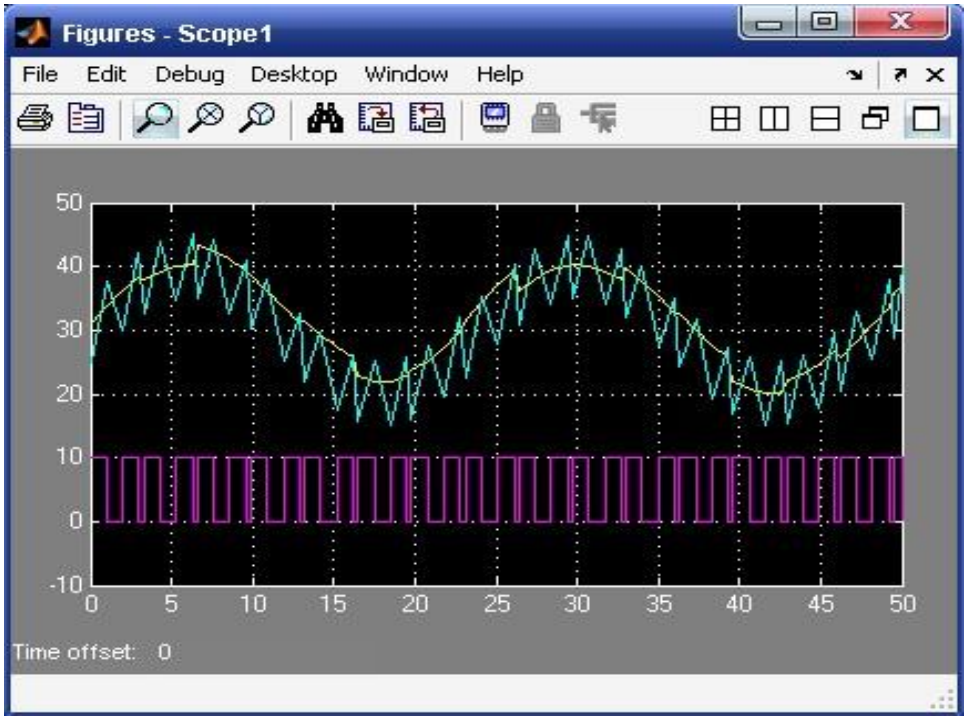

Figure 7: Simulation Results of ON/OFF control based System

Figure 8: Simulation Results of ANN based control System

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A CASE STUDY ON ULTRA LOW POWER WIRELESS BODY MOUNTED SENSORS FOR HEALTH MONITORING

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Abstract—This paper describes the design of a custom LSI which operated at less power nearly 0.5 μW for wireless sensor nodes used in animal health monitoring systems. A wireless sensor network system is composed of sensors, signal processing units, receiver and other components. There is a huge requirement to monitor body temperature and activity of animal or human with low power consumption, low power sensors and ultra-low power signal processing are essential. This presentation depicts low power technologies of wireless sensor network system developed for chicken health monitoring system. The average power consumption calculated of the wireless sensor node is less than 1μW.Here the Measurement method with bimetal type and piezoelectric type MEMS sensors which need almost no electrical power and on chip circuits of multistep selectable voltage reference generator for comparators to detect the output signal of the sensors. The piezoelectric sensor which generates even 1 mV of output voltage can be utilized by this method. The LSI consists of CMOS combination logic circuits and works at low frequency and RC oscillator to decrease the power Utilization.

Index Terms— LSI, MEMS, ultra low power, sensor network, health monitoring, chicken.

I. INTRODUCTION

Wireless sensor networks which consist of a lot of wireless sensor nodes distributed in our surrounding and linked together are expected to be used for health and medical monitoring applications as well as environmental monitoring[1], control and security .In general a wireless sensor node, consisting of sensors, a transceiver (or transmitter), a battery. In addition to this the sensor node functions, miniaturized and performance improved by using Micro electro mechanical systems (MEMS) technology. The MEMS technology is contribute to realization of autonomous sensor nodes without batteries by providing a small high-efficient energy harvesting device. Recent research has focused on hen productivity, feed consumption, health, or the quality and investigating the dynamic behavior and activity of hens housed in indoor non-cage environments. In this paper we report the results of a lightweight wireless body mounted wireless sensor system used monitor the activity of laying hens within non-cage housing systems. As an application of wireless sensor network, our group has been developing a global avian influenza surveillance system by monitoring the health

of chickens with wireless sensor nodes in poultry farms[3]. The highly pathogenic avian influenza (HPAI) virus (H5N1) infection in birds has continued, and has acquired pathogenicity not only in birds but also in mammals. The more cases of migratory birds and domestic fowls increase, the more human cases increase and the variation of the virus progresses. Consequently, risks of occurrence of a pandemic flu with transmissibility among humans increase. Therefore a global avian influenza surveillance system for the early-stage detection of birds cases must be effective to defend human beings from an influenza pandemic.The concept of our avian influenza surveillance system[5] is initial diagnosis with body temperature and activity of a chicken. In previous research, we carried out the infection experiments and found that the both sensors are useful tool for early detection. Several percentages of chickens in poultry farms are attached with wireless sensor nodes with thermistor and accelerometer. When the surveillance system detects an anomaly state of the chickens, the system automatically alerts administrators through the internet. The system can also report a history of health conditions (fever and weakness) obtained by sensors. Finally, using these data, the administrators decide whether this incident is caused by avian influenza or not. Basically, chickens have vaccinations against diseases caused by viruses except for influenza. Thus if many chickens shows abnormal states, the cause is likely to be due to influenza viruses. Although chickens can become abnormal states by physical stresses, e.g. summer heat, we can find if the cause is influenza or not by finding that how the chickens showing abnormal state spread out in a chicken house. In the case that the cause is influenza, these chickens could increase in a concentric fashion. Thus, we have to attach a wireless sensor node to some quantity of chickens in a chicken house. This paper describes avian influenza outbreaks would be detected 2 days earlier if 5 % of chickens in a chicken[6] house are attached a wireless sensor node than the current patrol system by farm workers Radio frequency identification (RF-ID) system is used for identification in livestock industry or pets. The advantage of the RF-ID system is low cost and long life time, however, the communication length is less than 1 m and the measurement of the body temperature or movements of an animal can be done only when a reader is brought close to the tag. Thus, RF-ID system is not suitable for continuous monitoring. On the other hand, in the case that we use wireless sensor nodes with transmission function using the own battery the power consumption has to be decreased [7]. For the avian influenza surveillance system, the nodes should work continuously for periods of longer than 2 years without battery replacement. Because the period when chickens produce eggs well is about 500 days. In addition, since the weight of the wireless sensor node including a battery should be less than 1 g, small button battery has to be used. Thus, an upper limit of the average power consumption could be 1 μW level.

Previously,earliar a development of an ultra low power custom LSI which has signal processing and wireless transmission functions [8] and wing band type wireless sensor node [9]. This paper,describes a wireless sensor node using a “S” shaped piezoelectric micro-cantilever with more sensitive to tiny movements of a chicken than ordinary type

micro-cantilever. And thermistor is used as not only body temperature measurement but also mode change event generator to reduce the power consumption. In addition, a demonstration experiment using more than 100 wireless sensor nodes in a chicken house are reported.

II. TECHNICAL CHALLENGES

The major challenge involved in the behavior detection of chickens is two-fold, both of which stems from the size of the subject. First, the size and weight of the sensor should be such that when it is mounted on a chicken, it does not cause any significant change in its natural behavior. This limitation does not exist in larger animals like cattle and hence sensors equipped with better processing capabilities and larger batteries, which might be bigger in size, can be used without any considerable concerns. Second, due to their smaller size and general movement patterns, the magnitude of acceleration produced by their movement is not significant when compared to that of larger animals, and hence the state space of accelerometer values obtained from chickens is very small compared to that of larger animals. The brief and jittery movements produced by chickens result in a weak correlation between the accelerometer data and the activity of the individual, which makes the behavior detection non-trivial. Furthermore, while all the accelerometer data mentioned above has provided valuable information about the behavior of the individual animal, most sensors were designed to store the accelerometer data on the sensor itself. Therefore, at some point, the accelerometer needed to be physically retrieved for data recovery and subsequent analysis, and hence, the animal must be re-caught for the data to be accessible. Thus, the

current systems do not provide remote sensing and real-time instantaneous information about events of interest. Instantaneous access to data can be very useful for researchers and animal managers who could use this information about individual hen behavior to make adjustments to the system or catch problems at early stages.

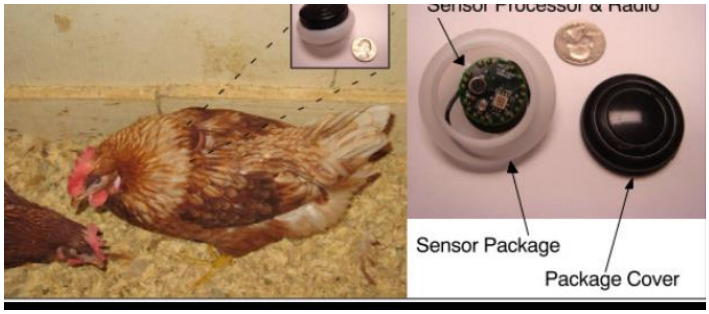

Fig: Photograph of a laying hen wearing a wireless sensor

III. LITERATURE REVIEW

In order to decrease the power consumption, the design that the LSI consists of CMOS combination logic circuits and works with 1.55V VDD (button battery). In addition, since the signal processing do not need high speed, this LSI operates using 1 kHz RC oscillator. The estimated consumption current of RC oscillator is 134 nA.

A. Input circuit for accelerometer

The enough data about activity of chickens for this surveillance system is the number of movement with 1 axis acceleration over a threshold exceeds a setting value. In this case, a 1 bit A/D converter, e.g. CMOS inverter and a comparator, is enough for this sensor. Although a CMOS inverter is the least power consumption circuit, the threshold voltage is high (about 0.7 V at 1.55 V of VDD). In

addition, the threshold voltage of a CMOS inverter cannot be adjusted. There could be individual specificity of the output voltage of a piezoelectric accelerometer. And the output voltage is very low (several mV) at slow chicken's movement. Thus, the designed one is a comparator of which threshold voltage can be changed as the input circuit of the accelerometer.

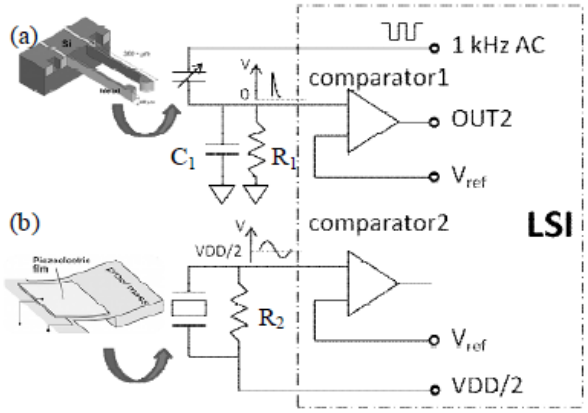

Figure 2. Input circuit for (a) MEMS bimetalthermometer
(b) MEMS piezoelectric accelerometer

Fig. 2 shows a circuit by which an output voltage of a piezoelectric accelerometer can be detected even if the output voltage is 1 mV at slow chicken's movement. Generally, a comparator most sensitively detects a voltage difference if the voltage reference (Vref) is the half of a supplied voltage (VDD).Thus ,to raise the output voltage of the accelerometer, one electrical pad of the accelerometer was connected to VDD/2. The comparator input is stabilized by R2 resister in fig. 1 connected to VDD/2 output. In the case that Vref is VDD/2 + 1 mV, the output of the comparator changes if the output voltage of the accelerometer is over 1 mV. In order to reduce the power consumption of the comparator, the bias current of the comparator was decreased down to 10 nA using an external 50 MΩ resister. The calculated total current of the comparator is 20 nA.

B. Input circuit for body temperature sensor

When a chicken is infected with the influenza, although the change of the body temperature depends on the viruses, the body temperature basically increases. For example, when a chicken is infected with a certain highly pathogenic avian influenza virus, the chicken died with slight (0.6 ^{0}C) fever. In this case, it is difficult to detect the infection with a body temperature sensor. However, since the activity of a chicken infected with any viruses decreases, we can find the infection earlier with the accelerometer. Because there are viruses which induce high fever (2.4 ^{0}C) and the infection can be found with a temperature sensor. From these results, we decided that a chicken of which body temperature is more than 42 ^{0}C (fever) or less than 38 ^{0}C (just before death) could be anomaly state. Fig. 2 shows the input circuit for the variable capacitor type MEMS bimetal thermometer. This sensor is composed of 2 bimetal cantilevers like fig. 2. One cantilever connects with an output of 1 kHz AC signal and the other cantilever connects with capacitor C1, resistor R1 and input of a comparator. First, one tip of the cantilever is away from another tip and the capacitance between 2 cantilevers is almost zero. In this case, the 1 kHz AC signal cannot go through the bimetal sensor. When the surrounding temperature change, the 2 tip of cantilevers approach each other. And then the capacitance between the 2 cantilevers increase and the AC signal starts to flow through the bimetal sensor. Thus, the sensor

works like a switch. The capacitance of C1 is for accumulation of the signal. The resistor R1 is for stabilize the voltage of input of the comparator. The temperature at which the AC signal starts to flow through the sensor can be changed by changing the length of the cantilever. We have been fabricating 2 bimetal sensors which are electrically on-state at more than 42 ^{0}C or less

than 38 ^{0}C. Since the basal body temperature of a chicken is 41 ^{0}C, these sensors are off-state when the chicken is in good physical health. Thus, in this health state the power consumption of the circuit is zero because the AC signal cannot be flow. On the other hand, when the health state of the chicken becomes bad, the AC signal flows to the input of the comparator and to the R1. In this case leak current of input of the comparator and the current flowing through R1 are consumed. If the R1 has high resistance, the power consumption of R1 can be neglected.

C. Multi-step voltage refecence (Vref) generator

Fig. 3 shows the on-chip circuit of Vref generator which gives 32 voltages from VDD/2 + 16 mV to VDD/2 -16 mV with 1 mV increment. Because Vref has to be optimized for each accelerometer, we need to be able to select the Vref by one-time programmable ROM. Generally, divided electrical potentials can be obtained by cascade connected transistors. However, if the voltage between the gate and the souse (V gs) is too small by large number of connected transistors, little current flows in the transistor. In the case of 1.55 V of VDD, the potential can be unstable. We connected transistors like fig. 3 to supply enough current. The calculated consumed current of this circuit was about 13 nA.

D. Work flow

Fig. 5 shows the work flow of the designed LSI. The MEMS bimetal thermometer changes the operation mode depending on the body temperature of a chicken. When the body temperature is from 42^{0}C to 38^0 C, the

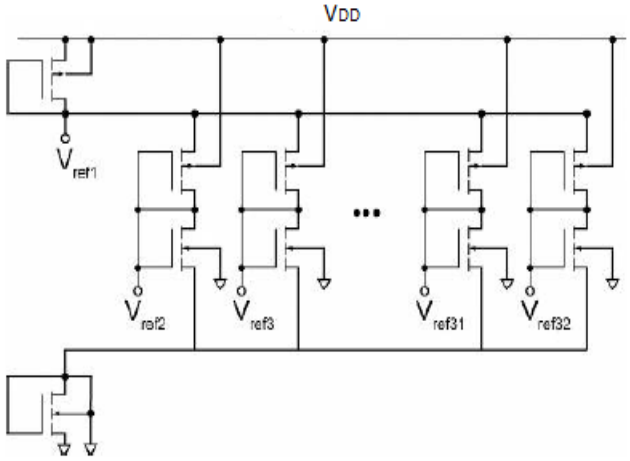

Figure 3. On-chip circuit of Vref generator for the omparators.

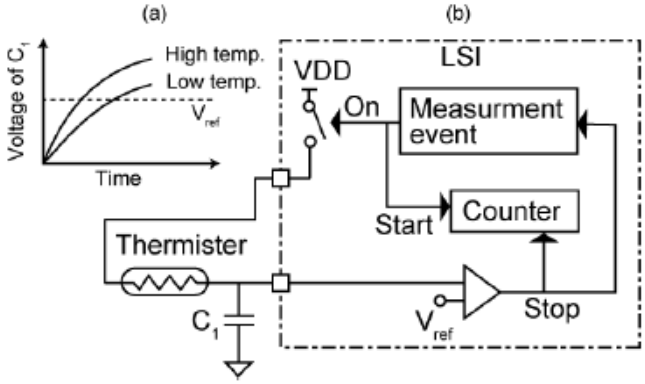

Figure 4. (a) Voltage change of the capacitance C1
(b)Measurement circuit for the thermister.

transmission event is occurred by the accelerometer. The LSI count the number of movement with acceleration over a threshold exceeds a setting value. If the count is over the setting value, the LSI transmits only the body

temperature data measured by thermister. The activity of a chicken is shown in the receiving frequency. Therefore, if the frequency of the receiving become low, we can find that the health state of the chicken is not good. On the other hand, the body temperature is more than 42^0C or less than 38^0C, the transmission event occurred by timer in the LSI. Because when the body temperature of a chicken is in that range, the chicken become low spiritedness then the transmission event almost does not occur by the accelerometer.

E. Measurement method for thermister:

fig.4 shows a circuit for a thermister. The thermister and capacitance C1 compose a integrating circuit. When the thermister measurement event occur, one electrode of the thermister is connected to the VDD and the counter in the LSI starts to work at the same time. When the voltage of the C1 increases up to a voltage reference, the counter stops. The value of the temperature is the count value.

IV. SYSTEM MODEL

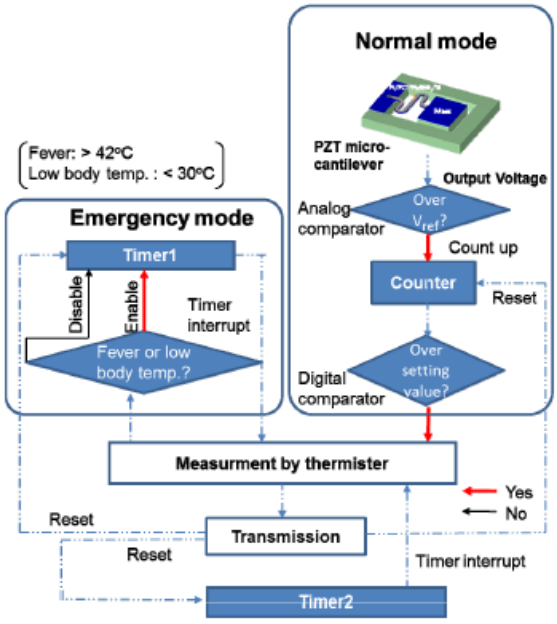

Figure 5:the work flow of the wireless sensor node

Fig. 5 shows a work flow of the developed custom LSI. There are two operation modes and the LSI changes the modes depending on the body temperature. In the normal state, the transmission event is occurred only when the activity, accumulated the number of acceleration which is over a threshold acceleration, exceeds a threshold number. If the chicken is infected and becomes weak, the transmission event may not be generated. In this case, we cannot know whether the wireless sensor node was broken or the chicken became weak for a long time. To avoid this situation, we designed that the transmission event can occur by a timer (Timer1) when the chicken's body temperature becomes abnormal state. In this system, the interval time is set to 10 minutes. In this system, the thermistor checks the body temperature per the transmissions and changes the mode if the body temperature is over 42 ^{0}C (fever) or below 30 ^{0}C (low body temperature caused by the death). In the previous research, a switch type MEMS temperature sensor which composed of two bimetal cantilever always monitors the body temperature and changes the mode if the body temperature becomes abnormal state [8,9]. The power consumption of this MEMS sensor is almost zero. However the current consumption of the input circuit is need and it is better to reduce the number of components on this wireless sensor node to decrease the cost. In this system, we use another timer (Timer2) to alternate the MEMS temperature sensor. In this case without the MEMS sensor, the event to measure the body temperature by the thermistor is never occurred unless the chicken's activity is over the threshold. This timer generates the event of thermistor measurement. In order not to increase the power consumption, the interval time of this timer is set to relatively longer time, such as 30 minutes. To realize this work with ultra low power, we must decrease the power

consumption of the components which always work. In this system, the clock source and activity sensor and the circuits for signal processing of the sensor input are mainly power consumed devices. In this system, we introduced a piezoelectric micro-cantilever as a zero power activity sensor and a comparator.
The piezoelectric micro cantilever can generate charges by chicken's movements, then the necessary power to activate this sensor itself is zero. In the previous research, piezoelectric micro- cantilever with ordinary shape was used [8,9]. The cantilever generated charges, however, the output voltage is small not enough to detect at tiny movement of a chicken. In this research, "S" shaped piezoelectric micro-cantilever [10] like fig. 6 is used. The output voltage of the "S" shaped micro-cantilever is about several mV at 0.05G and 6 Hz of input acceleration.

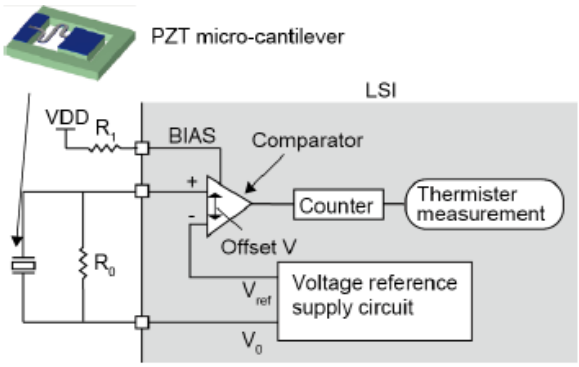

Figure 6: Schematic diagram of the work flow of the developed wireless sensor node.

The required data to detect an abnormal state of chickens at an early stage were already decided by the simulation using data obtained by influenza infection experiments [5]. The results indicated that the infection can be detected before more than about 40 hours of the death with detecting the fever. Although a chicken infected with HPAI viruses basically has a fever, there are HPAI viruses, such as A/chicken/Yamaguchi/7/2004(H5N1)/CkYM7 , which cause the death without a fever [11].
However, the activity of chickens infected with all viruses is decreased. We developed a detection method using the number of 1-axis acceleration which exceeds a threshold. In this case, the average detection time was about 6 hours with detecting the lower activity than before 24 hours [5]. Using this method, we can use 1 bit A/D converter. Fig. 6 shows the circuits to realize the above method at ultra low power. A comparator is used as 1 bit A/D converter. The output signal of the comparator is entered into a counter. If the count value exceeds a threshold value, the thermistor measurement event occurred based on the work flow. The calculated current consumption of the comparator including bias current is 20 nA. In this system, a voltage generator for the reference voltage of the comparator was integrated. The calculated current consumption of this voltage generator is 16 nA.

Table 1: Power consumption of the developed wireless sensor node.

	current (nA)
1kHz RC clock	134
BIAS for comparator	10
comparator	10
Voltage reference	30
Logic off leak	22
Total standby current	206
Total standby power	320 nW

Table 1 shows the calculated current consumption at standby state. The total power consumption is 320 nW using 1.55V button battery. Assuming that the transmission current, time and transmission interval are 10 mA, 2 ms and 5 minutes, the average current consumption is about 70 nA. Therefore the total average power consumption including thermister measurement is about 460 nW. If a small button battery with 30mAh is used, the estimated life time is more than 10 years.

V.RESULTS

Fig. 7 shows the developed wing band type wireless sensor nodes with "S" shaped piezoelectric micro cantilever and thermistor. This wireless sensor node consists of two parts connected by a flexible cable. One part is the main substrate including custom LSI, ceramic packaged piezoelectric micro cantilever, passive components and patterned loop antenna for 315MHz. The custom LSI was bonded to a printed circuit board directly and then covered by a resin. The other part is battery substrate with thermistor. A SR726W with battery capacity of 30 mAh and size of \7.9 mm and 2.6 mm height was used. The battery fixture has two holes at both sides to support the fixing pin. The main substrate also has two holes to pass the fixing pin. How to fix the wing band type wireless node to a chicken is to pass the fixing pin through chicken's arm and the holes in the main substrate, then the end of the fixing pin was bent like a stapler. The demonstration experiment was carried out in a chicken house. We attached 120 wireless sensor nodes to chickens and monitored the chicken's health for 1 week. Fig. 8 shows a result. It was found that the necessary data for the system could be measured during this period.

VI.CONCLUTION

We developed the ultra low power wireless sensor node with continuously monitoring of activity for chicken health monitoring system. The calculated power consumption of the wireless sensor node with piezoelectric micro-cantilever and thermistor is 320 nW. If SR726W with 30mAh of battery capacitance is used, the estimated life time is morethan 10 years.

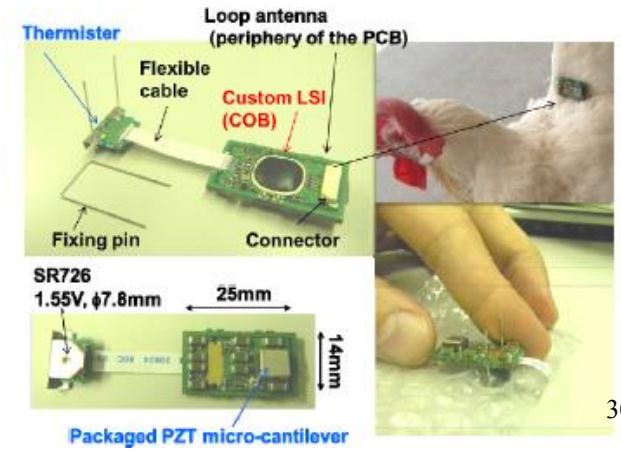

Figure 7: Photograph of the developed wing band type wireless sensor node.

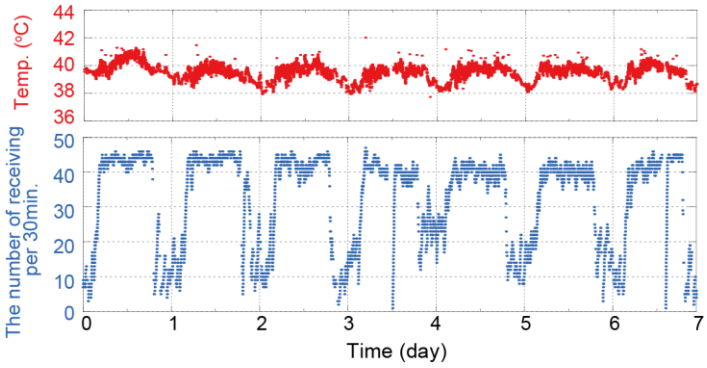

Figure 8: Results of the body temperature change and activity change

We also carried out the demonstration experiment with the developed wireless sensor node. 120 wireless sensor nodes were attached to chickens and monitored the body temperature and activity of the chickens. The results indicated that the obtained data is enough to detect the abnormal state of chickens at an early stage.

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COOPERATIVE SPECTRUM SENSING IN COGNITIVE RADIO: A REVIEW

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Abstract—

As the bandwidth is limited, the available spectrum is being congested day to day. Cognitive Radio It adjusts the parameters and protocols dynamically to supply unused areas within the total usable spectra. There are a numerous techniqes to identify the unused spectrum areas like Energy Detection, Matched Filter Detection, Cyclostationary Feature Detection. Spectrum sensing can be enriched by allowing different users to share their local sensing observations and to cooperatively decide on the licensed spectrum occupancy. Spectrum sensing is considerably increased by permitting com pletely different users to share their nativesensing observations and to hand and glove want the authorised spectrum occupancy. Further, it has some limitations such as high computational complexity and increased sensing time.

Index Terms—

Cognitive radio, Spectrum sensing, Cooperative spectrum sensing, Energy detection, Cyclostationary feature detection.

I.INTRODUCTION

Since spectrum is a finite resource, the effective use of available spectrum is an important prerequisite for designing of wireless system. The transceiver in cognitive radio system has the control to observe that communication channels are in use and that don't seem to be, and instantly get in unoccupied channels but avoiding occupied ones. For the further discussion, it is useful to distinguish between the two different definitions of cognitive radio:

1. All the transmission parameters, i.e., modulation format, coding, center frequency, transmission times, bandwidth, and so on are adopted by a fully cognitive radio. Even though a fully cognitive radio is stimulating from a scientific point of view, it currently seems too complicated for practical purposes.
2. Cognitive radio adapts the transmission frequency, bandwidth, and time according to the environment. This kind of cognitive radio is also called Dynamic Spectrum Access (DSA).

Here we have three kinds of models for DSA:

a) Dynamic exclusive model.

b) Hierarchical access model

c) Open sharing model

The main principle of hierarchical cognitive radio is that the secondary users do not disturb the primary users. This can be done by three important approaches: interweaving, overlay, and underlay. In the interweaving approach, the radio knows those parts of the spectrum that are not being used at a certain time, and transmits in those; thus, such a radio is a spectrum-sensing radio. In an overlay approach, the cognitive radio senses the transmitted signal of the primary user, and adjusts its signal in such a way

that it does not disturb the primary receiver yet it transmits in the similar band. In the underlay approach, the secondary user does not adapt to the existing environment, but always keeps its transmit Power Spectral Density (PSD) so low that its interference to primary users is insignificant [13]. The remaining of the paper is planned as follows. Section II contributes principles of cognitive radio while the cyclostationary feature detection presented in Section III. Section IV shows literature review and lastly section V concludes the paper.

II.PRINCIPLES OF COGNITIVE RADIO

There are three main functions involved in cognitive radio those are spectrum sensing, spectrum management and spectrum sharing.

Fig.1 Cognitive Cycle

Spectrum sensing: The cognitive radio has to identify which portion of the time–frequency plane are not used by primary users. The sensing has to be done in the presence of noise, so that the sensing cannot be completely reliable. Furthermore, it is important to determine the signal level of the detected radiation. [13]. Different types of Spectrum sensing techniques are shown in fig2.

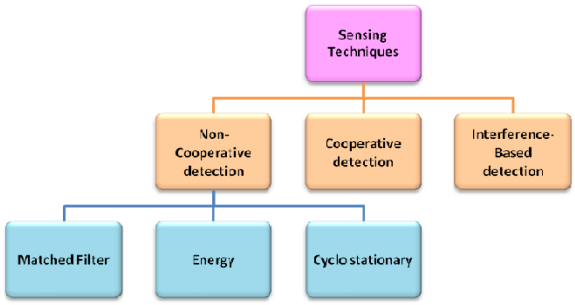

Figure 2: Types of Spectrum Sensing

Spectrum management: Here, the secondary system decides when, and in which part of the spectrum, to transmit. This decision is difficult for several reasons:
(1) The secondary system has only causal knowledge of the spectrum occupation, i.e., it knows only which parts of the spectrum were free in the past and the present, but it has to make assumptions (that are not necessarily correct) about how the primary system will work in the future, i.e., at the time when the secondary system will actually transmit.
(2) The sensing information on which the decisions of the secondary system is based are not perfect.

Spectrum sharing: A decision on how to divide up the free spectrum that the secondary system uses. It must be noted that spectrum sharing and spectrum management are strongly related – spectrum might be usable for a particular secondary transmitter (TX), but not for another. [13]
Spectrum mobility: Vacate the channel when a licensed user is detected is known as spectrum mobility

III. CYCLOSTATIONARY FEATURE DETECTION

In order to separate PU signal and CR signal, this technique evaluates signals periodicity. Based on the periodicity, this detection method can simply isolate the noise from the PU signal. PU signals are combined with sine wave carrier signals their autocorrelation and mean arrival periodicity which is

considered as being cyclostationary. We can separate noise signal from modulated PU signal with the help of spectral correlation function and thus sense if PU is present. [12] Basic flow diagram of CFD is shown below:

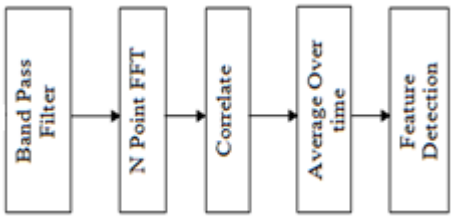

Fig2.Block Diagram of CFD

The Cyclic Autocorrelation Function (CAF) is calculated as:

$$R_x^{\alpha}(\tau) = \frac{1}{T}\int_{\frac{-1}{T}}^{\frac{1}{T}} R_X(t+\frac{\tau}{2}, t-\tau/2)e^{-j2\pi\alpha t}dt$$

Cyclic spectral density (CSD) is obtained as:

$$S_x^{\alpha}(f) = \int_{-\alpha}^{\alpha} R_x^{\alpha}(\tau)e^{-j2\pi f\tau}d\tau$$

The signals which the primary users transmits are generally coupled along with cyclic prefix, spreading codes etc. which result in the periodicity of their statistics like mean and auto correlation. When the CSD for such signals is calculated, it helps in emphasizing such periodicities. Correlated signal's fourier transform provides peak at frequencies which are specific to a signal and looking for these peaks helps in determining the presence of the primary user, whereas noise is random in nature and it does not exhibit such periodicities hence it doesn't get highlighted when its correlation is done. [14]

IV.LITERATURE REVIEW

A. *Cyclostationary-Based Cooperative Compressed Wideband Spectrum Sensing in Cognitive Radio Networks (IEEE 2017)*

A cooperative cyclostationary compressed spectrum sensing algorithm is proposed to enable accurate, reliable and fast sensing of wideband spectrum. In the proposed algorithm each secondary-user (SU) sends the compressed data vector to the fusion center (FC) which has a copy of the sensing matrices for all cooperated SUs. Then, at the FC, the fast Fourier transform accumulation method (FAM) based on cooperative multitask compressive sensing (MCS) algorithm is employed to recover the spectral correlation function (SCF) from the compressed measurements. The proposed algorithm has two main components. The first component exploits the cooperation between SUs to produce an estimate of the investigated signal spectrum using multi-task compressive sensing. In the second component, the cyclic feature detection is performed based on the recovered SCF function. Simulation results obtained provides us the wellness and the effectiveness of the proposed method against both noise uncertainty and sampling rate reduction. [1]

B. Cyclostationary Feature based Detection using Window Method in SIMO Cognitive Radio System (IEEE 2016)

With some recent developments in the field of wireless communication at rapid pace, users are getting a number of applications which require the precious bandwidth to work on. As the bandwidth is limited, the available spectrum is being congested day by day. Cognitive Radio System (CRS) plays an important role in such scenario. It dynamically adapts its parameters and protocols to provide unused spaces in the total usable spectra. There are a number of ways to detect the unused spectrum/holes/white spaces like Energy Detection, Matched Filter Detection, Cyclostationary Feature Detection (CFD), Wavelet Transform, Filter Bank, Eigenvalue based Detection, Covariance based Method, Multiple antenna method and Multitaper Method. In this paper, a spectrum sensing technique is proposed which is based on the cyclostationary spectrum sensing in multiple antenna cognitive radio by Maximal Ratio Combining (MRC) method.

Spectral Correlation Density (SCD) is computed by FFT Accumulation Method (FAM) to perform Cyclic Analysis. Simulation results show that CFD for lower SNRs as the proposed scheme can detect the primary user with a probability of 90 percent approximately at 20dB. [2]

C. Group-based Multi-bit Cooperative Spectrum Sensing for Cognitive Radio Networks (IEEE 2016)

In cooperative spectrum sensing, a multi-bit combination rule shows better sensing performance than one-bit hard combination rules at the sacrifice of the reporting overhead. In order to overcome the trade-off between the sensing performance and the reporting overhead, they proposed a group-based multi-bit cooperative spectrum sensing scheme with a limited reporting overhead. The proposed scheme uses contention based reporting for restraining the reporting overhead along with achieving multiuser diversity with an increased number of secondary users (SUs). Also, Secondary Users report one-bit sensing results to a fusion center instead of sending multi-bit quantization information and the rest of the information is embedded in the time slot. The simulation results declares that, as the number of SUs increases, the proposed scheme improves the sensing performance as well as the average throughput of SUs whereas the conventional one-bit or multi-bit combination schemes show a trade-off between the sensing performance and the throughput of SUs. [3]

D. Cyclostationary Detection Based Spectrum Sensing for Cognitive Radio Networks. (2015)

Cyclostationary detection Based spectrum sensing is used for cognitive radio networks. The already awailable first-order and second-order cyclostationary detection algorithms is precised, which can be thereafter used as a brief tutorial on detection theory of the cyclostationary signals. After this, a cooperative spectrum sensing method for a cognitive radio networks with multiple terminals and one fusion center is proposed. It is shown that the proposed method have reliable performance even in low signal-to-noise ratio (SNR) region. Also, the increasein number of secondary users (SUs) leads to improved detection performance, especially at low SNR. [4]

E. Simple Diversity Combining Techniques for Cyclostationarity Detection Based Spectrum Sensing in Cognitive Radio Networks(IEEE 2014)

Simple diversity combining techniques for cyclostationarity detection based spectrum sensing in cognitive radio networks is discussed. The provided techniques depends on maximum cyclic autocorrelation function (MCAS) techniques. The MCAS judges whether received signals include an orthogonal frequency division multiplexing (OFDM) signals or not, by comparing the peak and non-peak values of a cyclic autocorrelation function (CAF). The presented diversity techniques attempt to increase signal-to-noise ratio (SNR) of CAF which is composed of the peak and non-peak values of CAF. In the presented techniques, the CAF SNRs which obtained at some received antennas are combined whereas general diversity combining techniques combines some received signals. The presented results are compared with some conventional results, and computational and theoretical analysis results show that the presented techniques can improve the spectrum sensing performance. [5]

F. A Weighted Diversity Combining Technique for Cyclostationarity Detection Based Spectrum Sensing in Cognitive Radio Networks. (IEEE 2015)

A weighted diversity combining technique for the cyclostationarity detection based spectrum sensing of orthogonal frequency division multiplexing signals in cognitive radio is presented. In cognitive radio systems, secondary users must detect a desired signal in an extremely low SNR environment. In these environments, multiple antenna techniques like maximum ratio combining are not effective as energy of target signal is also not strong and it is difficult to obtain the signal synchronization of some of the received signals. For traditional cyclostationarity detection based spectrum sensing, they have used a cyclic autocorrelation function (CAF). In this paper, a CAF Signal to Noise Ratio is defined using the signal and noise components of the

CAF, and we attempt to improve sensing performance to use a different weight for each component of the CAF. The presented results are compared with some conventional results and show that the presented technique can improve the spectrum sensing performance. [6]

G. Performance Analysis of Cyclostationary and Energy Detection Spectrum Sensing Techniques. (IEEE 2015)

The latest policies of spectrum allocation results in inefficient use of spectrum. In today's scenario dynamic spectrum access is the need and cognitive radio is a novel technology which improves spectrum utilization. In this paper cognitive radio along with spectrum sensing techniques is taken into account. Energy detection based spectrum sensing techniques and cyclostationary detection based spectrum sensing techniques are discussed in detail along with their block diagrams and flow charts. The paper also illustrates the performance analysis of energy detector over various fading environments viz. AWGN, Rayleigh, Rican and MIMO. Implementation of energy and cyclostionary detectors is performed using Matlab and their results are shown using graphical analysis with the help of ROC (receiver operating characteristics) curves. [7]

H. Experimental Analyses of Spectrum Sensing Using Cyclic Autocorrelation Function Diversity Combining Techniques in Cognitive Radio. (IEEE 2014)

Experimental analyses of spectrum sensing of an orthogonal frequency division multiplexing signal using cyclic autocorrelation function (CAF) diversity combining techniques in cognitive radio is discussed. Traditionally, the CAF diversity combining based spectrum sensing technique has been presented. The techniques is based on an equal gain combining and has a low computational cost in comparison with other cyclostationarity detection based spectrum sensing using space diversity. The paper provides the experimental results to validate the effectiveness of the CAF diversity combining technique. For experimental analyses, a testbed for the evaluation of multiple receive antennas based spectrum sensing is developed. The developed testbed is mainly composed of a Universal Software Radio Peripheral (USRP) / GNU Radio which is one of the software defined radio receiver, and the spectrum sensing technique is experimentally demonstrated at an anechoic chamber using 470710MHz frequency band allocated to ISDB-T (terrestrial digital broadcasting) in Japan. From these results, the effectiveness of the CAF diversity combining techniques is validated. [8]

I. ***Performance of Cooperative Spectrum Sensing with Soft Data Fusion Schemes in Fading Channels. (IEEE 2013)***

Cognitive radio (CR) systems should have the ability to detect the presence of licensed primary user (PU) reliably. Cooperation among multiple CRs helps to enhance the reliability of detection of the PU in case of unreliable decision by a single CR due to channel uncertainties. In this paper, cooperative spectrum sensing (CSS) based on energy detection in cognitive radio networks (CRN) which uses soft combination of the observed energy values from different CRs is considered. More precisely, we study the performance of CSS with several soft data fusion schemes namely, (a) Square law selection (SLS) (b) Square law combining (SLC) (c) Maximal ratio combining (MRC) that can be applied at fusion center (FC). The performance of CSS has been assessed under several cases of sensing (S) channels such as AWGN, log-normal shadowing, Rayleigh and Rician fading channels. Comparative performance of CSS for various soft data fusion schemes under different fading channels has been studied for various values of average S-channel SNRs, time bandwidth products, different number of CRs. The effect of shadowing and fading parameters on missed detection performance of CSS is shown. Further, the performance comparison between soft data fusion schemes and hard decision fusion schemes is also highlighted. [9]

V. CONCLUSION

To utilize the wireless communication efficiently spectrum sensing cognitive radios remained introduced which utilize the holes present in the spectrum. The encouraging feature of a cognitive radio system is spectrum sensing and various sensing techniques which it uses to sense the spectrum. Spectrum is an enormously important resource in wireless communication systems, and it has been a central point for research over the last decades. CR is one of the finest solution to utilize the available spectrum more efficiently through opportunistic spectrum usage. CSS is an efficient technique to improve detection performance by discovering spatial diversity at the outflow of cooperation overhead. CFD is improved than both the preceding detection techniques since it produces better results at lowest SNR, i.e. for values below -30 dB. The performance of energy detection gets better with increasing SNR because of the increase in "probability of primary detection" from zero at -14 dB to 100% at +8 dB and harmoniously the "probability of false detection" recovers from 100% to zero.

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