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Digital Color Image Reconstruction using Interpolation Methods-Implementation and Evaluation

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***Abstract*—The invention of Charge Coupled Devices made digital color imaging cost effective and easy. It captures fifty percent of Green, twenty-five percent of Blue and twenty-five percent of Red color intensity of the original scene. Later those discarded and missing color samples are being estimated for restoring the full color image. Different companies employ different Interpolation Methods in reconstructing the full color image by estimating the missing color samples. In this research paper Non-adaptive and Adaptive Interpolation Methods are mathematically analyzed and implemented using MATLAB. The resultant images are presented for subjective evaluation. Minimum Mean Square Errors and Signal to Noise Ratios are obtained, and are presented for Objective Performance Evaluation of the algorithms. All the artificial and embedded vision devices, robotic vision devices and machine vision devices employ these color image reconstruction methods for digital color image restoration.**

Keyword- CCD, Color Image Reconstruction, Interpolation Methods, MMSE, SNR.

I. INTRODUCTION

The 2009 Noble Prize winning invention of charge coupled device (CCD) in 1969 by W.S. Boyle and G.E. Smith revolutionized the way images are captured, stored, processed and transmitted [1]. During an image capture process, a digital camera performs various processing mechanisms of the imaging pipeline, an important component of it is colour filter array (CFA) interpolation i.e., to recover a full-resolution image from its CFA data.

To produce a colour image, there should be at least three colour samples at each pixel location. A more cost-effective and relatively less complex solution is to put a CFA in front of the sensor to capture one colour component at a pixel and then interpolate the missing two colour components. Among many CFA patterns, the most commonly used is the Bayer pattern [2]. The Bayer CFA array is shown in Fig.1.

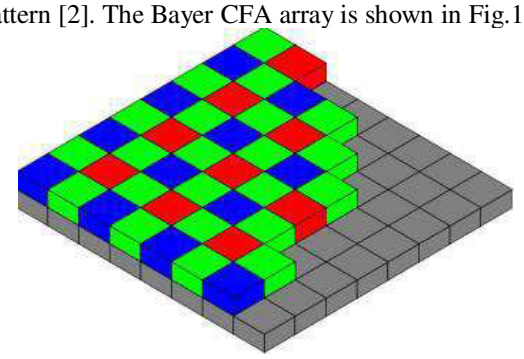

Fig. 1. Bayer Pattern of Color Filter Array

Here the Green filters are in quincunx (interlaced) grid with Red, Blue filters fill up the empty locations. As shown in Fig. 2, the rest of the sensor array is determined by the repeating this pattern both horizontally and vertically, R. Kimmel [3]. Here 50% of Green 25% of Red and 25% of Blue pixels of the original image will be available after sub sampling the datasets. The green channel is measured at a higher sampling rate than the other two because the peak sensitivity of the human visual system (HVS) lies in the medium wavelengths, corresponding to the green portion of the spectrum, D. Alleysson, S. Susstrunk and J. Herault [4]. Although we limit our discussion to the interpolation problem with reference to the Bayer pattern here, the interpolation methods developed for Bayer pattern can in general be extended to other patterns. Because of the mosaic pattern of the CFA, this interpolation process has been widely known as “demosaicing”. Systematic analysis and comparison of different CFA patterns are referred to recent works.

II. LITERATURE REVIEW

The presence of CFA between lens and sensor produces ‘mosaic’ of color samples. The mosaic of colors needs to be undone to recover three color planes in order to obtain a full color representation of the scene information. This process interpolating the missing color sample is referred to as demosaicking, Ngai Li, Jim S. Jimmy Li, and Sharmil Randhawa [5]. There are a variety of methods available for this interpolation process [6]- [7].

Interpolation Methods for Digital Color Image Reconstruction are classified as Non -adaptive algorithms and Adaptive algorithms. 1.Nearest Neighbor Replication (NNR) also called as Closest Neighborhood Interpolation Algorithm (CNA), 2. Bilinear Interpolation (BILIN), 3. Median Interpolation(MIA), and 4. Smooth Hue Transition Interpolation(SHTIA) belong to first category and 5. Edge Sensing Interpolation-1 (ES-1) fall under Adaptive algorithms category. These are the interpolation methods studied, analyzed and implemented, and then their performance is evaluated at subjective and objective levels in this research article.

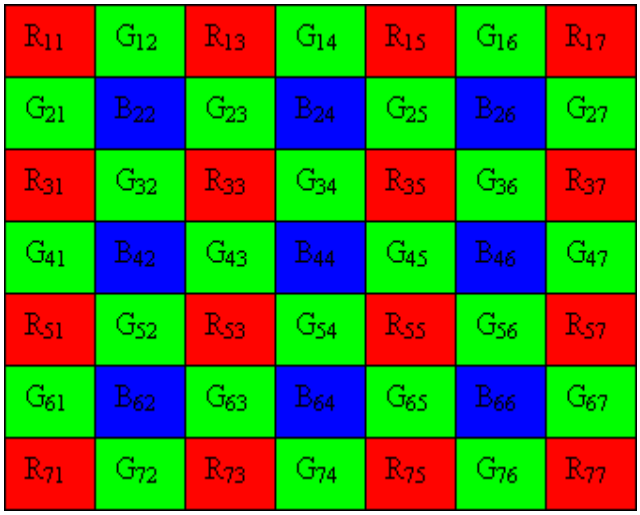

Fig. 2. Bayer CFA Pattern for Interpolation Procedure

A. *Non -adaptive Interpolation Methods for Digital Color Image Reconstruction*

1) Nearest Neighbor Replication (NNR) Method: It's also called as Closest Neighborhood Interpolation Algorithm (CNA). It is the simplest Demosaicking algorithm. It assigns a color value with the nearest known red, green or blue pixel value in the same color plane. There is usually some ordering as to which (left, right, top, or below) nearest neighbor to use for the particular implementation, Ozawa.N [8]. However, it does not do a good job of interpolation, and it creates zigzag zipper color artifacts that distort the image.

2) Bilinear Interpolation (BILIN) Method: This is another Simplest and little faster method of interpolation algorithms. The bilinear interpolation allocates the missing color component with the linear average of the adjacent pixels with same color component, Hamilton and Adams [9]. For example, the pixel location (2,2) in Fig. 2 contains *blue* component only. Hence the missing *green* component can be estimated as average of the left, right, top and bottom *green* pixel values. The missing *red* component can be estimated as average of the four diagonally adjacent corner neighbors containing *red* pixels. Arabic Numbers are used to represent rows and columns of green, red and blue colors.Bilinear Interpolation Process is given in steps below from (1.1) to (1.3).

a) Interpolation of Green Pixel G_{22} in position Blue Pixel B_{22} is given by

$$G_{22} = \frac{G_{12} + G_{32} + G_{21} + G_{23}}{4} \tag{1.1}$$

b) Interpolation of Blue Pixel B_{22} in position Blue Pixel B_{22} is given by

$$B_{22} = B_{22} \tag{1.2}$$

c) Interpolation of Red pixel R_{22} in the position of Blue Pixel B_{22} is given by

$$R_{22} = \frac{R_{11} + R_{33} + R_{31} + R_{13}}{4} \tag{1.3}$$

Similar Procedure can be followed for interpolating other missing pixels.

3) Median Interpolation(MIA) Method: If median interpolation is used at B_{22} for interpolating missing color samples G_{22} and R_{22}, it allocates the missing color component with the "median" value of the adjacent pixels of same color component, as opposed to the linear average used in bilinear interpolation. This provides a slightly better result in terms of visual quality as compared with the bilinear interpolation. However, the resultant images are still blurry for images with high frequency contents, and for high resolution still imaging system, this is still not acceptable. Median Interpolation Process is given in steps below from (1.4) to (1.6). T. W. Freeman [10].

a) The Chrominance B_{22} at B_{22} is available

$$B_{22} = B_{22} \tag{1.4}$$

b) To find the Chrominance R_{22} of the Bayer pattern at B_{22}, we have to calculate the median of the neighbour pixels R_{22}

$$R_{22} = Median\left(R_{11}, R_{13}, R_{31}, R_{33}\right) \tag{1.5}.$$

c) To find the missing Luminance pixel lines G_{22} at B_{22}, the median of the neighboring pixels of G_{22} is to be calculated

$$G_{22} = Median\left(G_{21}, G_{23}, G_{12}, G_{32}\right) \tag{1.6}$$

4) Smooth Hue Transition Interpolation (SHTIA) Method: The key problem of the color artifacts in both bilinear and median interpolation is that the hue values of adjacent pixels change suddenly (non-smoothly). On the other hand, the Bayer CFA pattern can be considered as combination of a luminance channel (green pixels) and two chrominance channels (red and blue pixels). The smooth hue transition interpolation method interpolates these channels differently, David.R.Cok [11]. The missing *green* component in every *red* and *blue* pixel locations in the Bayer pattern can first be interpolated using bilinear interpolation as discussed before. The idea of chrominance channel interpolation is to impose a smooth transition in hue value from pixel to pixel. In order to do so, it defines blue "hue value" as B/G, and red "hue value" as R/G. For interpolation of the missing blue pixel values m n B, in pixel location (m, n) in the Bayer pattern, the following three different cases may arise, as given in steps below from (1.7) to (1.9).

a) As shown in pixel location in (2,3) Fig.2, If the pixel location (m, n) contains Green color component only and the adjacent left and right pixel locations contain Blue color component only,then the Blue information in location (m, n) can be estimated as follows:

$$B(m,n)=G(m,n)\times\frac{1}{2}\times\begin{Bmatrix}\left(B(m,n-1)/G(m,n-1)\right)\\+\left(B(m,n+1)/G(m,n+1)\right)\end{Bmatrix} \quad (1.7)$$

b) As shown in pixel location (3,2) in Fig.2, If the pixel location (m,n) contains Green color component only and the adjacent top and bottom pixel locatins contain Blue color component only, then the Blue information in the location (m,n) can be estimated as follows:

$$B(m,n)=G(m,n)\times\frac{1}{2}\times\begin{Bmatrix}\left(B(m-1,n)/G(m-1,n)\right)\\+\left(B(m+1,n)/G(m+1,n)\right)\end{Bmatrix} \quad (1.8)$$

c) As shown in pixel location (3,3) in Fig.2.; If the pixel location (m, n) contains Red color component only. Obviously, four diagonally neighboring corner pixels contain Blue color only, Then BLUE information in location (m, n) can be estimated as follows:

$$B(m,n)=G(m,n)\times\frac{1}{4}\times\begin{Bmatrix}\left(B(m-1,n-1)/G(m-1,n-1)\right)\\+\left(B(m-1,n+1)/G(m-1,n+1)\right)\\+\left(B(m+1,n-1)/G(m+1,n-1)\right)\\+\left(B(m+1,n+1)/G(m+1,n+1)\right)\end{Bmatrix} \quad (1.9)$$

The interpolation of missing *Red* pixel values can be carried out similarly. Depending on the location, interpolation step happens, and the definition of "hue value" changes. For example, if the pixel value is transformed into logarithmic exposure space from linear space before interpolation, instead of *B/G* or *R/G*, one can now define the "hue value" as *(B-G)* or *(R-G).* This is coming from the fact that *log(X/Y) = log(X) – log(Y) = X' – Y'*. Here *X'* and *Y'* are the logarithmic values of *X* and *Y* respectively. Since the linear/nonlinear transformation can be done using a simple table look-up and all the division for calculating hue value is replaced by subtraction, this helps reduce computational complexity for implementation.

B. Adaptive Interpolation Methods for Digital Color Image Reconstruction

These algorithms are relatively complex and do perform better compared with Non-Adaptive Interpolation Algorithms. In this research paper two Adaptive algorithms viz., Edge Sensing Interpolation Algorithms 1 and 2 are studied, implemented and their performance is evaluated at subjective and objective levels.

1) Edge Sensing Interpolation-1 (ES-1) Method: The edge sensing adaptive demosaicking algorithm uses a set of threshold values to determine whether to average adjacent pixels on the right and left side or adjacent pixels on the top and bottom side of the pixel being interpolated. As the name alludes to, this algorithm is especially important in Demosaicking edges within a picture. Essentially the algorithm determines where a particular direction of adjacent pixels (top-bottom or left-right) is exclusively greater than a given threshold value, as shown in equations below from (1.10) to (1.13). If this is the case, then most likely a line or edge exists and therefore when averaging adjacent pixels for Demosaicking, it is best not to smooth in the direction where the gradient values are higher than a given threshold value. Where this method fails is along diagonal lines, since the gradients are only taken along the horizontal and vertical directions.Edge Sensing Interpolation-1 process is given in steps below. Hibbard, R.H., [12].

a) Finding the gradient in horizontal direction of green pixel G_{33}.

$$G(H)=Mod\left(G_{32}-G_{34}\right) \quad (1.10)$$

b) Finding the gradient in the vertical direction of green pixel G_{33}

$$G(V)=Mod\left(G_{23}-G_{24}\right) \quad (1.11)$$

c) Finding the threshold of the vertical and horizontal gradient.

$$T=\frac{G(H)+G(V)}{2} \quad (1.12)$$

d) Finding G_{33} at R_{33}

$$\begin{aligned}&If\\&G(V)\prec T\\&Then\\&G_{33}=\frac{G_{23}+G_{43}}{2}\\&Elseif\\&G(H)\prec T\\&Then\\&G_{33}=\frac{G_{32}+G_{34}}{2}\\&Elseif\\&G_{33}=\frac{G_{23}+G_{34}+G_{32}+G_{34}}{4}\end{aligned} \quad (1.13)$$

III. PERFORMANCE EVALUATION

The evaluation of performance of Interpolation methods is done at two levels i.e., Subjective and Objective levels. Wenmain Lu and Yap-peng Tan [14].

A. Subjective Performance Evaluation

Fig. 3 shows from top to bottom the original image, 2D and 3D Bayer arrays of the test image 1 i.e., image of Macaws, a standard test image taken from the Kodak test image data base. Fig. 4 shows from top to bottom the original image, 2D and 3D Bayer patterns of test image 2 i.e., image of St. Mary's Engineering College, Hyderabad. Fig. 5 to Fig. 9 show the resultant images of test image1 obtained using Interpolation methods 1 to 5. Fig. 10 to Fig. 14 show the resultant images of test image 2 implemented for Interpolation methods 1 to 5. MATLAB is used for implementation. Fig. 3 to Fig. 14 are presented here for the

evaluation of the interpolation methods at subjective level. The viewer can observe and interpret the results for the performance of the algorithms but this method is not a perfect one. Hence Objective Performance evaluation is necessary.

Fig. 3. Original image, 2D and 3D Bayer Array of Test Image 1

Fig. 4. Original image, 2D and 3D Bayer Array of Test Image 2

Fig. 5. Resultant Image of test image 1 for interpolation method 1

Fig. 6. Resultant Image of test image 1 for interpolation method 2

Fig. 7. Resultant Image of test image 1 for interpolation method 3

Fig. 8. Resultant Image of test image 1 for interpolation method 4

Fig. 9. Resultant Image of test image 1 for interpolation method 5

Fig. 10. Resultant Image of test image 2 for interpolation method 1

Fig. 11. Resultant Image of test image 2 for interpolation method 2

Fig. 12. Resultant Image of test image 2 for interpolation method 3

Fig. 13. Resultant Image of test image 2 for interpolation method 4

Fig. 14. Resultant Image of test image 2 for interpolation method 5

B. *Objective Performance Evaluation*

The Objective Performance metrics used here to evaluate the performance of the interpolation methods are Minimum Mean Square Error (MMSE) and Signal to Noise Ratio (SNR) obtained through the implementation of the algorithms for test images 1and 2 using MATLAB.

- Minimum Mean Square Error (MMSE)

  MMSE corresponds to the expected value of the squared error loss or quadratic loss. It measures the average of the squared error. Minimum is its value, better is the performance of the interpolation method.

$$MMSE = \frac{\sum_{x=1}^{m}\sum_{y=1}^{n}\left[I_o(x,y) - I_r(x,y)\right]^2}{(m \times n)} \quad (1.14)$$

  Where (m×n): size of the image, $I_o(x, y)$: Original Image, $I_r(x, y)$: Reconstructed Image.

- Signal to Noise Ratio(SNR)

  SNR is a measure used to quantify how much a signal has been corrupted by the unwanted signal. It is defined as the ratio of signal power to the noise power corrupting the signal.

$$SNR = [-10\log]\frac{\frac{1}{KL}\sum_{k=1}^{k-1}\sum_{l=1}^{l-1}\left(I_o(k,l) - I_r(k,l)\right)^2}{255^2}[dB] \quad (1.15)$$

  Where the product KL: Spatial Resolution of the image; the numerator represents the squared average pixel value of the image; and the denominator represents the squared color resolution.

  The objective performance metrics MMSE and SNR values obtained using Interpolation Methods 1 to 5 (CNA/NNA, MIA, BILIN, SHITA and ES-1) for test image 1 and 2 respectively are Tabulated in TABLE I to TABLE IV.

TABLE I. OBJECTIVE PERFORMANCE METRICS-MMSE OF TEST IMAGE 1

S.No.	Interpolation Method	Minimum Mean Square Error		
		Red	Green	Blue
1	CNA/NNA	6.9342	4.3953	7.1951
2	MIA	3.6307	2.3016	3.7778
3	BILIN	**3.4694**	2.3193	3.5620
4	SHITA	3.8672	2.3463	2.5114
5	ES-1	3.7620	1.9892	2.2534

TABLE II. OBJECTIVE PERFORMANCE METRICS- SNR OF TEST IMAGE 1

S.NO.	INTERPOLATION METHOD	SIGNAL TO NOISE RATIO		
		RED	GREEN	BLUE
1	CNA/NNA	43.6874	45.6535	43.5272
2	MIA	46.1088	49.2817	45.9656
3	BILIN	46.4683	49.2485	46.3652
4	SHITA	45.9152	49.1982	47.5434
5	ES-1	45.9725	49.9153	47.8817

TABLE III. OBJECTIVE PERFORMANCE METRICS- MMSE OF TEST IMAGE 2

S.No.	Interpolation Method	Minimum Mean Square Error		
		RED	GREEN	BLUE
1	CNA/NNA	34.1288	26.7500	35.8306
2	MIA	31.8643	21.0043	33.0435
3	BILIN	32.9541	24.4220	33.5819
4	SHITA	33.0005	24.5569	34.7842
5	ES-1	30.6912	19.7867	32.8111

TABLE IV. OBJECTIVE PERFORMANCE METRICS- SNR OF TEST IMAGE 2

S.No.	Interpolation Method	Signal to Noise Ratio		
		Red	Green	Blue
1	CNA/NNA	36.0550	37.7186	41.2688
2	MIA	36.5409	38.7566	36.4215
3	BILIN	36.4251	38.1801	36.3667
4	SHITA	36.2688	38.1603	36.0885
5	ES-1	36.7096	39.0134	36.2601

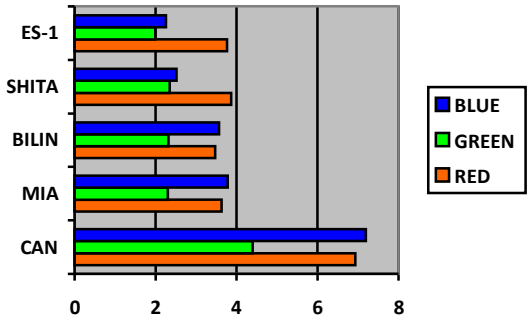

Fig. 15. Bar chart of MMSE values of test image 1 for interpolation methods 1 to 5

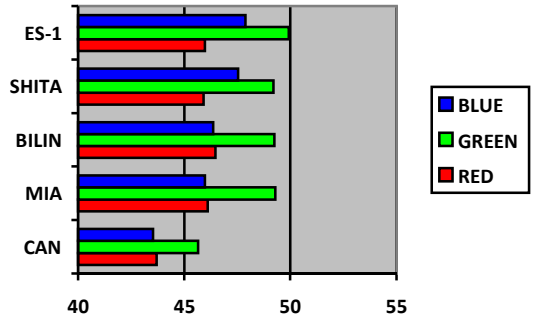

Fig. 16. Bar chart of SNR values of test image 1 for interpolation methods 1 to 5

IV. INTERPRETATION OF THE RESULTS

The resultant images presented in Fig. 3 to 14 will help the viewer in evaluating subjectively the performance of the interpolation methods. But all images look alike to a naked eye. Hence the Objective performance metrics MMSE and SNR will help anyone to evaluate objectively which interpolation method is better. Minimum is the value of MMSE; and greater is the value of SNR, better is the performance of the algorithm. From the graphic charts of MMSE and SNR shown in Fig. 15 and Fig.16; and from observing Table I to Table IV, it is clear that Edge Sensing-1 Interpolation method do better compared with other algorithms. But its MMSE is least and SNR is greater relatively. Graph chart of resultant MMSE and SNR values of interpolation methods 1 to 5 for test image 1. For want of space, bar charts of MMSE and SNR values of Test Image 2 are not shown here but Tables.

V. CONCLUSION

In this paper, four non adaptive and one adaptive, altogether five color image reconstruction algorithms are implemented using MATLAB, after due theoretical study and mathematical analysis. The comparative performance analysis-subjective and objective quality (MSE& SNR) of reconstructed images is done. For the digital design of machine, robotic or artificial vision devices, if we were to choose one only from the algorithms we have considered here, and then edge sensing algorithm-1 can be preferred.

VI. FUTURE ENHANCEMENTS

The interpolation methods can be evaluated based on their computational complexities. And other objective performance evaluation metrics can also be explored and implemented.

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DESIGN OF DYNAMIC ACCURACY CONFIGURABLE MULTIPLIER USING DUAL QUALITY 4:2 COMPRESSOR

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Abstract

In this paper, four 4:2 compressors with high flexibility of switching between the exact and approximate operating modes is designed. Dual-quality compressors provide higher speeds and lower power consumptions at the cost of lower accuracy in approximate mode. The efficiencies of this compressor can be evaluated using 32-bit Dadda multiplier. Here, a Dadda multiplier is also designed and their results are analysed. Dadda multiplier can be used to evaluate the performance of compressor.

***Index Terms*—4:2 compressor, Dadda multiplier, accuracy, approximate, computing, configurable, delay, power.**

I. INTRODUCTION

Among different arithmetic blocks, the multiplier is one of the main Blocks, which are widely used in different applications especially signal Processing applications[1,2]. There are two general architectures for the multipliers, which are sequential and parallel. While sequential architectures are low power, their latency is very large. On the other hand, parallel architectures (such as Wallace tree and Dadda) are fast while having high-power consumptions. The Parallel multipliers are used in high-performance applications where their large power consumptions may create hot-spot locations on the die. The speed of a processor greatly depends on its multiplier's performance. This in turn increases the demand for high speed multipliers, at the same time keeping in mind low area and moderate power consumption. Over the past few decades, several new architectures of multipliers have been designed and explored. Multipliers based on the Booth's and modified Booth's algorithm is quite popular in modern VLSI design but come along with their own set of disadvantages. [3]In these algorithms, the multiplication process, involves several intermediate operations before arriving at the final answer. In order to address the disadvantages with respect to speed of the above mentioned methods, and explored a new approach to multiplier design based on ancient Vedic Mathematics.

The number of half and full adders count to the total delay in Conventional multiplier [4]. The use of compressor structures which perform more than three bit addition. 4-2 compressor has five inputs and three outputs, as shown in Fig. 1.1 The four inputs X0, X1, X2, and X3, and the output have the same weight. C_{in} is the output carry of preceding module and C_{out}, the carry output of current stage is fed to the next compressor. The output Carry is weighted one binary bit order higher. The compressor is governed by the following basic equation:

$$X_0+X_1+X_2+X_3+C_{in}=Sum+2(Carry+C_{out})$$

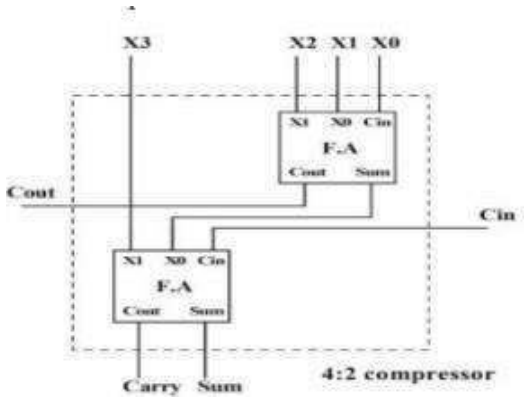

Fig 1.1 Block diagram of a 4:2 compressor

Besides, to accelerate the carry save summation of the partial products, it is imperative that the output C_{out} be independent of the input C_{in}. The conventional architecture of a 4:2 compressor consists of two serially

connected full adders. This circuit leads to a long critical path delay[5,6]. Also of un even delay profiles of outputs from different inputs.

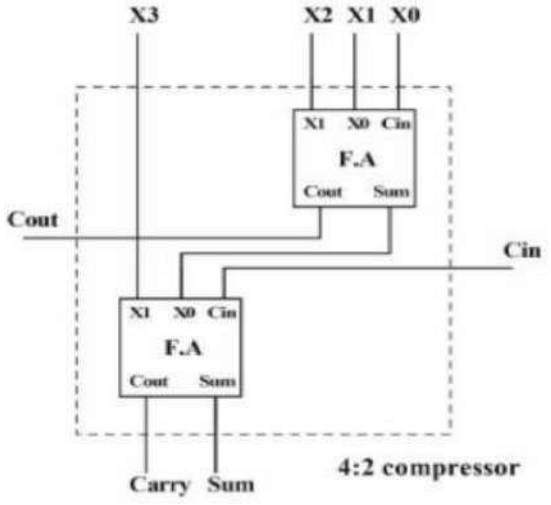

Fig1. 2. Conventional 4-2 compressor scheme

The overall structure of the proposed structure is shown in Figure 1.3.

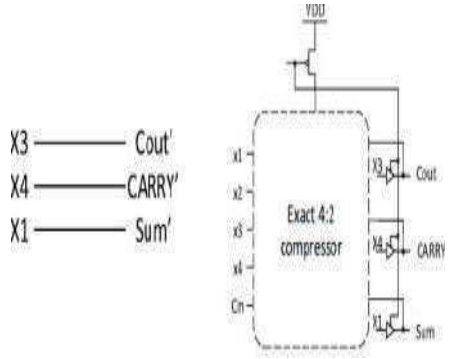

Fig1. 3 Approximate part and overall structure of DQ4:2C2

The previous structures, in the approximate operating mode, had maximum power and delay reductions compared with those of the exact compressor. In some applications, however, a higher accuracy may be needed. In the third structure, the accuracy of the approximate operating mode is improved by increasing the complexity of the approximate part whose internal structure is shown

II. EXISITNG METHOD

The 4:2 compressors has five input signals, including four main inputs and an input carry bit (C_{in}), coming from the previous stage, and three output signals including Sum and Carry main outputs and an output carry signal (C_{out}) which serves as the C_{in} of the next neighboring block. It is worth mentioning that the C_{out} signal is independent of the C_{in} input due to the elimination of carry propagation through the multiplier tree[14,15,16]. A 4:2 compressor cell generates Sum, Carry and C_{out} outputs from×1, ×2,×3, ×4 and C_{in} inputs.

Sum = x + x + x + x + C …….(i)

Carry = Majority [(x + x + x), x, C] ……(ii)

C = Majority (x, x, x) ……(iii)

The gate-level and the transistor-level designs are two different approaches for designing blocks such as 4:2 compressors. The major drawback of this approach is its limited optimization capability.

III. PURPOSED METHOD

To reduce the delay of the partial product summation stage of parallel Multipliers, 4:2 and 5:2 compressors are widely employed. The focus of this paper is on approximate 4:2 compressors. First, some background on the exact 4:2 compressor is presented. This type of compressor, shown schematically in Fig. 3.1, has four inputs (x_1–x_4) along with an input carry (C_{in}), and two outputs (sum and carry) along with an output C_{out}. The internal structure of an exact 4:2 compressor is composed of two serially connected full adders, as shown in Fig. 2. In this structure, the weights of all the inputs and the sum output are the same whereas the weights of the carry and C_{out} outputs are one binary bit position higher.

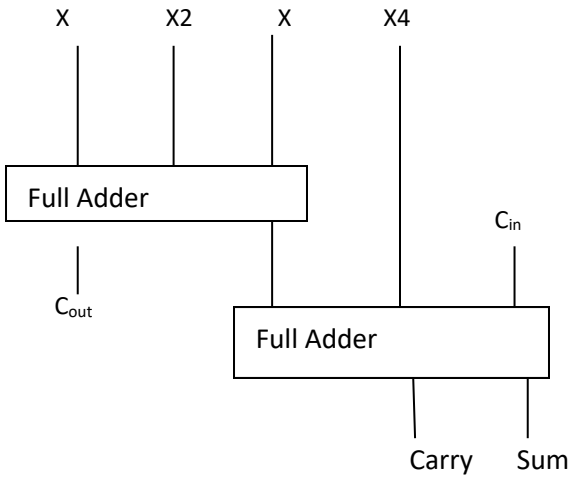

Fig3.1. Conventional 4:2 compressor.

The proposed system of 4:2 compressor consist of Half-adder, full –adder and 4 2 compressors, EXOR gates

tend to contribute high amount of area and power. For the process of approximating half-adder, EXOR gate of the Sum is changed with OR gate. This results in one error in the Sum output. Sum = x1+x2; Carry = x1.x2. In the process of approximation of full-adder in the multiplier, one of the EXOR gates is replaced with OR gate to reduce hardware complexity. Carry is altered in such a way it has no error. The proposed dual quality 4:2 compressors operate in two accuracy modes. They are Approximate Mode and Exact Mode. Power gating technique is turn off the unused components of approximate part. In the exact operating mode, the delay of this structure is about same as that of the exact 4:2 compressor. The structure of NAND gate of the approximate part is not used during the exact operating mode. The output sum, carry, c_{out} can be obtained from

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus C_{in} \quad \text{.....(iv)}$$

$$Carry=(x1 \oplus x2 \oplus x3 \oplus x4)C_{in} + x1 \oplus x2 \oplus x3 \oplus x4)\ x4 \ldots (v)$$

$$Cout = (x1 \oplus x2)\ x3+(x1 \oplus x2)\ x1 \ldots\ldots\ldots (vi)$$

Dual-Quality 4:2 Compressors are utilized in the reduction module of four approximate multipliers. In terms of transistor count, the first design has a 46% improvement, while the second design has a 49% improvement. In terms of power dissipation, the first design has a 57% improvement and the second design has a 60% improvement over CMOS implementation at feature sizes of 32 nm. In terms of delay, the second design has a 44% improvement compared to the exact compressor and 35% improvement compared to the first design on average at CMOS feature sizes of 32 nm. The proposed multipliers show a significant improvement in terms of power consumption and transistor count compared to an exact multiplier. Advantages of proposed system includes signal processing and data mining with tolerable error, compressors can also utilize in multimedia signal processing application, reducing the design complication, increase in performance and power efficiency, and reduced power and error rate.

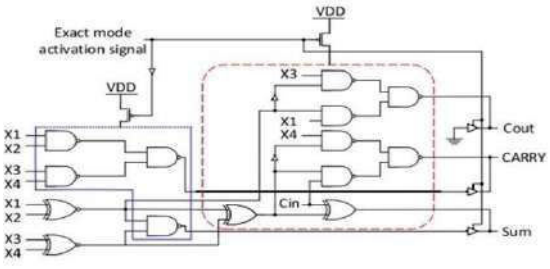

Fig 3.2 Overall Structure of DQ4:2 compressors

Description of the Structure consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact operating mode, the supplementary and some parts of the approximate parts are utilized.

The language used is Verilog, a hardware description language(HDL). It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip−flop. Verilog supports a design at many levels of abstraction. The software used here is Xilinx software controls all aspects of the design flow. Through the Project Navigator interface, you can access all of the design entry and design implementation tools. You can also access the files and documents associated with your projects because implementation is dependent on up-to-date synthesis results.

IV. RESULTS AND DISCUSSIONS

In this section, first, the efficacies of the proposed 4:2 compressors in the approximate operating mode are investigated.

DESIGN 1 OUTPUT**:** The proposed design 1 yielding an error rate of 37.5%. This is less than the error rate using the best approximate full-adder cell. The power consumption is reduced when compared to other proposed system.

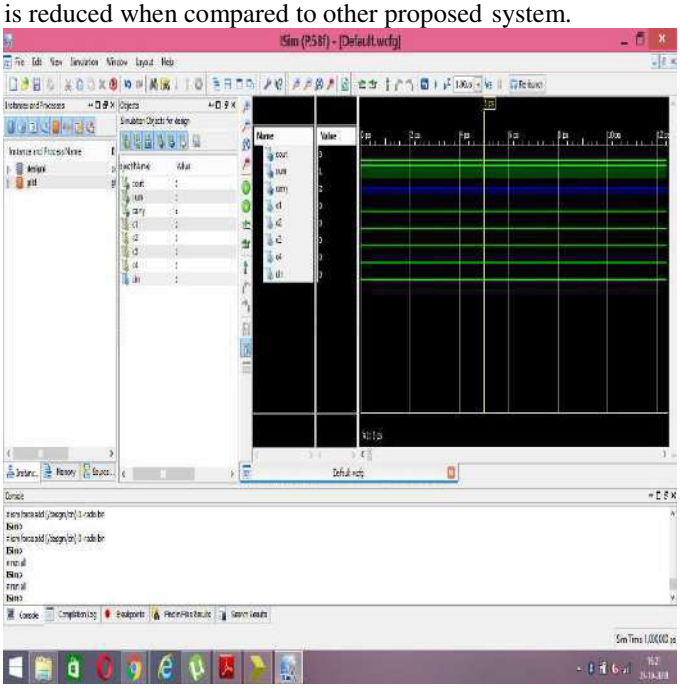

Fig 4.1. Design 1 output

RTL schematic**:** It models a synchronous digital circuit in terms of the flow of digital signals between hardware registers, and the logical operations performed on those signals. The structural description of design 1 circuit may

lead to easy identification of a process. The transistor count is reduced to 48.

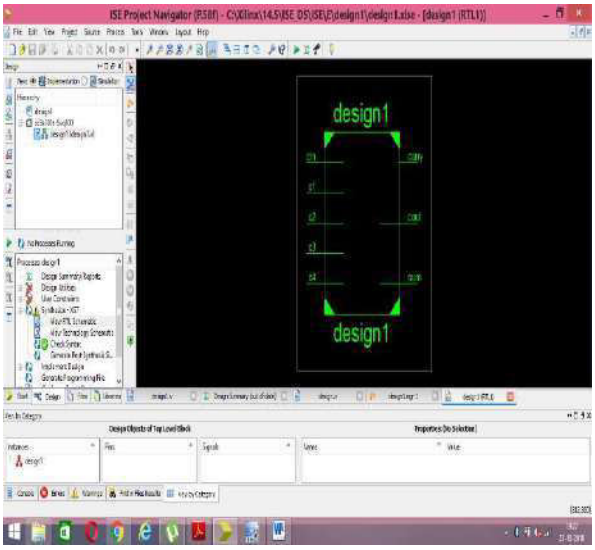

Fig4.2. Design 1 RTL Schematic

Design 2 outputs: A second design of an approximate compressor is proposed to further increase performance as well as reducing the error rate can be ignored in the hardware design. The power dissipation up to 0.010096 in design methodology.

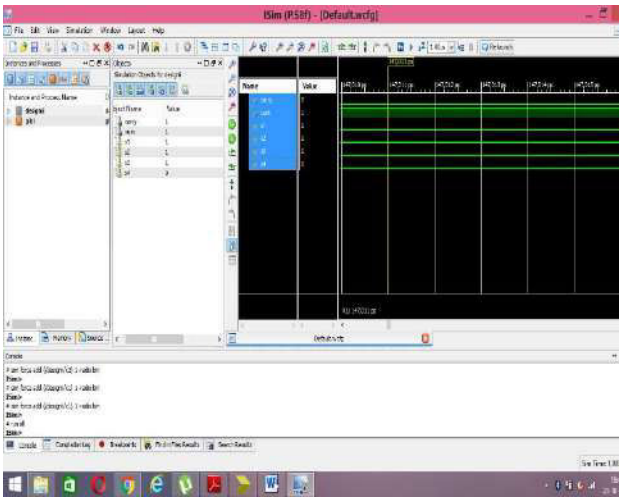

Fig4.3. Design 2 output

RTL schematic: The transistor count is further reduced to 42. In terms of delay, the second design has a 44% improvement compared to the exact compressor and 35% improvement compared to the first design on average at CMOS feature sizes of 32 nm.

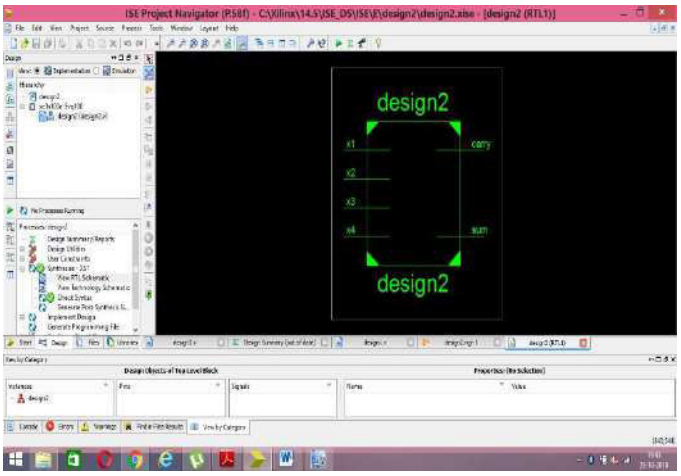

Fig4.4. Design 2 RTL schematic

Output for Approximate part: In the process of approximation of full-adder in the multiplier, one of the EXOR gates is replaced with OR gate to reduce hardware complexity. This results in change of values of output in last two cases out of eight cases. Carry is altered in such a way it has no error.

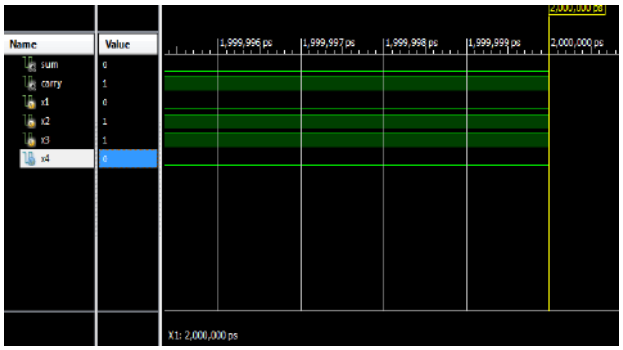

Fig4.5. Output for approximate part

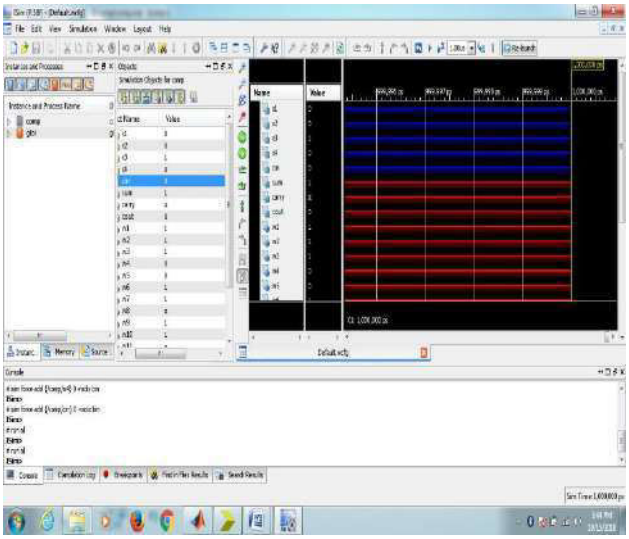

Fig4.6. Simulated output

Implementation of Dadda multiplier for comparative Study: First, the efficacies of the proposed 4:2 compressors in the approximate operating mode are investigated. In the comparative study, which is performed by utilizing them in the Dadda multiplier, the design parameters of the multipliers are compared with the two approximate 4:2 compressors proposed.

Fig4.7: 32 bit dadda multiplier

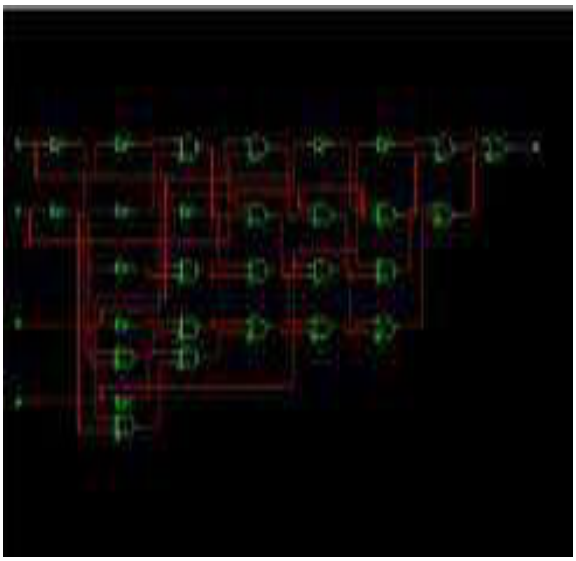

Fig4.8 Technology schematic for dada multiplier

V. Comparison

Finally, the delay, area and power approximate 32-bit Dadda multipliers using the proposed compressors are lower compared with the exact Dadda multiplier, on average, by 49.3%, 68% and 83.7%, respectively. Also, when compared with the Dadda multiplier realized by the proposed approximate compressors of, the delay, area, power, energy, and EDP of the approximate 32-bit Dadda multipliers realized by our proposed compressors are better, on average, by 29% (69%) and 52% respectively.

VI. CONCLUSION

In this project, we presented four DQ4:2Cs, which had the flexibility of switching between the exact and approximate operating modes. In the approximate mode, these compressors provided higher speeds and lower power consumptions at the cost of lower accuracy. Each of these compressors had its own level of accuracy in the approximate mode as well as different delays and powers in the approximate and exact modes. These compressors were employed in the structure of a 32-bit Dadda multiplier to provide a configurable multiplier whose accuracy (as well as its power and speed) could be changed dynamically during the runtime. Our studies revealed that for the 32-bit multiplication, the proposed compressors yielded, on average, 46% and 68% lower delay and power consumption in the approximate mode compared with those of the recently suggested approximate compressors. Also, utilizing the proposed compressors in 32-bit Dadda multiplier provided, on average, about 33% lower NED compared with the state-of-the-art compressor-based approximate multipliers. When comparing with no compressor-based approximate multipliers, the errors of the proposed multipliers were higher while the design parameters were considerably better. Finally, our studies showed that the multipliers realized based on the suggested compressors have, on average, about 93% smaller FOM value compared with the considered approximate multipliers.

VII. FUTURE WORK

The proposed work developed and designed a new 4:2 compressor. In the future this can applied in image processing and signal processing applications. It ensures high speeds, low delay and small area of the multipliers.

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DESIGN AND IMPLEMENTATION OF HIGH PERFORMANCE MAC UNIT CARRY SKIP ADDER

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ABSTRACT

In this paper, we proposed a new architecture of multiplier -and- accumulator (MAC) for high-speed arithmetic and low power consumption. Multiplication occurs frequently infinite impulse response filters, fast Fourier transforms, discrete cosine transforms, convolution, and other important DSP applications. The objective of a good multiplier and accumulator (MAC) is to provide a less area, good speed and low power consuming chip also to consume significant power in VLSI design, and to reduce its dynamic power . The aim of this project is to design and implement the MAC unit for high-speed DSP applications. For designing the MAC unit using carry adders. The MAC unit implementation is done using VHDL, synthesized and simulated using Xilinx ISE.

I.INTRODUCTION

Digital signal processing is one of the important technologies applied in most areas such as wireless communications, audio and video processing, and industrial control. Digital signal processing (DSP) applications constitute the important operations, which usually involve many multiplications and accumulations. The main aim of MAC design has been to enhance its speed, because speed and throughput rate are always important in the digital signal processing systems. Due to the increase of portable electronic products, low power designs have also become major considerations, because the limited battery

energy of these portable products restricts the power consumption of the system. Therefore, the motivation behind this project is to investigate various pipelined MAC architectures and circuit and the design techniques which are suitable for the implementation of high throughput signal processing algorithms. The aim of this project is to design the VLSI implementation of pipelined MAC for high speed DSP applications. For designing the MAC, various architectures of carry adder are considered. The total process is coded with Verilog to describe the hardware.

II. MAC Architecture

A design of high performance 16 bit Multiplier-and-Accumulator is designed. The Multiplier is designed using an array multiplier and the adder is carry skip adder. The attractive feature of the carry skips adder structure is reducing the delay based on the MAC unit. This will increase the speed and improve the area utilization and power consumption. The total design is coded with Verilog-HDL and the synthesis is done using Xilinx ISE Compiler.

BLOCK DIAGRAM

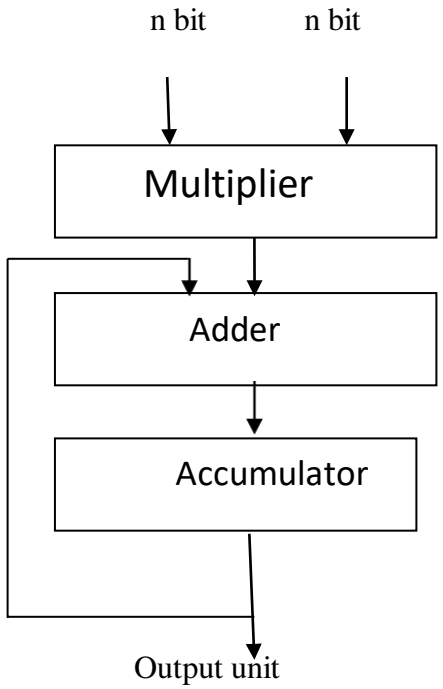

Fig : MAC architecture

MAC Unit is a fundamental block of the computing devices, especially Digital Signal Processor (DSP). The MAC unit performs multiplication and accumulation process. Basic MAC unit consist of multiplier, adding and accumulator .Multiplier circuit is based on adding and shift algorithm .Each partial product is generated using the multiplication of the multiplicand with one multiplier bit. The generated partial product are shifted according to their bit orders and then added. An adder is a digital circuit which performs addition of numbers. In

many computers and other kinds of processor adders are used in the arithmetic logic units or ALU. An accumulator is a registered element used for short-term, intermediate storage of arithmetic and logic data in a computer's CPU(Central Processing Unit) .

A. Carry skip adder

A carry-skip adder (also known as a carry-bypass adder) is an adder implementation that improves the delay of a ripple-carry adder compared to other adders. The worst-case delay can be improved by using several carry-skip adders to form a block-carry-skip adder. The critical path of a carry-skip-adder begins at the first full-adder, passes through all adders and ends of the sum-bit .Carry-skip-adders are chained to reduce the overall critical path.

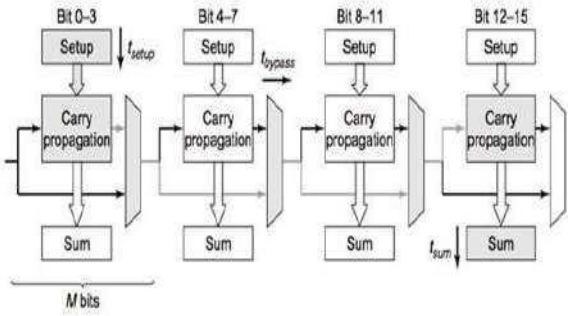

Fig : Block diagrm of carry skip adder

B. Array Multiplier

An array multiplier is a digital combinational circuit used for multiplication of two binary numbers by employing an array of half adder and full adders. They are well known for their regular structure. N X M bits are used for the generation of partial product and some area of multiplier are added to the N partial product and they require N-1 bit adders. The shifting of partial product is done by simple routing and they do not require any logic. For the performance optimization first the critical timing path should be identified , which are nontrivial. The critical path expression for the propagation delay can be expressed as

T mulitiplier= [(M-1) +(N-2)]t carry + (N-1) t sum+ tand

Where t represents the propagation delay between the input and the output carry, tsum represents the delay between the input carry and a sum bit of the full adder, and t is the delay of AND . In order to get the effective processing elements linear pipeline is implemented .The multiplication of the M bit Multiplicand and N bit multiplier yields N X M matrix of partial product. The reduction of partial product is made by the parallel application results in a matrix with a height of two.

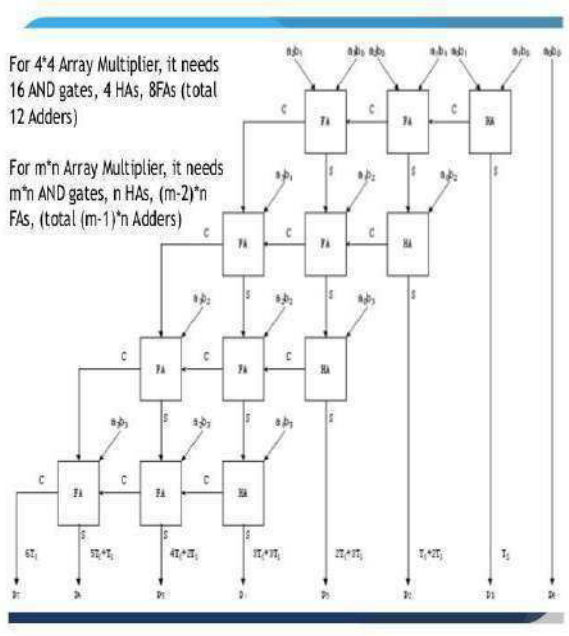

Fig: Array multiplier architecture

C. Comparison

The table shows the parameter analysis of area, power and delay comparing the conventional adder and proposed adder.

Parameter	Conventional Adder	Proposed Adder
AREA No of LUT Transistor count	 88 32	 98 18
DELAY	5.978	4.392
POWER Frequency	 100 MHZ 1.048	 100 MHZ 1.024

Fig : Comparison of Area ,Delay and Power

D. Advantages

- Less area
- Less delay
- Least gate count

III.EXPERIMENTAL RESULT

In this paper, A design of 16 Software Overview The Xilinx software controls all aspects of the design flow. By the Project Navigator interface, we can access all of the design entry and design implementation tools. We can also access the files and documents related to our project. There are four panel sub-windows in the Project Navigator. The top left is the Start, Design, Files, and Libraries panels, which implies display and access to the source files in the project as well as access to running processes to the currently selected source. The Start panel is used for quick access to open the projects also frequently access reference material, documentation and tutorials. At the bottom of the Project Navigator indicates the Console, Errors, and Warnings panels, which display status messages, errors, and warnings. The right is a multi-document interface (MDI) window which is referred as the Workspace. The Workspace is useful to view design reports, text files, schematics, and simulation waveforms. Windows can also be resized,

undocked from Project Navigator, moved to a new location within the main Project Navigator window, tiled, layered, or closed. We can use the View Panels menu commands to open or close the panels. Bit Multiplier-and-Accumulator (MAC) is implemented and a static CMOS CSKA structure called CI-CSKA was proposed with MAC, which implements high speed and consumes less power. The high speed was achieved by altering the structure through the concatenation and instrumentation techniques. The multiplier is designed using an array multiplier and the adder is designed to carry skip adder. Also , AOI and OAI compound gates were exploited for the carry skip logics. Verilog-HDL is used for coding and the synthesis is done using the Cadence RTL compiler.

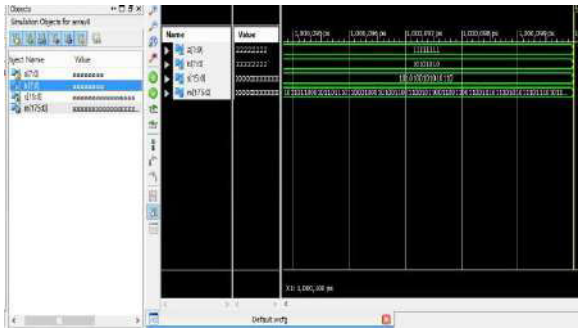

Fig: Output of Array multiplier

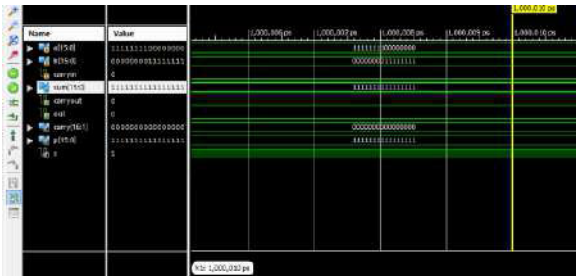

Fig: Output of Carry skip Adder

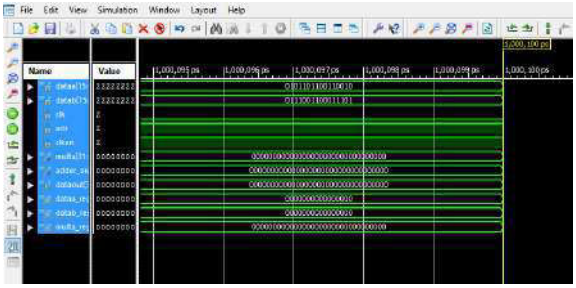

Fig : Output of MAC unit

IV. CONCLUSION

In this paper, a design of high performance 16-bit Multiplier-and-Accumulator (MAC) is implemented which exhibits a higher speed and lower energy consumption .The speed enhancement can be modified through the concatenation and Instrumentation technique. The carry skip adder in the middle includes a parallel adder structure to increase the slack time, which

reduce the energy consumption by reducing the supply voltage.

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ARCHITECTURE DEVELOPMENT OF COST-EFFICIENT MICRO CONTROL UNIT FOR WBSN

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Abstract-**Data transmission of Electrocardiography(ECG) signal over Wireless Body Area Network(WBAN) is currently a widely used system that comes together with challenges in terms of efficiency and affectivity.In this study,an effective Very-Large-Scale Integration(VLSI) circuit design of lossless Electrocardiography(ECG) signal transmission over WBAN.The proposed design was realized based on a novel lossless compression algorithm which consists of an adaptive fuzzy prediction,a voting-based scheme and a tri-stage entropy encoder.The tri-stage entropy encoder is composed of a two-stage Huffman and LFSR(Linear feedback shift register) encoders with static coding table using basic comparator and multiplexer components.A pipelining technique was incorporated to enhance the performance of the proposed design.The proposed design was fabricated using a 0.18 CMOS technology containing 8405 gates with 2.58Mw simulated power consumption under an operating condition of 100MHz clock speed.**

Index Terms—Wireless sensor networks, micro control unit,lossless compression,very large scale integration(VLSI).

I.INTRODUCTION

In modern days,applications of wireless body sensor networks(WBSNs)have become wider and wider.These applications provide an effective solution for many health care.In future trend of development,such as wireless sensor system for analyzing infectious disease nodes and efficiently protecting sensitive personal data in network security,the usage of WBSNs technique is improved rapidly.As the result of light-weight for wearable and portable application,development of an efficient device to monitor physical signals via the VLSI technique has become an important trend.

The author Lee et.al [8] proposed an efficiency complementary metal-oxide-semiconductor(CMOS) sensor for body temperature detection.The blood pressure can be detected by a magnetoelastic skin curvature sensor proposed in [9].The pH value can be measured by an ISFET sensor proposed in[10].Although all these sensors provided efficient devices to capture the various physical signals,the WBSNs suffered from the limitation of wireless transmission bandwidth,computing resource and energy in batteries.

Several studied concerned hardware-oriented architecture of WBSNs has been presented recently.For saving more power consumption and keep longer using time, an adaptive power controller and adaptive fuzzy controller designed.A multi lossless body-signals compressor was presented in portable monitoring system.

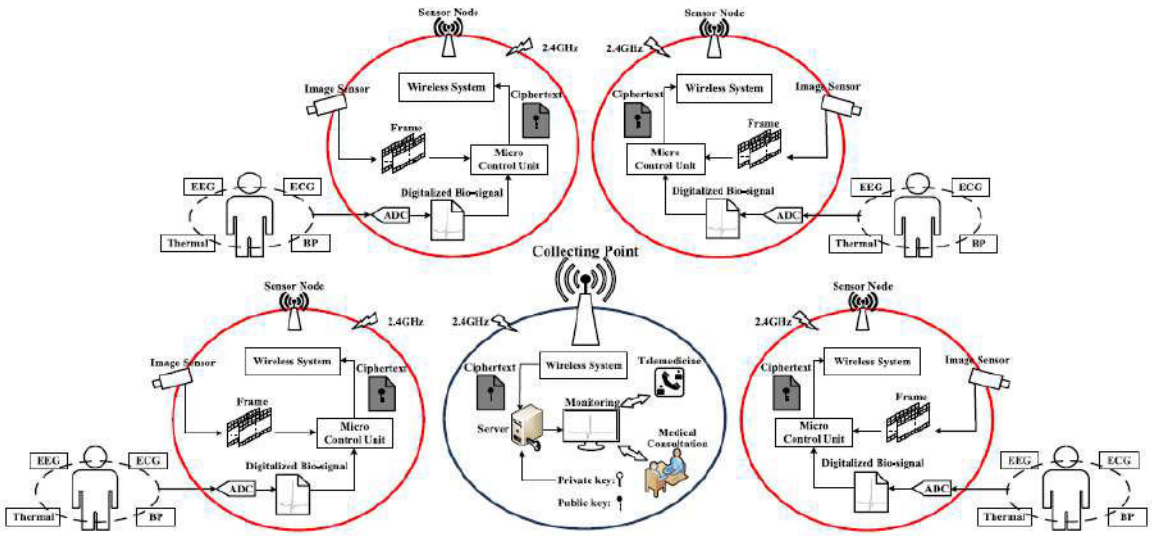

Fig.1 WBSNs system and the arichitecture of wireless sensor nodes

Recently for handling various bio-signals and processing physical signals in WBSNs,a multi-sensor micro control unit(MCU) was designed [11].A bio-signal processing technique was used to improve siganl quality in medical applications successfully.By using specific mathematical operations the physical signals can be analyzed.

II. WIRELESS BODY SENSOR NETWORK SYSTEM

Fig.1 shows the WBSNs system and the architecture of wireless sensor nodes.A typical WBSNs composed a bunch of wireless sensor nodes.Each nodes consists of analog-to-digital converter(ADC),a micro control unit(MCU),and a wireless transceiver with an antenna.

The ever-increasing interest in wireless communications has resulted in the development of new technologies and applications for the personal use of radio frequencies. Technologies advancement in integrated circuits(Ics),coupled with that of wireless technology and physiological sensors,opens up opportunities for developing small, low power, light weight and intelligent physiological monitoring devices.These devices can form a Wireless Body Sensor Network(WBSN), launching a new era of using technology to unobtrusively obtain physiological measurements for improved well-being monitoring.This paper aim to give a comprehensive review on the use of wireless sensor technology for monitoring behavior related to human physiological responses.

In WBSNs are applicable in different physical signals, such as electroencephalography(EEG), Electrocardiogram(ECG), thermal and blood pressure(BP), are captured with the help of different sensors.Now, the MCU needs to process and merge the physical and image data are then sent to processed and merge

data to a 2.4 GHz band communication system for transmission.

III. ARCHITECTURE OF MICRO CONTROL UNIT

The architecture of MCU has been developed in order to develop a MCU design for wireless body sensor networks, a cost-efficient and power-efficient. Fig. 2 shows the architecture of the proposed MCU design. First, the physical data are detected from the four body sensors from human beings.The detected data is in the form of analog and then it can be transformed as digital data by an analog-digital converter (ADC) device. Second, these digital data are processed by the proposed MCU design that consists of an asynchronous interface, a multi-sensor controller, a register bank, a hardware-sharing filter, a lossless compressor, an encryption encoder, an error correct coding (ECC), a QRS complex detector, a power management. At last, the processed digital data will be sent to the UART interface for transmission. All these operations and functions in the proposed MCU design are of low-complexity, which is suitable for development of WBSNs and implementation with a cost-efficient and high performance architecture via the VLSI technique.

A.Multi-Sensor Controller

The WBSNs contain sensors that are used for detecting different physical signals from the human body. By generating a control signal to a 4-to-1 multiplexer, the multi-sensor controller can handle four different sensors, such as sensor1, sensor2, sensor3 and sensor4 as shown in Fig. 2.The multi - sensor controller can select one of four signals according to the control signal sent from the MCU. Since the multiplexer selects the sensor properly, with the help of MCU

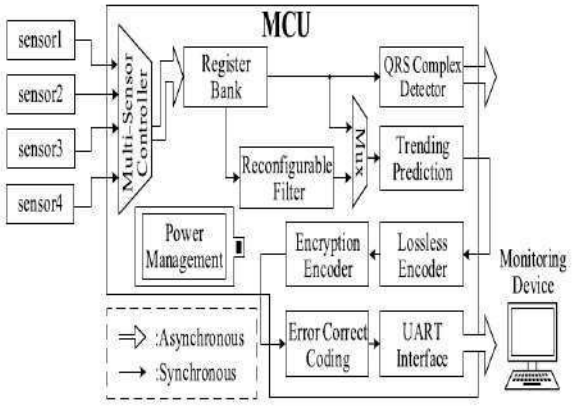

Fig. 2 Proposed micro control unit

successfully. More than one sensor is active at any and sending signals to the MCU simultaneously. In addition, the multi-sensor controller also controls the signals to store the data in one of four-line register buffers in the register bank of the MCU. Therefore, based on the design of the multi-sensor controller, the proposed MCU design can be efficient one and also prevent data from missing.

B. Register Bank

The register bank was designed in order to process four different signals, in the proposed MCU. In the proposed architecture of the register bank consists of four line buffers X_1, X_2, X_3, X_4, and one multiplexer. There are 16 shifts-registers are used to store the four values for each channel. The proposed MCU produces a control signal by the finite state machine circuit to classify different sensor data. Each channel in the register bank stores four values: one current value X_i (t) and three past values X_i (t-1), X_i (t-2) and X_i (t-3) where ``i" is the index of line buffer. Each register can receive only one value of physical signal in each time.

C. Reconfigurable Filter

In order to process the signals in different requirements, there are three types of filters which is designed to achieve the abilities of different physical signals filtering: sharpen filter, binomial filter, and average filter. Here the Sharpen filter can be represented by G(x), Binomial filter can be represented by P(x), Average filter can be represented by A(x).

Sharpen filter $G(x)$ uses Gaussian equation [17] to increase the intensity of high frequency and filter out low frequency parts of the signal. Binomial filter $P(x)$ can be obtained by Pascal's triangle [18], and the filter can enhance central value and cutoff high and low frequency noises from the signal. Average filter $A(x)$ uses the same weighting coefficients to calculate average value of the signal stored in register bank. By using these different kinds of filters, the physical signals can be observed apparently.

D. QRS complex detector

In order to achieve the target of the proposed multi control unit for WBSNs, heartbeats are considered by a QRS complex detector. To obtain the heartbeats information in the real time, the proposed QRS complex detection algorithm will detect the information and record the QRS information by analyzing the critical regions of the ECG signal. For example, the *R* and *S* points usually appear at the maximum (*Max*) and minimum (*Min*) values in the ECG signals respectively. Hence, the critical regions in the heartbeats can be easily detected according to information on the detected R and S points. Two thresholds *High* and *Low* are used to determine whether the values enter into the critical regions while the process is taking place. The *R* and *S* points are recorded as *Max* and *Min* values in order to update the values of *High* and *Low* thresholds, respectively. The High threshold can be evaluated by

$$High = (Max - (\frac{(Max - Min)}{2^n}))$$

The Low threshold can be evaluated by

$$Low = (Max - (\frac{(Max - Min)}{2^n}))$$

E. Lossless Compressor

In order to reduce the power consumption caused by the wireless communication and maintain the integrity of physical signals, a lossless compressor is used. The lossless compressor includes two and they are, an adaptive trending predictor and a hybrid entropy encoder was created for the WBSNs. Lossless Compressor is a class of data compression algorithms that allows the original data to be perfectly reconstructed from the compressed data. To be able to reduce the data redundancy efficiently, an adaptive three-trending-prediction algorithm was proposed. The current value $X_i(t)$ was forecasted by the past three values of the $X_i(t-1)$, $X_i(t-2)$ and $X_i(t-3)$.

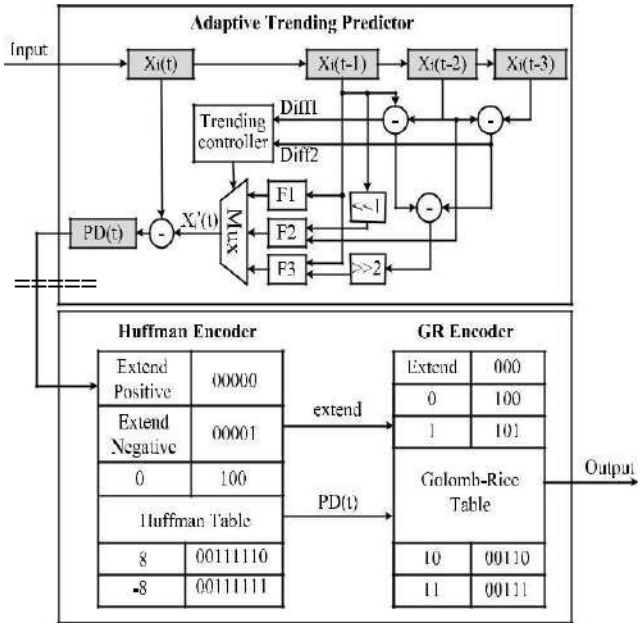

Fig. 3 Architecture of proposed Lossless Compressor

Fig. 3 shows the architecture of the proposed lossless compressor. It consists of an adaptive trending predictor and an hybrid entropy encoder. The predictor contain 1 register, 3 subtractors, 1 multiplexer, 3 prediction function generators, and 1 trending controller. The trending controller produced control signals to select a result of $X_i^0(t)$ from three predicted function generators *F1*, *F2*, and *F3*. Finally, the prediction difference (*PD(t)*) can be produced by calculating the difference between $X_i(t)$ and $X_i^0(t)$. The extensible hybrid-entropy encoder consists of a modified Huffman and absolute GR encoder.

F.Huffman Coding

Huffman coding [15] is a classic entropy coding algorithm, it is mainly used for the probability distribution of target values is centralized. However, the silicon area of a Huffman encoder will be enlarged for the depth of the Huffman coding tree. Hence, a limited Huffman coding technique was selected as the rst stage of the proposed entropy coding methodology.

The main idea of Huffman Coding is to assign variable-length codes to input characters, the length of the assigned codes are based on the frequencies of corresponding characters. The most frequent character gets the smallest code and the least frequent character gets the largest code.The variable-length codes assigned to input characters are Prefix Codes, means the codes (bit sequences) are assigned in such a way that the code assigned to one character is not prefix of code assigned to any other character. This is how Huffman Coding makes sure that there is no ambiguity when decoding the generated bit stream.

On the other hand, two extending codes, positive and negative extending codes, were added to encode the values beyond the range of the limited Huffman coding table, which successfully improved the performance by removing a sign bit of Golomb-Rice (GR) codes and reduced half silicon area.

FLOWCHART OF HUFFMAN ALGORITHM

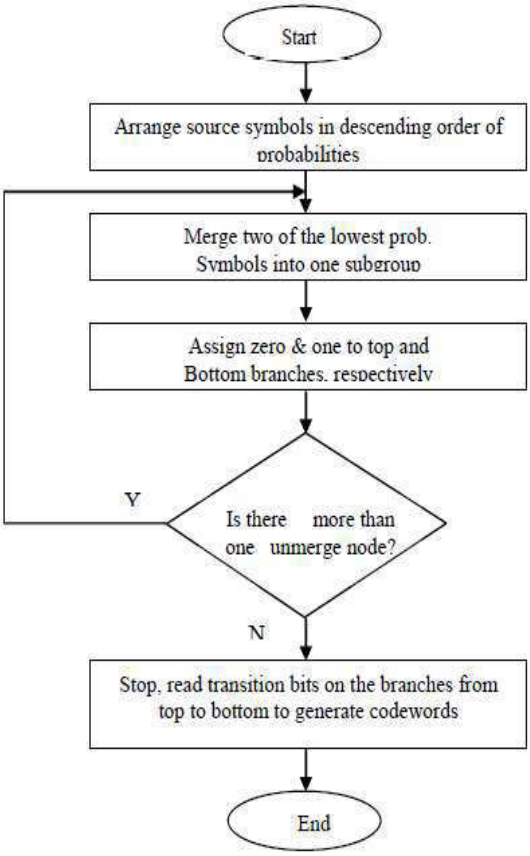

Fig. 4 Flow chart of Huffman algorithm

G. Encryption Encoder

Encryption Encoder prevent the personal information from being cracked. It is a technique used to transfer the plaintext to ciphertext for WBSNs. EEC is based on ElGamal cryptography which is a kind of asymmetric encryption coding.ElGamal

algorithm is an efficient way to prevent the personal information by using two key and they are, public key and private key. Public key s an confidential parameter and private key is an open parameter.

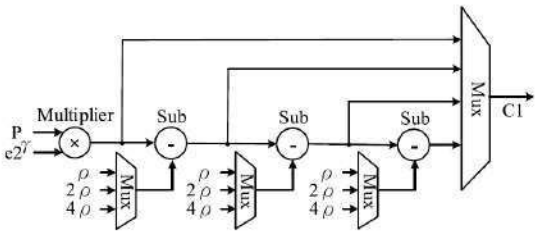

Fig. 5 Architecture of the proposed encryption encoder

where p is the plantext,e2 is the public key Fig. 5 shows the architecture of the proposed encryption encoder. It consists of 1 multiplier, 3 subtractors, and 4 multi-plexers. The remainder values ciphertext C_1 were calculated. Finally, the simplied encryption encoder provides both low-cost architecture, and produces better security for the proposed MCU design.

To be able to decrypt the ciphertext which is sent from sensor node, the private key is used. The wireless sensor nodes used public keys to encrypt the personal information, but they cannot use the public key to decrypt the ciphertext. However, the private key set by the administrator is the only one which can decrypt the text

H. Error Correct Coding

ECC can used to increase the reliability for wireless transmission. The Encrypted data is given to the block.ECC add an additional bit called redundancy code before transmission.So th receiver can able to check whether transmission data are correct or not before decoding.It is also used to decrease the transmission error.

H. Universal Asynchronous Receiver/ Transceiver Interface

UART is used to transmit the bit stream to other devices. It communicate between hardware and PC.

IV. EXPERIMENTAL RESULT

This work was synthesized by using a Xilinx ISE software. Xlinx software controls all aspects of the design flow.

Fig 6 shows the Design summary of proposed MCU design.Design Summary provides access to design reports, messages, and summary of results data. Message filtering can also be performed.Design Utilities Provides access to symbol generation, instantiation templates, viewing command line history, and simulation library compilation.User constraints provides access to editing location and timing constraints.

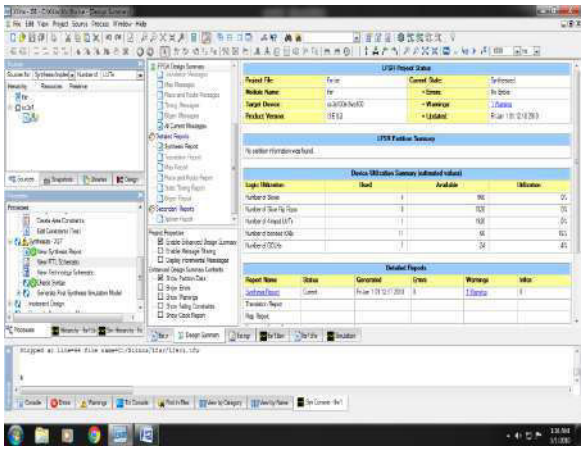

Fig.6 Design Summary of Proposed MCU

Fig.7 shows the coding window of the proposed MCU design. In computing, a linear-feedback shift register (**LFSR**) is a shift register whose input bit is a linear function of its previous state. However, an LFSR with a well-chosen feedback function can produce a sequence of bits that appears random and has a very long cycle.

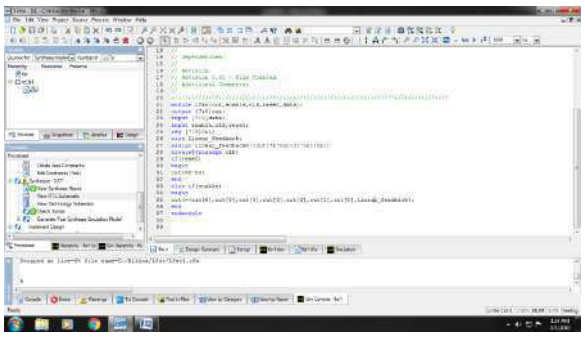

Fig.7 Coding Window of proposed MCU

Fig 8 shows the RTL schematic of proposed MCU. By using this LFSR technique various cryptography applications can be generated by pseudo random numbers. The overall number of random state produced by the LFSR is determined by the feedback polynomial which reduces the delay to an considerable amount compare to that of other methods.

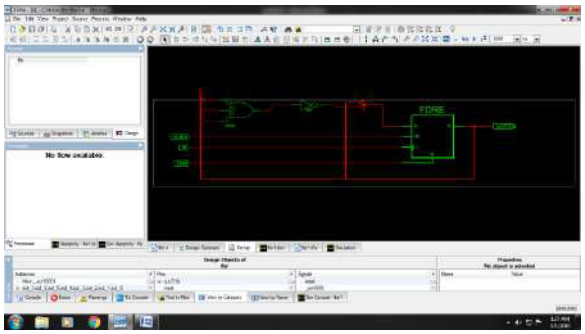

Fig.8 RTL Schematic of proposed MCU

Fig 9 shows the stimulation output of the proposed MCU. When discussing a sequence of random numbers, each number drawn must be statistically independent of the other.

Random number generator is a computational device to generate a sequence of numbers or that lack any pattern. LFSR gives those random pattern generation

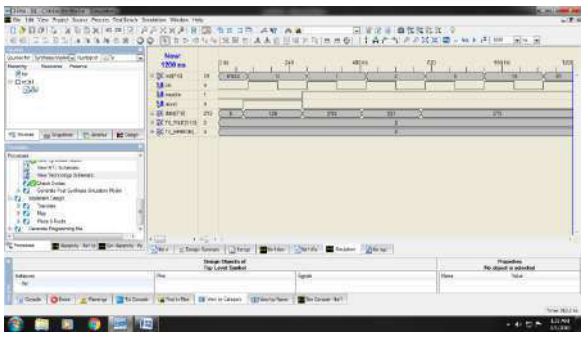

Fig. 10 Stimulated Output

Compared with the previous studies, this work is better in the block of QRS detector and an encryption encoder, but has higher performance, higher security, higher reliability, higher compatibility, more functions, and more exibility than previous designs.

V.CONCLUTION

In this paper, a VLSI architecture of a cost-efficient and micro control unit (MCU) design for WBSNs was presented. The novel hardware-sharing reconfigurable filter was design for reducing the chip area. To reduce the possibilities of misdiagnosis and decrease the transmission power, the lossless compressor consist of an adaptive trending predictor and an extensible hybrid entropy encoder was developed. Through adding an asymmetric architecture of encryption encoder (EEC), the personal information can be protected while wireless transmission. On the other hand, an additional architecture of QRS complex detector was design, which provided more information of physical signals such as heart-beats. The simulation results shows, the proposed MCU design was synthesized by the VLSI technique. Compared with previous designs, this work had better for lower cost, higher compression rate, more functions, and higher security than previous studies.

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VLSI ARCHITECTURE FOR CDMA TECHNOLOGY USING WALSH CODE GENERATOR

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Abstract **– A Code Division Multiple Access (CDMA) is implemented in an on-chip crossbar due to its fixed latency, reduced arbitration overhead, and higher bandwidth. The overloaded CDMA interconnect (OCI) architecture used is the Walsh code generator to enhance the capacity of CDMA (Network on Chip) NoC by increasing the spreading codes. In the serial OCI crossbar, it can achieve 100% higher bandwidth, 31% less resource utilization, and 45% power saving, while in parallel OCI crossbar it achieves N times higher bandwidth compared to serial OCI crossbar at the expense of increased area and power consumption**

Keywords: Code Division Multiple Access (CDMA), Overloaded CDMA Interconnect (OCI), Network on Chip (NoC)

I. INTRODUCTION

System on Chip integrates several intellectual property (IP) blocks into a single chip. All of these IPs need to communicate in the Gbps range. So the on-chip communication requirements for these systems are very demanding. The IP blocks must comprise an interconnection architecture and several interfaces to connect the peripheral devices. The interconnection architecture includes many physical interfaces and communication mechanisms. On-chip data transfer affects the area, performance and the power utilization of the System on Chips (SoC). Developing a suitable high-performance on-chip interconnect architecture has been of supreme significance while considering the high-speed computing technologies. Network on Chips (NoC) provide a way to prevail over the restrictions inherent in regular bus-based interconnection schemes and offers several benefits like high throughput, lower energy dissipation, flexible scalability, and design reusability.

Code-division multiple access (CDMA) is another medium sharing technique that leverages the code space to enable simultaneous medium access. In CDMA channels, each transmit-receive (TX-RX) pair is assigned a unique bipolar spreading code and data spread from all transmitters are summed in an additive communication channel. The spreading codes in classical CDMA systems are orthogonal (cross-correlation between orthogonal codes is zero). These codes enable the CDMA receiver to properly decode the received sum via a correlator decoder. To enable the medium sharing classical CDMA systems to rely on Walsh– Hadamard orthogonal codes. CDMA has been used as an on-chip interconnect sharing technique for both bus and NoC interconnect architectures. Reduced power consumption, fixed communication latency, and reduced system

complexity are the advantages of using CDMA for on-chip interconnects. A CDMA switch has less wiring complexity than SDMA crossbar and less arbitration overhead than a TDMA switch and thus provides a good compromise of both.

Overloaded CDMA is a well-known medium access technique deployed in wireless communications where the number of users sharing the communication channel is boosted by increasing the number of usable spreading codes. To increase the interconnect capacity of on-chip interconnects, overloaded CDMA concept can be used. Multiple Access Interference (MAI) limits the capacity of the CDMA system. By overcoming the MAI problems, interconnect capacity of the CDMA can be significantly increased without degrading the performance or increasing the resource utilization. CDMA channel overloading is a known technique mainly used in wireless communications to increase the communication channel capacity. This technique increases the number of elements sharing the ordinary CDMA bus while keeping the system complexity unchanged by using simple encoding circuitry and relying on the accumulator-based decoder with minimal changes. The conventional method can be advanced by the TDMA OCI (T-OCI) and Parallel-OCI (P-OCI) topologies to increase the bus capacity by 100%. Code overloading for both topologies relies on exploiting special properties of the used spreading code set, namely Walsh code family to add a set of identifiable non-orthogonal spreading codes. NoCs provide a scalable solution for large SoCs, but they exhibit increased power consumption and large resource overheads. To make the crossbar more efficient, a Parallel Compare and Compress (PCC) based codec can be used in the crossbar architecture. This reduces the surplus area needed to store the message data. Also, it provides a security for the data that transmitted through the crossbar.

The paper is organized as follows Section II Network on Chip and section III covers proposed the method of CDMA and section IV covers Walsh Code Sequence and section V Results and discussion and conclusion is given in section VI.

II. NETWORK ON CHIP

Network-on-Chip (NoC) is an advanced design method of communication network into System-on-Chip (SoC). It provides a solution to the problems of traditional bus-based SoC. It is widely considered that NoC will take the place of traditional bus-based design and will meet the communication requirements of next SoC design. A router is the key component and known as the communication backbone in NoC. Fig 1 shows the basic structure of NoC.

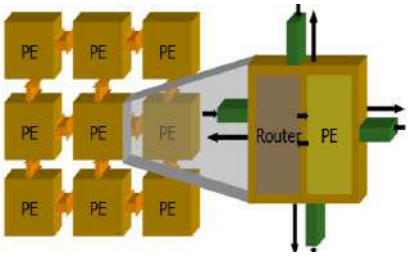

Fig 1: Basic structure of NoC

The NoC is placed on a single chip, which is separated into several regular tiles. A tile is a part of the chip that contains an Intellectual Property (IP) core or Processing Element (PE) and a network router, which is the main component in NoCs. The IP cores are usually heterogeneous in such design because the applications are heterogeneous. The NoC can have general purpose processors, application

specific cores, memory modules, input or output devices and so on. The PE performs computation and communicates with other PE by messages, which are sent through the communication network. By using a Network Adapter (NA), the PE is connected to the network. Its function is to provide an interface between the PE and the network. It also specifies how the communication services are made available to any PE type.

The NA provides mainly two interfaces: one for PEs and another one for the network. It handles the messages generated by the PEs by breaking them into several smaller units called packets. A packet is the logical unit of information that is transmitted through a network route using routers. The packet is composed of the following parts: a header, a data payload, and a tail. The packet header is the front of a packet and it contains the information about the source and destination NoC routers. This helps the NoC to decide the path of the packet. The data payload holds the data transmitted by the PE core across the NoC. The packet tail marks the end of the packet and typically contains codes for error checking and correction.

The communication channel in NoC is the combination of transmitter, physical links, and the receiver. It makes the physical connection between several PEs. The function of the transmitters is to convert digital to analog signals and receivers are used to convert analog signals to digital signal respectively. Analog signals are carried by a set of wires or fibers known as the physical link. Some other important terminals used for communication purpose in NoC's are flit and phit. A packet is made of flow control units, named as flits. A flit is the minimum unit of information that can be transformed across a link and either accepted or rejected. Each flit is made of one or more physical units called phits. The phit is the minimum size datagram that can be transmitted in one link transaction. In most of the cases, both the flit and phit are equal.

The router is the another important NoC component which drives the information through the network. It uses a routing algorithm to determine which of the possible paths, from source to destination are used as routes and which route is taken by each particular packet. Buffers are used at the input ports of the router to store the flits until the router can handle them. The router contains a crossbar switch that provides the means to route the information. A switching mechanism determines how and when the data traverses its route in NoC architectures packet switching is used. That means messages are broken into a sequence of packets and that packets are individually routed.

III. PROPOSED METHOD OF CDMA

CDMA is a spread spectrum technique which encodes the information prior to transmission onto a communication medium, permitting simultaneous use of the medium by separate information streams. By using CDMA encoding, the interconnecting wiring can be reduced to a certain extent. It relies on the principle of codeword orthogonality, such that when multiple code words are summed they do not interfere completely with each other at any point in time and can be separated without loss of information. The channel utilization can be increased by spreading the channel bandwidth using the spread spectrum technique. There are two types of mainly used techniques; one is called Frequency Hopping Spread Spectrum (FHSS) and is currently and the

second one is called Direct Sequence Spread Spectrum (DSSS) which is generally used in civil application systems. CDMA is a spread spectrum multiple access techniques. A spread spectrum technique is one which spreads the bandwidth of the data uniformly for the same transmitted power. A pseudo-random code which has a narrow ambiguity function, unlike other narrow pulse codes, is known as the Spreading code. In CDMA a locally generated code runs at a much higher rate than the data to be transmitted.

The main advantages of CDMA technique are listed below,

- It increases the efficient use of communication media.
- Anti-jam capability.
- Anti-interference capability.
- Low probability of intercept.
- Anti-multipath capability.
- Multi-access capability.

The CDMA technique uses various spreading codes to encode and decode the message sent and received. One of them is Walsh code.

Walsh-Hardmard sequences are used in the CDMA to transmit and receive the signals. Orthogonal codes are those, which provide a zero cross-correlation when there is no offset between the codes. They make use of Orthogonality property, which refers to dot product between the two spreading codes, is equal to zero. Hadamard transform is one of the best- known code expansion techniques to generate orthogonal codes. Walsh sequences are generated by mapping codeword rows of a Hadamard transform. Also, it can be generated by using the Walsh code generator circuit which is shown in Fig 2. The important property of the Walsh spreading code is that it obeys the balancing property.

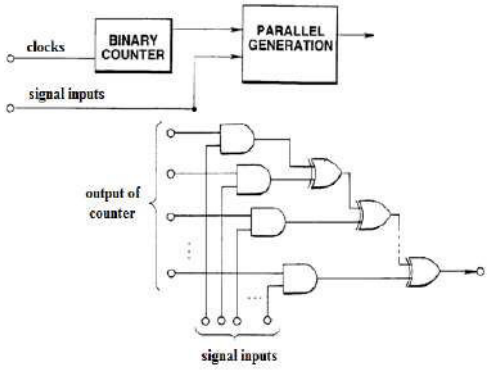

Fig. 2 Walsh code generator circuit.

IV WALSH CODE SEQUENCE IN CROSSBAR SWITCH

The Fig.3 illustrates the high-level architecture of a CDMA-based NoC router.

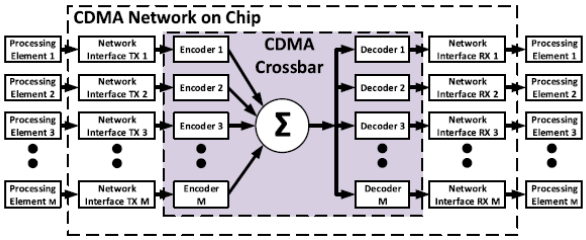

Fig 3 High-Level Architecture of a CDMA-based NoC router

The physical layer of the router is based on the classical CDMA Switch. The classical CDMA crossbar as shown in Fig. 4 consists of three sections. They are the encoder section, channel section, and decoder section. In the encoder part, the spreading code generator module (Walsh spreading code) generates binary orthogonal code which has a chip

length of N is XORed with the transmitted data bit and sent out serially. It indicates that a single bit is spread in a duration of N clock cycles. The number of TX-RX ports sharing the CDMA router equals M = N – 1 for Walsh spreading codes. Serial streams from all transmit PEs sharing the crossbar are added together and the binary sum is sent to the decoding section, which is connected to the receiving ports.

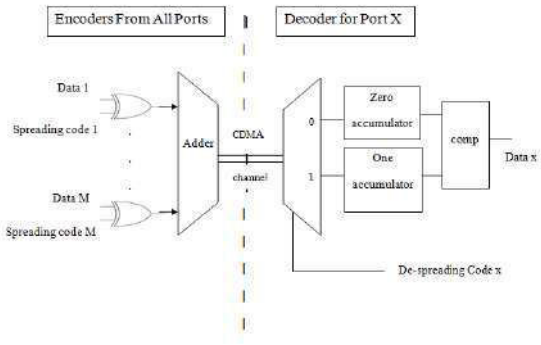

Fig.4 Conventional CDMA Crossbar Switch.

Binary encoding and signalling is multilevel signalling for implementing the channel adder due to its superior performance, reliability, and its inherent support by digital platforms. The decoder is implemented as a wrapper that crosses correlates the serialized channel sum with the signature code assigned to the TX-RX pair. The decoding process is periodic and the decoding cycle lasts for N clock cycles. The spreading operation is realized using a correlator decoder that correlates the received channel sum with the spreading code assigned to the TX-RX pair. Two accumulators are used to realize the correlator decoder. According to the assigned CDMA code, the received sum is passed to the zero accumulator when the current chip value is "0" and to the one accumulator when the chip value is "1," which is equivalent to multiplying the crossbar sum by ±1. At the end of the decoding cycle, the decoder has received the sum of spreading codes or their complements encoded according to the data spread by the transmit ports. Decoding the crossbar sum containing an orthogonal code or its complement using other orthogonal codes (cross-correlation) results in adding the same value to both accumulators. Decoding the crossbar sum containing an orthogonal code or its complement using the same code (autocorrelation) makes the value of one accumulator greater than the other accumulator by the number of ones in the code, which equals N/2 spreading codes. The cross-correlation between orthogonal codes yields zero, while autocorrelation (multiplying the code by itself or its complement) yields ±N/2. Therefore, the difference between the one and zero accumulators is always ±N/2 for orthogonal spreading codes. This can be directly derived for the accumulator decoder using the correlation definition and Walsh code orthogonal property.

Overloaded CDMA is a technique used to increase the number of users sharing the communication channel is boosted by increasing the number of usable spreading codes. This concept can be applied to on-chip interconnects to increase the interconnect capacity. The CDMA router has M transmit/ receive ports. The main difference between the overloaded and classical CDMA routers is that $M > N - 1$ for the former due to channel overloading. Each Processing Element is connected to two Network Interfaces (Nis), i.e., the transmit and receive Network Interface modules.

During the data transmission from a PE, the packet is divided into flits to be stored in the transmit NI first-input first output (FIFO). The router arbiter then selects M winning flits at most from the top of the Network Interface FIFOs to be transmitted during

the current transaction. Each of the selected flits has a destination address to avoid the conflicts and a winner from two conflicting flits is selected. This is done on the basis of the router's priority scheme. The employed priority scheme is the fixed winner that takes all priority schemes; only one of the transmitters is given a spreading code and is acknowledged to start encoding.

Once this process is completed, the router then assigns CDMA codes to each of the transmit and receive Network Interface (NI). Network Interfaces with empty FIFOs or conflicting destinations are assigned all-zero CDMA codes such that they do not contribute Multiple Access Interference (MAI) to the CDMA channel sum. Afterward, flits from each NI are spread by the CDMA codes in the encoder module. The data are spread into N chips, where N is the CDMA code length that equals the number of clock cycles in a single crossbar transaction. Spread data chips from all encoders are summed by the CDMA crossbar adder and the sum is sent out serially to all decoders. The encoding/decoding process lasts for N synchronized via a counter. At each decoder, a code is cross-correlated with the received sum to decode the data from the summed chips. The decoded flits are stored in the receive NI FIFOs until they are read by the PEs.

Two architecture variants of the crossbar can be implemented by using the same structure. They are TDMA Overloaded on CDMA Interconnect (T-OCI) and Parallel Overloaded CDMA Interconnect (P-OCI). The non-orthogonal codes imitate the TDMA signalling scheme. The encoding/decoding scheme used in the architecture provides a novel approach that enables coexistence between CDMA and TDMA signals in the same shared medium. Therefore, the developed encoder is called TDMA overloaded on CDMA interconnect (T-OCI). The Parallel Overloaded CDMA Interconnect (P-OCI) crossbar employs the same Walsh and Overloaded Codes as the T-OCI crossbar; however, the data spreading and decoding are parallelized.

There are several advantages for the overloaded CDMA crossbar when compared with the conventional CDMA crossbar. They are:

➢ Increases the channel capacity

In Overloaded CDMA the number of users sharing the communication channel is boosted by increasing the number of usable spreading codes. This increases the channel capacity.

➢ Reduction in area

The area can be reduced by using the PCC based architecture. Because the area needed to store the data bits can be reduced by the compression technique.

➢ Fixed communication latency

The CDMA technique only offers fixed communication latency. The conventional CDMA and T-OCI crossbar variants exhibit the same latency, which is N clock cycles because a single data bit is spread in N chips. The latency of the P-OCI crossbar, however, is only one cycle.

V. RESULTS AND DISCUSSIONS

1. SIMULATION OUTPUT FOR CDMA

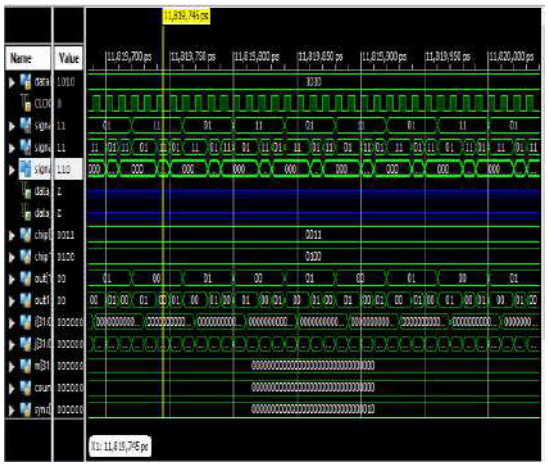

Fig.5 Simulation output for CDMA transmission

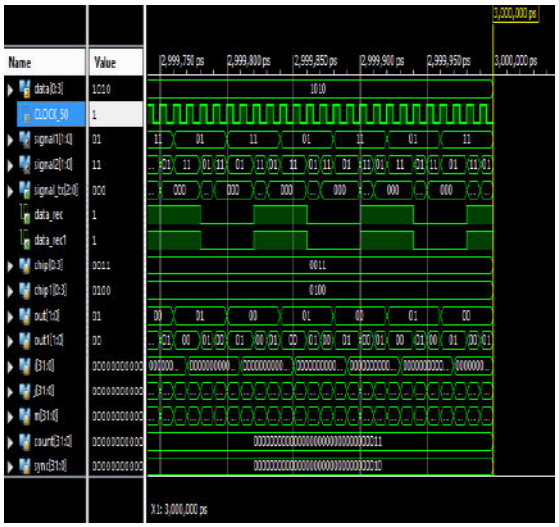

Fig.6 Simulation output for CDMA receiver

2. SIMULATION OUTPUT FOR TRANSMITTER SECTION

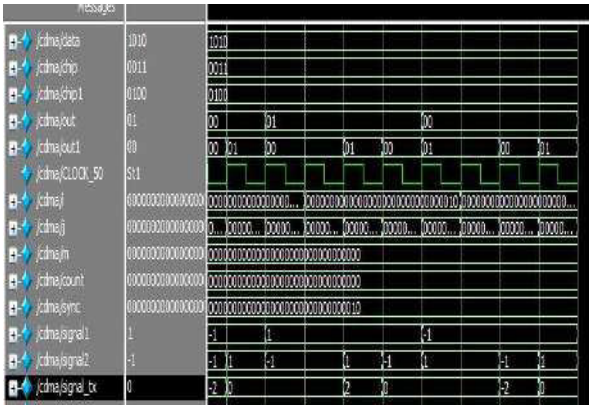

Fig.7 Simulation output for transmitter section

3. SIMULATION OUTPUT FOR COUNTER

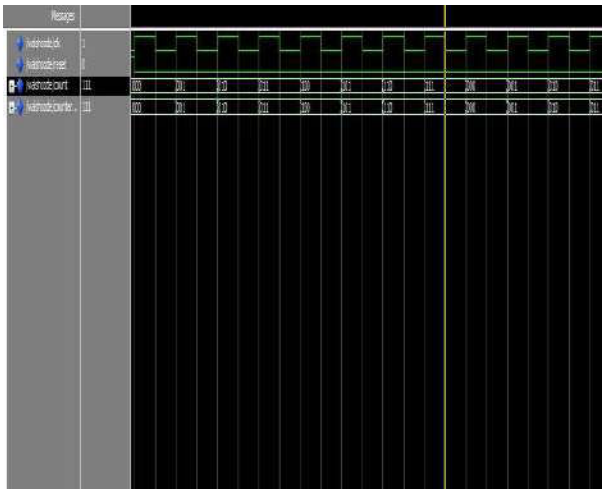

Fig.8 Simulation output for counter

4.SIMULATION OUTPUT FOR DEVELOPMENT OF COUNTER IN WALSH CODE GENERATOR

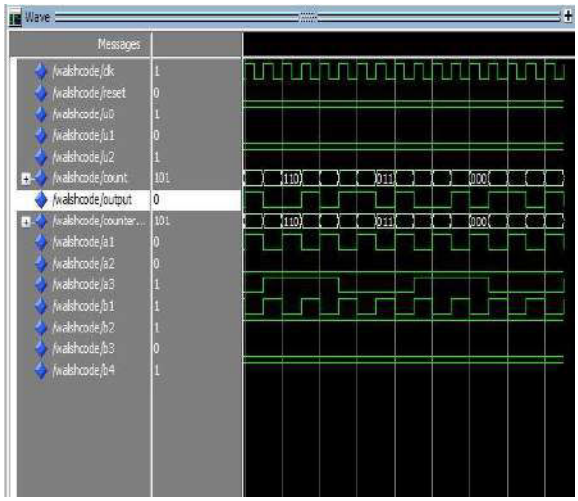

Fig.9 Simulation for counter + walsh code output

5. SIMULATION OUTPUT FOR ORTHOGONAL AND NON-ORTHOGONAL SEQUENCES

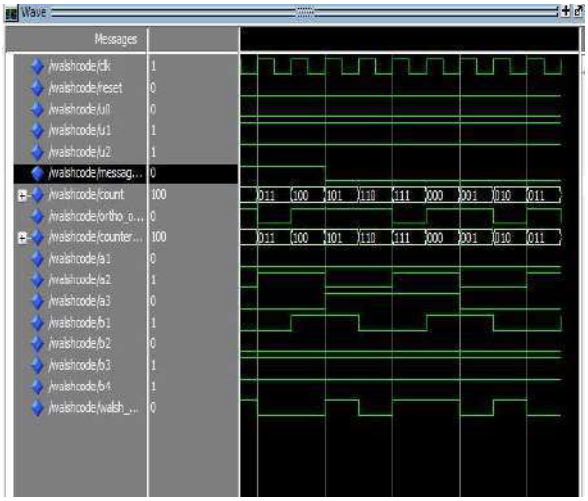

Fig.10 Simulation output for orthogonal sequence

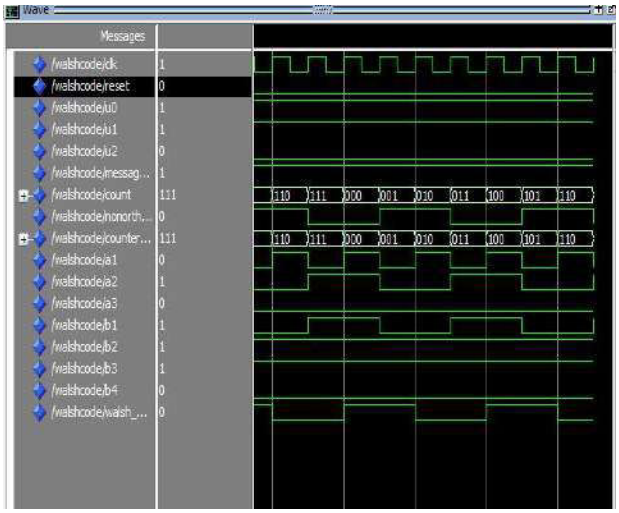

Fig.11 Simulation output for non-orthogonal sequence

6. RTL SCHEMATIC FOR ENCODER

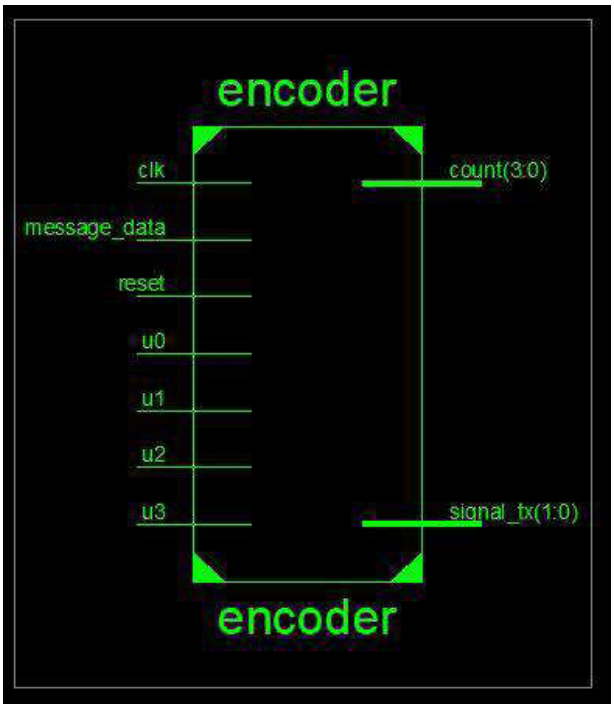

Fig.12 Signal representation

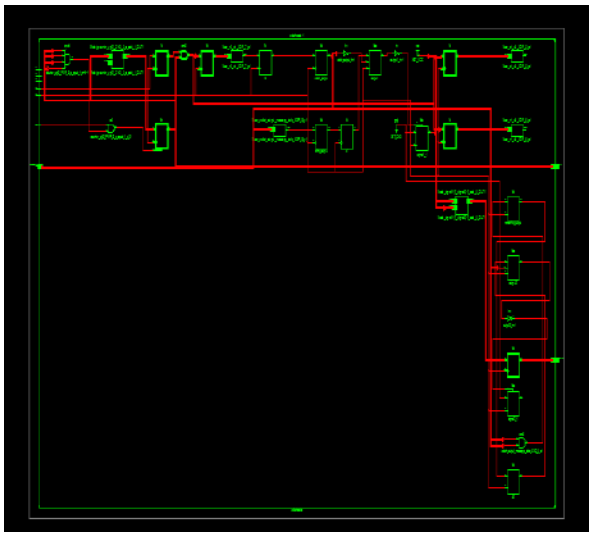

Fig. 13 RTL representation

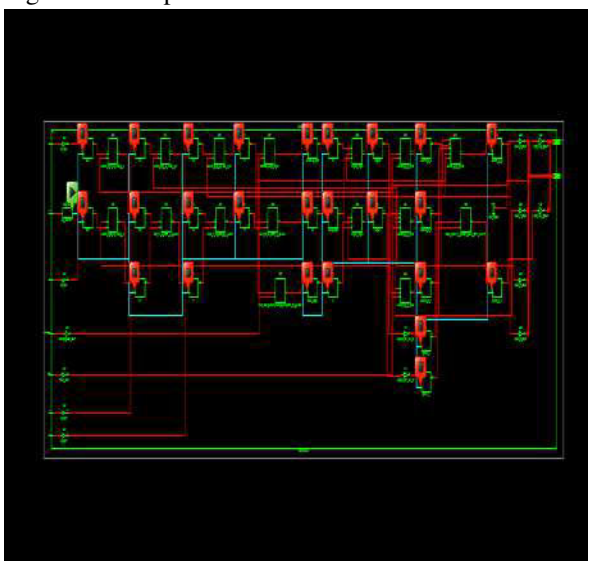

Fig. 14 Technology

7. SIMULATION OUTPUT FOR ENCODER

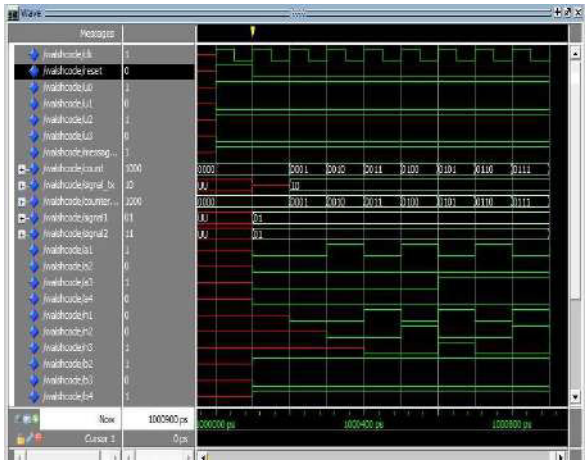

Fig.15 Simulation output for encoder

Table I Hardware Utilization

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	25	126,800	1%
Number used as Flip Flops	25		
Number of Slice LUTs	18	63,400	1%
Number used as logic	18	63,400	1%
Number using O6 output only	18		
Number of occupied Slices	8	15,850	1%
Number of LUT Flip Flop pairs used	20		
Number with an unused LUT	2	20	10%
Number of fully used LUT-FF pairs	18	20	90%
Number of unique control sets	1		
Number of slice register sites lost to control set restrictions	7	126,800	1%
Number of bonded IOBs	13	210	6%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	1.72		

From the table, the number of slice registers used is 25 and the available bits are 126,800 and the utilization is 1%. The total number used as flip-flops is 25. The number used as logic and the number of slice LUTs used is 18 and bits available is 63,400 and the utilization is 1%. The number using O6 output only is 18. The number of occupied slices used is 8 and the available bits are 15,850 and the utilization is 1%. The number of LUT flip-flop pairs used is 20. The number with an unused LUT used is 2 and the available bits are 20 and the utilization is 10%. The number of fully used LUT-FF pairs used is 18, the available bits are 20 and the utilization is 90%. The number of unique control sets used is 1. A number of slice register sites lost to control set restrictions used is 7 and the available bits is 126,800 and the utilization is 1%. The number of bonded IOBs, used in this project is 13 and available IOBs are 210 and utilization is 6%. The numbers of

BUFG/BUFGCTRLs used are 1 and the available bits are 32 and the utilization is 3%. The number used as BUFGs is 1. The average fan-out of non-clock nets is 1.72.

It is clear that power consumption is low compared to the previous works and also TRNG plus digital processor produces high randomness number.

V. CONCLUSIONS

One of the most important factors which affect the performance of the system on chips is on-chip interconnects. The most suitable interconnection method which is capable of addressing several high-performance applications is Network on Chip. The widely used method to implement on-chip crossbars is Code Division Multiple Access (CDMA). Overloaded CDMA is used to intensify the capacity of the CDMA based Network on Chip and to overcome the problems due to Multiple Access Interference (MAI). In overloaded CDMA, the communication channel is overloaded with non-orthogonal codes to increase the channel capacity. Two crossbar architectures that leverage the overloaded CDMA concept namely, T-OCI and P-OCI are advanced to increase the CDMA crossbar capacity. To make the crossbar more efficient a PaCC codec is implemented in between the adder and the decoder section. It uses a PRLE scheme and observes the continuous flow of 0/1. If they are all 0 or 1, all the k bits are bypassed in one clock cycle. In addition to the compression of data it also provides security by encrypting the data. The simulation results show that the PaCC based crossbar become more efficient by effectively balance the area and performance.

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Outage Analysis/SER of a cooperative wireless network based on opportunistic relaying

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Abstract— **In this paper, an adaptive relay node selection algorithm based on the opportunity is proposed to balance the network energy consumption. we analyze the SER and outage probability of opportunistic relay selection in a set-up using decode and forward and where the available channel state information (CSI) is not available. The relay is selected opportunistically to maximize the end-to-end signal to noise ratio received at the destination. At destination Maximal Ratio Combining(MRC) is done to exploit diversity. The statistics in terms of (PDF) and (CDF) have been derived and used for determining outage probability for varying channel conditions. The outage performance and SER with fixed and opportunistic relaying have been compared. It has been shown that the proposed algorithm can improve the network performance by deferring the earliest death time of the nodes, balancing the energy consumption of each node, and extending the network life cycle.**

Keywords—pro-active relaying,Channel state information, WSN, cooperative relaying, outage probability.

I. INTRODUCTION

In recent years, there has been a rapid development in building and deploying sensor networks which is promoted by the recent advances in MEMs-based technologies and low-power short range radios. With the advantage of broadcast in wireless medium, cooperative communication is proposed, which allows multiple nodes to simultaneously transmit the same packet to the receiver so that the combined signal at the receiver can be correctly decoded. Since the cooperative communication can reduce the transmitter power and extend the transmission coverage, it has been widely advocated in terms of increased capacity, improved transmission reliability, spatial diversity. The research of classical cooperative relay communication technology has focused on the improvement of system performance, but takes no account of the energy efficiency of the system. At present, from an energy efficiency stance, the literature [2, 3] demonstrated that the energy consumption of the wireless communication network can be improved by cooperative diversity techniques. This paper proposes an adaptive relay node selection algorithm based on opportunity with the purpose of balancing node energy consumption, making the node to be more efficient and working in longer hours, and improving the performance of wireless sensor network (WSN), which can effectively and greatly achieve a balance of network energy consumption and extend the life cycle of the wireless sensor network.

II. RELATED WORKS

In [6], it has been shown that a decentralized relay selection protocol based on opportunistic feedback from the relays yields good throughput performance in dense wireless networks. This selection strategy supports a hybrid-ARQ transmission approach where relays forward parity information to the destination in the event of a decoding error. Such an approach, however, suffers a loss compared to centralized strategies that select relays with the best channel gain to the destination. This paper closes the performance gap by adding another level of channel feedback to the decentralized relay selection problem. It is demonstrated that only one additional bit of feedback is necessary for good throughput performance.

In [7], a fully opportunistic relay selection scheme to study cooperative diversity is employed in a semi analytical manner. In the framework, idle Mobile Stations (MSs) are capable of being used as Relay Stations (RSs) and no relaying is required if the direct path is strong. The relay selection scheme is fully selection based: either the direct path or one of the relaying paths is selected. Macro diversity, which is often ignored in analytical works, is taken into account together with micro diversity by using a complete channel model that includes both shadow fading and fast fading effects. The results show that the relay selection gain can be significant given a suitable amount of candidate RSs.

In [8], the authors develop a framework to analysis the reliability-reliability tradeoff (RRT) and security-reliability tradeoff (SRT) in the random CRNs, where the security and reliability are quantified in terms of secrecy outage probability and connection outage probability. The RRT evaluates performance tradeoff between the primary and the secondary networks and the SRT evaluates the performance tradeoff inside the secondary network. Furthermore, they propose an opportunistic relay selection (ORS) scheme to enhance the secondary confidential transmission. It is demonstrated that the ORS scheme significantly improves the RRT and SRT as the density of relays increases, and outperforms the conventional direct transmission when the density of relays is larger than a certain value.

Wireless Sensor Networks (WSNs) consists of a large no. of sensor nodes which are usually battery powered and designed to operate for a long period of time .Consequently, minimizing the energy consumption is a very important consideration in WSNs. In this paper the focus is on the usage of opportunistic relay selection algorithm for the purpose of improving the performance of cooperative

network. The outage probability analysis of the proposed relay selection algorithm has been compared with fixed relaying system and it has also been shown that the network performance is improved by extending network life cycle.

III. System Model

We assume that wireless sensor cooperative communication network contains n sensor nodes and a destination node, in which n sensor nodes can work as a source node to send data,

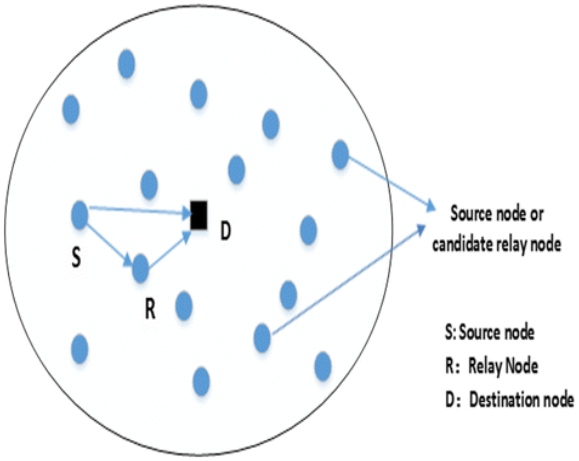

Figure 1: System Model

and also function as a relay node to forward data, as is shown in Fig. 1. We assume that the relay node is selected from the candidate relay nodes. According to the requirement of the bit error rate (BER) threshold, we select the relay node that BER is lower to assist the source node to send information to the destination node. The BER threshold is the direct link BER.

In this system, besides the channel between the source node (S) and destination node (D), there also exist channels between the source node and each relay node (R) and each relay node and destination node. dsd represents the distance from S to D, dsri between S and R, and drid between R and D. In the model above, the entire relay process can be divided into two time slots [7].

In time slot 1, S sends the information data to R and D, then the received signals $Y_{s,r}(t)$ and $Y_{s,d}(t)$ come, respectively, from R and D:

$$Y_{s,r}(t) = \sqrt{P_A} h_{s,r} x(t) + n_{s,r}$$
$$Y_{s,d}(t) = \sqrt{P_A} h_{s,d} x(t) + n_{s,d} \quad (1)$$

P_A is the transmission power of S, $h_{s,r}$ and $h_{s,d}$ are the channel coefficients of S to R and to D, and $n_{s,r}$ and $n_{s,d}$ are the corresponding Gauss white noise.

In time slot 2, R will forward the message to D, at which D receives the signal $Y_{r,d}(t)$ from the relay node that is given:

$$Y_{r,d}(t) = \sqrt{P_R} h_{r,d} x(t) + n_{r,d} \quad (2\text{-}1)$$

P_R means the transmission power of R, $h_{r,d}$ represents the channel coefficient of R to D, and $n_{r,d}$ shows the corresponding additive Gauss white noise. Without loss of generality, we suppose that $n_{s,r}$, $n_{s,d}$, and $n_{r,d}$ are subject to a Gaussian distribution with a mean of zero and a variance of N_0. If the relay node adopts the AF relaying mode, then there is

$$Y_{r,d}(t) = \beta h_{r,d} Y_{s,r}(t)) + n_{r,d} \quad (2\text{-}2)$$

β is the relay amplification factor. If D adopts the maximum ratio combination, the received signal of the destination node is

$$Y(t) = \omega_1 Y_{s,d}(t) + \omega_2 Y_{r,d}(t) \quad (3)$$

ω_1 and ω_2 are weighted factors. This paper assumes that the transmission adopts the BPSK modulation method.

IV. Proposed Opportunistic Relay Selection Algorithm

We assume that all the nodes are half duplex; hence the transmission between s-d takes place in two time slots. At the start of each coherence time a relay r_* is opportunistically selected from the set of relays and this method is called proactive relay selection which is more energy efficient and outage optimal method [4]. We assume that each terminal is equipped with a single antenna. Here h_{sd}; h_{sri} and h_{rid} are denoted as fading coefficients of the channels between the source s and destination d, the source s and the i^{th} relay and the i^{th} relay and destination d, respectively. The channel is modeled as at fading Rayleigh distributed with variances σ^2_{sd} ,σ^2_{sri} , and σ^2_{rid} respectively. We assume that the additive noise is zero-mean complex Gaussian with variance N0 in all channels.

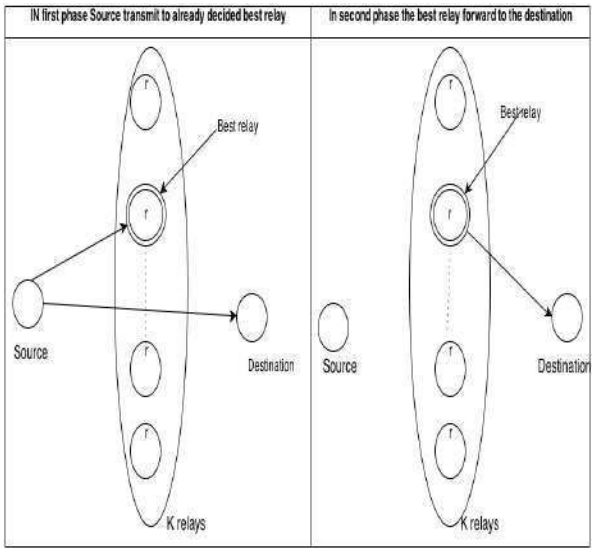

Figure 2: Proactive Opportunistic Relaying

The basic description of Proactive opportunistic relaying here best relay is known to all before the communication starts and in 2nd phase the best relay cooperates by forwarding the information signal to destination.

The flow chart of the OAR selection algorithm proposed in this paper is shown in the Fig. 2. In this paper, such a cycle is called a round number or a wheel. The OAR selection algorithm is considered from the goal of meeting the minimum BER requirement. That is to say, the BER of the data transmission from *S* to *D* is calculated firstly, and set it as the threshold for selecting candidate relay nodes. Then, the relay node calculates the average BER at the time of forwarding data, and automatically determines whether the average BER is less than the BER threshold. If so, these relay nodes constitute a set of candidate relay nodes that assist the source node to complete data transmission efficiently.

In AF relay mode, the SNR (signal to noise ratio) of the receiver with its maximum ratio is

$$\gamma_d = \gamma_{s,d} + \sum \frac{\gamma_{s,r}\gamma_{r,d}}{\gamma_{s,r} + \gamma_{r,d} + 1} \quad (4)$$

$\gamma_{s,d} = P_A|h_{s,d}|^2/N_0$ represents the SNR of the direct link,
$\gamma_{s,r} = P_A|h_{s,r}|^2/N_0$ represents the receiver SNR of *R*,
$\gamma_{r,d} = P_R|h_{r,d}|^2/N_0$ represents the receiver SNR of *D* from *R*.

Under the circumstances of high SNR, 1 in formula (4) can be ignored and be approximated as

$$\gamma_d = \gamma_{s,d} + \sum \frac{\gamma_{s,r}\gamma_{r,d}}{\gamma_{s,r} + \gamma_{r,d}} \quad (5)$$

According to the basic knowledge of communication theory, the BER formula based on SNR can be expressed as $P_e = Q\sqrt{k\gamma_d}$.

The constant *k* is related to the modulation mode.

V. Symbol Error Rate Analysis

Symbol Error Rate is a metric which signifies that out of transmitted symbols, what is the probability of getting information signal in error at the receiver.

The constant k is related to the modulation mode. In binary phase shift keying, the value of K is 2,

$$Q(x) = 1/\sqrt{2\pi}\int_x^{+\infty} e^{\frac{-t^2}{2}dt}.$$

In this way, the BER formula can be used to calculate the direct transmission link. That is, the BER of *S* to *D* is

$$P_e(d) = Q\left(\sqrt{k\gamma_d}\right) \quad (6)$$

Similarly, we can calculate the BER from *S* to the candidate relay node R_i, that is

$$P_e(S,R_i) = Q\left(\sqrt{k\gamma_{s,r}}\right). \quad (6.1)$$

The candidate relay node has two kinds of cases: correct reception and incorrect reception.

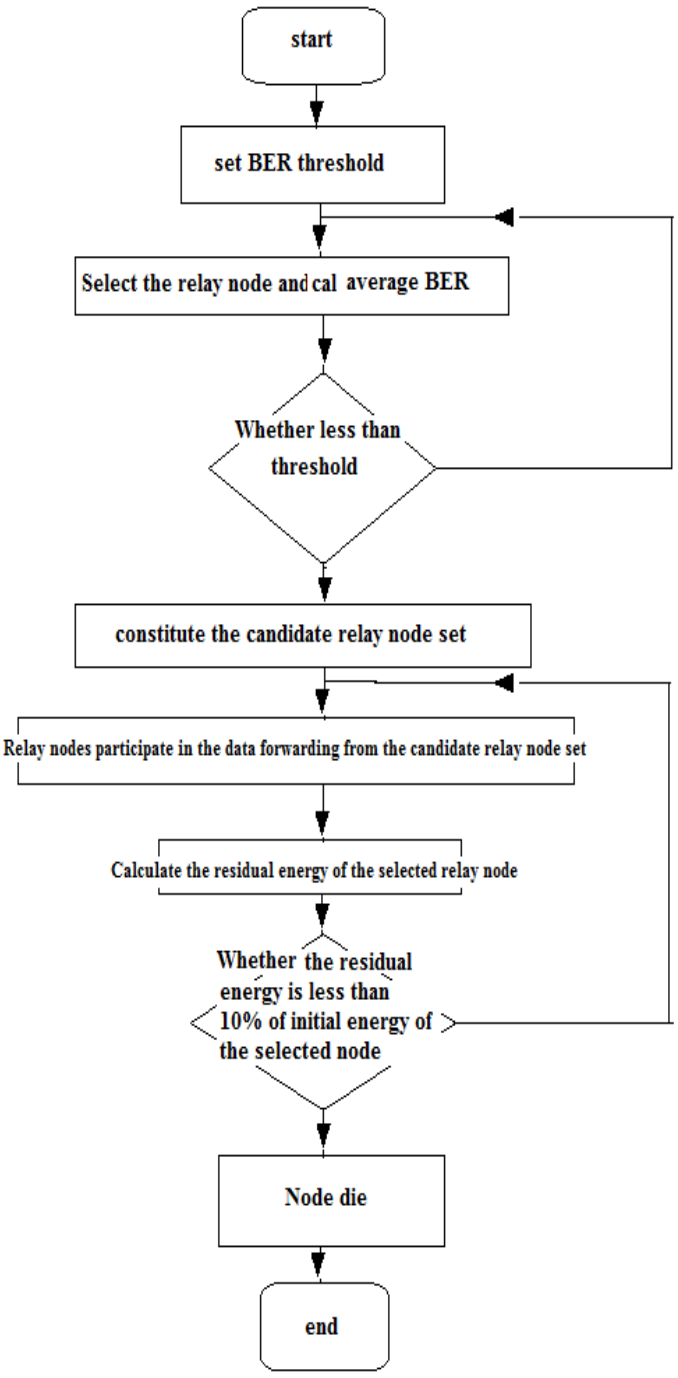

Figure 3: The flow chart of the Opportunistic relay selection algorithm

When the candidate relay node R_i receives correctly, with the help of a single R_i, the BER from *S* to *D* can be expressed as

$$P_e(S,R_i,D) = Q\sqrt{K(\gamma_{s,d}+\gamma_{r,d})} \quad (6.2)$$

When the candidate relay node R_i receives incorrectly, it does not transmit power, which means that it does not assist in transmitting information. At this time, the BER between S and D can be expressed as

$$P_e(S,D) = Q\left(\sqrt{k\gamma_{s,d}}\right). \quad (6.3)$$

Thus, when a single relay node R_i is selected, its average BER can be expressed as

$$P_e(i) = \left(1 - P_e(S,R_i)\right) * P_e(S,R_i,D) + P_e(S,R_i) * P_e(S,D) \quad (7)$$

In this Opportunistic relay selection algorithm, the relay nodes that meet the requirement of BER $P_e(i) < P_e(d)$ making up the candidate relay nodes assist the source node to complete the efficient transmission of data together.

It has been shown that [8] the average SER can be determined using Moment Generating Function(MGF) based approach. The average SER expressions obtained are tight lower bounds for the average SER
MGF can be expressed by using PDF as

$$M_Z(s) = \int_0^{\infty} f_z(x)\, e^{-sx} dx \quad (8)$$

Where $f_z(x)$ is the PDF of the SNR. And with the help of SNRs MGF average SER for M-ary PSK modulated signal can be determined as

$$SER = \frac{1}{\pi}\int_0^{\frac{(M-1)\pi}{M}} M_z\left(\frac{g}{sin^2\theta}\right) d\theta \quad (9)$$

Where M is for M-ary PSK modulation and

$$g = Sin^2\left(\frac{\pi}{M}\right).$$

SER for threshold opportunistic relaying (from this paper)

$$SER_{OR} = P_{out}(\gamma_{sr})P_{er}(\gamma_{sd}) + \left(1 - P_{out}(\gamma_{sr})\right)P_{er}(\gamma_{\beta}) \quad (10)$$

Where γ_{sd} and γ_{β} denotes the SNR of link s - d and end-to-end SNR respectively. The term $P_{out}(\gamma_{sr})Per(\gamma_{sd})$ denotes the event of error, when threshold at relay is not met means the link s-r* is in outage and so at destination the only available signal is from source. While the term $(1-P_{out}(\gamma_{sr})P_{er}(\gamma_{\beta})$ signifies the event of error, when at relay the threshold criteria is met means the instantaneous SNR of the link s-r* is greater than the threshold, and so it cooperates by forwarding the signal to destination and now the signals available at destination are from source and relay both.

VI. Outage Probability Analysis

The Outage probability is defined as the probability that the end-to-end SNR falls below a certain threshold value γ_{th} as

$$Pout = P_r(\gamma \le \gamma_{th}) = F_{\gamma}(\gamma_{th}) = \int_{-\infty}^{\gamma_{th}} f_{\gamma}(x)\, dx \quad (11)$$

Where $f_{\gamma}(x)$ is the PDF of SNR.

VII. Simulation Results

The plot in Fig 4 the SER of opportunistic relay selection algorithm and Fixed relaying is compared and has been Plotted. The SER expression derived in section IV. The results shown are for k(no.of relays)=5.

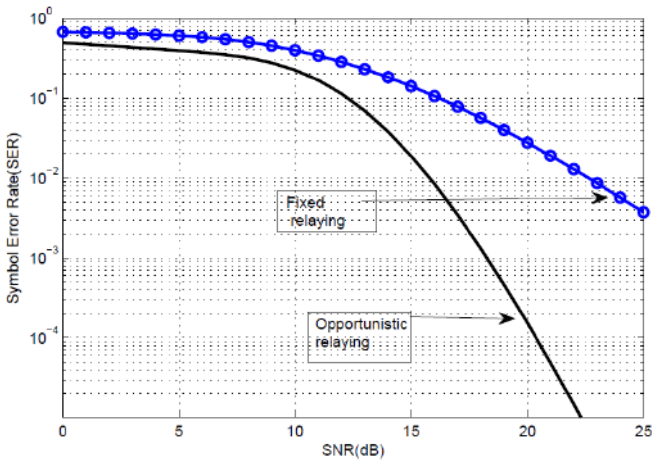

Fig 4: Comparison of Symbol Error rate for opportunistic relaying and fixed relaying

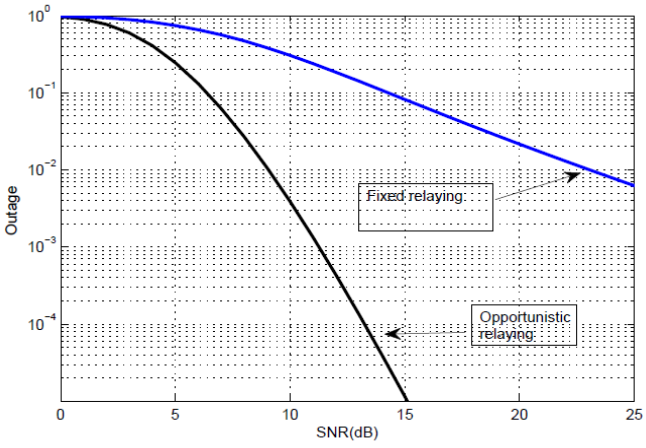

Figure 5: Comparison of Outage Probability performance for opportunistic relaying and fixed relaying.

The plot in Fig 5 the Outage probability of opportunistic relay selection algorithm and Fixed relaying is compared and has been Plotted. The results shown are for k(no. of relays)=5.

The plot in Fig 6 aims to show that how is our system performance going to change if the numbers of relays are different here for the same channel condition different number of relays have been taken into account. Here result has been shown for 3; 4 and 5 number of relays are cooperating in opportunistic relaying. For increase in the number of relays the system performance improves approximately by an order of more than 1 dB for increase in number of relays BPSK modulation.

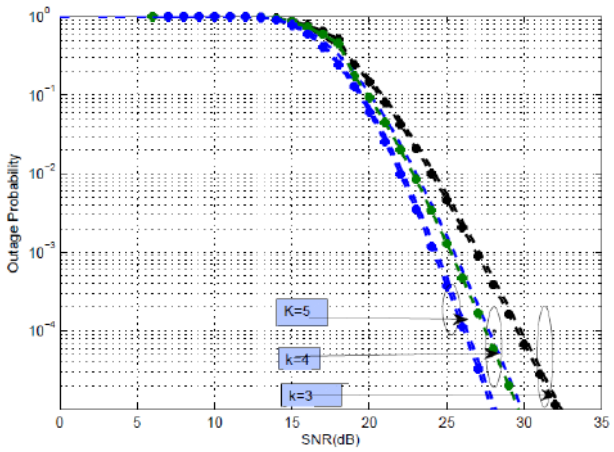

Figure 6:Outage Probability of opportunistic relaying with varying number of relays.

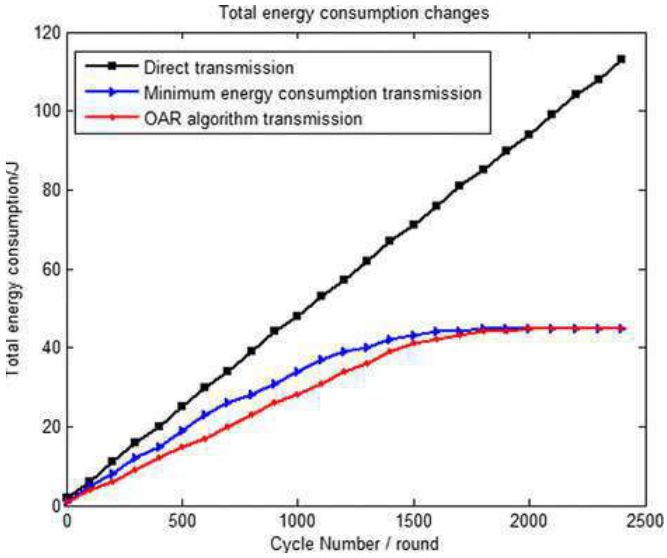

Figure 7: The number of Dead nodes.

In order to verify the validity of the proposed OAR selection algorithm, the number of network dead nodes of three algorithms is compared under the same initial energy. As shown in Fig 7, since the direct transmission is not taken into account of the adaptive adjustment process of the node based on the opportunity, the number of dead nodes in the direct transmission is more than the minimum energy consumption transmission and OAR selection algorithm transmission. At the same time, the minimum energy consumption standard to select relay node, it does not count the average energy consumption of all nodes, thus accelerating the death time of the first node.

VIII. Conclusion

Opportunistic relaying is one of the best relaying protocol to get diversity it provides with a diversity gain of K+1, where K is number of relays. Only one relay is engaged in cooperation and only one additional time slot is required for the overall communication and thus it increases the network efficiency and bandwidth efficiency. The threshold based opportunistic relaying performs better than non-threshold based opportunistic relaying as propagation error is minimized in former. It is found that the proposed OAR algorithm can improve the network performance by deferring the earliest death time of the nodes, balancing the energy consumption of each node, and extending the network life cycle.

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TEMPLATES FOR ARITHMETIC OPERATION IN DSP

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***Abstract* - To develop templates so as to do all the combination of mathematical operations occurring DSP is much simpler manner. In this we develop a new architecture so as to develop those combination of templates depending upon the operation of the DSP. These templates can be used whenever the combination of mathematical equations occur such as A(X+Y)+k, for this equation we can develop template with combination addition and multiplication, the advantage of these templates are, whenever these combination operation occur, we can directly make use of the architecture and make the operation in DSP easy.**

Keywords:- Digital Signal Processing (DSP)

I . INTRODUCTION

Digital Signal Processing normally consists of lots of addition, multiplication and subtraction operation for it different applications. The multiplication operation is a vast and time consuming process, which consists of partial products. Booth multipliers are used in the architecture to reduce the partial product since in DSP we have multiplication operations also, as in normal multiplication we have n partial products so by using booth multiplier we can reduce the partial product by n/2, which is also known as radix-4. Modern systems target high-end application domains requiring efficient implementations of computationally intensive digital signal processing (DSP) functions. The incorporation of heterogeneity through specialized hardware accelerators improves performance, gain and reduces energy consumption. Although application-specific integrated circuits (ASICs) form the ideal acceleration solution in terms of performance and power, their inflexibility leads to increased silicon complexity, as multiple instantiated ASICs are needed to accelerate various kernels

.

We propose a high-performance architectural scheme for the synthesis of flexible hardware DSP accelerators by combining optimization techniques from both the architecture and arithmetic levels of abstraction. We introduce a flexible datapath architecture that exploits CS optimized templates of chained operations. The proposed architecture comprises flexible computational units (FCUs), which enable the execution of a large set of operation templates found in DSP kernels. The proposed accelerator architecture delivers average gains of up to 61.91% in area-delay product and 54.43% in energy consumption compared to state-of-art flexible datapaths sustaining efficiency toward scaled technologies. The arithmetic optimizations at higher abstraction levels than the structural circuit one significantly impact on the datapath performance.

In timing-driven optimizations based on carry-save (CS) arithmetic were performed at the post-Register Transfer Level (RTL) design stage. In common sub expression elimination in CS computations is used to optimize linear DSP circuits. Developed transformation techniques on the application's DFG to maximize the use of CS arithmetic prior the actual datapath synthesis. The aforementioned CS optimization approaches target inflexible datapath, i.e., ASIC, implementations. CS representation has been widely used to design fast arithmetic circuits due to its inherent advantage of eliminating the large carry-propagation chains. CS arithmetic optimizations rearrange the application's DFG and reveal multiple input additive operations (i.e., chained additions in the initial DFG), which can be mapped onto CS compressors. The goal is to maximize the range that a CS computation is performed within the DFG.

II. TEMPLATES

The paper already existing templates consists of either full of addition operation or either multiplication, there was no combination of both multiplication and addition operation in a single template was available. So in this available templates it can only be used for either addition/subtraction and next template for multiplication, so if in DSP a combination of addition/subtraction and multiplication occurs, we have to make use of two template combination to form that equation, which makes the work and operation complicated. The Booth recorder which is used to reduce or minimize the partial product consists of SMB section for addition of the inputs and then to the output of the same the third input as X is given for multiplication. The CSA is the arithmetic used to do the multiplication process, the main advantage of CSA is that is reduces the carry and the final block used is Carry Look Ahead (CLA).

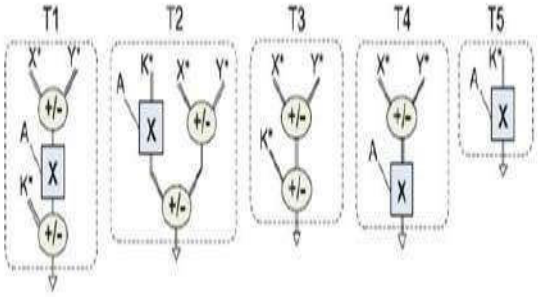

Fig 1:- Block of Combinational Templates

This templates can be used for equation such as (A+B) +C-D, we have just multiplication operation templates which can be used for equation such as (A.B), and for operation such as (A+B).(C+D) we should make use both the templates which hence results in complication and vast operation. So in order to avoid this we develop new architecture to develop the combination of templates with addition/subtraction and multiplication available in single template which makes the work easy by increasing the performance and reducing the delay and more makes the work simple.

The figure shows the modified templates with combination of addition and multiplication combination. The Modified booth is used to reduce the partial product by n/2 to make the multiplication operation with minimum number of partial product. In the already existing architecture of Booth we have adder for addition of inputs and then the output of it as Y is given to the MB section with a third input X for multiplication. Since the adder used separately for addition causes some amount of delay because of critical path delay. So in order to reduce this delay we develop a new architecture for this MB where we fuse the MB with Sum to get a new section known as SMB, where the inputs for addition is directly given to the

SMB and we get an output as Y to which we give a third input X to the SMB itself. So all the inputs are directly given to SMB, this reduces the critical path delay which was caused because of separate adder used. It shows the already existing MB and shows the Booth with new introduce architecture as SMB.

In the SMB we have three different schemes to the operations which mainly consists of adders such as full adder, half adder, conventional full adder as FA* and FA** and also conventional half adder as HA* and HA**. So in order to avoid this we develop new architecture to develop the combination of templates with addition/subtraction and multiplication available in single template which makes the work easy by increasing the performance and reducing the delay and more makes the work simple. Since the adder used separately for addition causes some amount of delay because of critical path delay. So in order to reduce this delay we develop a new architecture for this MB where we fuse the MB with Sum to get a new section known as SMB.

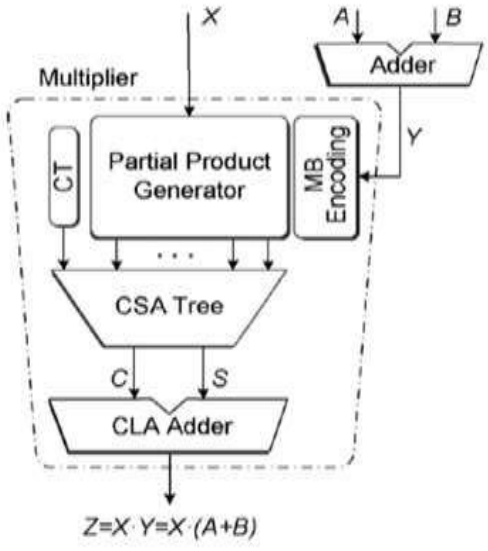

Fig 2 :- Block of existing Modified booth

As in this figure we can see an adder used for addition of two inputs A and B, which thus results in critical path delay at Y, so in order to reduce this we have a new architecture of SMB . Booth multiplication algorithm consists of three major steps as shown in the structure of booth algorithm figure that includes generation of partial product called as recoding, reducing the partial product in two rows, and addition that gives final product.

For a better understanding of modified booth algorithm & for multiplication, we must know about each block of booth algorithm for multiplication process. This modified booth multiplier is used to perform high-speed multiplications using modified booth algorithm.

This modified booth multiplier's computation time and the logarithm of the word length of operands are proportional to each other. We can reduce half the number of partial product. Radix-4 booth algorithm used here increases the speed of multiplier and reduces the area of multiplier circuit. In this algorithm, every second column is taken and multiplied by 0 or +1 or +2 or -1 or -2 instead of multiplying with 0 or 1 after shifting and adding of every column of the booth multiplier.

Thus, half of the partial product can be reduced using this booth algorithm. Based on the multiplier bits, the process of encoding the multiplicand is performed by radix-4 booth encoder. The composition of an array multiplier is, there is a one to one topological correspondence between this hardware structure and the manual multiplication . The generation of n partial products requires N*M two bit AND gates.

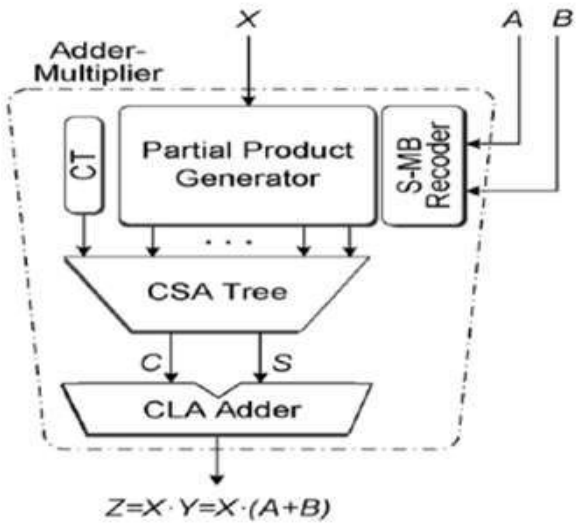

Fig 3:- Block of SMB

III. RADIX 4 BOOTH ALGORITHM

The steps given below represent the radix-4 booth algorithm:

a) Extend the sign bit 1 position if necessary to ensure that n is even.

b) Append a 0 to the right of the least significant bit of the booth multiplier.

c) According to the value of each vector, each partial product will be 0, +y, -y, +2y or -2y.

If we take the partial product as -2y, -y, 0, y, 2y then, we have to modify the general partial product generator.

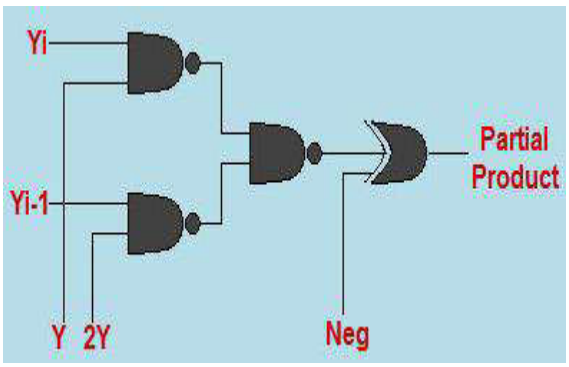

Fig 4:- Partial product generator

Now, every partial product point consists of two inputs (consecutive bits) from multiplicand and, based on the requirement, the output will be generated and its complements also generated in case if required. The 2's complement is taken for negative values of y. There are different types of adders such as conventional adders, ripple-carry adders, carry-look-ahead adders, and carry select adders. The carry select adders (CSLA) and carry-look-ahead adders are considered as fastest adders and are frequently used. The multiplication of y is done by after performing shift operation on y – that is – y is shifted to the left by one bit.

Hence, to design n-bit parallel multipliers only n2 partial products are generated by using booth algorithm. Thus, the propagation delay to run circuit, complexity of the circuit, and power consumption can be reduced.

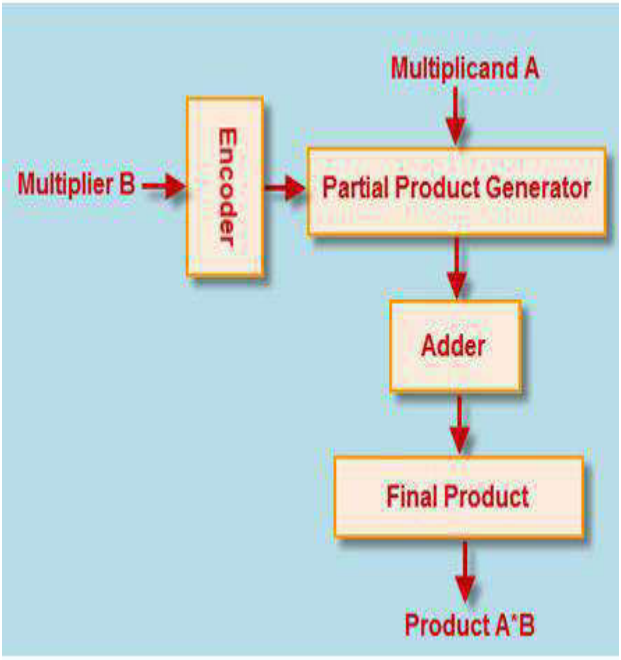

Fig 5: -Modified booth flow chart

Booth multiplication algorithm or Booth algorithm was named after the inventor Andrew Donald Booth. It can be defined as an algorithm or

method of multiplying binary numbers in two's complement notation. It is a simple method to multiply binary numbers in which multiplication is performed with repeated addition operations by following the booth algorithm.

Again this booth algorithm for multiplication operation is further modified and hence, named as modified booth algorithm. Booth's algorithm examines adjacent pairs of bits of the 'N'-bit multiplier Y in signed two's complement representation, including an implicit bit below the least significant bit, y−1 = 0. For each bit yi, for i running from 0 to N − 1, the bits yi and yi−1 are considered. Where these two bits are equal, the product accumulator P is left unchanged. Where yi = 0 and yi−1 = 1, the multiplicand times 2i is added to P; and where yi = 1 and yi−1 = 0, the multiplicand times 2i is subtracted from P. The final value of P is the signed product. The carry save arithmetic is variety of arithmetic-dominated circuits.

Carry save arithmetic occurs naturally in a variety of DSP applications, and further opportunities to exploit it can be exposed through systematic data flow transformations that can be applied by a hardware compiler. Field-programmable gate arrays (FPGAs), however, are not particularly well suited to carry-save arithmetic. To address this concern, we introduce the "field programmable counter array" (FPCA), an accelerator for carry-save arithmetic intended for integration into an FPGA as an alternative to DSP blocks.

In addition to multiplication and multiply accumulation, the FPCA can accelerate more general carry-save operations, such as multi-input addition (e.g., add integers) and multipliers that have been fused with other adders. Our experiments show that the FPCA accelerates a wide variety of applications than DSP blocks and improves performance, area utilization, and energy consumption compared with soft FPGA logic. The extension for the above project is Multiplier. Experimental results are seen by using Xilinx ISE .

Modern embedded systems target highend application domains requiring efficient implementations of computationally intensive digital signal processing (DSP) functions. The incorporation of heterogeneity through specialized hardware accelerators improves performance and reduces energy consumption . Although application-specific integrated circuits (ASICs) form the ideal acceleration solution in terms of performance and power, their inflexibility leads to increased silicon complexity, as multiple instantiated ASICs are needed to accelerate various kernels. Many researchers have proposed the use of domain specific coarse-grained reconfigurable accelerators in order to increase ASICs' flexibility without significantly compromising their performance.

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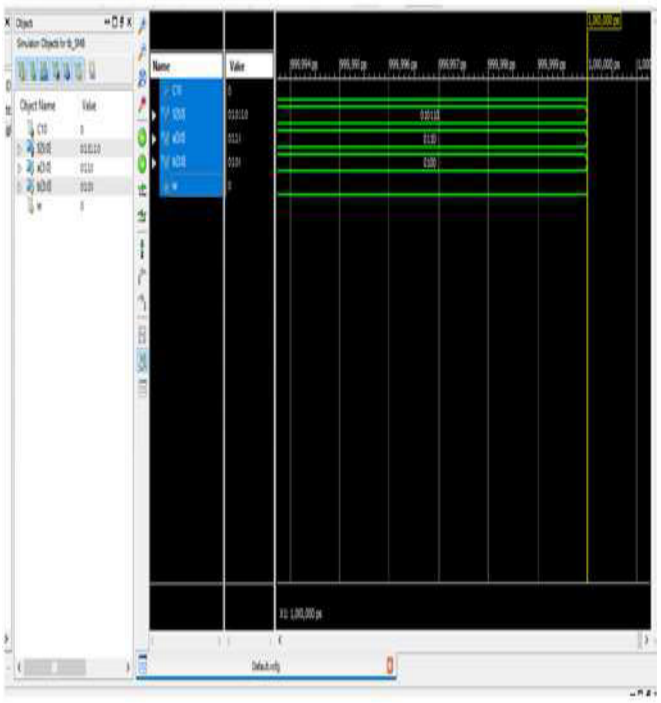

Fig 6:- SMB2 output for four bit numbers

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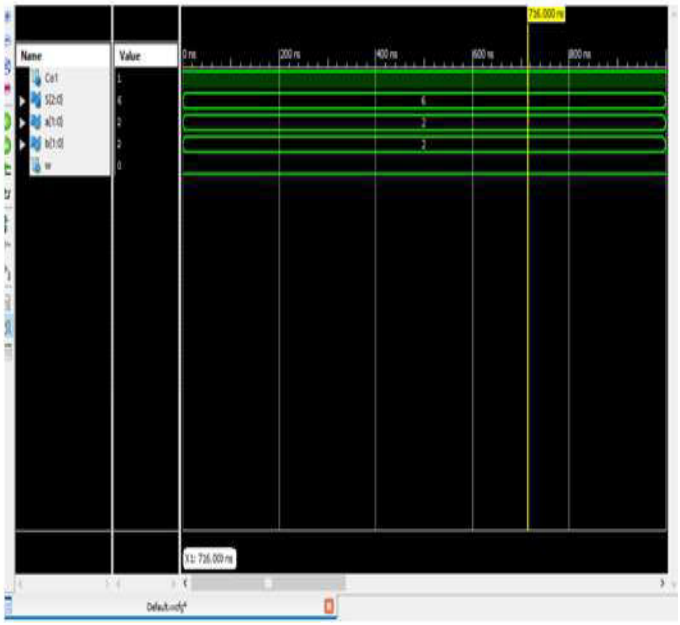

Fig 7: SMB2 output of two bit number in unsigned form

The area of a FA and a HA is 7 and 3 gate equivalents respectively. The delays of the sum and carry outputs of a FA are 4 and 3 gate equivalents respectively, while those of a HA are 2 and 1. The output of the SMB2 for a four bit number is shown in

figure 6 and 7 respectively further by this idea we can develop all the other two schemes and also check all the outputs. The output of the Modified booth section is also compared with the already existing booth and the result of the comparison is that we find less critical path delay and also increased performance in the modified booth with SMB schemes.

V. CONCLUSIONS

This paper focuses on developing an architecture to produce combinational templates which can do almost all the combinational operation available in DSP. We propose a technique for the direct recoding of the sum of two numbers to its MB form. We make use of alternative designs of the proposed S-MB recoder and use the SMB2 scheme in the MB. The proposed recoding schemes, when they are incorporated in FAM designs, yield considerable performance improvements in comparison with the most efficient recoding schemes. Thus this was a successful architecture to reduce the delay and increase the performance to make the modified booth more effective, and hence the overall performance of this architecture would be high with minimized delay.

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Keywords:- Digital Signal Processing (DSP)

I . INTRODUCTION

Digital Signal Processing normally consists of lots of addition, multiplication and subtraction operation for it different applications. The multiplication operation is a vast and time consuming process, which consists of partial products. Booth multipliers are used in the architecture to reduce the partial product since in DSP we have multiplication operations also, as in normal multiplication we have n partial products so by using booth multiplier we can reduce the partial product by n/2, which is also known as radix-4. Modern embedded systems target high-end application domains requiring efficient implementations of computationally intensive digital signal processing (DSP) functions. The incorporation of heterogeneity through specialized hardware accelerators improves performance and reduces energy consumption. Although application-specific integrated circuits (ASICs) form the ideal acceleration solution in terms of performance and power, their inflexibility leads to increased silicon complexity, as multiple instantiated ASICs are needed to accelerate various kernels

.

We propose a high-performance architectural scheme for the synthesis of flexible hardware DSP accelerators by combining optimization techniques from both the architecture and arithmetic levels of abstraction. We introduce a flexible datapath architecture that exploits CS optimized templates of chained operations. The proposed architecture comprises flexible computational units (FCUs), which enable the execution of a large set of operation templates found in DSP kernels. The proposed accelerator architecture delivers average gains of up to 61.91% in area-delay product and 54.43% in energy consumption compared to state-of-art flexible datapaths sustaining efficiency toward scaled technologies. The arithmetic optimizations at higher abstraction levels than the structural circuit one significantly impact on the datapath performance.

In timing-driven optimizations based on carry-save (CS) arithmetic were performed at the post-Register Transfer Level (RTL) design stage. In common sub expression elimination in CS computations is used to optimize linear DSP circuits. Developed transformation techniques on the application's DFG to maximize the use of CS arithmetic prior the actual datapath synthesis. The aforementioned CS optimization approaches target inflexible datapath, i.e., ASIC, implementations. CS representation has been widely used to design fast arithmetic circuits due to its inherent advantage of eliminating the large carry-propagation chains. CS arithmetic optimizations rearrange the application's DFG and reveal multiple input additive operations (i.e., chained additions in the initial DFG), which can be mapped onto CS compressors. The goal is to maximize the range that a CS computation is performed within the DFG.

II. TEMPLATES

The paper already existing templates consists of either full of addition operation or either multiplication, there was no combination of both multiplication and addition operation in a single template was available. So in this available templates it can only be used for either addition/subtraction and next template for multiplication, so if in DSP a combination of addition/subtraction and multiplication occurs, we have to make use of two template combination to

form that equation, which makes the work and operation complicated. The Booth recorder which is used to reduce or minimize the partial product consists of SMB section for addition of the inputs and then to the output of the same the third input as X is given for multiplication. The CSA is the arithmetic used to do the multiplication process, the main advantage of CSA is that is reduces the carry and the final block used is Carry Look Ahead (CLA).

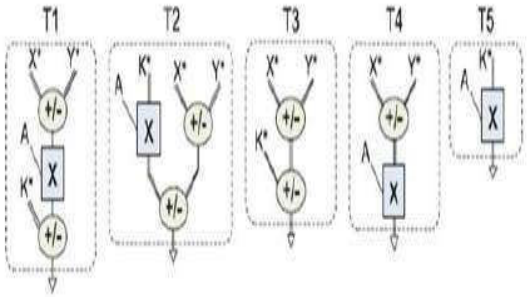

Fig 1:- Block of Combinational Templates

This templates can be used for equation such as (A+B) +C-D, we have just multiplication operation templates which can be used for equation such as (A.B), and for operation such as (A+B).(C+D) we should make use both the templates which hence results in complication and vast operation. So in order to avoid this we develop new architecture to develop the combination of templates with addition/subtraction and multiplication available in single template which makes the work easy by increasing the performance and reducing the delay and more makes the work simple.

The figure shows the modified templates with combination of addition and multiplication combination. The Modified booth is used to reduce the partial product by n/2 to make the multiplication operation with minimum number of partial product. In the already existing architecture of Booth we have adder for addition of inputs and then the output of it as Y is given to the MB section with a third input X for multiplication. Since the adder used separately for addition causes some amount of delay because of critical path delay. So in order to reduce this delay we develop a new architecture for this MB where we fuse the MB with Sum to get a new section known as SMB, where the inputs for addition is directly given to the SMB and we get an output as Y to which we give a third input X to the SMB itself. So all the inputs are directly given to SMB, this reduces the critical path delay which was caused because of separate adder used. It shows the already existing MB and shows the Booth with new introduce architecture as SMB.

In the SMB we have three different schemes to the operations which mainly consists of adders such as full adder, half adder, conventional full adder as FA* and FA** and also conventional half adder as HA* and HA**. So in order to avoid this we develop new architecture to develop the combination of templates with addition/subtraction and multiplication available in single template which makes the work easy by increasing the performance and reducing the delay and more makes the work simple. Since the adder used separately for addition causes some amount of delay because of critical path delay. So in order to reduce this delay we develop a new architecture for this MB where we fuse the MB with Sum to get a new section known as SMB.

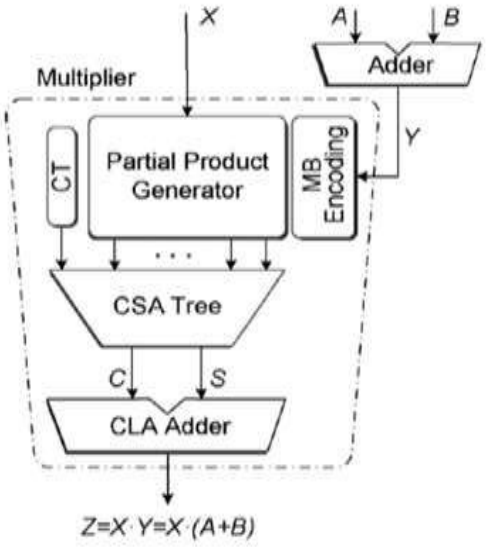

Fig 2 :- Block of existing Modified booth

As in this figure we can see an adder used for addition of two inputs A and B, which thus results in critical path delay at Y, so in order to reduce this we have a new architecture of SMB . Booth multiplication algorithm consists of three major steps as shown in the structure of booth algorithm figure that includes generation of partial product called as recoding, reducing the partial product in two rows, and addition that gives final product.

For a better understanding of modified booth algorithm & for multiplication, we must know about each block of booth algorithm for multiplication process. This modified booth multiplier is used to perform high-speed multiplications using modified booth algorithm.

This modified booth multiplier's computation time and the logarithm of the word length of operands are proportional to each other. We can reduce half the number of partial product. Radix-4 booth algorithm used here increases the speed of multiplier and reduces the area of multiplier circuit. In this algorithm, every second column is taken and multiplied by 0 or +1 or +2 or -1 or -2 instead of multiplying with 0 or 1 after shifting and adding of every column of the booth multiplier.

Thus, half of the partial product can be reduced using this booth algorithm. Based on the multiplier bits, the process of encoding the multiplicand is performed by radix-4 booth encoder. The composition of an array multiplier is, there is a one to one topological correspondence between this hardware structure and the manual multiplication . The generation of n partial products requires N*M two bit AND gates.

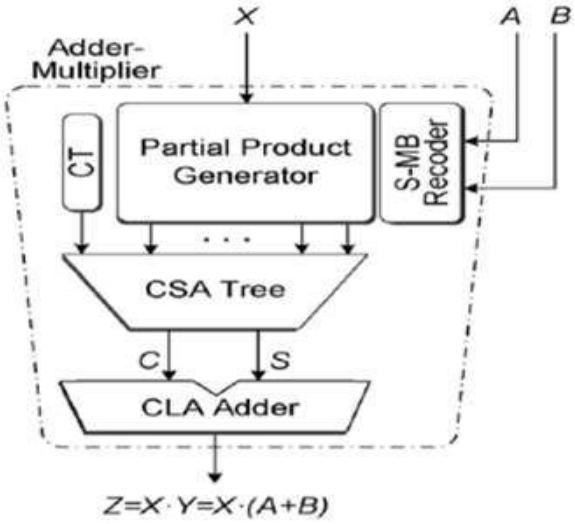

Fig 3:- Block of SMB

III. RADIX 4 BOOTH ALGORITHM

The steps given below represent the radix-4 booth algorithm:

d) Extend the sign bit 1 position if necessary to ensure that n is even.

e) Append a 0 to the right of the least significant bit of the booth multiplier.

f) According to the value of each vector, each partial product will be 0, +y, -y, +2y or -2y.

If we take the partial product as -2y, -y, 0, y, 2y then, we have to modify the general partial product generator.

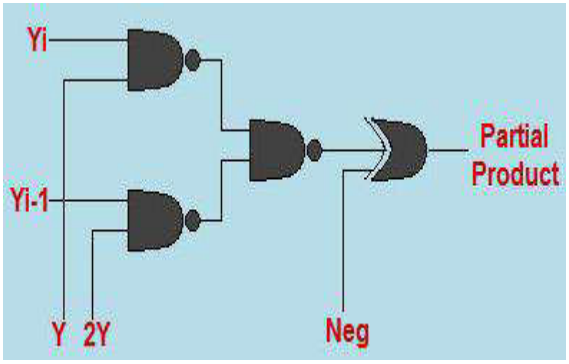

Fig 4:- Partial product generator

Now, every partial product point consists of two inputs (consecutive bits) from multiplicand and, based on the requirement, the output will be generated and its complements also generated in case if required. The 2's complement is taken for negative values of y. There are different types of adders such as conventional adders, ripple-carry adders, carry-look-ahead adders, and carry select adders. The carry select adders (CSLA) and carry-look-ahead adders are considered as fastest adders and are frequently used. The multiplication of y is done by after performing shift operation on y – that is – y is shifted to the left by one bit.

Hence, to design n-bit parallel multipliers only n2 partial products are generated by using booth algorithm. Thus, the propagation delay to run circuit, complexity of the circuit, and power consumption can be reduced.

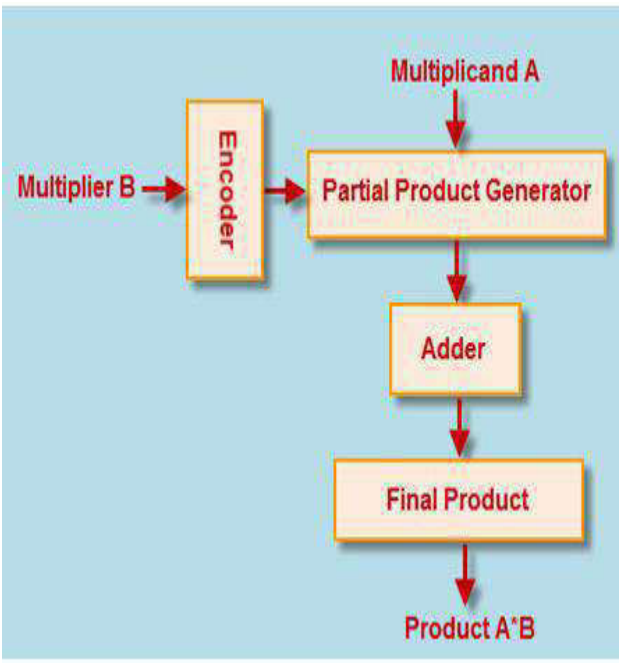

Fig 5: -Modified booth flow chart

Booth multiplication algorithm or Booth algorithm was named after the inventor Andrew Donald Booth. It can be defined as an algorithm or method of multiplying binary numbers in two's complement notation. It is a simple method to multiply binary numbers in which multiplication is performed with repeated addition operations by following the booth algorithm.

Again this booth algorithm for multiplication operation is further modified and hence, named as modified booth algorithm. Booth's algorithm examines adjacent pairs of bits of the 'N'-bit multiplier Y in signed two's complement representation, including an implicit bit below the least significant bit, $y_{-1} = 0$. For each bit y_i, for i running from 0 to N − 1, the bits y_i and y_{i-1} are considered. Where these two bits are equal, the product accumulator P is left unchanged. Where $y_i = 0$ and $y_{i-1} = 1$, the multiplicand times 2^i is added to P; and where $y_i = 1$ and $y_{i-1} = 0$, the multiplicand times 2^i is subtracted from P. The final value of P is the signed product. The carry

save arithmetic is variety of arithmetic-dominated circuits.

Carry save arithmetic occurs naturally in a variety of DSP applications, and further opportunities to exploit it can be exposed through systematic data flow transformations that can be applied by a hardware compiler. Field-programmable gate arrays (FPGAs), however, are not particularly well suited to carry-save arithmetic. To address this concern, we introduce the "field programmable counter array" (FPCA), an accelerator for carry-save arithmetic intended for integration into an FPGA as an alternative to DSP blocks.

In addition to multiplication and multiply accumulation, the FPCA can accelerate more general carry-save operations, such as multi-input addition (e.g., add integers) and multipliers that have been fused with other adders. Our experiments show that the FPCA accelerates a wide variety of applications than DSP blocks and improves performance, area utilization, and energy consumption compared with soft FPGA logic. The extension for the above project is Multiplier. Experimental results are seen by using Xilinx ISE .

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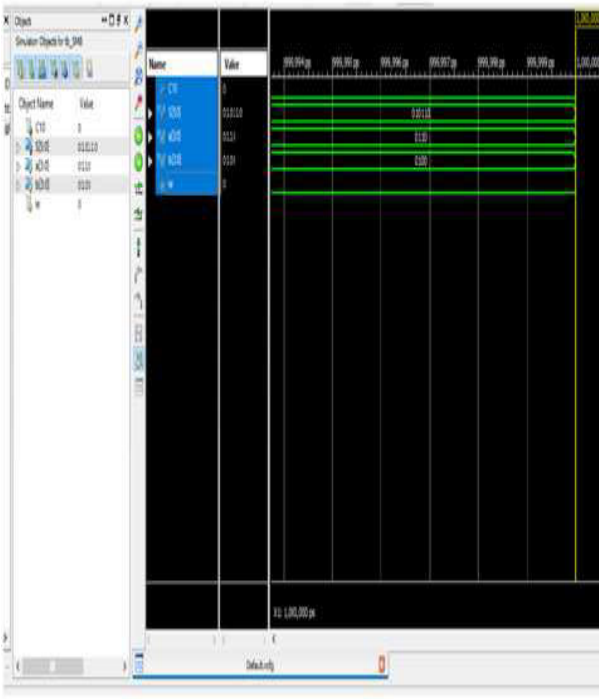

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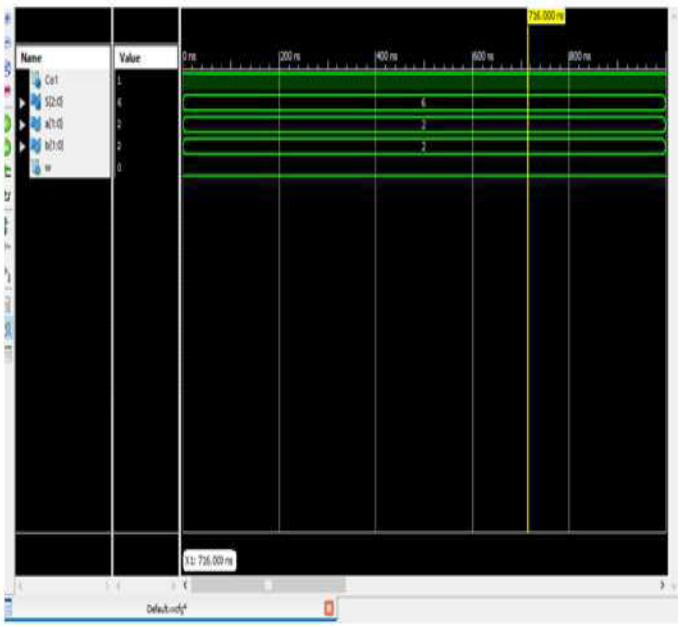

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AN EFFICIENT APPROXIMATE RECONFIGURABLE ADDER USING SIMPLE CARRY PREDICTION

J.B.Abisha Jey[1], S.Amutha[2]
PG Scholar, Assistant Professor, ECE, Marthandam College of Engineering and Technology, Kuttakuzhi.

ABSTRACT:

With the advent of rapidly increasing adder configuration to precise the adders and power consumption for accurate result. An appropriate computing is a difficult approach for the IC design in low power process. To overcome certain drawbacks the reconfigurable adders is developed. However this design reduces the large area, nearly 39%. We modify the simple accuracy configurable adder design that reduces the error and it is helpful for the error correction. In this paper the proposed simple accuracy configurable adder is used to get accurate accuracy levels. This implementation reduces the complexity to reduce the dynamic level of approximation. Appropriate adder achieves efficient energy system design. In this technique the speed of the system is increased to receive the predicted data quickly. Compared to configurable adder this adders are more efficient and reconfigurable. The MSB value prediction is predicted easily by the reconfigurable adder design. Computing is a recently used process to get research attention. However the system reduce the large area overhead, as they predict the carry and redundant computing. The technique used in this paper is simple accuracy configurable adder to improve the accuracy-power-delay.

Keywords: Error detection. Critical path delay, delay adaptive, accurate mode, rectified, truncation error.

I.INTRODUCTION:

Appropriate computing is a growing technology that has been recently modified design [1]. Low power technology has already launched concept based on the power methodologies. Appropriate computing that enable efficient hardware and software implementation and used in variety of application such as audio, video processing, etc. This technique improves the performance, error correction and error detection if possible by using this process.

The paradigm of appropriate computing fully concentrated on arithmetic logic circuit which enhances and activate as a building blocks for computing circuit design. This process has established modified potential in appropriate computing. Several adders have been developed in the reconfigurable design. Such design gains 60% power reduction for DCT(Discrete Cosine Transform) computation without changing the images in the appropriate circuit. In normal realistic case accuracy requirement vary for different applications in audio, video and mobile computing. Power modes may vary based upon the accuracy. In addition to the SARA (Simple Accuracy Reconfigurable Adder) technique the errors can be eliminated. The important concept designed behind the technique is that accuracy can be adjusted using the methods such as dynamic voltage and frequency scaling to retain the accurate accuracy power tradeoff. The benefit of this accuracy modification method enhances to reduce the delay and area, where errors occur at the critical path associated with the significant bit.

In early decades appropriate computing cannot be done efficiently and accurately, but the recent techniques enhances appropriate accuracy in computing [1]. By using the design of simple accuracy configurable adder the error detection and correction in the circuit is possible. [2]Dynamic levels of approximation is used to reduce the area and thereby to improve the accuracy by the adder circuit. The baseline of the reconfigurable adder contains the significant redundancy and the error correction/detection circuit moreover increases area overhead. In past few, accuracy configurable adder design has been developed. The error correction value is predicted from the least significant bit and the accuracy improves to enroll the required configuration. To overcome the drawback and to achieve actual accuracy level the error correction circuit uses the reconfigurable adder design.

Few works that establish to focus on appropriate computing in the VLSI design. In this paper the fast reconfigurable adder design is proposed. As longer the error correction/detection can be predicted in simple way. In addition this method support for the degradation process. The reconfigurable adder design composed of CRA (Carry Ripple Adder) and CLA (Carry Lookahead Adder) for extra prediction. So that quite large area is degraded into smaller area.

II.SYSTEM STRUCTURE:

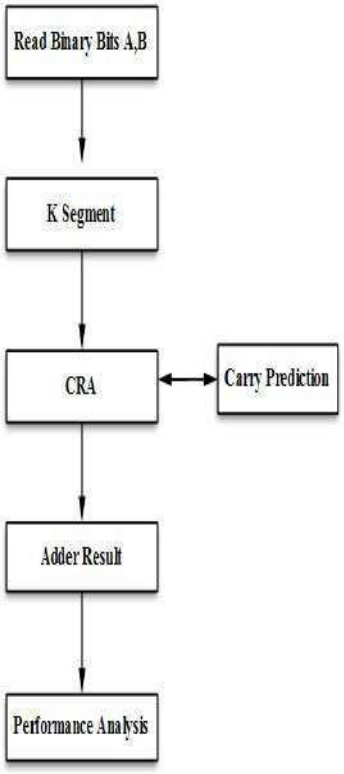

Figure1: System Structure

In this system structure, binary data bit "A" and "B", operates on two operands and the data is loaded using a gate level schematic of the reconfigurable adder. It is composed of a 'k', segments by which the k segment separate the binary bits .In the carry ripple adder the bit is propagated and it computes the sum and carry. Meanwhile the carry prediction circuit predicts the optimal approximation values. A new method simple accuracy reconfigurable adder is designed to stimulate the adder result. Finally the area, power delayed can be analyzed by the performance analysis.

III. MODULES OF PROPOSED TECHNIQUE:

1. Carry Ripple Adder:

Carry Ripple Adder is a extra configurable carry prediction circuitry, similar as the carry look-ahead part of CLA (Carry Look-ahead Adder). Adders are CRA designs while the carry-prediction circuit is similar to the carry look-ahead part of CLA. Further, its carry prediction can be configured to different accuracy levels. However, the complicated carry prediction induces large area overhead. The RAP-CLA scheme uses CLA for its baseline where the carry-ahead of each bit is computed directly from the addends of all of its lower bits. Its carry prediction reuses a part of the look-ahead circuit rather than building extra dedicated prediction circuitry, and hence is more area-efficient than GDA. Its carry prediction also reuses part of the sub-adders rather than having dedicated prediction circuitry.

A ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascaded, with the

carry output from each full adder connected to the carry input of the next full adder in the chain. In the ripple carry adder, the output is known after the carry generated by the previous stage. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay. All gates are equally loaded for simplicity. All delays are normalized relative to the delay of a simple inverter.

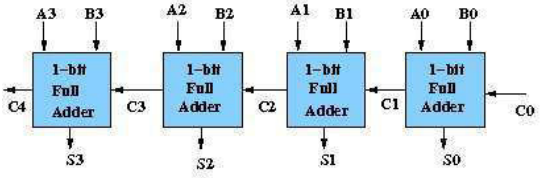

Figure2: Carry Ripple adder

2. Carry Prediction:

Prediction methods initialize with an accurate adder and use carry prediction for optional approximation. As such, they no longer need error detection/correction and do not incur any data stall. In addition, they intrinsically support graceful degradation. A new carry-prediction-based accuracy configurable adder design SARA (Simple Accuracy Reconfigurable Adder) is introduced. It is a simple design with significantly less area than CLA, and it has not been achieved in the past in accuracy configurable adders.

3. Configurable Adders:

We review a few representative works on accuracy configurable adder design and show the relation with our method. These designs can be generally categorized into two groups: error-correction-based configurations and carry prediction-based configurations.

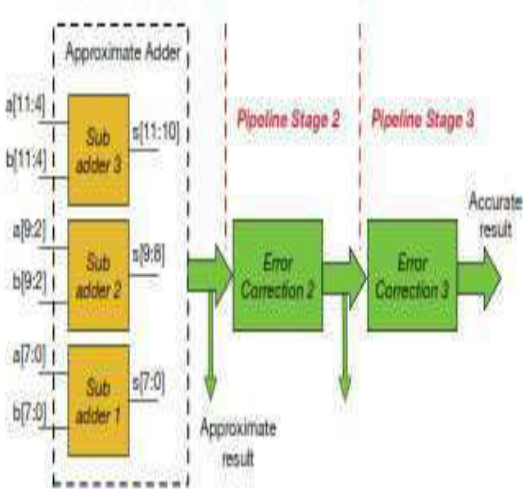

Figure3:Error-correction-based configurable adder.

The main idea of an error-correction-based approach is shown in Figure. The scheme starts with an approximate adder (the dashed box), where the carry chain is shortened by using separated sub-adders with truncated carry-in. In order to reduce

the truncation error, the bit-width in some sub-adders contains redundancy. For example, subadder2 calculates the sum for only bit 8 and 9, but it is an 8-bit adder using bit [9:2] of the addends, 6 bits of which are redundant. Even with the redundancy, there is still residual error which is detected and corrected by additional circuits. In Figure, the errors of sub-adder2 must be corrected by error-correction2 before the errors of sub-adder3 are rectified by error-correction3. As such, the configuration progression always starts with small accuracy improvements. The redundancancy and error detection/correction reduces large area overhead. Since the error correction circuits are usually pipelined, an accurate computation may take multiple clock cycles and could stall entire data path, depending on the addend values.

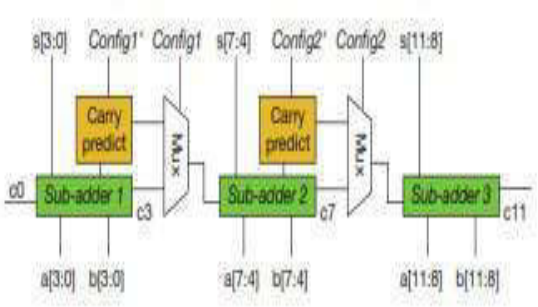

Figure4:Carry-prediction-based configurable adder.

The framework of carry-prediction-based methods shown in Figure. These schemes start with an accurate adder design, which is formed by chaining a set of sub adders. Each sub-adder comes with a fast but approximated carry prediction circuit. By selecting between the carry-out from sub-adder or carry prediction, the overall accuracy can be configured to different levels. Such an approach does not need error detection/correction circuitry. Moreover, the configuration of higher bits is independent of lower bits. This leads to fast convergence or graceful degradation in the progression of configurations. In GDA, the sub-adders in CRA designs by which the carry-prediction circuit is similar to the carry look-ahead part of CLA. Further, its carry prediction can be configured to different accuracy levels. However, the complicated carry prediction induces large area overhead. The RAP-CLA scheme uses CLA for its baseline where the carry-ahead of each bit is computed directly from the addends of all of its lower bits. Its carry prediction reuses a part of the look-ahead circuit rather than building extra dedicated prediction circuitry, and hence is more area-efficient than GDA. However, its baseline is much more expensive than GDA.

IV.RESULTS AND DISCUSSION:

Simple Carry Prediction Approximate Adder is a predicted carry look ahead adder, coupled between a lower order adder and a higher order adder. In simple carry Prediction adder , the adder inputs are 7133 and 1244 and the output is 8377.

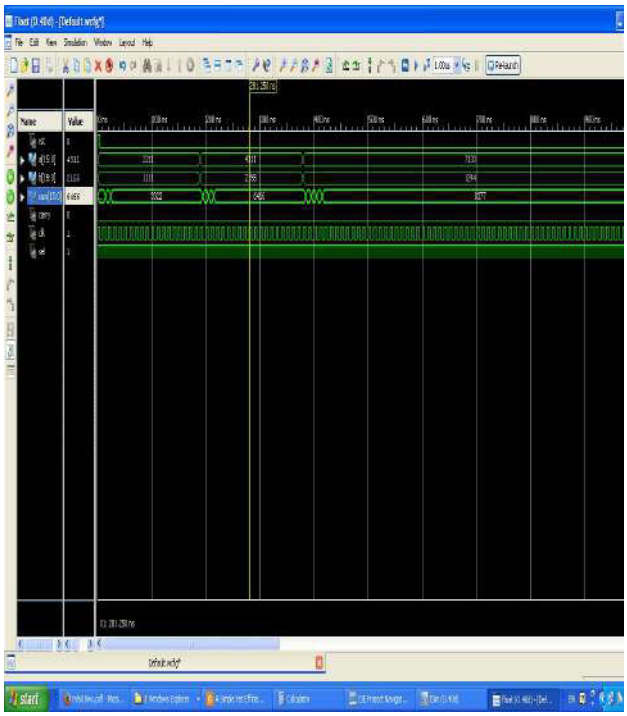

Figure5: Simulation output for Simple Carry Prediction Approximate Adder

Timing Summary:

- Speed Grade: -3
- Minimum period: 1.473ns (Maximum Frequency: 678.771MHz)
- Minimum input arrival time before clock: 4.574ns
- Maximum output required time after clock: 4.382ns
- Maximum combinational path delay: 6.056ns

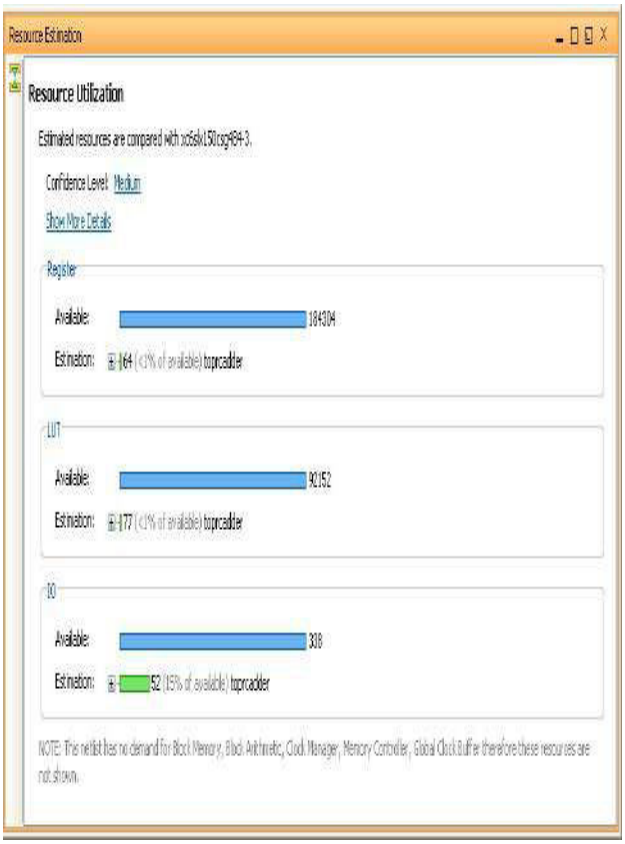

Figure6:Resource Prediction from Xilinx Synthesizer

For Resource Utilization used both Register and LUT to savings in terms of processing time and retrieving a value from memory is often small amount of fast storage, although some registers have specific hardware functions, and may be read-only or write-only.

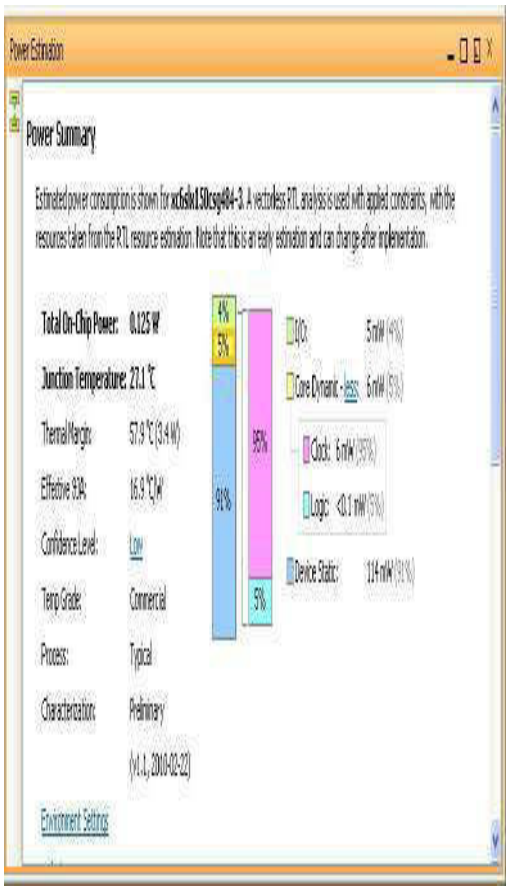

Figure7: Power Estimation from Xilinx Synthesizer

Power summary have both static and dynamic power. Also the power dissipation is estimated by Synopsys PrimeTime considering, including both static and dynamic power. The power-delay tradeoff can be obtained by different accuracy configurations or varying supply voltages.

4 Comparative Analysis of Parameters

The comparison here involves the performance of the parameters discussed so far.Table1 represents Area (%) obtained from different method discussed.

Table : Analysis of Delay, Area and Power

S. No.	Delay (ns)	Power (mw)	Energy (pJ)	Area(No. of.LUTs)
1	13.073	29	379.12	28
2	12.451	27	336.18	28
3	13.691	27	369.66	59
4	14.380	30	431.40	39

V.CONCLUSION:

A simple accuracy reconfigurable adder (SARA) design is proposed. It has an reconfigurable adder that reduces the delay and power. The proposed method has significant low power delay product than the previous work. At the same time accuracy level is somewhat improved. Further optimization of the proposed also done which improves the accuracy. In addition simple accuracy reconfigurable adder has considered lower area. The most important aspect of this proposed method is that maintaining the accuracy. The accuracy-power-delay efficiency is further improved by a delay-adaptive reconfigurable technique.

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Efficient overburden CDMA for NoC

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***Abstract*--On-chip interconnect networks causes congestion which affects the performance in current system-on-chips. Code division multiple access (CDMA) has rigid delay, trimmed intervention expense and superior transfer capacity. Because of this features, it's been projected for On-Chip crossbars. In CDMA, the standard division is facilitated in the secret language bit by appointing a bounded quantity of unrelated scattering codes of N chip range to the processing elements distributing the link. In the existing work overburden CDMA communicate (OCI) to improve the aptitude of CDMA situated NoC (network-on-chip) crossbars by escalating the adding up to of good dispersion codes. In this paper, the normal adder is replaced with Han Carlson Adder (HCA) in OCI Crossbar to achieve high-speed parallel addition, reduction in power and area. High-speed operation in T-OCI, P-OCI circuitry by implementing HCA at the time of addition. Analogized with the existing OCI on a Cyclone-2 FPGA kit, the serial OCI attains greater transmission capacity, 30% less resource consumption, 25% power retaining and less delay, while the parallel OCI Crossbar attains N times greater transmission capacity.**

Index Terms : CDMA interconnect, NoC, Overburden CDMA Crossbar, Han Carlson Adder

I. INTRODUCTION

"On-chip" connections overwhelmingly contact impressive gross region, execution, along with the authority confirmation of current facilitated circuits like 'system on-chips' (SoCs). Ever escalating the message on high deteriorates the snap up reached by counterpart evaluating as claimed by Amdahl's act [1]. Consequently, on the increase productive eminent pursuance integrated links plays a major role in assessing technical applications. On-chip networks are the on the whole ascendible link pattern that is apt for addressing a mixture of submission requests and greet uncommon operation parameters [15]. In NoCs, information is treated as packets, at one time as on-chip processing essentials (PEs) are careful as complex nodes consistent by switches and routers. On chip networks grant an adaptable result for great on-chip systems, but they show enlarged faculty eating and significant source overheads [7].

For enabling the concurrent channel access here we use a different medium dispensing skill called Code-division manifold access (CDMA) In CDMA method, every one transmit-receive (TX-RX), two of a kind, is assigned an only one of its kind bipolar scattering secret language and facts drape from every part of transmitters are added in a preservative reporting link. In conventional CDMA spreading codes are an orthogonal and the orthogonal codes cross-correlation results nil and that makes the collector in CDMA to the right to figure out the obtained added value from a correspondent decoder. In CDMA systems medium dispensing is done by the Walsh-Hadamard orthogonal codes. CDMA advanced as an on-chip be integrated distribution procedure for in cooperation automobile and NoC interconnect architectures [11]. Lots of return of via CDMA for on-chip interconnects rope in abridged brawn exhaustion, fixed interaction remission, and abridged structure complication [12]. Comparing with other technologies CDMA switch has low wiring problem and overhead. Overburden CDMA is one of the popular access method spread out in wireless media, someplace the various user distributions the contact means is elevated by greater than ever the add up to of usable dispersion codes with the cost of greater than ever 'MAI' (multiple access interference) [13]. Theory of overburden CDMA is able to be practical to on-chip interlinks which improves the interlock ability [15].

Adders are deep essentials in calculation operations. Dual adders are utilized as a position of a digital route for addition, multiplication operations and for hovering aim multiplication and division. For that reason, adders are supporting gears and civilizing their show is one of the key provocation in digital designs. Computer reckoning algorithm has traditional drop bounds on a region and lingers of n-chip additions, effective earlier changes straightforward with the summation area, and its terminal possessed with an $O(\log_2 n)$nature.

This paper described in six sections, The On-chip CDMA interconnects and Han Carlson adder related work given in II. Preliminaries regarding overburden CDMA in cellular media, conventional CDMA Crossbar switch, code design for OCI, parallel and serial OCI designs and components described in Section III. Han Carlson Adder in Section IV. Results and comparative analysis in Section V. Conclusion in Section VI.

II. RELATED WORK

Utilizing CDMA is like an avenue contact plan in crossbar switches gives propitious features like the set undertaking delay and upward in depths negotiation. The scalable CDMA-based outermost channel to lower the equivalent assigning position and point-to-point(PTP) links along with escape elevated TDMA controller [17]. The indicated method decreases join deem once second-hand at the linking of many surroundings to numerous PEs because the numbers from the surroundings are joined and dispatched on smaller number lines. The encourage in the undertaking delay awaited to facts expanding is customary for the reason that peripherals habitually drive at lesser iterations over control processing elements(PE). A new CDMA channel operation and a TDMA come apart transaction channel are analogized in [11]. A CDMA situated NoC and a PTP bidirectional ring situated NoC are compared in [21], and the difference exhibits the CDMA NoC's preset numbers passing on latency is parallel to the most excellent justification delay of the PTP constant duct width. The rigid figures handing over remission of the CDMA situated NoC is attributed to concomitant be integrated allocation by the association nodes. A stratified CDMA situated star NoC and the CDMA router linking done in star to star along with a star to mesh topologies and analyzed in terms of fair network large hierarchy topologies in [22], [23].

For a 2-D on-chip network this CDMA situated multicast exchange is employed in [24]. Because of code space multiplexing, The CDMA situated exchange agrees parallel data communication. The multicasting hop count decreased by this method and it agrees the target PEs made by packets concurrently, that is favored for practical uses. A CDMA of 14 node set-up has shown in [25]. The Tx-Rx duo is set by the spreading codes is effective depend on the call from every node. Two building blocks are proposed in this CDMA situated network, they are namely serial and parallel CDMA networks. The CDMA takes every data in spreading code is given to one-time period in the serial network where all the data is given that same clock period in the parallel network. The CDMA situated parallel and serial networks possess been analogized with a classical CDMA, TDMA bus and a net placed NoC. The uniform CDMA's bandwidth is greater to net placed NoC's throughput for the consistent network area due to concurrent behavior of CDMA [15].

There are quantity of adder architectures are available, the counterpart affix architectures of adder circuits bear meeting place stand straight to the drive too fast by that effective yield is gained. The time O(log n) gives the n-bit information total [26]. The foundation for parallelism with move give impression of being prematurely accumulation technique done by two people namely Weinberger along with Smith. The base of parallel prefix adders that the calculation done in prefixes are regarded towards regularity and it performed in parallel, this is established by P.M. Kogge along with H.S Stone.

III. PRELIMINARIES

This section discusses, in wireless media, the role of this overburden CDMA, the conventional CDMA Crossbar switch are presented [17]. The code structure for OCI, building blocks of OCI in serial along with parallel manner are described.

A. Overburden CDMA role in wireless transmissions

DSSS-CDMA is the foremost loom as average allocation of radio communications someplace a settle of opposite scattering codes poised of an issue of chips in segment N are accumulated by the sent message bits just as all information morsel is unfolded in N time periods. An only one of its kind scattering convention is given to each Tx-Rx two of a kind division the transfer channel. Information flows of user's allocation the bus are multiple and concurrently sent to the addition medium link. Despreading is obtained by giving the correlation business to the gained sum, anywhere all accepter knows how to obtain its facts by doing correlation with the allotted diffusion code. Orthogonal nature among the distribution codes bonds exceptional finding of each programming expected in the avenue addition by utilizing the associative and distributive conventions of the tallying sum procedure accepted by the transmission bus. In radio transmissions, true locations of the standard addition are affected due to indiscriminate properties increases, namely multipath, fading, noise and which also causes for getting the more error in bits(BER) of received information. In an unfavorable, in the scattering convention array, amount of unrelated codes is customarily narrow to the scattering secret language time taken by N, which decrease the network exploitation ability. In wireless media novel, introduction of Overburden CDMA to expansion in the quantity of scattering codes aside summing non-orthogonal codes which perhaps spotted at accepter part[13]. Escalating the bus consumption advance at overhead of lighten the orthogonal nature necessities of the unroll codes and escalating MAI and this gives hike in BER.

In wireless media, this projected overburden CDMA's spreading bits are guided with intricate acceptor designs wear and tear of multiuser detection as a replacement for of the easy matched filter or correlator accepter employed in plain direct sequence spread spectrum code division multiple access. Here, the CDMA situated NoC ability increased by applying this overburden CDMA approach in wireless media [15].

B. Classical CDMA Crossbar Switch

The router's material layer which is based on the conventional CDMA conferred in [17]. The switch is made up of a quantity of XOR encoders, a physical link addition circuitry and decoders which are situated on the accumulator. For encoding, Walsh scattering code set produces the binary symmetric code of length N, is encoded with the conveyed message data bit and forwarded out in serial manner. It tells that a 1-bit enlargement done in a span of N time periods. Accordingly, the frequency f_t of the crossbar affairs and managing clock frequency f_c , both denoted as $f_t = f_c/N$

For Walsh scattering codes, the number of transmitter(TX) and receiver(RX) ports taking CDMA switch equal to the M = N–1. Crossbar sharing done in serially by the all transmitted PEs and they are summed, the sum sent to the decoder part of the circuit filling the Rx ports. The binary signaling and encoding has great execution, responsibility, and its intrinsic inherent carry by digital policies, this is reason for using it to implement the bus addition over the multilevel signaling. The message bits through the CDMA crossbar exchange is in terms of equation:

$$S(i) = \sum_{j=1}^{M} d(j) \oplus C_o(j,i) \tag{1}$$

Here, m bit digital value is S(i) produces bus total in the duration of i*th* time period. the width of crossbar m =[log2 M], message bits d*(j)* is from the j*th* encoder, $\oplus$ gives XOR behavior and $C_0(j,i)$ gives i*th* part of j*th* symmetric scattering code. The addition circuitry in conventional CDMA crossbar with inputs M = N−1 bits along with m = $\log_2$N = [log2 M] yield information.

The correlator decoder understands by the two accumulators. As demonstrated by the dispensed CDMA code, zero accumulator gets obtained total when the existing chip denomination is '0' and one accumulator gets the sum when the denomination is '1'. This is practically identical towards magnifying crossbar total with ±1. The CDMA sum along with crossbar total for the different spreading code logical conditions are shown in [15]. Differentiating the two accumulators particularly shows the encoded data; if the data of zero accumulator is greater when its compared with 1 accumulator, then the issued message bit is '1', otherwise bit is '0'. Hence, the association action able to choose the encoded message with null faults in view of dismissing subjective effects. The magnification situated correlator is replaced with a inclusion situated one, this is the prime choice of accumulator decoder.

C. Overburden CDMA interconnect

Because of focus overloading the main difference among the overloaded and conventional CMDA network device is M>N-1. Network interfaces are attached by each PE which transmits and obtain NI Modules. While packet sending from each PE, to store in transmit NI Queue every single packet splits into flow control digits. The arbiter chooses M gaining flow control digits from leading NI Queue and sent at the time present activity. To avoid disputes, elected flow control digits need to have dedicated target address, as stated by router's priority plan gainer from two disputing flow control digits is elected. Employed prime plan is the stable gainer that hold of all prime plans; only one sender and receiver will be provided with a spreading code, is accepted as true to begin the encoding. As soon as it is done, the network device(router) allocates CDMA codes to every NI transmit and NI receive. NI's having void queue's or dispute destinations are allocated with all zero CMDA codes so they will not give a contribution to MAI to CDMA channel total. At a later, in encoder part, Flow control digits from every single NI are divided by CDMA Codes. N chips of Information is divided, and N is length of CDMA that is same as amount of time period mono crossbar activity. All decoders will receive a sum sequentially which is the addition of smear information chips from every encoder by CDMA cross bar adder. Using counter, decoding or encoding procedure continues till "N" frequencies occurs at same time [15].

a. Top-level design of OCI Crossbar

Primary goal of the active manuscript is growing quantity of storage elements by distributing typical CDMA cross bar, throughout the time preserving the density of the theory consistently by means of uncomplicated encoding design and depending on the decoder which is situated on accumulator having nominal differences. To reach this objective, a few alterations to the typical CDMA cross bar are ahead in position. For single bit interdependence, Figure. 1 characterizes the esteemed design of OCI cross bar. The unchanged architecture is imitated for a multi-bit CDMA switch. The CDMA switch split by transmitter-receiver ports of length M, that uses computational twofold addition circuitry having M bit information sources and yield is m-bit, which shows m =$\log_2$M for adding spreading message from the Tx ports. The mentioned and duct designs take the advantage of adder. For facilitating the message spreading and dispreading, encoder and decoder envelope coupled by all PEs. The cryptogram task along with intervention undertakings take usage of controller stall. The XOR operation is used for unrelated dissipating codes and an AND operation is used for related(non-orthogonal) dissemination codes. The operation of AND as pursues, if the Rx message bit is '0', it assigns the bunch of

zeros for the complete dissemination period, here MAI(multiple access interface) on bus will not occur; if the Rx message bit is '1', then the encoder assigns an related dispersal code. Along these lines, being the encoder is AND, the developed MAI dissemination cod e gives its value '1'or '0'. The regular CDMA crossbar's XOR encoder is not used for OCI encoding due to supplements of dispersal codes, thus the MAI caused by XOR gates for both one and zero. For both unrelated and related widening, an amalgam encoder introduced and its with XOR, AND gates, along with mux as depicted in fig.1. The execution of related along with related information by dual decoder models.

b. Code structure for OCI

The family of Walsh–Hadamard dissipating codes highlighted peculiarity which empowers CDMA to be coordinated over-burdening. The contrast between any continuous course wholes of information advance with related widening bits to the different quantity of transmitter and receiver set is constant, i.e. M, careless dispersal information. These home incomes that for the N−1 TX-RX sets utilizing affective Walsh unrelated bits, particular may encode extra N−1 fact codes in back to back contrasts among the N length chips making unrelated code. By the use of this rule facilitate 100% adding of related dispersal codes, that makes efficient classical CDMA crossbar. In this way, in non-orthogonal encoder, message for transmission is '1' an all alone appropriation piece at an individual vacancy in the spreading stage is extra to the lead aggregate, which causes the continuous expansion change to go amiss. The non-orthogonal codes pretend to be the TDMA flagging arrangement as both cryptogram is made out of a particular sign of "1"sent in an express schedule opening. The encoding or decoding plot offered in this address give a novel think about that empowers concurrence among code and time division multiple access motions for the_steady joint channel. In this way, the private encoder is known as TDMA overburden on OCI (T-OCI). An encoding/deciphering case of dual TDMA Overburden CDMA Interlink bits to diffusing arrangement guidelines length of N=8 is demonstrated in fig.2. A different quantity of unrelated codes ought to be utilized all the while to diversion save the dimension difference material merchandise of Walsh codes. The scientific establishments for the entirety encoded conspire and decoded plot in Ahmed el at [1].

c. Building Blocks of OCI crossbar

For every crossbar and associated duct designs, there are duo alternatives are acknowledged. The actualization of duct designs is to improve the crossbar actualization recurrence, and the data transfer capacity by collection impractical duct registers which are used for diminishing the crossbar crucial range. The description of architectures of OCI crossbar are explained below.

Crossbar Scrutinizer: the initial for every crossbar exchange, this scrutinizer appoints scattering bits towards various encoders. There is no change among the crossbar exchange in terms of, because the unrelated codes are settled at acceptor side which are appointed at the transmission side. Consequently, the switch port begins the connection towards acceptor side it directs, here encoder should be appointed for scattering code which also must equals the acceptor side decoder. A particular decoder gets the appeal from various dual ports, scrutinizer permits single entryway and rejects another as indicated by the predefined intervention conspire [21]. The crossbar scrutinizer circulates concord signs towards Tx-Rx storage places with coordinating scattering bits to allow Tx encoders along with Rx decoders.

2) *Hybrid Encoder*: The encoder is crossover, it be equipped for encoding both the information to be specific unrelated and nonorthogonal. The XOR and AND operation done between Rx messages and dissipating bits for creating unrelated/related mushroom information, individually. On the basis of bit model appointed to an encoder, a multiplexer picks between the unrelated and related contributions as shown in fig.1(a). The encoder is copied 'N' time for the P-OCI crossbar.

3) Crossbar Adder: The quantity of crossbar transmitter and receiver ports coordinated towards M=2(N-1) for dispersing codes of range N. On the basis of TDMA-OCI crossbar encoding method, when we apply '1' to the adder, its mutually exclusive among the related ports. There are assured zeros of N-2, as surrounded by 2(N-1) information to the addition circuitry, where maximal quantity N of '1' chips. Accordingly, one Mux is introduced for the election of one admission from the related TDMA encoded information bits and removes left out bits as '0'. Hence, the admissions which addition circuitry includes N-1 from unrelated encoders along with 'one' from mux, so it's clear that its having N admissions as portrayed in fig.1(d). The quantity of considered essential phases of registry to duct the addition circuit is $\log_2 N$, this shown in fig.1(d). For parallel OCI, this crossbar addition circuitries are repeated for N times.

4)Custom Decoder: For various CDMA decoding methods, the decoder models are 4 in number. They are namely 1). Unrelated TDMA OCI, 2). Unrelated Parallel OCI, 3). Overburden(related) TDMA OCI, 4). Overburden Parallel OCI. An accumulator's execution of correlation acceptor is expressed in terms of unrelated TDMA-OCI decoder. For unrelated message non-propagation, N-1 accumulator decoders are called in the whole CDMA crossbar models. The up-down accumulator replaces the dual various accumulators and the outcome is divergence of dual acuumulators of ordinary CDMA decoder as depicted in fig.1(f).

As reporting to the non-propagation code chip, the crossbar total parameter's addition/subtraction done by the accumulator and restarts for each N time period

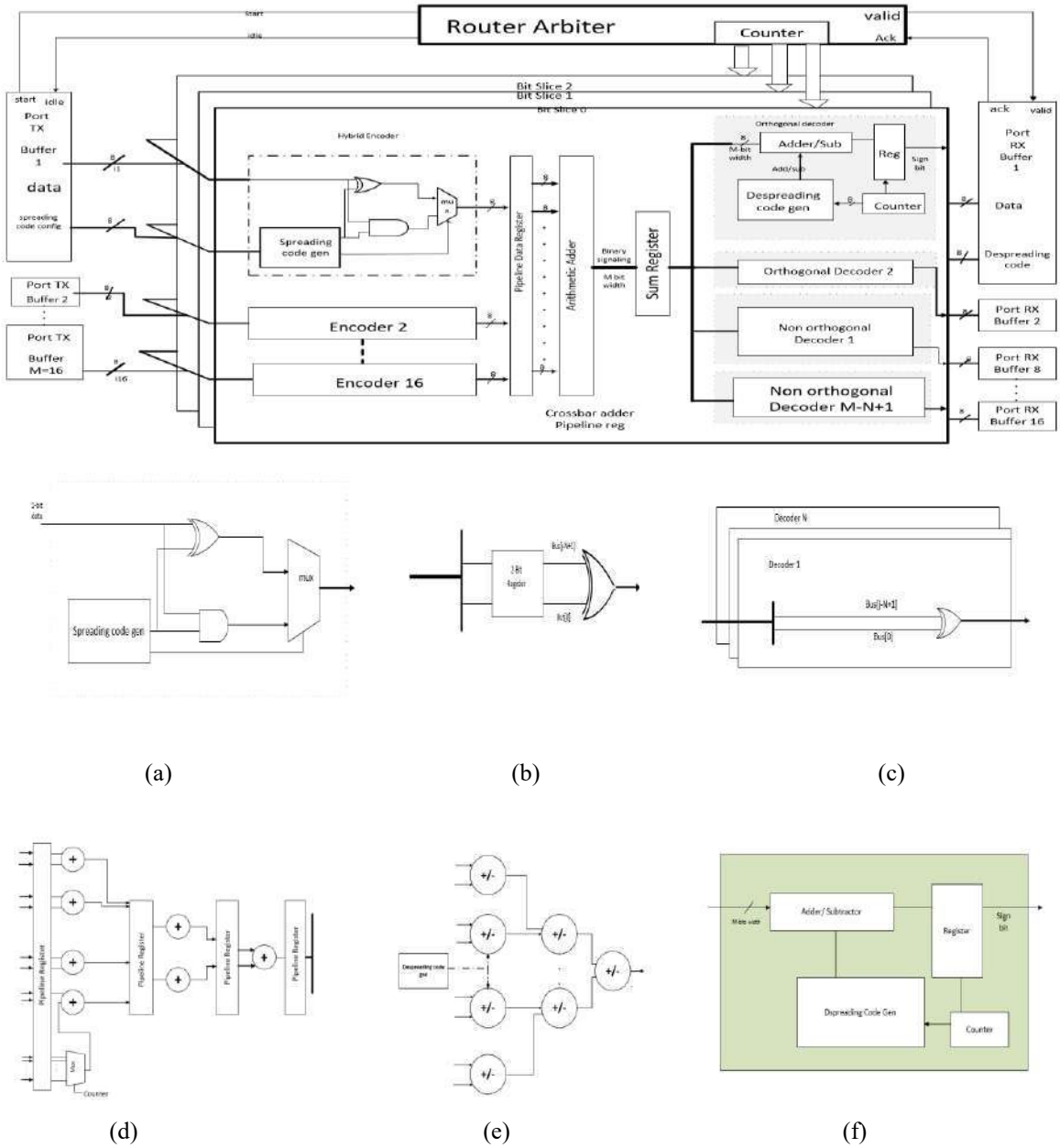

Fig 1. Top level design of OCI Crossbar. (a) TDMA-OCI/Parallel-OCI hybrid encoder. (b) TDMA-OCI non-orthogonal decoder. (c) Parallel-OCI non-orthogonal decoder. (d) TDMA-OCI pipelined crossbar tree adder (duplicated N chances for P-OCI crossbar). (e) Parallel-OCI orthogonal decoder. (f) TDMA-OCI orthogonal decoder.

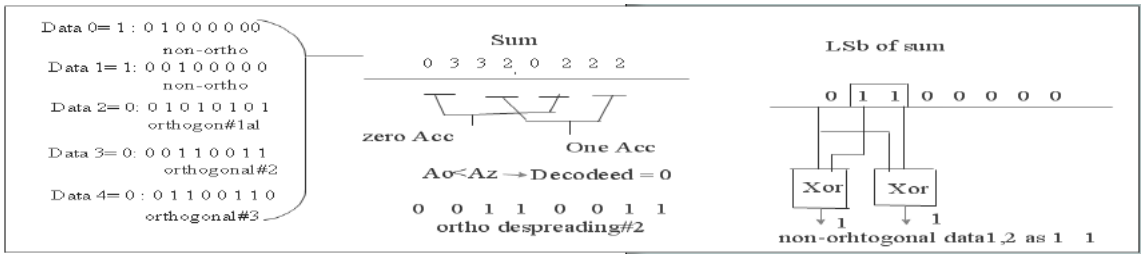

Fig .2 Encoding /Decoding of orthogonal codes and two non-orthogonal code.

The decoding bit is depending on the sign bit of the accumulator's output, that +ve clue gives '1' and –ve clue gives '0' decoding bits. An accumulator presented as parallel addition circuitry due the Parallel-OCI unrelated decoder contrasts from contrasts against TDMA-OCI unrelated decoder in getting addition total parameter simultaneously not progressively as portrayed in fig.1(e). A two bit register is used in TDMA-OCI overburden(related) decoder to accumulate the LSB (least significant bit) s of 2 added parameters as shown in fig.1(b), at S(0) is primary one and S(j-N+1) is 2nd, that the j represents the quantity of TDMA-OCI decoders $(N \leq j \leq 2N-2)$ and widening code length N. This 2-bit information urged XOR gate, that unwinds non-orthogonal(related) accomplish message. Fig.1(c) shows that the TDMA OCI decoder is copied N chances for executing Parallel OCI. There is no need of two-bit register in P-OCI non-orhtogonal(related) decoder due to all the bit values remain in a time. The N-1 unrelated and related decoders exist in TDMA OCI and Parallel OCI crossbar designs.

IV. HAN CARLSON ADDER

In Overloaded-CDMA crossbar we have an adder circuitry to add the encoded messages together to produce a sum signal. We are performing additions with normal adder which takes the large delay for parallel additions. To this extent, we are replacing normal adders with the design of Han Carlson adder to achieve high-speed parallel addition and it also reduces the area and power. In prefix accumulation we wastage three stages to enlist the total in pre-proocessing, prefix-processing and post-preparing.

The aim of combining is to reckon the sum S, for the two parts A and B of length *n* in binary. The first phase, for *n* bit sum adder calculates the generate(g) and propagate(p) phases per bit of the operands according to the following equations.

$$\begin{aligned} g_i &= a_i . b_i \\ p_i &= a_i \oplus b_i \end{aligned} \tag{2}$$

From the equation 2, prefix addition performed. The prefix operation Θ, is described as :

$$(g_i, p_i) \Theta (g_j, p_j) = (g_i + p_i \bullet g_j, \quad p_i \bullet p_j) \tag{3}$$

For every prefix activity, the operation associates the 2 AND operations along with 1 OR operation. Here two vital characteristics namely idempotency and associativity shown by the prefix operation. Therefore, it gives the following:

$$(g_{m\ldots i}, p_{m\ldots i,}) \Theta (g_{i\ldots n}, p_{i\ldots n}) = (g_{m\ldots n}, p_{m\ldots\ldots n}) \tag{4}$$

$$(g_{m\ldots i}, p_{m\ldots i,}) \Theta (g_{i\ldots n}, p_{i\ldots n}) = (g_{m\ldots j}, p_{m\ldots j}) \Theta (g_{i\ldots n}, p_{j\ldots n}) \tag{5}$$

The calculation of carry for any bit point is given as below equation (5), as a loop of prefix operations:

$$(g_{i\ldots 0}, p_{i\ldots 0}) = (g_{i-1}, p_{i-1}) \Theta (g_{i-2}, p_{i-2}) \ldots\ldots\ldots (g_1, p_1) \Theta (g_0, p_0) \tag{6}$$

Equation (7) tell that carry generated from equation (6),

$$c_i = g_{i\ldots 0} + p_{i\ldots 0} \bullet c_0 \tag{7}$$

The last phase, the carry bits and propagate bits are used to calculate the sum. This shown in equation as:

$$s_i = p_i \oplus c_i \tag{8}$$

From equation (8), it's clear that the post addition operation performed with the propagated bits and carry bits. The prefix operators are known as 'parallel prefix adder' which are required to build the adders. For the calculation of group g's (gi…j) and group p's (pi…j), they apply the associativity and idempotency property of the prefix operators.

A Kogge-Stone adder consequences in an allocation of side-by-side networks and for this reason bottleneck, unchanging still the architecture regulates the fan out to unification and calculates the carry in O(log n) time [29]. On the other side, prefix per node in graph is calculated by a Brent Kung adder, restricting the reasonable fan-out to integrity, but without the using of wires [30]. The Han Carlson figure of a 16-bit analogy prefix adder uses a particular Brent Kung platform Kogge-Stone plan and terminated by a further Brent-Kung show for the terminal playhouse of the prefix calculation.

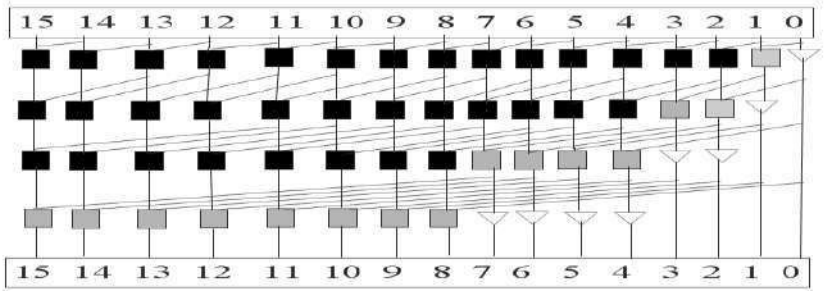

Fig .3 Han Carlson Adder

Further processing after the calculation of the parallel prefixes is like for completely the similar prefix adders. The prefix calculation phase of a 16- bit Han Carlson adder is exposed in fig. 3. It t is experiential from Fig. 3 there are five prefix calculation phases for the Han Carlson adder, which is one additional than the Kogge-Stone design (log216=4) for the unaffected word size.

IV. RESULTS AND COMPARATIVE ANALYSIS

This section discusses, the performance evaluation outcomes of the OCI Crossbar with normal adder and the proposed Han Carlson Adder are presented.

1. *OCI Crossbar evaluation*:

In this, normal OCI CDMA and OCI with HCA are compared and these crossbars calculated for widening bits of ranges N {8,16}. Crossbar designs with the different quantity of ports, whole fulfilment measurements are assimilated to M quantity crossbars. The estimation outcomes, covering capital usage conveyed as quantity of LUTs (Look Up Tables) along with flip flops(FF) for each port per port, ultimate crossbar recurrence, effective power exhaustion for each port and transmission limit are shown in fig. (4). The fig.4(a) shows that, OCI crossbar with HCA's resource usage is 30% less than the ordinary OCI crossbar for a N length widening bits. As N spreading code length raises, resource usage for each port is increased, because of gaining crossbar intricacy.

The working recurrence reduction done with crossbar adder's crucial way range for all mentioned designs. A confined length of N widening codes of different CDMA crossbar, unrelated propagating and non-propagating designs are same and related information encoders and decoders are functioning equal to unrelated widening circuit of small crucial way range. The admission part of addition hardware equivalent to the quantity RX ports M, that changes by CDMA crossbar model. The crossbar recurrence of OCI with HCA crossbar is minimal higher when it compared with OCI with normal addition circuitry because of improving the addition design for a constant widening bit length 'N' shown in fig.4(b). The fig.4(c) shows that, gaining crossbar data transfer capacity in OCI with HCA than that of OCI with normal adder, it satisfies the recurrence reduction with expanding N from overburdening. The chart balanced transmission capacity is drawn to a one for each port linked through CDMA crossbar. The upgradation of CDMA crossbar with HCA data transfer capacity over the traditional CDMA crossbar for Parallel OCI along with TDMA OCI crossbar is striking for constant N. By and large, the CDMA crossbar data transfer capacity, i.e BW is expressed by the progressive condition:

$$BW = Wf_c \frac{M}{\Gamma} \tag{9}$$

From condition (9) bandwidth, that thickness of port is W in bits, the crossbar time recurrence is f_c, M is quantity of crossbar ports, quantity loop for encoding the one bit information from whole ports is Γ [15].

The effective power diversion for each port assessed with a tool called Xilinx Vivado to one crossbar activity, 25% is diminished for OCI with HCA against the TDMA-OCI crossbar because of the offered limit upgrade for a widening code N of length as shown in fig.4(d). In any case, because of the expanded zone and parallel encoding disentangling of Parallel OCI crossbar, the effective power diversion is less when it compared with OCI with the normal adder. The power diversion for each port raises for whole CDMA crossbars by expanding N, because of extended magnitude and intricacy of crossbar elements.

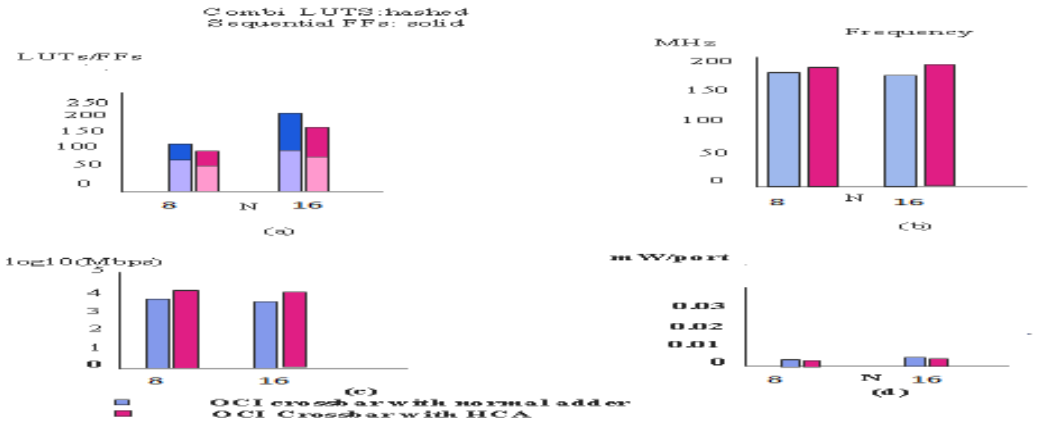

Fig.4 Execution outcomes of OCI crossbar for N range spreading code. (a) resource utilization(b) Frequency (c)Bandwidth (d)Dynamic power in mW per port.

2. *OCI for Network On Chip: Experimental Evaluation*

For complete operation of Network On Chip takes the importance of OCI crossbars, the 5 OCI switches are used to develop the 65-hub star topology, in 13 PEs every single is associated with OCI switch of N=8, a Spatial division multiple access' basic switch is linked by 5 OCI switches [15]. The effectiveness of OCI with normal adder and with HCA on Cyclone-2 FPGA kit as shown in table.1.

Table. I Experimental results:

System	Area				Delay	Dynamic power
	Slices	LUTs	FFS	IOBs		
OCI system	58	102	54	36	18.346 nsec	0.18W
OCI with HCA	42	73	46	27	16.803 nsec	0.14W

The table I provides the resource utilization expressed in the several Look Up Tables (LUTs), flip flops (FF) and input-output blocks, greatest latency and dynamic power consumption. Comparing the numerical values, we can see that area is reduced by 30%, 12% less delay and 25% reduction in power consumption. The throughput Θ which can find out as:

$$\Theta = \frac{N_c \times N_b \times N_p}{t_c} \tag{10}$$

Where, quantity of synthesis clock periods is N_c, N_b is the quantity of bits/packet, the quantity of packets obtained by destination PEs is N_p, the clock period is t_c. The throughput of the OCI with HCA is higher than OCI with normal adder because of its lower time period.

VI. CONCLUSION

In this paper, a normal adder replaced with Han Carlson Adder(HCA) in OCI Crossbar. This thought of HCA because of its parallel addition concept and less complexity. NoC router's material layer is enabled by this overburden CDMA crossbar. In overburden CDMA, the transfer drain is overburdened with non-orthogonal codes to become more intense the channel ability. The occurrence of the OCI crossbars is analyzed with and without HCA in crossbar addition and examined on a Xilinx Cyclone-2 FPGA kit. The effective power is 25% diminished for the OCI crossbar, where HCA is used for crossbar addition. The OCI with HCA crossbar drains 30% less resources than that of ordinary OCI system. Observing the heaviness of CDMA links and CDMA's improvement methods intended as part of the preceding impending study points.

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QUALITY INSPECTION OF ENGINE BEARINGS USING MACHINE VISION SYSTEM

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Abstract-The growth of an industry is majorly based on the quality of the product. When there is a fault in the manufactured product in one of the batch, the entire batch is being rejected because of the single faulty product. Quality has become one of the important factor deciding the growth of the industry. Industries nowadays are being automated in every phase of the manufacturing process. Here, an automated system is developed for the inspection of the product developed for the automobile industry. The bearing is one of the parts which play a major role in the connections with the engine and the shafts. Therefore, the bearing has to be perfect as faulty bearings will lead to a greater damage regardless of others. In the automated system the bearing is inspected for the missing operations in the product. The faulty product is rejected and would be checked for rework or to be scrapped. The inspected products are then being sent for the packing process. Through the automated inspection system, the production rate of the product can be increased also increasing the reputation of the industry. The objective of the proposed work is to develop a machine vision system for quality inspection of bearing efficiency. The LabVIEW based approach is carried out for the implementation here.

Keywords: Machine Vision System, Engine Bearings, Quality Inspection, Fault Detection, Automated System.

INTRODUCTION

Today's world is looking for the quality of product and delivery of such products is increasing. The defective products are not accepted by the consumers as that would affect their market value.In order to avoid these problems, inspection of a product is required at the final phase of the manufacturing process. The inspection of the product is done either by human power or automated inspection through machine. The quality has become the important factor as a need of the customer. Product quality is determined at the manufacturing line where there are quality inspections made either manually or through some automated systems. If an unprocessed product passed through without quality check, which may lead to a major issue where the industry could even loose the customer and their market value. The unfinished/defective part skipped to the packing session happens mainly due to the human error.

Based on the survey, has been the motivation for the development of the automated inspection system for inspecting the products using the Machine Vision System (MVS). The error occurs due to unconscious or visual problems when a human is employed to inspect large number of finished product, for example in industries production rate per shift is 1 lakh product and a shift consists of 7 hours in which a labor should be able to check 23 parts within a minute.In some case due to human nature inspecting more number of good products,visual mistake would happen when an unfinished product is given on the run.So, to eliminate this problem machine vision system is used for the inspection of the finished parts.

The objective of the proposed work is to develop an automated inspection system which would identify the defects in the product and to increase the production rate in the industry. To achieve the objective of the proposed work an automated system is developed to identify the defects in a bearing. In the proposed system the identification of the fault is done using a camera and image processing technique is used to identify the defect and reject the defect product which would increase the quality which in turn will reflect in the increase in the production rate.

IMAGING TECHNIQUE

The visual inspection is the more reliable and healthy non-contact type fault detection technique, in order to automate the visual human inspection, camera and its associated system is used. The camera which is used for acquiring the image is called as machine vision camera which is mainly manufactured for vision application. The sensor used for machine vision cameras are of two types CCD and CMOS sensor in which CCD sensors are costlier than CMOS sensor. CMOS sensors are more reliable and less in cost which makes the visual automation cheaper.

The size of the bearing ranges from 25mm to 125mm. The image sensor size is very important while going for machine vision application.There are different sensor sizes available in the market such as 4mm, 6mm,8mm,9mm and 16mm in diagonal length and resolution for the application depends on the image sensor.Normally the resolution is spoken in the form of pixels but in machine vision application the resolution is take in mm with respect to pixels. The equation for selection resolution is given below.

Sensor resolution =2(Field Of View/Smallest Feature) ---- 1

Choice of lens is very important because lens determines the area to be in visible.The lens can be selected with the formula shown in equ 2. Before choosing the lens, imaging sensor must be selected.

Focul Length * Field of View = Sensor Size * Working Distance --- 2

For example, according to the calculation, if the focal length is 8mm and the sensor size is ½", then the lens must be a ½" lens which is specified in the lens. If a ¼" lens is used then output image will look like cropped image where the data can be missed out.

PROPOSED MACHINE VISION SYSTEM (MVS)

The machine vision system is one of the growing visual automation systems in industry to enhance the quality of the product. The system consists of different parts which can be listed out as camera, lens, lighting,housing, sensing element, rejection mechanism etc,. Bearing is the inspection element which moves on a conveyor at the speed of 1.2 second/bearing. Once the bearing is been sensed by the sensor the trigger signal is given to the camera via hirose cable, camera gets triggered and image is stored in buffer. This image is been transported to the system through USB communication medium.

Whenever the image trigger signal is obtained by the system through the data acquisition card, the program will process the image. The processed image is checked for the missing operations, if there are no fault operations then the bearing is given a 'OK' signal. The processed image if consists of certain fault conditions then a 'NOT OK' signal is given where the signal is passed to a rejection system, where a pneumatic arm pushes away the bad product for rework or to be trashed.

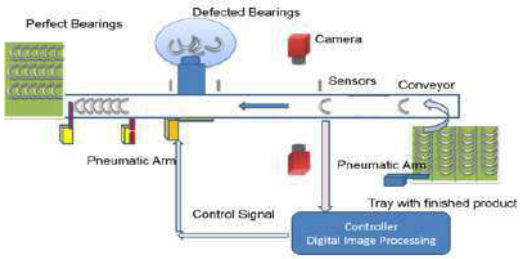

Fig 1. Proposed machine vision system

Fig 1. shows the top view diagram of the Machine vision system which consists of two cameras one is to capture the inner diameter of the bearing and another camera is used to capture outer diameter of the bearing.

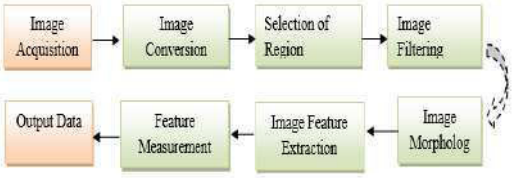

Fig 2. Techniques involved in the detection of the missing operation.

To identify the missing operations in the bearing, concepts of the image processing is adopted. Implementations of new algorithms are done to identify the fault with high accuracy. The algorithm involves filtering, segmentation, and so on. The software used to develop this system is LabVIEW with Vision toolbox, which consists of both acquisition and processing of image. Image acquisition is done through NI-IMAQdx file and further processing is done through vision assist. Fig 2. shows the general flow of the process involved in the detection of the missing operation.

EXPERIMENTAL SETUP

The automated machine vision inspection system developed in shown in Fig 3. The inspection of the product is done using the image processing technique in LabVIEW where Vision and Motion toolbox is used. The image which is captured in the camera is passed to the LabVIEW program with the help of the USB communication. The IMAQ-dx tool is used to grab the image into the program. Then the program is executed through the loops where the different processing techniques for identifying the missing operation is processed.

The processed image is checked for the missing operation, when the product consists of no missing operation then the system gives an OK signal, the product is passed for the next operation. If there are any missing operation in the product the program sends an NOT OK signal to the rejection system with the help of the Data Acquisition (DAQ) system, which intiates the rejection to push the defect product from passing to the next operation.

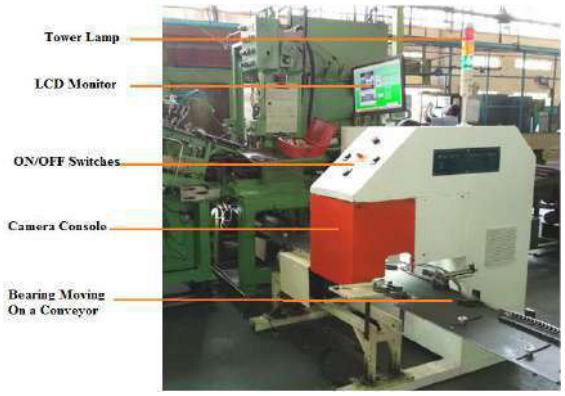

Fig 3. Automated Line with the MVS system in the industry.

Fig 4. Front panel of the automated system when the bearing is passed through camera.

In this proposed system the CPU which is used consists of i3 6th generation processor, 4GB RAM, 1TB Sata Harddisk with Windows 8 operating system. The Fig 4. shows the front panel of the image in the automated system.

RESULTS AND DISCUSSIONS

The missing operations are being observed through the image acquired with the help of the camera. The captured image is passed to the LabVIEW through the USB communication, and the image is shown in the front panel GUI of the system. The missing operations such as 'HOLE', 'CHAMFER', 'NOTCH' and 'GROOVE' are being detected in the bearing. In certain types of bearings, the above-mentioned operations may present or may not be present based on the locomotive and the place of the bearing where it is to be installed.

Chamfer Inspection

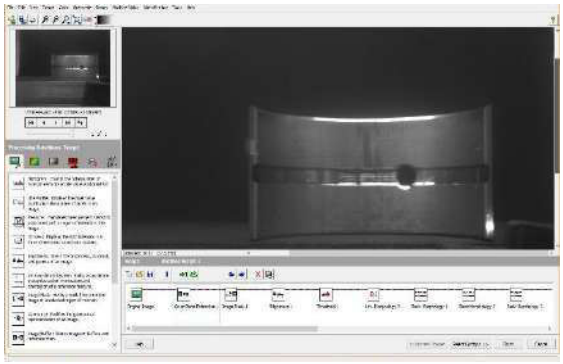

Fig 5. Image of bearing inspected for Chamfer operation

The Chamfer is one of the operations done during the process. The chamfering of bearing is done at the top and bottom of the alloy side and steel side. If there is any missing of chamfer due to tool damage of power failure which causes failure in engine.

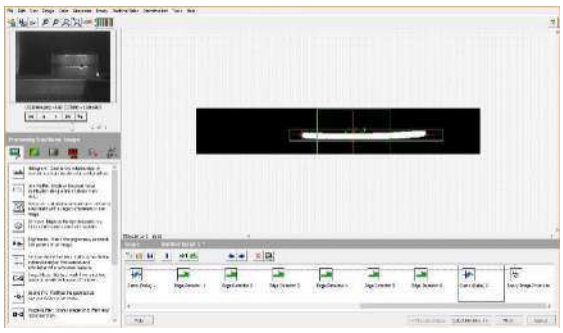

Fig 6. Measurement of the Chamfer to determine the operations has been successfully done or is there any miscalculation.

The Fig 5, Fig 6 are the operations involved in the identification of the Chamfer. The bearing which is inspected for the missing of the chamfer will undergo all these steps to make sure the presence of the chamfer in the bearings. The missing of the chamfer in the bearing will lead to the rejection of the bearing from the line for rework.

I. *Hole Inspection*

Hole plays the major role in passing the oil to the system so if there is any problem which will cause insufficient oil flow to the system and causes damage to the engine. The problem in hole operation during process can occur when sudden power shut down or tool problem or improper pressure level to the machine.

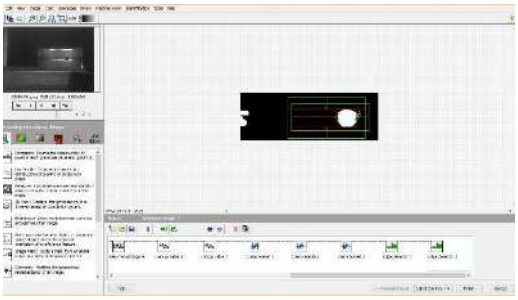

Fig 7. Edge detection is applied for the circle with the values.

$$G(x,y) = \frac{1}{2\pi\sigma^2} e^{-\frac{x^2+y^2}{2\sigma^2}} \quad \text{----3}$$

To determine the edges of the hole, edge detection technique is used and the edge of the hole is marked. The values of the edges are noted and are used in the processing to determine the characteristics of the hole in the image. If the decision of the values are same as hole the output will be provided as true else it program provide false as decision.

II. Groove Operation

The groove is one of the area where helps the oil from the hole to flow through the system. The missing of groove in the bearing causes more wear and tear in the rotating part of the engine which causes heating and ceasing of engine. The groove in the bearing will be at the center or at the edges of center called as full groove or banana groove respectively.

To identify the groove in the bearing, the bearing is first masked based on the region of interest. Then the image is converted and the threshold is applied to mark the groove in the bearings. After segregating the groove, edge detection technique is used to identify the groove edges.

III. Notch Operation:

The notch is the last operation of the quality inspection of the bearing, the notch is one parts in the bearing which is used for the connection with the engine rods. The notch is identified by comparison of the edges of the notch and the edge of the bearing.

As discussed above the four operations of the bearing are tested in the automated inspection system through the camera. The image of the bearing is captured in the production line. The image is then processed by the LabVIEW software to identify the 4 operation at the same time.

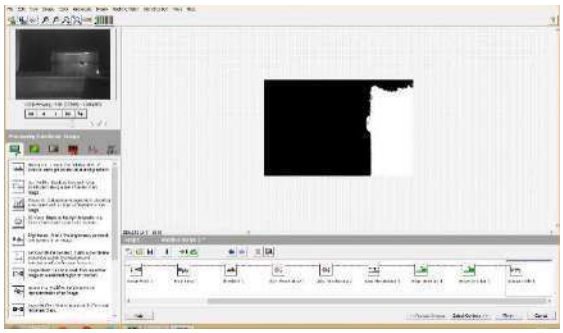

Fig 8. Detection of the notch by comparing the edge position of the notch with the edge position of the bearing

As the captured image consists of all the four operations the image is give an OK signal which is passes for the next operation. If there is any one missing operations such as Hole missing, Notch missing, Groove missing, and chamfer missing, the bearing is rejected by the system Table 2.

Depicts the result taken from the industry in the year 2016 for the month of January to July with the calculation of efficiency. In addition to the inspection, the data of the inspected image is collected such as Chamfer pass/fail, Groove pass/fail, Hole Pass/Fail, Notch Pass/fail and Bearing OK/Not OK and stored in spreadsheet format for further analysis of Quality assurance cell as shown in the Figure.

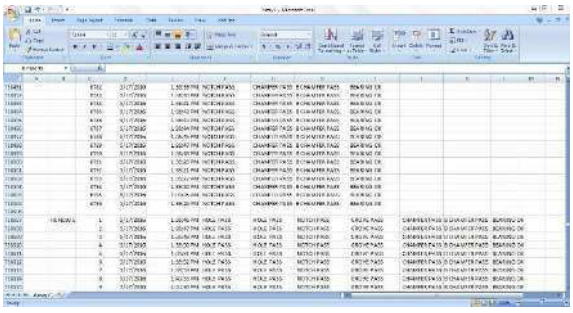

Fig 9.Stored data of the inspected bearing in spread sheet file.

TABLE I

Inspection time taken and the number of rejections during the Inspection in a shift of 8 hours

Description	Time Taken to Inspect the product per shift of 8 hours	No of product can be inspected in a shift of 8 hours	No of product manufactured in a shift of 8 hours
Manual Process	3.7 seconds	7,783	20,000
Automated Process	1.5 seconds	19,200	

The data shown in the Table 2. is taken from the spread sheet which is stored during the period of 2016 . The data contains approximately 8 Lakhs of inspected component details for the duration of January to July and the Table 2. Describe the efficiency of the machine by considering the rejection of ok bearings.

TABLE II

Data of Inspected bearing during the year 2016

2016	No. of Inspected bearings	No. of Accepted Bearings	No. of Rejected Bearings	True Positive value	False Negative value	%Efficiency
January	43,282	42,736	546	464	82	99.810
February	1,17,148	1,15,911	1237	994	243	99.792
March	1,59,789	1,59,114	675	580	95	99.940
April	74,743	73,257	1486	1146	340	99.545
May	1,57,489	1,56,721	768	470	298	99.810
June	1,76,259	1,73,999	2260	1486	774	99.560
July	78,407	77,038	1369	934	435	99.445

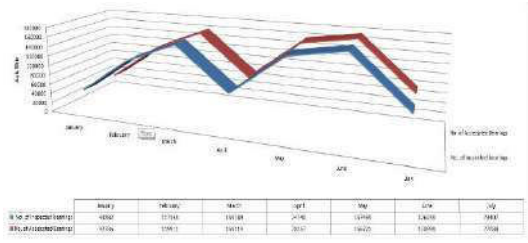

Fig 10. Comparison graph of input bearing vs acceped bearings

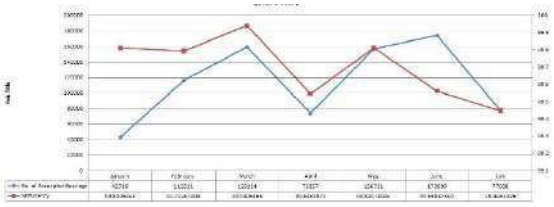

Fig 11. Comparison graph of acceped bearings vs effecency in percentage

As the data says that the efficiency of the system is 99 percent and the 1 percent deficiency is due to some changes in conveyor mechanism and lighting issues. The main slogan of quality inspection is that ok pices can be rejected but defective pices never been accepted. So the result says no defective pices are accpted and only some of the ok pieces are rejected.

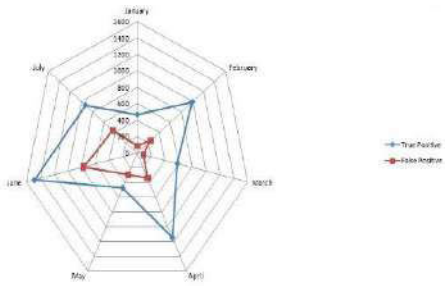

Fig 12. Comparison graph of True Positive and False Negative values

6. CONCLUSION

The quality inspection of the products are being the most important process to maintain the company's reputation and it is 100 percent ensured that none of the defected piece is passed. There are various products related to the quality inspection of the final procduct, industries are looking for the best device at cheapest cost. The Machine Vision System which is developed above has shown that the number of products inspected per shift is more as 19,200 compared with the maual inspection. The deficinecy in the inspetion process is also less compared to the manual process. Thus it is proven as the best product with low cost for the quality inspection of the products. The automated system is commisioned and working at the industry to identify the missing operations of the bearings. By the results above the system has shown better results for the bearings.

ACKNOWLEDGEMENT

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Fiber Bragg Grating sensor for impact analysis

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Abstract **- An optical Fiber Bragg Grating (FBG) is a single mode optical fiber with a periodic variation of core refractive index. The refractive index variation in a selected region of the fiber core is created by using standard methods. It is seen that Fiber Bragg Grating based Sensors (FBGSS) offers some unique advantages over the conventional sensors in impact analysis. Highly stressed surfaces often require accurate methods for the analysis of impact. FBGSS are well suited for this purpose as they can be easily embedded in the modern hybrid composite materials. Distributed sensing is also possible with FBG's connected in series. We are reporting the development of a FBG sensor for the analysis of impact. A simple set up is developed and the experiments are carried out. The analysis is done on a cantilever structure made up of stainless steel. FBG is suitably fixed on the cantilever structure. Impact is introduced using metal balls of known weights being dropped from a fixed height and guided through a pipe. A standard impulse force hammer is connected in parallel and measurements are taken for comparison. The FBG reflected spectrum is analyzed using an interrogator. A laptop is also interfaced for display and analysis. The FBG based set up developed can be used for the in situ measurement of other physical parameters with suitable modifications.**

Index Terms **- FBG; reflected spectrum; impact analysis; FBG interrogator; impulse force hammer.**

I. INTRODUCTION

The optical fiber consists of a high refractive index core surrounding by a low refractive index cladding and it works on the principle of total internal reflection of light. The optical fiber cables have many inherent advantages over other conventional cables that are used in the communication industry. They offer a very high bandwidth and they can be used in harsh environments. These cables are also immune to electromagnetic interference Because of these advantages optical fiber cables are replacing the conventional cables in the communication networks. The optical fiber is also widely used nowadays for the development of novel sensors. It has been proved beyond doubt that fiber optic sensors can be effectively used for the measurement of many physical and chemical parameters These sensors have been found to offer excellent solutions to once complicated measurement issues[1-3].

The fiber optic sensors are developed based on the modulation of light travelling through the fiber by the sensing environment. The optical fiber is used as the sensing medium in these sensors The modulation of light is studied with the help of various interrogators. There are various classifications of fiber optic sensors like intrinsic and extrinsic. Classification is also done based on the modulation scheme used. Some of the common applications are in structural health monitoring, pollution measurement and the estimation of other physical and chemical parameters. These sensors offer many advantages like distributed sensing and they can be easily embedded in modern hybrid composite materials.

FBG is developed and fabricated from a single mode optical fiber by creating a periodic variation in the refractive index along its core using standard methods. Depending upon the period of the grating that is being fabricated they are classified as Long Period Gratings (LPG) and short period grating or Fiber Bragg Grating (FBG). It has been observed that LPG's can be effectively used for various chemical sensing applications while FBG's are generally used inr physical sensing applications. The transmitted spectrum is analyzed in the case of LPG. In the case of FBG the object of analysis is the reflected spectrum. A shift in the peak reflected wave length observed in the case of FBG based on the physical parameter that is being measured.

The optical fiber based measurement of impact, vibration, strain, temperature, are active topics of many recent research and discussion [4- 5]. In this work we are reporting the design, and development and characterization of a simple FBG based sensor for the accurate measurement and analysis of impact. The developed scheme consists of high sensitive FBG being used for the measurement of impact loading. Impact loading is done on a cantilever structure using steel balls of standard weights being dropped though a pipe of fixed length. The FBG is suitably mounted on the cantilever structure. The reflected spectrum of the FBG is analyzed using an interrogator. The peak of the reflected spectrum of the FBG is found to be shifting with the impact that is being loaded and this is correlated for the analysis of the impact loading.

II. EXPERIMENTAL DETAILS

The experimental setup developed for the FBG based impact analysis is shown in Fig.1. The setup consists of an FBG, a cantilever structure of length 10 centimeter and thickness of 1 millimeter, an interrogator and a laptop. The FBG grating portion is suitably fixed suitably to this cantilever structure. The cantilever structure is also provided with a provision of providing impact using a standard impulse force hammer. Standard metal balls with calibrated weights are dropped onto the cantilever structure through a pipe from a height of 50 centimeters to introduce impact. The reflected spectrum is analyzed after applying the impacts. using an interrogator The FBG used for the measurement is having a peak reflected wavelength of 1532.4 nm. Since the FBG's are temperature sensitive the experiments have been carried out by keeping a constant room temperature of 22^{o} C. The graphs are plotted by interfacing with a laptop. Impact is also

imparted on the cantilever structure using a standard impulse force hammer for measurement and comparison.

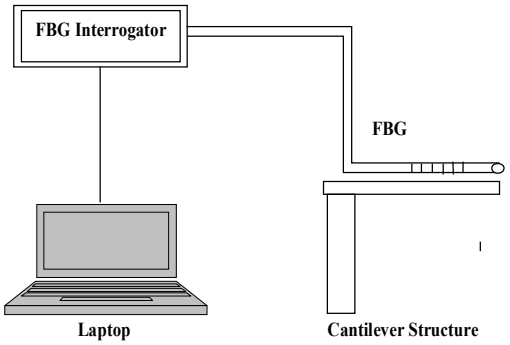

Fig. 1. Experimental setup for impact analysis using FBG.

The theory of operation can be summarized as follows.

The Bragg's law states that:

$$\lambda_B = 2n_{eff}\Lambda \quad (1)$$

In the above equation 'λ_B' is the Bragg wavelength, 'n_{eff}' is the refractive index of the fiber core and 'Λ' Bragg grating period [6].

The grating pitch and refractive index of the FBG is changed by the application of strain and the resultant elongation of the optical fiber. When temperature is kept constant, the Bragg wavelength shift can be written as:

$$\Delta\lambda_B = (1 - p_e)\lambda_B\epsilon \quad (2)$$

In the equation 'ε' is the applied strain.

'p_e' the effective photo elastic coefficient can be written as:

$$p_e = \left(\frac{n^2}{2}\right)[P_{12} - \nu(P_{11} + P_{12})] \quad (3)$$

Where 'ν' is the Poisson's ratio of the fiber and 'P_{ij}' is the Pockel's coefficients of the strain optic tensor.

The FBG reflected spectrum is given by [7] as:

$$R_{r1}(\lambda) = R_{r1}\exp\left[-4ln2\left(\frac{\lambda-\lambda_{r1}}{\sigma_{r1}}\right)^2\right] \quad (4)$$

σ_{r1} is Full Width at Half Maximum and R_{r1} is the reflectivity of the FBG.

III. RESULTS AND DISCUSSION

The reflected spectrum of the FBG is plotted and it is shown in Fig 2. The FBG reflected spectrum is analysed using an interrogator. A 30 gram metal ball is found to create an impact of 0.15 J on the cantilever structure when dropped from a height of 50 centimetres through a guided pipe. The peak wavelength of the reflected spectrum plotted against time with impact loading on the front of the cantilever structure is shown in Fig 3. The peak of the reflected spectrum is found to be shifting with the applied impact. The applied impact is varied in steps from 0.15 J to 0.02 J by varying the weight of the ball from 30 grams to 5 grams. The results obtained using spectrum analyser is plotted in Fig. 4. A distinct blue shift is observed in the spectrum as the impact is decreased..

The peak in the reflected spectrums is also plotted as impact load v/s wavelength and is given in Fig. 5. It shows linear characteristics. The impact loading point is shifted from the cantilever front end to the middle and the change in the peak wavelength of the reflected spectrum is shown in Fig.6. The middle loaded reflected spectrum is found to be different from the front loaded one. The exact location of impact can be determined accurately by connecting multiple FBG's in series. .

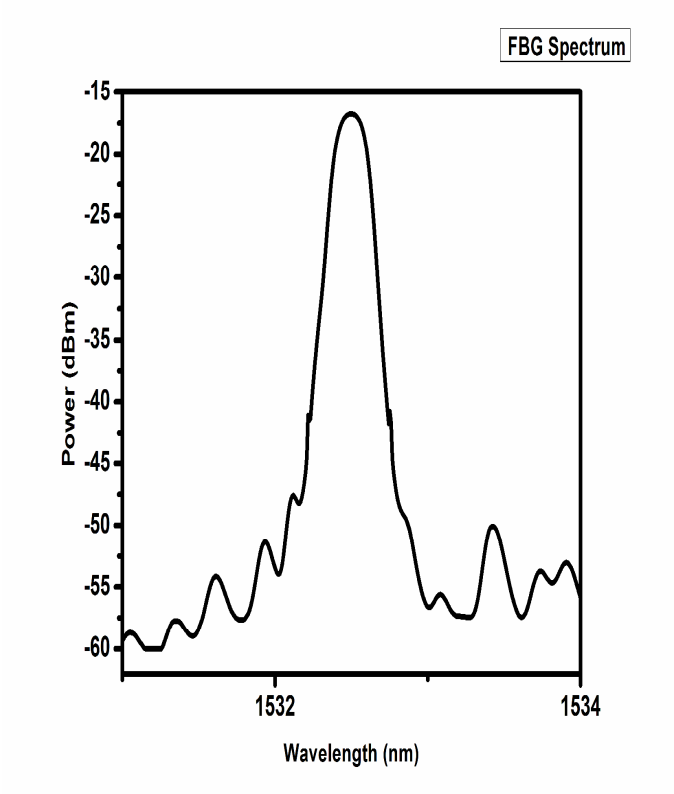

Fig. 2. The FBG sensor reflected spectrum

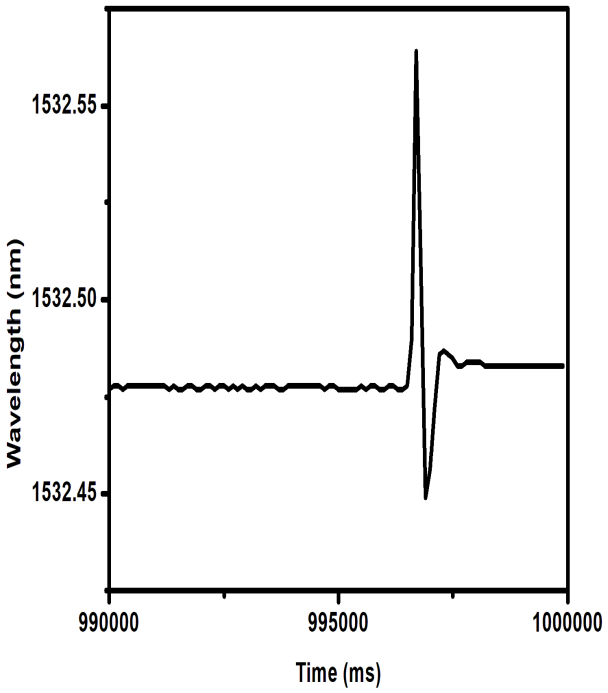

Fig. 3. The peak wavelength of the reflected spectrum plotted against time with impact loading on the front.

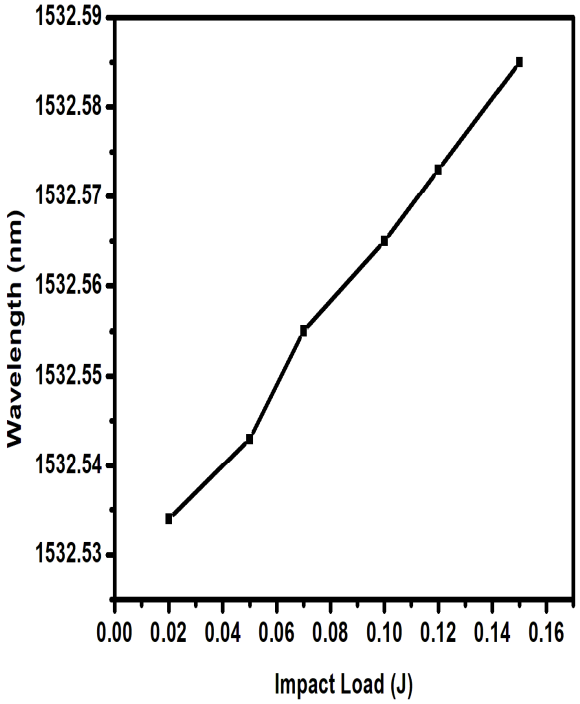

Fig. 5. The calibration curve of the FBG sensor

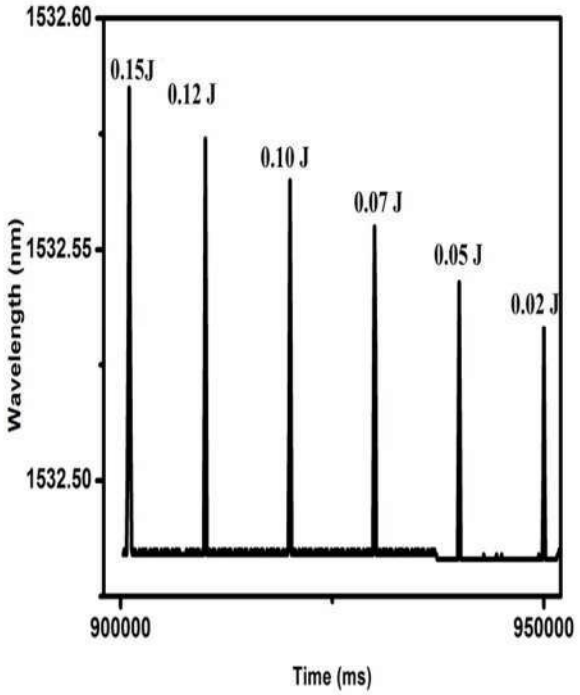

Fig. 4. The peak wavelength of the reflected spectrum plotted against the applied impacts.

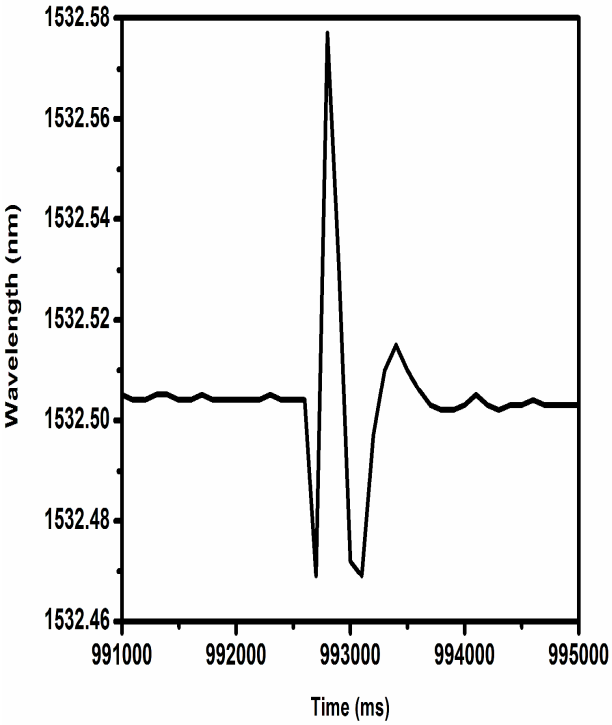

Fig. 6. The peak wavelength of the reflected spectrum plotted against time with impact loading on the middle.

IV. CONCLUSION

The experimental setup developed is established to be well suited for the analysis of impact. The impact analysis can be carried out with a fairly good degree of accuracy, resolution and repeatability using the method. Multiple FBG's can be connected in series and a detailed analysis can be done to find out the exact location of impact. With suitable modification in the setup, the developed method can be used for the measurement of other physical parameters like pressure, vibration and structural health monitoring. The experiment is repeated with a standard impulse force hammer and found that the results are matching.

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Optimized and Approximate Belief Propagation Decoder for Polar Codes

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***Abstract*—The polar code is one among the most effective error correcting code, attributable to the channel achieving property. In this paper, we propose an optimized approximate belief propagation (BP) decoder for polar code for the first time with efficiency in delay. BP decoder is parallel in nature and is more attractive for low-latency applications. Adder is one of the key hardware blocks in BP decoder. By introducing the approximate computation schemes and by using adders such as ripple carry adder and parallel self timed adder, delay can be reduced. The design is verified and synthesized using Xilinx ISE 14.7.**

***Index Terms*— Polar code, belief propagation, approximate computation, Ripple Carry Adder, PASTA adder.**

I. INTRODUCTION

The polar code is a new class of error correcting codes that demonstrably achieves the capacity of the underlying channels [2]. The result of a superb errors correcting performance is non inheritable when the code is satisfactorily long [3]. Among some manuscript's handling the hardware implementation [2] provided a coding structure that arranges all of the message bits in an absolutely parallel method. The absolutely parallel design is attractive but it is not acceptable for long polar codes because of the hardware complexity.

The polar codes are provably ability accomplishing and their regular structure promises energy-efficient codec designs. Different decoding concepts are introduced for polar codes[4-13]. Two main decoding concepts are successive cancellation(SC) and belief propagation(BP). SC decoding is serial and BP decoding is parallel nature. Belief propagation (BP) decoding had drawn lots of interest when creation of the polar codes took place. Based at the component graph representation of the codes [6], authors in [7], [8] had investigated the performance of the BP interpreting. Results showed that BP decoding had particular benefits with regard to the decoding latency and throughput.

The belief propagation (BP) decoding algorithm for polar codes is based on the factor graph representation of the code [7]. Each node is associated with two types of messages: left-to-right messages and right-to-left messages. In every new release, the message replacement will start from the leftmost column to rightmost column, then from the rightmost to leftmost. Adders are primary circuits to implement any mathematical operation in hardware form. Rapid and correct operation of virtual system depends on the performance of adders. The core of each microprocessor, digital signal processor (DSP), and information processing application specific integrated circuit (ASIC) is its data path. It is regularly the vital circuit thing if hardware cost and power dissipation is concerned. So here in this paper the belief propagation decoder (BPD) of polar codes is designed to offer approximated values with high performance in speed by using optimized adders.

I. RELATED WORK

A. Approximate BP Polar Decoder

Before giving information of BP polar decoders, [1] discussed about the division theme first. For (64; 32) polar code and discovered that the values of LLR specifically distributed within the interval of [-35, 35], this implies that one sign bit and 5 integer bits are needed a minimum for quantization to get satisfying performance [9]-[10].

Figure 1 shows factor graph of belief propagation decoding for (8, 4) polar code. Polar BPD illustrated for n-level factor graph [15]. For (8, 4) polar code, 8 represents information and 4 represents frozen bits. 8*(3+1) = 24 nodes are present in 3 level factor graph.

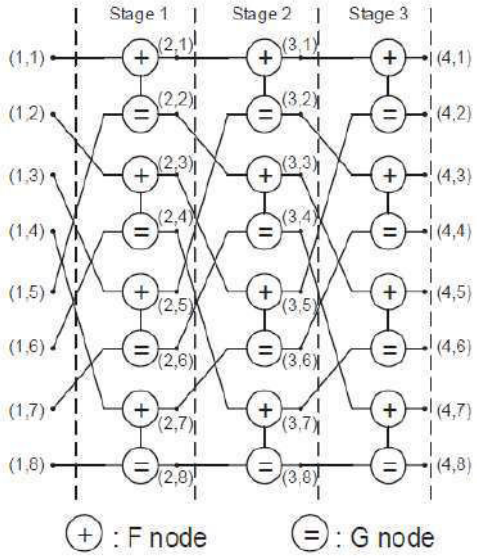

Fig. 1. Factor graph of BP decoding with N = 8

If $(p_{[n-1:k]}) \geq (q_{[n-1:k]})$, then the approximate G node predicts $(s_{[n-1:0]}) = (q_{[n-1:0]})$. Otherwise we have $(s_{[n-1:0]}) = (q_{[n-1:0]})$. However, while $(p_{[n-1:k]}) = (q_{[n-1:k]})$ and the neglected k bits of 'p' is small that those of q, got a wrong result. Supposing that p and q are random numbers with uniform distribution, then the chance of $(p_{[n-1:k]}) = (q_{[n-1:k]})$ and the possibility of the $(p_{[k-1:0]}) < (q_{[k-1:0]})$ are derived as follows:

$$P\left(p_{[n-1:k]} = q_{[n-1:k]}\right) = \frac{1}{2}^{n-k} \quad (1)$$

$$P\left(p_{[k-1:0]} = qb_{[k-1:0]}\right) = \frac{2}{2^{n+1}}^{k-1} \quad (2)$$

B. *Approximate Architecture for G Node*

Generally, LLR messages are in the form of sign magnitude. The purpose of G-node is magnitude comparison for finding minimum number from the inputs. In conventional G-node, almost all bits from MSB to LSB are need to be compared to find minimum number. There might be a chance of delay with conventional G-node to find which is small. Conventional G-node result in a long time as well as high power consumption. The error rate(ER) for the approximated G-node is represented in equation (3).

$$\text{ER}=\frac{1}{2}^{n-k}.\frac{2^k-1}{2^{k+1}}=\frac{2^k-1}{2^{k+1}} \quad (3)$$

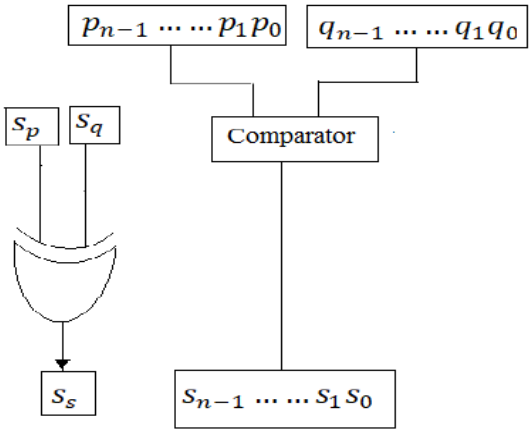

Fig 2: Conventional G node.

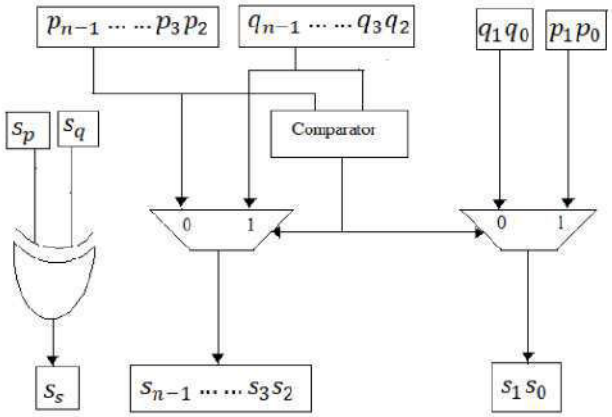

Fig. 3. Approximate architecture for G-node

According to (3) for a specific n, a bigger k will purpose more overall performance loss and less hardware in take [12]. Half of-rate polar codes with code period N = 64 for simulation used in [1]. The quantization scheme includes 1 sign bit, 5 integer bits, and three fractional bits.

C. *Approximate Architecture for F Node*

Notice that the conventional F-node suffers from long delay because of change in information format. Also, delay and hardware utilization increased due to AOU and comparator in traditional structure. So, in this phase, an efficient approximate structure for F node is shown in Fig. 4. For this approximate architecture, subtraction is at once executed rather than doing data conversion before computation. As a result, we only want one data format conversion for F node. $m_a + m_b$ & $m_a - m_b$ are computed at a time and the value of m_s is selected from those values. When S_a ^ S_b= zero, the F node puts in force $m_a + m_b$. Otherwise, it implements $m_a - m_b$. When $m_a \geq m_b$, S_s =S_a. Otherwise, $S_s = S_b$.Approximate computation schemes are added to alleviate the contradiction between higher throughput and hardware consumption. Add one unit (AOU) plays most important role in very last computation. In Fig. 5 shown below, only add 1 to the m low-order bits of the input data. In addition, the carry out generated when including one is dropped without being propagated to MSB bits. These m low-order bits are set to 1, if the carry out bit is equal to 1.

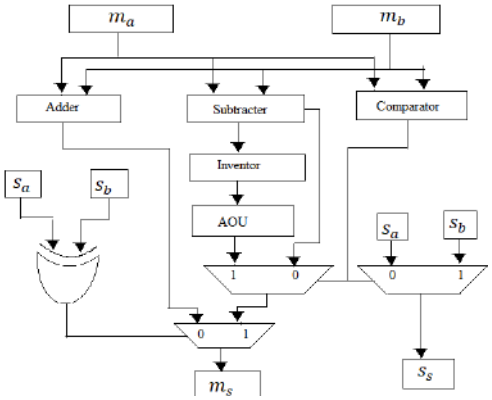

Fig. 4. Approximate architecture for F-node

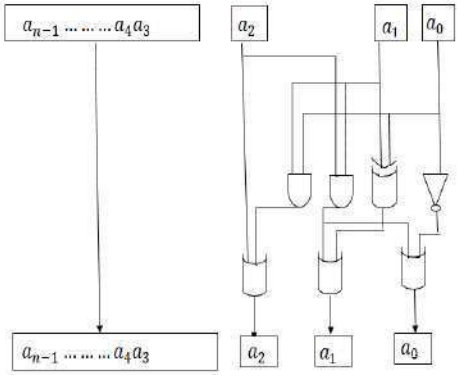

Fig 5: Block Diagram of Approximate AOU

I. PROPOSED WORK

The approximation-based circuits of F-node is modified to attain delay efficiency; by changing various types of adders and their variation in terms of delay are observed. Fig. 2 gives the

conventional architecture of G node and approximate circuit is shown in the Fig. 3.

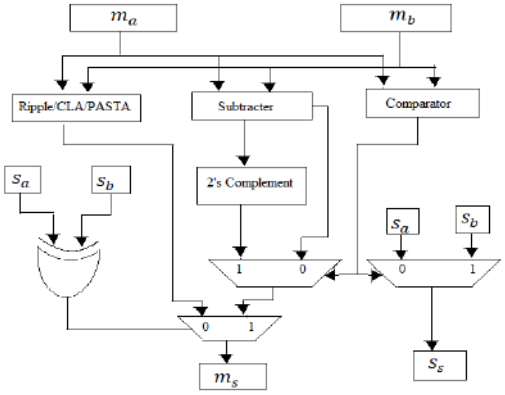

Fig 6: Proposed F node.

Figure 6 shows proposed F-node. When compared to existing architecture of F-node, the proposed architecture shows the reduction in terms of area. Here m_a and m_b are the inputs and m_s is output. Here the adder which plays a major role in computation in F-node is modified. The add one circuit and inventor is replaced by 2's complement block. The performance of the F-node is verified by trying different types of adders in it. The adders considered are ripple carry adder, and PASTA adder.

A. *Ripple Carry Adder*

This method is an asynchronous addition networks. Linking the N full adders printed material N bit Binary adder. In this perform of going before entire adder turns into the enter bring for the following complete adder. It ascertains total and convey as indicated by the accompanying conditions.

$$S_i = A_i \hat{} B_i \hat{} C_i \quad (4)$$

$$C_{i+1} = A_i.B_i + B_i.C_i + C_i.A_i \quad (5)$$

Where i = 0, 1, 2, 3 …n-1

RCA is the slowest in all adders yet anyway exceptionally smaller in size. If the ripple carry adder(RCA) is completed with the useful resource of concatenating N complete adders, the delay of such an adder is 2N gate delays from C_{in} to C_{out}.

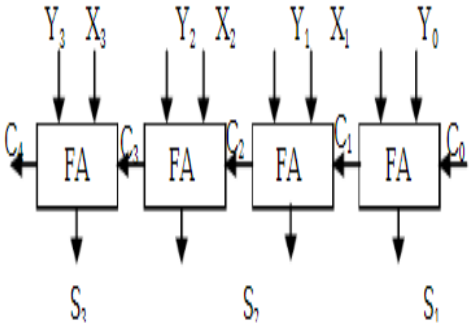

Fig 7: Block Diagram of RCA

B. *PASTA Adder*

Another adder is Pasta adder, the general block figure of the Parallel Self-Timed Adder (PASTA) is exhibited in Fig.8. Multi bit adders frequently developed from single piece adders utilizing combinational and successive circuits for offbeat or synchronous structure.

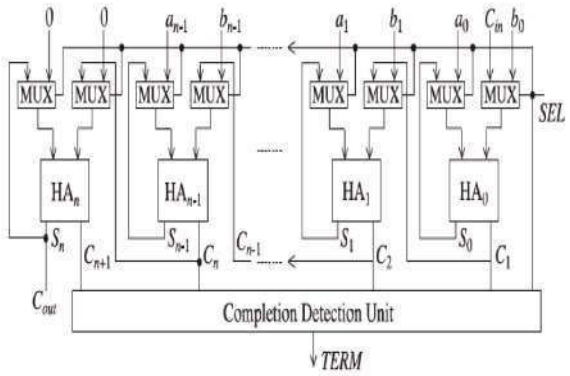

Fig 8: Parallel self- Timed adder.

The contribution for two-input multiplexers relates to the request acknowledgement flag and can be a zero to one amendment signification by SEL. It will initially choose the real operands among SEL equal to zero and can change to input/convey ways that for ensuing cycles utilizing SEL equal to one. The adder ab initio acknowledges two operands to perform half-additions for every bit. during this manner, it emphasizes utilizing previous created convey and aggregates to perform half-adder over and over till all convey bits are eaten and settled at zero dimension. Ripple carry adder is just arrangement of full adders associated consecutive wherever carry propagates from 1^{st} full adder to last one. Delay is most extreme for this situation on the grounds that the yield won't get produced until the point when convey has proliferated until the last full adder. Convey look forward contains combinational circuit which computes already. Area is to a great extent expanded for this situation. Obviously, delay is substantially less.

II. Results And Discussions

To show the advantage of the proposed approximate F-node over F-node in BP decoder, the relating execution results distinctive types of adders in F-node design is explained. It has shown that the planned approximate BP decoder shows sensible hardware reduction than the correct one. Compared with the prevailing F-node in decoder, the reduction in delay is discovered. The Comparison results are shown in below mentioned table I.

Here the below two tables presents the results (in terms of area in LUT's and delay in nanoseconds) with comparison. Table shows the comparisons between F nodes with different adders.

TABLE I

F-node Comparison with Different Adders

Adders in F-node	Area(LUT's)	Delay(ns)
RCA	51	12.093
PASTA	46	10.431

Figure 8 shows simulation results of F-node. The first waveform represents 8bit output, which is indicated by 'm'. Second waveform represents sign bit output, which is indicated by 's'. Third and fourth waveforms represents 8bit inputs, indicated by 'ma', 'mb' respectively. Remaining two waveforms represents sign bits of inputs, indicated by 'sa' & 'sb'.

Fig 9: F-node simulation result.

Figure 9 shows simulation results of G-node. The first waveform represents sign bit output, which is indicated by 'sz'. Second waveform represents 8-bit output, which is indicated by 'Z'. Third and fourth waveforms are represents two sign bit inputs, indicated by 'sx', 'sy' respectively. Remaining two waveforms represents 8-bit inputs, indicated by 'X' & 'Y'.

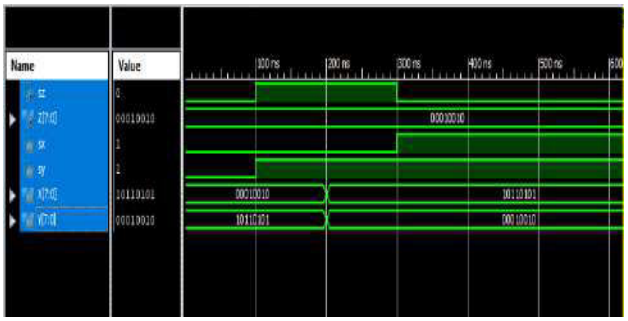

Fig 9: G-node simulation result.

Fig 10: BPD simulation result.

Figure 10 shows simulation results for BPD. The first eight waveforms are represent final output, which is indicated by d1, d2, d3, d4, d5, d6, d7 & d8 respectively. Next eight waveforms represent inputs, which is indicated by u1, u2, u3, u4, u5, u6, u7 & u8 respectively.

III. Conclusion

In this paper, optimized and approximation supported BP polar code decoder is implemented. The results shows that an approximate computation method causes negligible performance degradation compared with the standard one in addition to reducing the delay. Delay seems to improve even more (13.74% for 8 bits) using PASTA adders/subtractors in F-node of BPD. This approximation of architecture can be applied for other polar decoders in future.

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MODELLING OF NON-LINEAR SYSTEMS USING SOFT COMPUTING TECHNIQUES FOR USE IN CONTROLLER DESIGN

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ABSTRACT
Modelling of a process can be data-driven using techniques such as System Identification or based on first principles. With system identification, the process model is identified by acquiring and processing raw data from a real-world system and choosing a mathematical algorithm with which to identify a mathematical model. Various kinds of analysis and simulations can be performed using the obtained model before it is used to design a model-based controller. However, it should be noted that a mathematical model is never a perfect alternative to the real life process. Nevertheless, a reliable modelling exercise needs to be adopted so that the process or model mismatches remains as small as possible. Modelling of the processes using the soft computing proves to be one of the best techniques with minimal model mismatch. And this project aims at modeling non-linear systems using soft computing techniques. The model is generated using fuzzy, neural and neuro-fuzzy techniques using real time data sets. The validity of the models is then compared by taking mean-square error as performance criteria.

1.1 INTRODUCTION ABOUT THE PROJECT

The project aims at modelling non-linear systems using soft computing techniques like neural networks, fuzzy and ANFIS. The nonlinear systems considered for modelling are Conical Tank System (CTS) and Quadruple Tank System (QTS). In CTS the non-linearity is due to its shape and QTS has performance limitations due to loop interaction and multivariable right-hand plane zeros. In fuzzy modelling the T-S fuzzy model proposed by Takagi and Sugeno described by IF-THEN rules is used for representing local input-output relations of non-linear systems. The model output is exactly mapped to plant or system output by using various clustering techniques. A neural network is a massively parallel distributed processor made up of simple processing units called artificial neurons which has a natural propensity for storing experimental knowledge. Here using neural fitting models of CTS and QTS are formed using input-output data set. The neural fitting helps to exactly fit between a set of input numerical data set and output numerical data set. Then modelling is done using ANFIS technique to obtain accurately mapped model. ANFIS uses hybrid learning technique for forming the model. ANFIS uses adaptive learning capability of neural network and transparency of fuzzy for modelling. All the above methods are done by using input – output data. Then root mean square error (RMSE) of each model is verified to analyse best modelling technique among these three soft computing techniques.

2. SYSTEM DESCRIPTION

2.1 CONICAL TANK SYSTEM

Figure 2.1 Laboratory setup for conical tank system

The conical tank process is a type of nonlinear process in which the nonlinearity is due to its shape. Here input variable is the flow rate of water into the tank and output variable is the level of the tank. The level of the water in the tank is measured by means of the differential pressure transmitter and is transmitted in the form of a current signal of 4-2O mA to interfacing hardware of the PC. After implementing the concerned control algorithm in the PC, the control signal is transmitted to the I/P converter in the form of a current signal of 4-20mA which then passes the air signal on to the pneumatic control valve. The pneumatic control valve is actuated by this signal to produce the required flow to the process tank. There is a

constant circulation of liquid in the system. For the purpose of modelling the conical tank system the open-loop input-output data is used. The Figure 2.1 shows the laboratory setup of conical tank system.

2.2 QUADRUPLE TANK SYSTEM

Figure 2.2 Laboratory setup for quadruple tank system

The Quadruple tank process is a laboratory process that consists of four interconnected tanks and two pumps. The process inputs are u1 and u2 (input voltages to pumps, (0-10 V) and the outputs are y1 and y2 (voltages from level measurement devices (0-10V). The target is to control the level of the lower two tanks with inlet flow rates. The output of each pump is split into two using a three way valve. Thus each pump output goes to two tanks, one lower and another upper, diagonally opposite and the ratio of the split up is controlled by the valve. With the change in position of the two valves, the system can be appropriately placed either in the minimum phase or in the non-minimum phase. Let the parameter γ be determined by how the valves are set. The Figure 2.2 shows the laboratory setup of quadruple tank system.

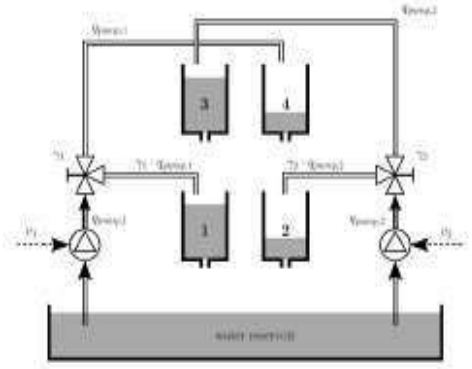

Figure 2.3 Schematic diagram of quadruple tank system

. Consider the Figure 2.3, if $\gamma 1$ is the ratio of the first tank, then $(1-\gamma 1)$ will be the flow to the fourth tank. The voltage applied to pump 1 is V1 and the corresponding flow is k1V1. The parameters $\gamma 1$, $\gamma 2$ ε (0, 1) are determined from how the valves are set prior to an experiment. The flow to tank 1 is $\gamma 1$k1V1 and the flow to flow tank 4 is $(1- \gamma 1)$ k1V1 and similarly for tank 2 and tank 3. The acceleration due to gravity is denoted by g. The measured level signals are y1=kch1 and y2=kch2.e position of the valve. With the change in position of the two valves, the system can be appropriately placed either in the minimum phase or in the non-minimum phase.Let the parameter γ be determined by how the valves are set. The Figure 2.2 shows the laboratory setup of quadruple tank system.

3. ALGORITHM

The flowchart given by Figure 3.3 shows the steps involve in ANFIS training. In this, first the training and checking data i.e. input-output data set will be loaded to ANFIS. The training data is used for training the FIS and checking data is used for testing or validation purpose. Then using the hybrid algorithm the premise parameters of input membership functions and consequent parameters of output linear models are optimised to meet the performance index. Then training is done till the given epoch count or error tolerance is reached. The trained FIS is then checked and validated using the given checking data. For CTS the FIS generated using FCM and subtractive clustering are loaded as initial FIS for ANFIS. Then ANFIS training is provided for data set after selecting grid partitioning too to use grid partitioned FIS as initial FIS. The same procedure is followed for QTS also but it is done separately for tank 1 and 2.

Figure 3.1 Flow chart of ANFIS training

4. RESULT

4.1 MODELLING OF CONICAL TANK SYSTEM

4.1.1 Comparison between Neural Network Model Output and System Output

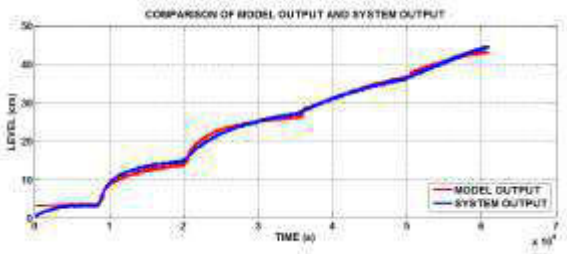

Figure 4.1 Comparison between neural network model output and system Output

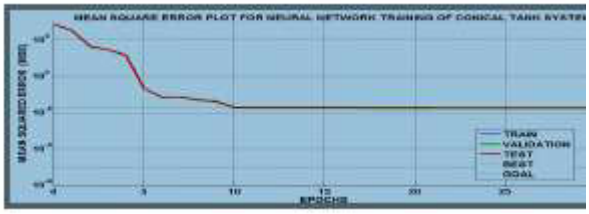

Figure 4.2 Root mean square error plot for neural network training

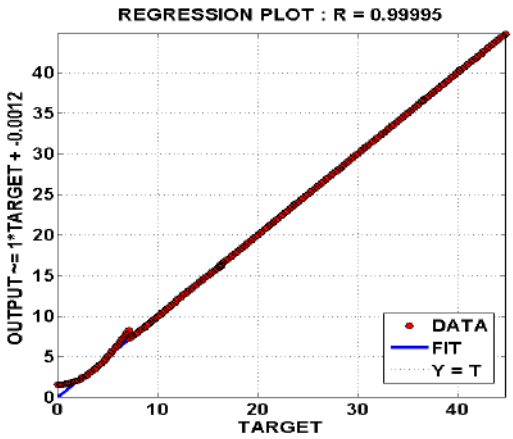

Figure 4.3 Regression plot for neural network training of conical tank system

4.1.2 Comparison between Fuzzy Model Output and System Output

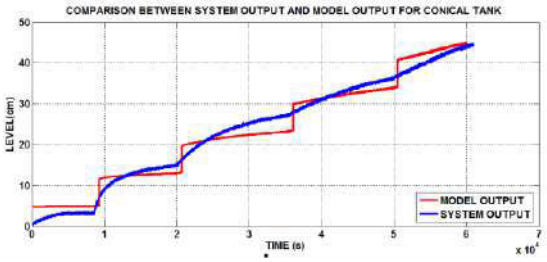

Figure 4.4 Comparison between FCM clustered fuzzy model output and system output

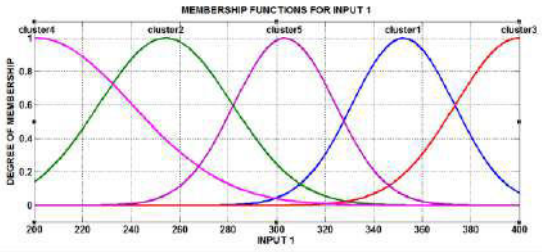

Figure 4.5 Membership functions of input 1 of FCM clustered fuzzy model

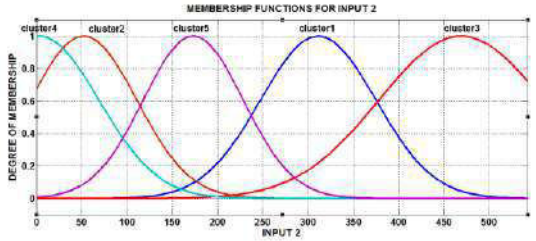

Figure 4.6 Membership functions of input 2 of FCM clustered fuzzy model

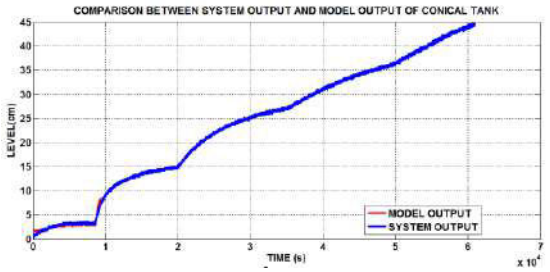

Figure 4.7 Comparison between subtractive clustered fuzzy model output and system output

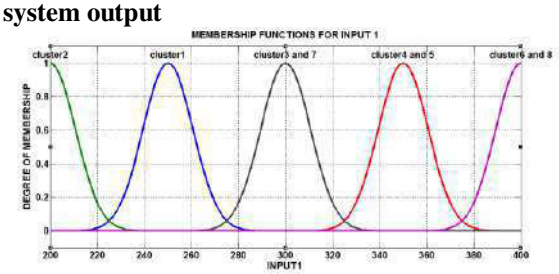

Figure 4.8 Membership functions for input 1 of subtractive clustered fuzzy Model

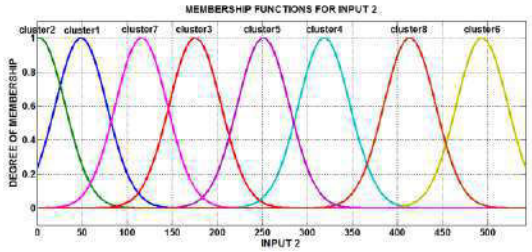

Figure 4.9 Membership functions for input 2 of subtractive clustered fuzzy Model

4.1.2.2 Subtractive Clustering

The results show that subtractive clustered fuzzy model is very accurate anddoes not require further training. It used eight Gaussian membership functions for mapping input data sets.

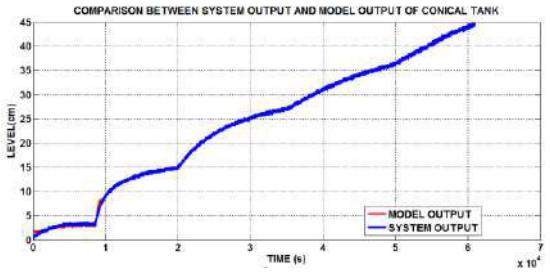

Figure 4.7 Comparison between subtractive clustered fuzzy model output and system output

The Figure 4.7 shows how accurately the fuzzy model models the conical tank system. It is seen that the fuzzy model output overlaps the real time output of CTS. The Figure 4.8 and Figure 4.9 show the membership functions of inputs.

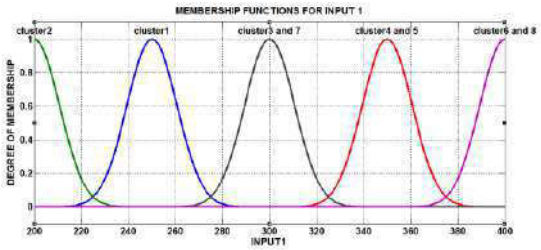

Figure 4.8 Membership functions for input 1 of subtractive clustered fuzzy Model

5. CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

The project deals with obtaining accurate representation of non-linear systems by applying soft computing techniques like fuzzy, neural network and ANFIS. The results showed that by using soft computing techniques non-linear systems can be accurately modelled. The accuracy of the models lies in selection of input and output parameters. The input-output data should contain the process characteristics of the system for it to be exactly modelled. Two non-linear systems having different types of non-linearities is thus exactly modelled and validated by taking root mean square error as performance index. ANFIS having the advantage of both fuzzy and neural networks had minimum RMSE .

5.2 FUTURE SCOPE

It is generally not possible to derive an accurate model of a process or plant especially with nonlinearities. If a reliable model is not available, it is quite difficult to design a controller producing desired outputs. Traditional modelling techniques are rather complex and time consuming when we incorporate entire dynamics of the process. By the application of soft computing technique any non-linear system can be modelled. The model can be further used for design of model based controllers. The models thus developed can be used in designing model based control schemes which offers robust controller performance.

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Analog optical Transmitter

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Abstract **- A low cost analog optical transmitter has been developed for optical communication applications. The new device is characterized and the results show very good performance over a wide frequency band. We have achieved a gain flatness of less than 1dB from 0.8 GHz to 2.3GHz which makes the device suitable for fiber optic communication.**

Index Terms **- Optical fiber; Analog modulation; Optical transmitter.**

I. INTRODUCTION

Recent communication uses optical means for transporting data. Introduction of fiber optic techniques makes the current communication system very fast and reliable. Main advantage of optical fiber communication are higher bandwidth and low transmission loss. Two different techniques used for optical communication are analog modulation and digital modulation. Digital fiber optic links are widely used for transporting voice and data for high speed internet [1]. Many other applications require analog modulation like microwave multiplexed signals [2, 3], subscriber services using hybrid fiber/coax [4], video distribution [5], Fiber to the Antenna [6] and Fiber to the Home [7].

The major components of fiber optic communication are a light source capable of fast modulation, an optical transmission medium and high speed photodetectors. Today fiber optic link is widely used to transmit and receive microwave signals from satellite antenna [8]. Coaxial cable has high attenuation (several hundred dBs/km). Main problem of analog modulation on optical signal is linearity issues over wide frequency band. Designing proper impedance matching circuit is also very critical for wide frequency band. In this paper we introduce a low cost device which is suitable for a wide variety of applications in optical communication

II. DESIGN PRINCIPLES

Transmitter converts the RF input signal to analog optical signal. This can be done by modulating the intensity of optical signal with RF input signal. This is amplified by a monolithic RF amplifier and then fed to the laser diode. Continuous wave intensity modulation of the RF signal on optical output is performed with a laser diode.

The Laser is driven by a Laser controller circuit configured with a laser driver; WLD3343 (Wavelength electronics Inc.). The required bias current for the Laser is set by the laser driver. When laser diode is biased with a current larger than the threshold current, ITH, the optical output power increases linearly with increasing input current. Analog links take advantage of this behavior by setting the dc operating point of the laser in the middle of this linear region. The laser driver provides proper bias current for laser diode. The major components of the transmitter circuit are: laser diode, laser driver, RF amplifier, bias tee and impedance matching network. Figure 1 shows the block diagram of the transmitter circuit.

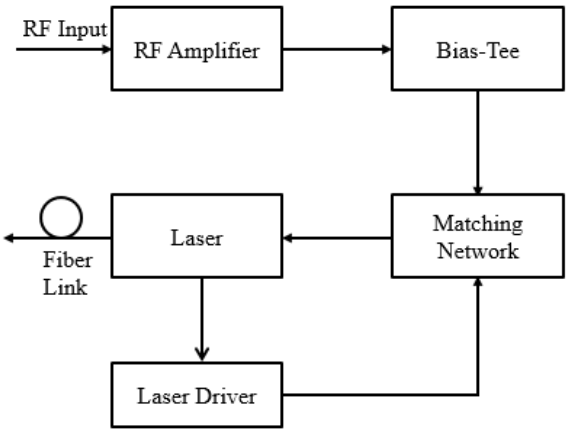

Fig. 1.Block diagram of fiber optic transmitter.

The Laser Diode used in the transmitter is an un-cooled DFB laser (DFB-1550-C5-2-A4-SA-A-A, Applied Optoelectronics Inc.) with coaxial package. Laser diode is characterized by measuring optical output power for different operating currents and threshold current is estimated as 15 mA from this data. At 70 mA laser output power reaches 5 mW (7 dBm). Laser diode is operated in the linear region of the L-I (Light Intensity-Current) curve between threshold (15 mA) value and maximum operating current, 70 mA. Constant DC bias current for laser is set at 40 mA which is almost the mid value of the operating ranges from 15 to 70 mA. Laser bias current is set at middle to avoid clipping of output signal which ensure the linearity. RF input signal is also applied to the laser diode which is superimposed to the constant DC bias current. RF signal modulates the intensity of the optical output power. An inbuilt photo detector (back facet monitor diode-BFM diode) in the laser module helps to monitor the optical output of the laser. Input RF signal is amplified by the GAL-5 (Mini Circuits).
Proper matching circuit (pi section network) using reactive components (inductor and capacitors) were designed 50Ω impedance with low impedance laser diode. To improve the gain flatness, a 15Ω resistor is added with load impedance.

III. Results and Discussion.

The transmitter circuit is tested using a calibrated network analyzer. The frequency is swept from 0.8 to 2.3 GHz. The RF power from the network analyzer is set to 0dBm. The optical power level of the laser diode output is set to 1mW (0 dBm). Transmitter circuit output (optical) is connected to the wide band optical to electrical converter (O/E converter) using a suitable fiber optic patch cord. The RF port of the O/E converter is connected to Port 2 of the network analyzer. O/E converter is basically fiber optic receiver equipment which has an optical input port and a RF output port. O/E converter receives the modulated optical signal from the transmitter circuit and converts to equivalent electrical signal. Figure 2 shows the test setup for characterizing transmitter circuit.

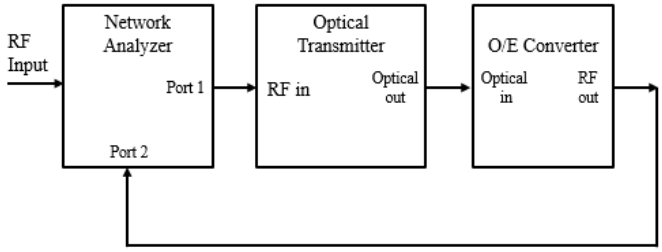

Fig. 2. Transmitter circuit test setup.

Performance of the transmitter circuit is analyzed by plotting S21 (forward gain) and S11 (return loss) data with network analyzer. Figure 3 shows the measured reflection and transmission characteristics of transmitter circuit. Results show that return loss of the transmitter is better than -10 dB and gain flatness is less than 1 dB from 0.8 GHz to 2.3 GHz.

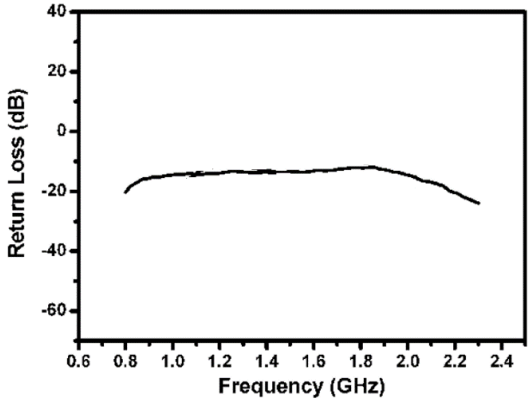

Fig. 3. Return Loss (S11) of Transmitter circuit

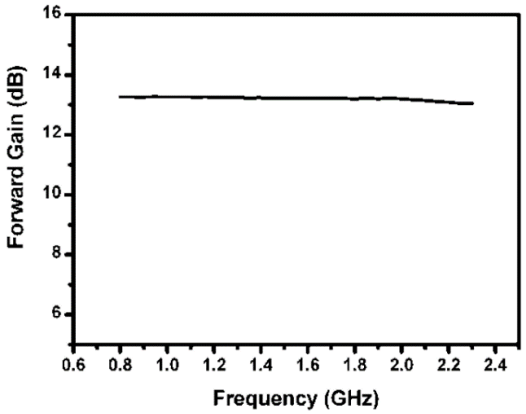

Fig. 4. Forward gain (S21) of Transmitter circuit

III. CONCLUSION

A simple and low cost design for wideband analog optical transmitter is presented here. The developed module gives good transmission and reflection characteristics performance over a frequency band of 0.8 GHz to 2.3 GHz. A gain flatness of less than 1 dB and return loss of minimum -10 dB is obtained for transmitter. The wideband performance of the system makes the device suitable for a number of useful applications like bidirectional optical communication link, FTTH/FTTA applications etc.

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VISUALIZATION CREATED IMAGE FAKE FINDING

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Abstract: **Nowadays, digital pictures may be simply changed by victimization superior computers, subtle photo-editing, tricks package, etc. These modifications will affect the authenticity of images, from law, politics, the media, and business. Detecting forgery in digital pictures is one in every of the most important analysis activities within the current time. In general, altering the digital image may disturb some underlying vision-based regularities that arise due to world, lens and sensor etc. Under this assumption, this paper presents new vision based image scientific tool lighting color based image forensic.**

Keywords**: Forensic, Forgery, Vision, Watermarking**

I.INTRODUCTION

The development of up to date digital image process techniques, the individuals will simply alter the content of digital image with none clues, typically in laws, politics, media and business etc. digital image forgery detection, is Associate in Nursing approach to find mechanically tampered county in digitally altered image, it classes into 2 approaches, specifically watermarking and forensics.

Watermarking is a lively approach; desires previous data to verify the credibility. Forensics could be a blind approach; it doesn't want any previous data to substantiate the credibility of the image. it's classified in to 2 ways specifically applied math primarily based image forensics (SBIF) and vision based image forensics (VBIF). SBIF verifies the credibility by gauging the statically inconsistencies like interference artifacts [1], Resampling detection [2], detector noise consistency [3], etc.

The natural properties from a range of sources, just like the world, the lens, and also the detector are accustomed prove the credibility. VBIF uses the properties and find the tampered region by activity lighting inconsistency in lambertian surface in single light [4], and aberration deviation [5], No single technique provides complete detection of solid pictures .devising a replacement techniques can strengthen the proof of forgery.

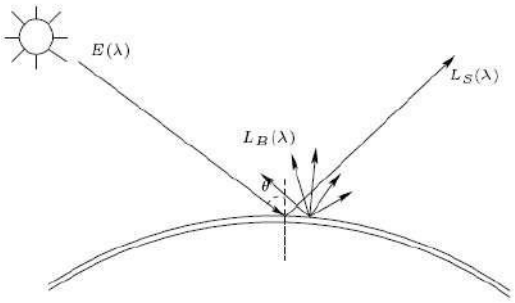


Fig.1: Dichromatic Reflection Model

The Color characteristic is one amongst the vital key to find the digitally altered image, however it's arduous to match the colour of 1 object with the opposite. Suppose a photograph is taken to a lower place a continuing illumination [6], the illumination color of all objects ought to be constant throughout the whole image. If image is altered, the illumination consistency could also be altered. during this paper we have a tendency to propose a brand new technique by estimating the illumination color consistency by detection the mirror like region.

II.IMAGE FORENSIC USING DICHROMATIC MODEL

The Color characteristic is one in every of the necessary key to find the digitally altered image, however it's laborious to match the colour of 1 object with the opposite. Suppose a photograph is taken to a lower place a continuing illumination, the illumination color of all objects ought to be constant throughout the complete image. If image is altered, the illumination consistency could also be altered. During this methodology we have a tendency to use this property and that we gift a replacement VBIF methodology to find the altered portion within the digital

Image by estimate the illumination modify the reflective region.

A.BASIC COLOR IMAGE FORMATION

The light supply emanates the non-particulate radiation of specific shadowy composition. A photographic image could also be captured beneath totally different sources of illumination. Even in outdoor photography, the natural lightweight could modification throughout the day in shadowlike composition. The spectral composition of the well-lighted supply may be measured in terms of the normalized color property given by each the RGB values and r-g values [12].

Color image formation will be explained with the assistance of the dichromatic reflection model [13]. in keeping with this model, reflection of any non-homogeneous materials could also be mixture additive reflection and diffuse reflection. For Associate in Nursing object lit by one supply the mirrored light-weight will be modulated as represented in equation (1).

(1)

Where SS (λ) and SB (λ) area unit spectral surface coefficient for surface and body part and E (λ) is that the color of the supply light-weight. for many form of materials spectral surface coefficient for the surface area unit constant over the actinic ray. This equation will be rewritten in terms of RGB device response as is represented in equation (2)

(2)

Where R, G, and B: be the detector values in the image .S and B be the surface and body parts. Avoirdupois unit (λ) and LS (λ) are going to be 2 vectors of surface and body parts that spans the 2 dimensional plane referred to as dichromatic plane. The dichromatic lines for one source of illumination represented in Figure.2

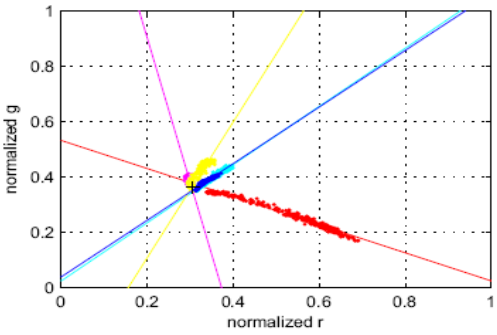


Fig. 2: Dichromatic Reflection model

B.FORGERY DETECTION BY ESTIMATING ILUMINATION COLOUR IN SPECULAR REGION

Detecting cast region in digitally altered image includes following route. The forgery detection algorithmic rule are often delineate in Figure.3

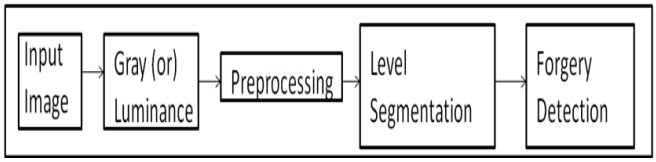


Fig.3 The Flow Diagram of Forgery Detection Algorithm

Specular region detection is crucial in estimate of illumination color. Perceiving mirror like regions involves ulterior preprocessing operations like filtering, distinction stretching [14] etc.

C.PREPROCESSING

Input image is reborn in to grey or brightness for quick process and to research the link between white and black space. The binomial low pass filter and distinction stretching accustomed find the mirror like regions accurately [15].the flow sheet of preprocessing operations area unit delineated in Figure.4

Fig.4: The Flow Diagram of Preprocessing Operations

Gray (or) luminance: Before giving input to the extent segmentation the user got to choose the reflective regions properly. Choosing the reflective regions within the color image are very little advanced. the primary step is to convert associate input image of a digital to a gray scale for police investigation the reflective region. The gray scale image is

analyzed by a relationship between a white square measure and a black for the input image, simply and created to quicker process than a color image.

Binomial Low Pass Filtering: The binomial low pass filters (BLPF) ar utilized in order to accurately notice the mirrorlike region from the digital image and take away a noise of the image. The BLPF is applying a size of mask (e.g., 3×3, 5×5) in line with the dimensions of mirror like regions within the pictures [15].

Contrast Stretching: The image may be eliminated to a steep intensity transition of the item except the lighting gradation fashioned naturally the objects from the image. Adapt a high distinction from the image. The distinction ought to be clearly the highlights and shadows fashioned by the sunshine from the image.

D.LEVEL SEGMENTATION

Trim down the amount of levels to indicate up the mirror like regions within the image. The 8-bits for grey image levels square measure Convert 256 into ten [16]. The luminousness image levels diminish into ten .from the paper they need reduced up to fifty levels, the sample reduction of 256 to ten levels for a grey image square measure represented in Fgiure:5

GRAY	LUMINANCE	GRAY	LUMINANCE
0-25	16-38	0	16
25-50	38-60	25	38
50-75	60-82	50	60
75-100	82-104	75	82
100-125	104-126	100	104
125-150	126-148	125	126
150-175	148-170	150	148
175-200	170-192	175	170
200-225	192-214	200	192
225-255	214-236	225	214

Fig.5: Level Segmentation

E.FORGERY DETECTION USING DICHROMATIC PLANE

Tominaga and Wandell such as, some way to approximate the fuel colourize the image with the assistance of the dichromatic reflection model. reflective regions hold dominant fuel color, its inputs to the dichromatic reflection model. R G B vectors of that regions square measure rotten victimisation principal element analysis and mapped in to line in dichromatic reflection model that may span the complete dichromatic plane. Objects beneath identical supply can ran into within the line provides the fuel vector and conjointly gives the color property values that fuel color. The steps up to dichromatic plane square measure delineated in Figure 6.

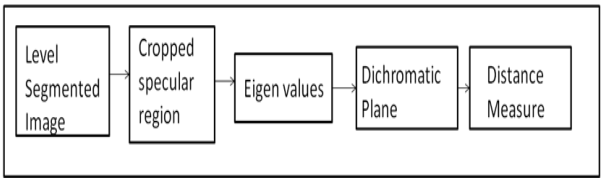


Fig.6 : The steps to plot dichromatic plane

Cropped Specular Regions: To estimate the illumination colourizer the image, regions round the reflective highlights square measure thought-about. once detective work the reflective regions user inputs the reflective regions of each object from the amount divided image to the dichromatic model

Eigen Values: Since the reflective regions hold the dominant colourizer the image Eigen values of every color matrix of reflective regions square measure calculable to plot because the line within the dichromatic reflection plane that may span the complete plane

Distance Measure: The intersection points of any 2 lines in dichromatic plane will be calculable by victimization the formula delineated in equation (14) & (15). Consider the point of any two lines as (x1, y1) (x2, y2) for line1 and(x3, y3) (x4, y4) for line 2

(14) (15)

By work the points within the on top of equation 3&4 offer 2 linear equations with 2 unknowns by resolve the values of that 2 unknowns x & y illustrate the intersection points of any 2 lines. we have a tendency to known a solid region, by considering anyone line as a reference line within the dichromatic plane and located the intersection points of all different lines with relation to the reference line and therefore the tampered regions are noticed by means that of

taking the gap of all intersection points the purpose with the utmost distance can shows the proof of forgery. the gap between 2 intersection points are obtained by victimization Euclidian distance are shown in equation (16)

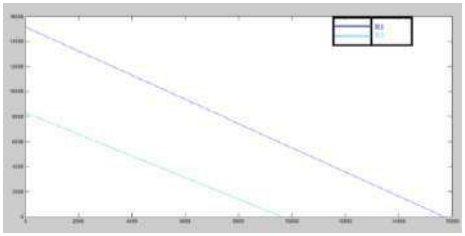
Let P1, P2 be the two points and p11, p12, p21, p22 be the vectors of that points

 (16)

The line that doesn't meet with alternative lines and therefore the line that doesn't have shut intersection are a tampered object.

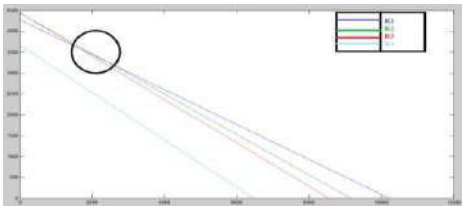
Dichromatic planes area unit essentially classified in to four categories1) plane with 2 objects with no intersection 2) Plane with quite 2 object while not intersection of tampered object 3) Plane with quite 2 objects with intersection of tampered object 4) Plane with shut intersection while not tampered object area unit shown in Figure seven (a) - (d).

Dichromatic plane for tampered object without intersection points



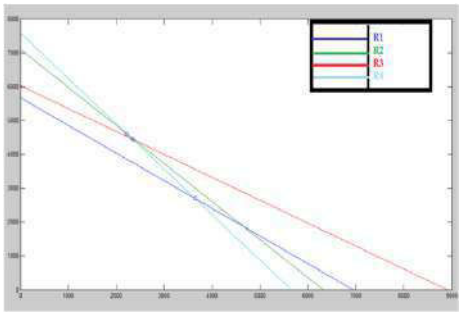
(a)

Dichromatic plane for tampered image without intersection point



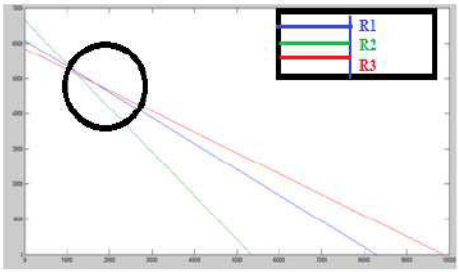
(b)

Dichromatic plane for tampered image with intersection points



(c)

Dichromatic plane for authentic image



(d)

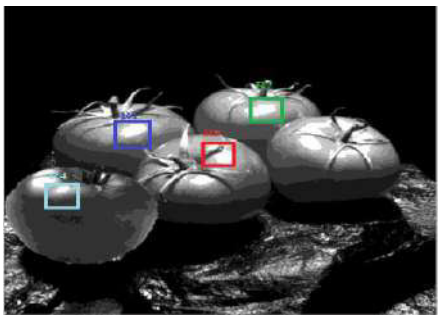
Fig.7 (a) indicates image as a non-authentic image but it fail to spot which region is tampered (b) indicates region R4 (sky blue color line as tampered object because it don't have intersection point others (c) plane describes that region R1 (blue line) as tampered region .it intersection points is not close to other three regions (d) an authentic image intersection points are very close

II.RESULT AND ANALYSIS

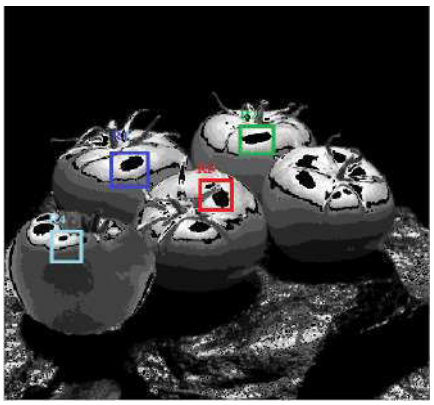
The experiments were dispensed in a very system having Intel® CoreTM2 couple processor T6600 with speed two.2 GHz and 4GB RAM. The implementation was done by mistreatment MATLAB 7 .6. Solid pictures were created by repeating the objects from one image and pasting on another image that's underneath completely different illuminants conditions was done by mistreatment the picture writing software package Adobe Photoshop. The various cases tested like 1) pictures with no intersection for a tampered object. 2) Pictures with intersection for a tampered object.3) pictures with no intersection tampered object with 2 objects.

Dataset 1: A tampered image with no intersection point

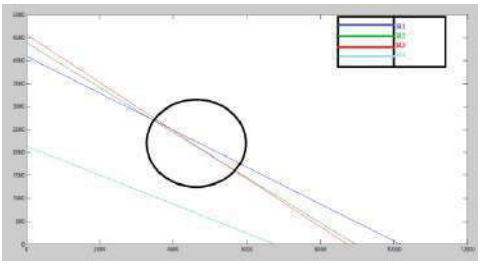
(a)



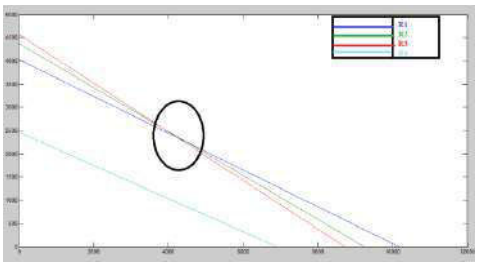
(b)



(c)



(d)

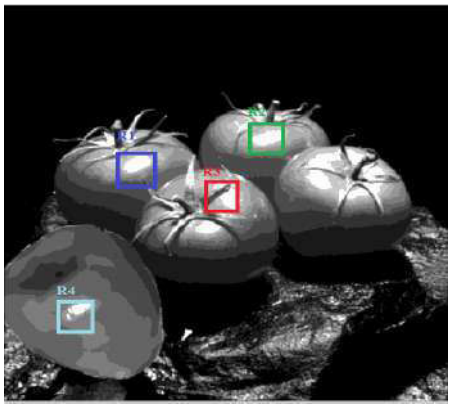


(e)

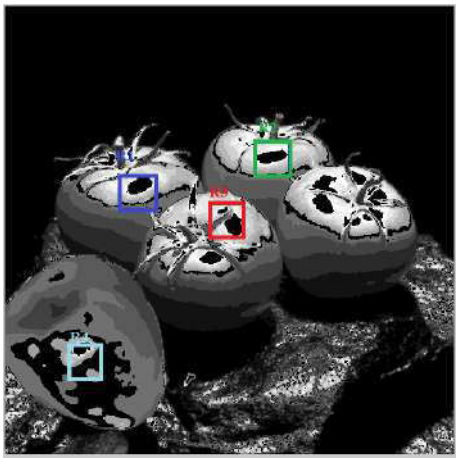
Fig.8 (a) Input image (tampered image from Photoshop) (b) User interactive cropped regions after level segmentation using gray. (c) User interactive cropped regions after level segmentation using luminance. (d) Estimated dichromatic lines for cropped regions in gray level segmented image (indicates R4(sky blue) line as a tampered object it does not have intersection with other lines).(e) Estimated dichromatic lines for cropped regions in luminance level segmented image (indicates R4(sky blue) line as a tampered object it does not have intersection with other lines

Dataset 2:A tampered image with no intersection point

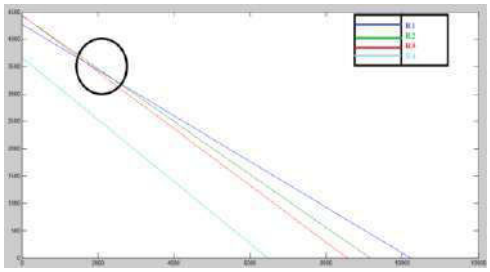
(a)



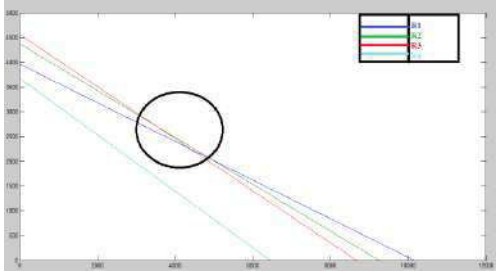
(b)



(c)



(d)



(e)

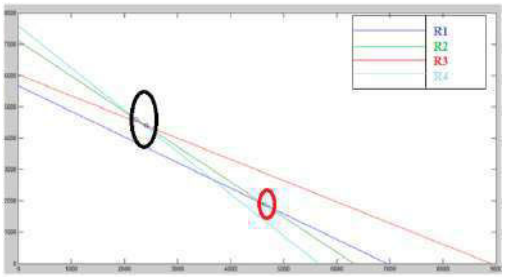
Fig.9 (a) Input image (tampered image from Photoshop) (b) User interactive cropped regions after level segmentation using gray. (c) User interactive cropped regions after level segmentation using luminance. (d) Estimated dichromatic lines for cropped regions in gray level segmented image (indicates R4(sky blue) line as a tampered object it does not have intersection with other lines).(e) Estimated dichromatic lines for cropped regions in luminance level segmented image (indicates R4(sky blue) line as a tampered object it does not have intersection with other lines)

Dataset 3: A non-authentic image downloaded from with intersection point

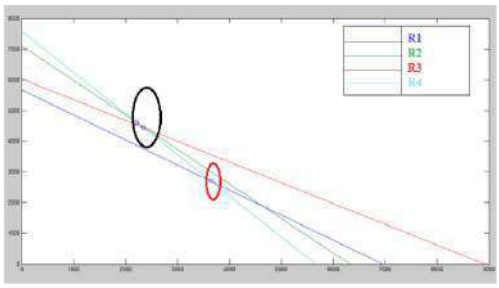
(a)

(b)

(c)



(d)



(e)

Figu.10: (a) Input image (tampered image from Photoshop) (b) User interactive cropped regions after level segmentation using gray. (c) User interactive cropped regions after level segmentation using luminance. (d) Estimated dichromatic lines for cropped regions in gray level segmented image (indicates R1(blue) line as a tampered object its intersection will not close to other three lines).(e) Estimated dichromatic lines for cropped regions in luminance level segmented image (indicates R1(blue) line as a tampered object its intersection will not close to other three lines)

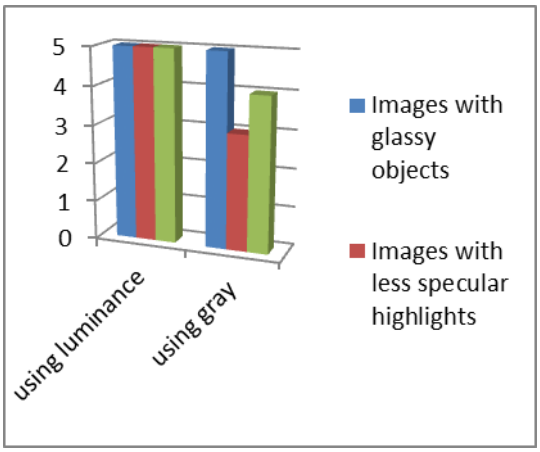
Specular region detection is one in every of the necessary modules within the illumination color based mostly image rhetorical that was detected exploitation 2 ways exploitation light and grey. The accuracy of those 2 ways area unit mentioned in table one Specular region detection is one in every of the necessary modules within the illumination color based mostly image rhetorical that was detected exploitation 2 ways exploitation light and grey. The accuracy of those 2 ways area unit mentioned in table 1.

TABLE 1

ACCURACY OF SPECULAR REGION DETECTION

Types of images	no of image	Using gray	Using luminance
Images with glassy objects	5	5	5
Images with less specular highlights	5	3	5
Images with high specular highlights	5	4	5

Chart 1.The specular region detection using gray and luminance



The input image should have reflective parts. Weak reflective regions square measure enough. and also the reasons we have a tendency to select reflective region detection is user need to choose or crop the reflective

region accurately as a result of for estimating the illumination color image in regions round the reflective highlights square measure thought of. If the image has over one object is tampered it'll show image as a non-authentic image however it'll fail to point that portion of the image is tampered. The higher than tool won't work well for human skins as a result of the mixer of reflective color with human color can have an effect on the belongings of illumination color therefore it'll not manufacture the higher output. These square measure all the a number of the datasets that we have a tendency to utilized in illumination color based mostly image rhetorical square measure shown in figure 8.

Fig.11: Shown some of the datasets that are used in this technique

III.CONCLUSION

In this paper we've got planned 2 totally different techniques- Illumination color based mostly image rhetorical. The technique can turn out higher results for pictures captured underneath constant illumination that possesses reflective regions in it. The planned techniques work well for pictures captured underneath constant illumination however fail to perform underneath advanced lighting atmosphere.

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ANALYSIS AND REDUCTION OF POWER IN ADPLL USING ADIABATIC LOGIC CIRCUITS

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Abstract: With a low power All Digital Phase Locked Loop (ADPLL) becomes more attractive, they offer better testing, programmable, stability and portable telephone in different tests, and ADPLLs can reduce system time and have a better noise immunity. The Digital System Clock Generation All Digital Grid-Locked Loop is widely researched to replace the traditional antilog PLL as the CMOS process technology enters the manometer regime. The purpose of the adiabatic logic technique is to reduce the energy consumption of various functions. Compared to standardized CMOS, losses in untouchable logic represent a big break. Only a handful of adaptation landscapes satisfy our needs, which are responsible for the standard CMOS design flow and PVT variant, and use a manageable number of powerful clocked power supplies. Adiabatic Logic Circuit Technique is designed with a dynamic phase frequency detection ADPLL imagines in a steady 0.25µm CMOS process technology and maximum electrical power consumption of 5.42mW. Adiabatic Logic Circuit with dynamic phase frequency detector is activated in the ADPLL TANNER EDA tool and analyzed to obtain various PFD circuit performance ADPLL which consumes low power.

Keywords: Phase Lock Loop (PLL), Adiabatic Logic Circuits.

1. Introduction

1.1 PHASE LOCKED LOOP

The grid-locked ring or grid lock ring (PLL) is an old technology from the 1930s. This is a control system that creates a release signal associated with the phase of an input signal. The wide range of PLL began with television receivers in the 1940s. PLL was used to synchronize horizontal and vertical curve lenses for coarse pulses. It is used for widespread use in the fields of communication, instrumentation, control systems, and multimedia instruments. Techniques for radio receptions were used for cohesive reception.

Types of PLL

PLL has four types. They are as follow as:

1. Linear PLL (Analog PLL)
2. Digital phase locked loop (DPLL)
3. All digital phase locked loop (ADPLL)
4. Software PLL (SPLL)

In addition, DPLL capable of implementing sophisticated signal processing in IC chips are much more flexible and more diverse than analog PLL. TBL is still referred to as a semi-analog circuit and a hybrid PLL. All digital PLL (ADPLL) and Software PLL (SPLL) have recently attracted more attention. Interest signals may be of any time wave, but usually a sinusoidal or digital clock. PLL is usually divided into broad categories listed on Table 1.

S.NO	PLL	PHASE DETECTOR	LOOP FILTER	OSCILLATOR
1	Linear PLL(analog PLL)	Analog	Analog	Voltage Controlled Oscillator (VCO)
2	Digital PLL(DPLL)	Digital	Analog	Voltage Controlled Oscillator (VCO)
3	All digital PLL (ADPLL)	Digital	Digital	Digitally Controlled Oscillator (DCO)
4	Software PLL (SPLL)	Software	Software	Software

1.1.1 Basic Concepts of PLL

A phase locked loop (Figure 1.1) is a device that locks a release signal grid associated with an input note signal phase. Although there are many different types, it is easy to see like an electronic circuit with a variable frequency oscillator and a discovery at the beginning. Building Discovery Comparing the phase of the signal with the phase of the intermediate signal, adjusts the oscillator to maintain the stages.

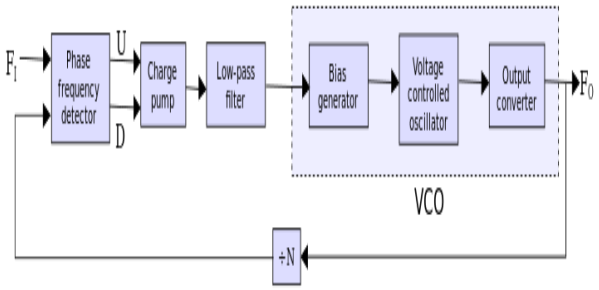


Figure 1.1 Block diagram of Basic PLL

1.3 Basic Operation of PLL

The basic function of PLL can be divided into three steps. They are as follows:

1. Phase detection captures the gap between the two entries and the

mean value generates an error signal that is the ratio of the difference in the difference.

2. A mesh filters then allows the average value to control the VAC frequency and the diagnostic output is used to suppress the high-frequency components.
3. The Oscillator generates an output signal, whose frequency cycle is a linear function of the filter signal control signal.

1.2 OPERATING STATES OF PLL

The PLL has Two operational states, the following:

1. Free running: The feedback loop is open and there is no external input frequency, the VCO swings in the natural frequency.
2. Capture limit: An external input signal is required and feedback loop should be completed. PLL has acquired frequency lock in the state.

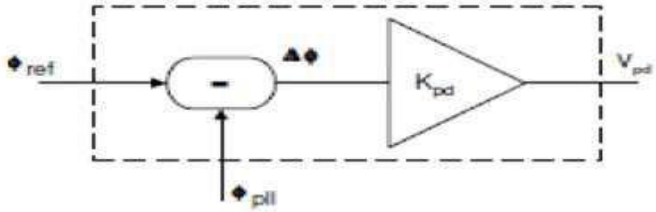
BASIC ELEMENTS OF PLL

A basic PLL is a negative feedback system that consists of

1. A Phase Detector,
2. A Low Pass Loop Filter,
3. A Voltage Controlled Oscillator (VCO) and
4. Feedback path and optional divider

1.5.1 Phase Detector

Stage detection Fig.1.2 can be classified based on various applications and processes. There are two types of building diagnostics, 1. Synopsis Fase Detectors and 2. Square signal build detectors. Cyanosiodile Fase Detector A phase detection gap (- π / 2 to + π / 2). This is an amplifier, which acts as a null memory device. The square signal level detection and sequence are called innovation and are implemented using continuous logical circuits.



1.5.2 Loop Filter

The loop filter is a low pass filter that is used to attenuate the noise and high frequency signal components from the phase detector. It provides a control signal to the oscillator which is proportional to the phase difference between the reference and the PLL output.

1.5.3 Oscillator

Oscillator is the most important building block of the PLL which generates the required clock signal with a controlled frequency. Oscillator can be classified based on the control signal applied as:

1. Voltage controlled oscillator (VCO): The control signal applied is a voltage signal.
2. Current controlled oscillator (ICO): The control signal applied is a current signal.
3. Digital controlled oscillator (DCO): The control signal applied is a digital word.
4. Numerical controlled oscillator (NCO): The control signal applied is a numerical value of the signals.
5. Software based oscillator: The control signal applied through the software.

The main constraints for the VCO are:

1. Phase stability
2. Large frequency deviation
3. High VCO sensitivity
4. Linearity of frequency versus control voltage
5. Capability of accepting wide band modulation.

1. A SURVEY OF RECENT RESEARCHES IN FIELD

Previous research, the adiabatic environmental productivity strongly depends on the effects of parameter variations in the power drop. The decay of the initial voltage is the most important effect on yield. Various effects on energy consumption are given due to indoor and indoor-divergent variations. The three logical families, the Competent Responsibility Rescue Logic (ECRL), the positive feedback of the Adiabatic Logic (PFAL) and 2N-2N2P are comparing the energy saving and operating frequency range. Finally, the differences in power loss due to parameter variations indicate that the logic should be firmly fixed on the family. Yanakidō and many others. [6] A procedure was

proposed
the approach to controlling the factor for the rapidly increasing integration of microleacran Adiabatic Logic with CMOS for low power applications. This paper provides a new half-life tapioca logic family, which uses filler-level cyanosed power clocks such as sensor for digital low power applications. The proposed two phases use adiabatic standard CMOS logic (2PASCL) cycle clocked adiabatic switch and energy recovery policy. By eliminating the diode in the charging path, the high output range is achieved and the diode's power consumption is eliminated. We design and design 2PASCL based NAS, NAND, NOR and Exclusive-OR logic gates with SPAS enabled using SPACE 0.18 MMS technology. For driving pulse gates with equal height for Vdd Sathish Kumar et al et al. [6] have proposed a

The practical approach to a dynamic phase frequency discovery focuses primarily on reducing power consumption and capable of reducing rapid locking and delay time. With a low power all digital grid locked (ADPLL) has become more attractive, they offer better test, programming, stability and portability in different tests, and ADPLL has excellent noise immunity. Time-T-digital converter TDC's goal is to measure the time difference between the rim of the signal. DTC is required for a phase mathematical algorithm through DTC assistance. Reduces the range, thus saving substantial energy. The complete ADPLL system improves the locking capabilities and the system's DTC linear. The design is most appropriate for high-speed grid frequency detection using DPFD technique. The proposed system for dynamic phase frequency discovery is constructed and the associated power is 20 μW.

Salvatore Levantino and many others have been proposed as attractive candidates for digital gut-locked loops with low zitter clock-frequency amplification based on pin-band grid detection. Unfortunately, the buildup size of the phase error, these systems, leads to head cycles of circular cycles like unwanted spots in the spectrum. The random noise that works as building blocks and titering signal will remove those holes. While DASCO, such as ΔΣ-DCO, has an inherent normal resolution, the size of these phenomena can further be analyzed and when the practical spectrum of random noise sources is considered. In this work, the expression of accurate accuracy is calculated in accounting form, introduced by two phase scales and DCO, and DC The noise of the phase, with 1 / F and 1 / f elements. Combine these results,
The proposed analysis and optimization are validated both numerically and experimentally on a 320-MHz digital bang-bang PLL fabricated in a 65-nm CMOS process.

Monoj Kumar et al proposed in the proposed article using the ADPLL design Verilog in FPGA. ADPLL is designed using Verilog HDL. Xilinx ISE 10.1 simulator is used for simulation of the Vellore Code. This paper provides details of the basic set of ADPLL. In this sheet, describes the function of the ADPLL. Its simulation decisions are also discussed using Xilinx. This provides the XPLinx vertex5 xc5vlx110t chip and ADPLL design FPGA implementation in its results. ADPLL 200 kHz central frequency is designed. The performance frequency range is ADPLL 189 Hz, which is 215 kHz, which is the locker of design.

Guzm Lada and many others have proposed ALL digital build-locked mesh. ADPLL has been a major contributor to the development of the control system and digital communication since 1980. ADPLL's design was a very important component with integrated environmental (IC) sophistication. The ADPLL still continues to give good results. Now a DGPLL has a great role in digital communication systems. This article presents the basic details of ADPLL. It provides a brief summary of basic ADPLL policy in order to control system and digital communications. It relates to the components of ADPLL and their comparison.

3. SYSTEM DESCRIPTION

3.1 ALL DIGITAL PHASE LOCKED LOOP

All digital bus locked loops (ADPLLs) are becoming more attractive because they have better performance, programming, stability, and mobile phones and ADPLLs in different processes to reduce system time and have great noise immunity. Digital digital clocked loop (PLL) for digital computer clock generation is widely researched instead of the traditional analog PLL. Figure 3.1 shows the basic block map of all digital grid locked mesh (ADPLL). ADPLL is built entirely from logical orbitals, and many digital digital digital digital digital digital digital digital digital digital digital digital digital digital digital digital digital DJ. There are many advantages of ADPLL since the input signal is due to digital signals. Digital control oscillator (DCO) to get good build and frequency errors. Only digital signals take the ADPLL input.

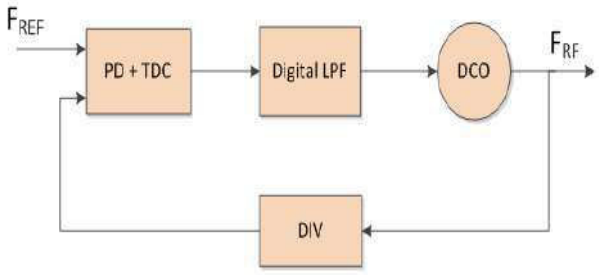


Figure 3.1 Block Diagram of All Digital PLL (ADPLL)

Basic Elements of ADPLL

The various elements of ADPLL consists of

1. Digital Phase Detector (PD)
2. Time-to-Digital Converter (TDC)
3. Digital Loop Pass Filter
4. Digitally Controlled Oscillator (DCO).

3.2 Frequency Dividers Falls under Three Categories:

(1) Flip-flop-based frequency dividers.
(2) Injection-locked frequency dividers and
(3) Regenerative frequency dividers.

Flip-flop-based frequency accounting vectors are available in two T-layers and negative feedback structures. This type of steering wheel is a digital function that delivers the repulsion sensing advantages. Furthermore, flip-flop-based accounting devices have frequency accounting patterns, which contain broader channels than different types of frequencies. This approach also makes the remaining signal positions of the CML circle.

Injected locked frequencies use a basic lens for incoming frequency frequency synchronization. The input signal is sent through the voltage nozzle of the voltage. When the low-power movement is reached, the needle locked frequency accounting extractors reveal the short-lock-range. Return to repeat frequency by holding a salad and low-pass filter in the closed-cycle feedback.

The remaining frequency accounting reveals high frequency compared to a needle lock, but uses many inactive elements in the process. Since the frequency accounting device is equipped with modern high speed systems, the overuse of inactive components is a lack of total chip-area and circuit compatible devices.

3.3 Digital Phase Detector

The Digital Grid Inventor's Volume Chart is shown in Figure 3.2. The round consists of two verge-induced reset flip plates, and their D-inputs are connected to a logical one. Signals A and B are the clock input method for DFF, and DFF B respectively. If Qa = Qb = 0, change in A is the reason for increasing QA. The subsequent changes have no effect on QA, and while B goes too far, Kate and Kate react again and again. Thus QA and QB are given at the same time through delayed total time delay and through the gate and the flip flops of the other side. The twin-edge T-flick-flop activation prompted a phase detector, a design that lost 33% of the power.

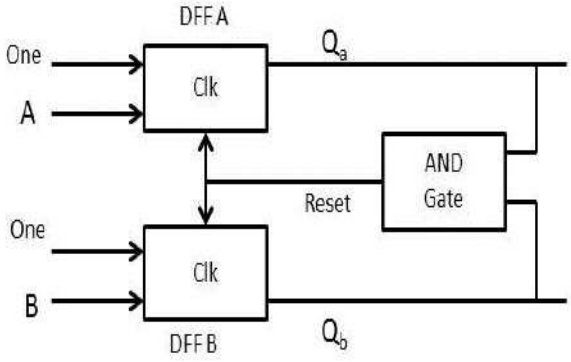


Figure 3.2 Digital Phase Detector Implementation using AND gate

Phase detectors may be split into two categories:

1. Phase only sensitive detectors
2. Phase / frequency detectors (PFD)

3.4 Phase Sensitive Detectors

Detectors for tumors that are only sensitive to the phase. They produce the output that is proportional to the grid difference between the two signals. When the interval between two incoming signals is constant, they form a constant voltage. When there is a frequency difference between the two signals, they produce different voltages. The build detection is the clock duty rotation. This means that a standard duty cycle, 1: 1 should be used. If the input duty cycles are not 50%, it will be a point error.

3.5 Phase Frequency Detectors

1. The intermediate difference between these circuits is the difference between a voltage rate at the rate of difference between ± 180 °. In this way, the AC component will not be produced when the loop is not out of the lock, and the output can be sent through the filter to release the output ADPLL. Various types of phase-bandwidth detection are available, such as:
2. Edge triggered JK flip flop phase frequency detector

3. Dual D type phase comparator
4. EX-OR gate phase frequency detector
5. Bang Bang phase frequency detector.

3.6 Time-to-Digital Converter

In ADPLL, the Digital Converter (TDC) acts as a Frequency Finder (PFD) time build. Figure 3.3 depicts the principle of time-to-digital switching based on digital delay tax. The initial signal is delayed by delayed components and modeled by the rising edge of the signal to stop. With the suspended signal, the sample process implemented by delayed leap cripples the late line of land. If the initial signal delayed the levels, if the model is not delayed by the initial assessment, it will have a higher value of flip-flop outputs if it produces a lower value. Consequently, this thermometer indicates that the higher the level of change in the index, the space signal is intermittently and indicates how much distance can be extended by stopping the signal.

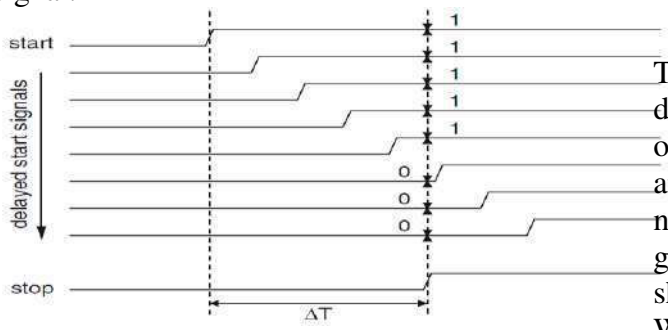


Figure 3.3 Operating Principle of TDC

The goal of the TDC is to measure the time difference between the rising edges of the “Start” and “Stop” signals in ADPLL.

TDC with delay line is used to measure the time intervals are:

Buffer delay line TDC

1. Inverter delay line TDC
2. Vernier delay line TDC
3. Parallel vernier TDC
4. Gated ring oscillator (GRO) TDC

3.7 Digital Loop Filter

Traditional cycle filter output (analog loop filter) due to release chamber reduces synchronizer efficiency, especially co-structure, loop delay. A basic construction block on a digital filter digital systems. With this work, it is worth using a more efficient and flexible digital filter by filtering the bulky passive cycle. The filter frequency response depends on the value of its coefficients.

The values of coefficients are calculated based on the required frequency record. These values are generally referred to as floating point numbers and they are highly accurate with precision accuracy. However, when a digital filter is processed, the encoding must be marked with a small number of bits that provide an acceptable solution to the numbers. The number of logs, the number of buses, partner and multiplies increases in the number of bits marked by a large number. Large sizes of enabled circuits result in a large square-sized chip, which is translated as increased power consumption.

3.8 Digital Controlled Oscillator

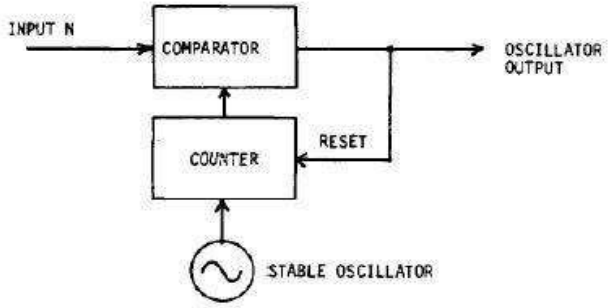


Figure 3.4 DCO Based on Counter Increment

The term "digital control oscillator" is used to describe a mixture of voltage-controlled osillor operated by a control signal from the digital-to-analog switch, and is sometimes used to describe numbered controller oscillators. Figure 3.4 A graphic display of a digital controlled oscilloscope shows.

When comparing content with the opposite content and when they are compatible, the comparator releases the output of the DCO which sends a output pulse and resets the reset. Controlling the contents of the DCO can be controlled by distinguishing N. This DCO is easy to use with fixed cells, but its power consumption is very high.

One aspect of the DCO's main design is to provide adequate controls and maintain the risk of acceptable risk. This is an important digital PLL performance parameter, which is simulated for this system. The DCO design tested seven bit input scenes using a linear feedback logging version. The frequency indicated for each control. DCO's operating range is 180 MHz 320 MHz. The DCO frequency for control words "0000000" is 48.93 MHz and 322.9MHz for "1111111".

SYSTEM ANALYSIS

4.1 EXISTING SYSTEM

A common delay-line vernier TDC and vernier TDC with delay latch chain architecture is

implemented to measure the time interval between two input signal to a digital output word.

4.1.1 Vernier Delay Line TDC

The Vernier Delay Line is capable of measuring time gap with TDC sub-entry resolution. It has two late lines, which delay both signals and prevent the signal. Delay in the first row is slightly larger than the second row delay. During the measurement, the first signal signal spreads with the first line of Mars. It seems like the signal stop signal pushes the signal. At each stage, it is delayed by 1- Delay2. A pair of late-line delayed stripes in a Vernier configuration are associated with each flip-flop of the corresponding pair pipes and presented in Fig 4.1

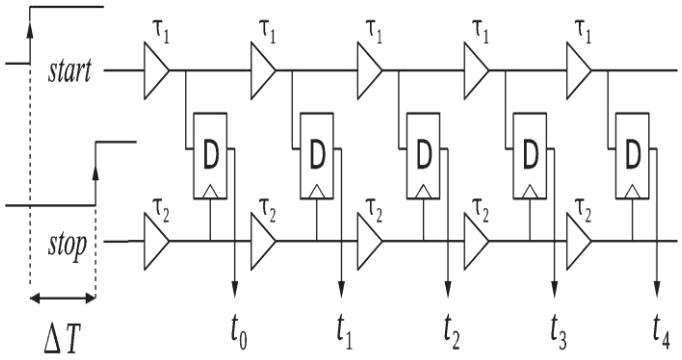


Figure 4.1 Illustration of Vernier Delay Line TDC

4.1.2 Vernier TDC with Delay Latch Chain

Delays latches can be modeled using buffers and multiplexers with zero delayed enclosure. Figure 4.2 shows the late latch chain vernier TDC has the following steps, where it is considered τ1> τ2.
TDC is ready for transition at the next stage where initial position and stop inputs are low. All delayed initial input will increase the thermometer code in tx releases gradually through a pulse delay latch next to the increasing edge.
Stop input next to the increased edge of the input, the latter set the latches of the latter stopping the campaign by the pulse delayed line.
If the pulse starts with the starting point, do not stop late delaying the latch and stop spreading the initial pulses.
The temperature measurement, ie, the release of delay in the release of delay is now time variable, ie, between two inputs ΔT.

Figure 4.2 Illustration of Delay Latch Chain Vernier TDC

4.1.3 Schematic Design of Delay Latch Chain Vernier TDC

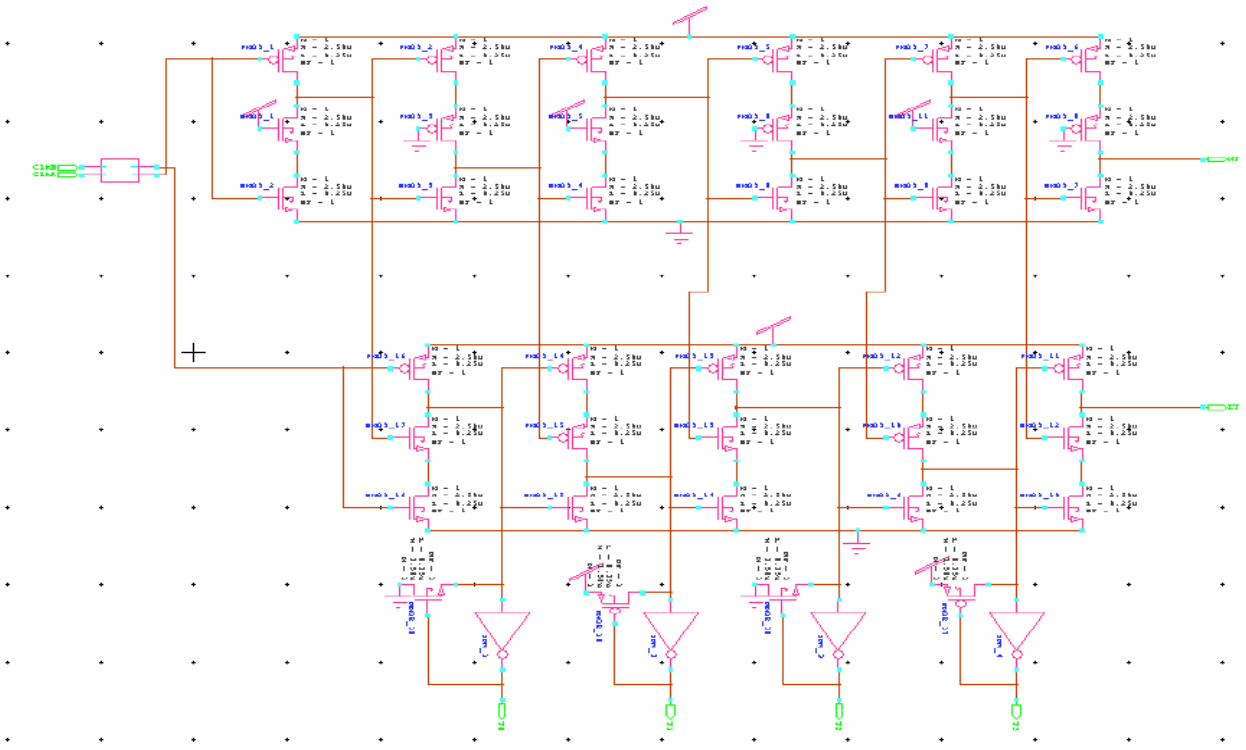


Figure 4.4 Implementation of Delay Latch Chain Vernier TDC

Delay latch chain NMOS variable and pMOS processing transistors are shown in 4.4. When a gas voltage is set to a maximum in a nMOS implementation transistor, the late delay acts as a delayed delayed component, and when the gas voltage is low, the output latch turns the latch to a floating point, so holds the current voltage value. The PMOS implementations operate with voltages of nMOS transistors, as well as filler gates. Depending on the process, voltage and temperature variation, transistors are applied to late-line inputers. Appropriate transistors always run nMOS and pMOS transistor gates, respectively, by combining the possibilities.

4.2 PROPOSED SYSTEM

The proposed system is to design a low power ADPLL using Adaibatic Logic Circuit. Figure 4.5 shows the overall implementation of ADPLL in TANNER EDA tool.

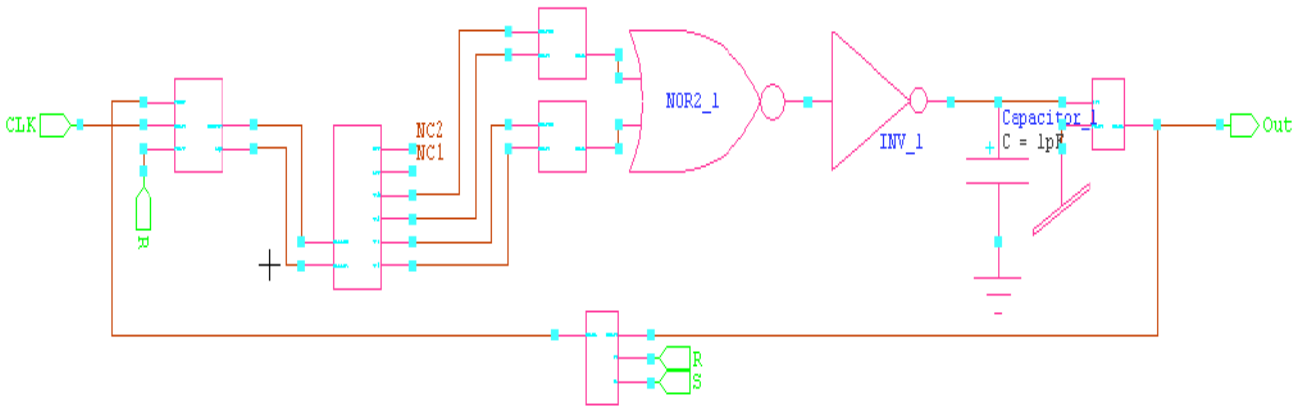


Figure 4.5 Implementation of ADPLL

4.2.1 Adiabatic Logic Circuits

The word ADIABATIC is derived from the Greek word ADIABATOS, which means that there is no energy loss in the form of hot loss, since there is no energy exchange with the environment. The capacitor logic is the time given to the low power circuit that performs logical review logic.

Generally used to reduce energy loss during charging and discharge operation of circuit operations. Antibiotic logic is known as energy recovery or money recovery recovery. The deformed logic structure reduces dramatic power shortages. Antibiotic switch technique can achieve low power loss but can be costly at cost.

4.2.2 Adiabatic Logic Techniques

Defective logic reduces power loss. The term adiabatic comes from the thermodynamics used to describe a process that does not have a heat exchange with the environment. These types of circuits are low circuits, which use logic that refuses to protect energy. A climate process is a term that holds total heat or energy in the system. This technique is recycled to power, rather than the expulsion of consumption power, which reduces overall power consumption. Addiction logic provides a way to use the energy stored in load capacitors, and is a traditional way of wasting this energy, pulling out a ground-mounted container. Blunt logic can be achieved by ensuring that the switch devices are small throughout. This can be achieved by charging the capacitor from the time-different voltage source or the standard current source.Adiabatic Circuits reduce dissipation by following key rules:

- Never turn on a transistor when there is a voltage potential between source & drain.
- Never turn off a transistor when current is flowing through it.

4.2.3 Concept of Low Power in Adiabatic Circuits

- The low power is required because of the low intensity of small devices such as cellphone batteries and the pediatric field of the heart pacemaker, however, the greater the energy loss it sinks to the heat. So the main purpose is to provide a new low power solution to VLSI designers. There are two types of power losses:Dynamic Component
- Static Component

Dynamic Component consists the signal transitions and short-circuit power dissipation while static component consists leakage power dissipation.

4.2.4 Adiabatic Logic Families

Most research focuses on building outright logic from CMOS. However, the current CMOS technology, although much more efficient in comparison with similar technologies, often changes when excessive heat is exchanged. Many designs have been generated by CMOS circuits implemented. Because Nanobelectronics is expected to distort a large amount of heat, the underpayic logic circuits use the current fourth components, such as silicon nanowires or carbon nanotubes. There are 2 types of Adlick logical families:Fully adiabatic logic family

- Quasi adiabatic logic family

Fully loaded logic family circuits lose their energy due to leak currents with non-autumn switches. Quasi adiabatic logic Family circuits are affected by normal energy efficiency losses in some places, which is generally a measure of capacity and proportion to the square of the Vaseline voltage. Following are the following families of moral logic:Split level Charge Recovery Logic.

- Two level Adiabatic Logic.
- Positive Feedback Adiabatic Logic.
- Efficient Charge Recovery Logic.
- Two Phase clocked adiabatic static CMOS logic.

4.2.5 Positive Feedback Adiabatic Logic

The structure of PFAL is shown in approximately 4. Two n-trees indicate logical functions. This logical family produces positive and negative outputs. The main difference in ECRL produces latch with 2 PMOS and 2 NMOS than 2 PMOS at ECRL and connecting functional modules to PMOS. Thus the focal point is equal to the smaller R is smaller. The ratio between the required power and the distorted one in a cycle is 3.4.

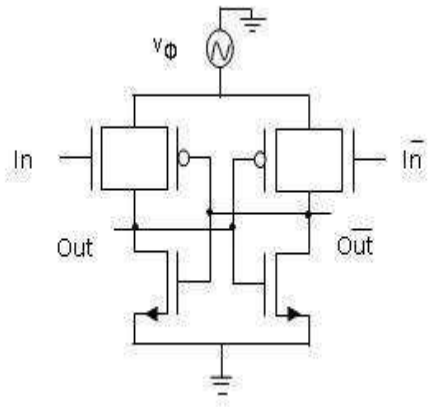


Figure 4.6 PFAL logic circuit

Two models and architectural design are on average with 36.64%. These two areas require many new ideas and greater creativity compared to other parts of the group. Improve the implementation of practical sessions, enhance student sessions in both areas, increasing the number of sessions in these areas and using techniques such as debates [13].

4.3 TANNER DEIGN FLOW

A complete analog design flow from schematic capture, circuit simulation, and waveform analysis to physical layout and verification in TANNER EDA tool is given in the figure 5.1.

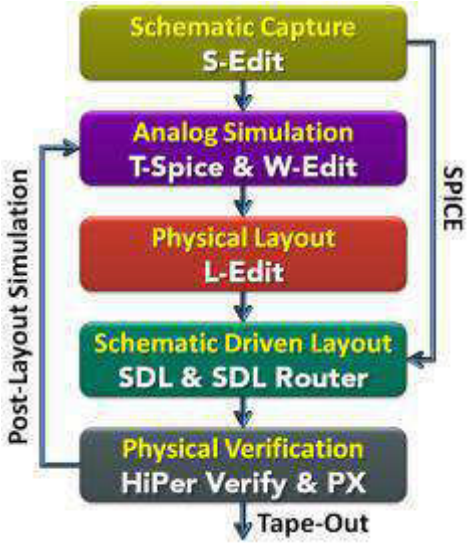


Figure 4.1 Design Flow Diagram of TANNER EDA Tool

4.3.1 S-Edit

S-Edit is hierarchy of files, modules & pages. It introduces symbol & schematic modes. S-Edit provides the facility of

1. Beginning a design.
2. Viewing, drawing & editing of objects.
3. Design connectivity.
4. Properties, net lists & simulation.

4.3.2 T-Edit

The T-Spice Pro's waveform analysis feature combines S-Edit, T-Spice and W to integrate and allow individual points in a circle that is analyzed. An analysis is described below. The heart of the T-spice movement is the input file (this is round explanation, net list & input site). Spice Circuit is a simple text file containing a modeling device device report & simulation command that simulated the T-Spice simulator language. Any text editor who can create and edit input files- a tool used to simulate Spice Round. It provides facilities

Design Simulation

1. Simulation Commands
2. Device Statements
3. User-Designed External Models
4. Small Signal & Noise Models

T-Spice lets you precisely characterize circuit behavior using virtual data measurements, Monte Carlo analysis, and parameter sweeping.

4.3.3 W-Edit

The ability to visualize complex number data as a result of VLSI circuit simulation is crucial to testing, understanding and improving these circuits. W-Edit is a wave Viewer, which provides easy-to-use, power and speed in a flexible environment designed for graphical data representation.

Customize the properties of axes, traces, challenges, maps, text and colors. Numeric data input for W-editing in the form of empty or binary text formats. The title and comment information provided by T-Spies is used in the automatic charts. The dynamic performance of the results is possible by combining the w-set of simulation running on T-spies.

Saves data with diagrams, tracking, print and ecosystems in files with WDB (W-Edit Database). W-Edit is considered as a data unit. Multiple output files can be viewed simultaneously in single or multiple windows; Traces can be copied and moved between maps and windows. Trace can trace the existing tracking to create new arithmetic.

4.3.4 L-Edit

This is a tool to reflect masks used to create an integrated circuit. It describes layout design based on files, cells & mask primitives. At the layout level, the component parameters are quite different from the size of the project. Therefore, it enables the user, before it can take time, to examine the environmental efficiency and the cost effective inflation. There are rules for designing a planned circuit design, which can be compared to the expected output.

4.3.5 SDL & SDL Router

SDL is integrated with L-Edit Layout Editor and allows tools to improve the speed and quality of the custom system and focus on layout quality by allowing the designer to manage routing flow. SDL imports a net list from any svmatic device and all the sub-subcategories

required will automatically occur, including parameters cells using parameters associated with each device on the net list.

4.3.5.**Physical Verification**

Extract the SPICE net list, which is compatible with the system, including devices (MOSFets, bipolar, etc.) and intermittent parasite. HiPer PX provides complete parasitic networks for each node including a vertical and lateral pairing capacity and resistance to each other. HiPer PX is integrated with L-Edit Layout Editor, allowing errors to be accurate location, faster redirect fixes, and faster debugging.

4.3 PROCEDURE FOR TANNER TOOL

The procedure for schematic design in S-simulation in T-edit and the corresponding wav in W-edit is described below:

1. Click the S-Edit 13.0 icon → S-Edit w appeared, the corresponding ETH ID is noted and the follow the installation step 4,5 & 9.
2. In S-Edit window →File → New →New design→Design Name→Create a path directory.
3. Cell→ New view → Design → view type as schematic→Schematic window is appeared.
4. Add→library→browse→all library file.
5. Using symbols draw the schematic design and place in and out port.
6. Click check view and hierarchy to know the error and warnings.
7. Click T-Spice→ include file IBM013→Netlist is generated.

8. Click simulation icon to generate the output waveform in W-Edit and power analysis is obtained for the particular design.

SIMULATION AND RESULTS

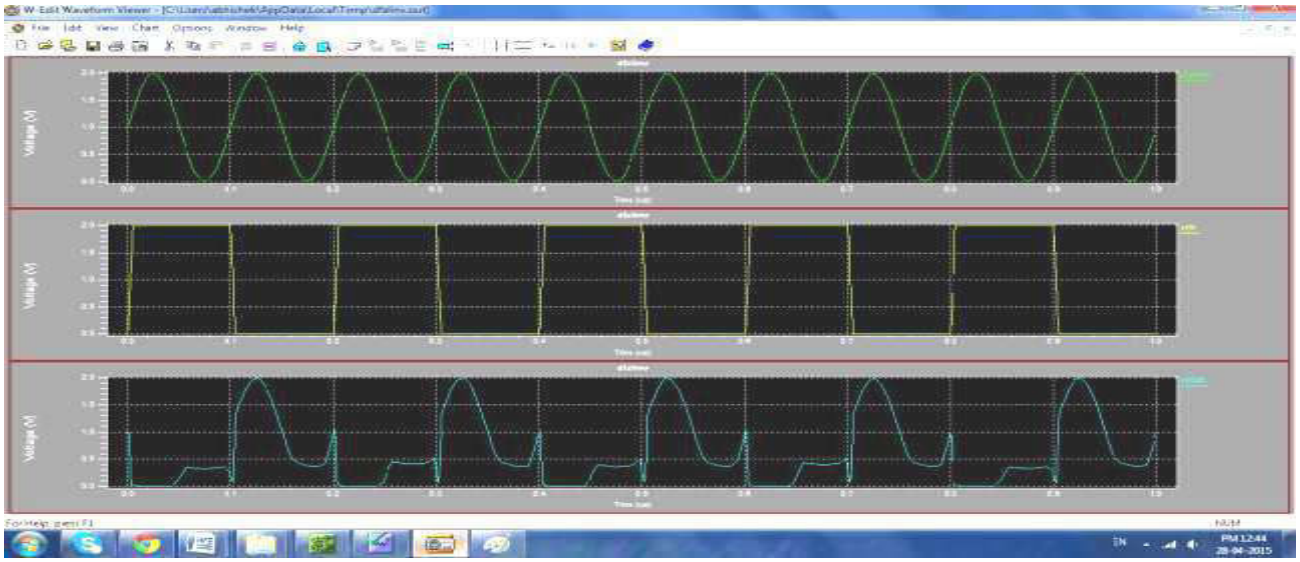


Figure 6.2 Waveform of Dynamic Frequency Detector with Adiabatic Logic Circuit

Dynamism grid freakski detector's digital direction and output waveform is found in the Adiabatic logic circuit 6.1. The average power is 5.42mW.

Simulated results are analyzed with the help of the DNA EDA tool. Various parameters of the current method and proposed method are listed in Table 7.1.

Table 1. **Table 7.1 Parameter Comparison**

Parameter	Delay Latch Chain TDC	Adiabatic Logic Circuit
Power Consumption in ADPLL	6.77Mw	5.42mW
Timing Analysis	11s	0.35s

CONCLUSION

The TANNER EDA tool's output waveform is based on the Dynamic Face Frequency Detector with Adiabatic Logic Circuit in ADPLL and is standardized using standard 0.25μm CMOS technology. Adiabatic Logic Circuit 1.8m supply of ADPLL architecture 1.8m with Dynamic Face Freeway Detector with maximum power consumption. The total power of the proposed ADPLL uses electricity at 5.42mW. Compared to various parameters, compared to Dynamic Face Frequency Detector with Adiabatic logical rotation in ADPLL, faster locking, high noise resistance and low power consumption, no need for voters and significantly reduced .

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An Efficient Feature Selection Technique for Keystroke Authentication Based on Low Impact Biometric Verification

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Abstract:
Advances in the field of Computer science and Technology also make Information Security an inseparable part of it. In order to deal with security, Authentication plays an important role. This paper presents a review on the biometric authentication techniques and some future possibilities in this field. In biometrics, a human being needs to be identified based on some characteristic physiological parameters. A wide variety of systems require reliable personal recognition schemes to either confirm or determine the identity of an individual requesting their services. The purpose of such schemes is to ensure that the rendered services are accessed only by a legitimate user, and not anyone else. By using biometrics, it is possible to confirm or establish an individual's identity. The position of biometrics in the current field of Security has been depicted in this work. We have also outlined opinions about the usability of biometric authentication systems, comparison between different techniques and their advantages and disadvantages in this paper.

1. Introduction

Computer systems and networks are now used in almost all technical, industrial, and business applications. The dependence of people on computers has increased tremendously in recent years and many businesses rely heavily on the effective operations of their computer systems and networks. The total number of computer systems installed in most organizations has been increasing at a phenomenal rate. Corporations store sensitive information on manufacturing process, marketing, credit records, driving records, income tax, classified military data, and the like. There are many other examples of sensitive information that if accessed by unauthorized users, may entail loss of money or releasing confidential information to unwanted parties [1- 9].

Many incidents of computer security problems have been reported in the popular media [1]. Among these is the recent incident at Rice University where intruders were able to gain high level of access to the university computer systems which forced the administration to shut down the campus computer network and cut its link with the Internet for one week in order to resolve the problem. Other institutions such as Bard College of the University of Texas Health Science centre reported similar breaches. Parker [10] reported that one basic problem with computer security is that the pace of the technology of data processing equipment has outstripped capability to protect the data and information from intentional misdeeds. Attacks on computer systems and networks can be divided into active and passive attacks [11-12].

1. Active attacks: These attacks involve altering of data stream or the creation of a fraudulent stream. They can be divided into four subclasses: masquerade, replay, modification of messages, and denial of service. A masquerade occurs when one entity fakes to be a different entity. For example, authentication sequence can be collected and replayed after a valid authentication sequence has taken place. Replay involves the passive capture of data unit and its subsequent retransmission to construct an unapproved access. Modification of messages simply means that some portion of a genuine message is changed, or that messages are delayed or recorded, to produce an unauthorized result.

2. Passive attacks: These are inherently eavesdropping on, or snooping on, transmission. The goal of the attacker is to access information that is being transmitted. Here, there are two subclasses: release of message contents, and traffic analysis. In the first subclass, the attack occurs, for example, on an e-mail message, or a transferred file that may contain sensitive information. In traffic analysis, which is more sophisticated, the attacker could discover the location and identity of communicating hosts and could observe the frequency and length of encrypted messages being exchanged. Such information could be useful in guessing the nature of information/data.

2. Keystroke Dynamics

The system is based upon the concept that the coordination of a person's fingers is neurophysiological determined and unique for a given genotype. A user typing or keystroke characteristics can be measured by examining the timing of the keystrokes or the pressure of the keystrokes. Vectors is used to represent the data. The vector was constructed using interleaved hold times and digraph latency times. The hold time of a

key time is obtained by subtracting the press time of the key from the release time of the key. A digraph is a two keystroke combination. The digraph latency is obtained by subtracting a first key's release time from a second key's press time. The ordering elements of the vector is not important but the vectors should be constructed such that the samples relating to a user are constructed in the same manner so that they can be properly compared. The components of the vectors are physical characteristics of a person's keystroke characteristics. These physical characteristics are used to construct vectors which are processed, transmitted and stored within the system as signals. The vector can be made up of data pertaining to the key press time, key release times, digraph latency times, key hold times, keystroke pressure, keystroke acceleration or deceleration, or any features relating to the user's keystroke characteristics. Once the data is collected and placed in vector format, the vectors can be analysed to determine if the user is authorized or an imposter. The data was normalized using the transformation linear method which is shown below;

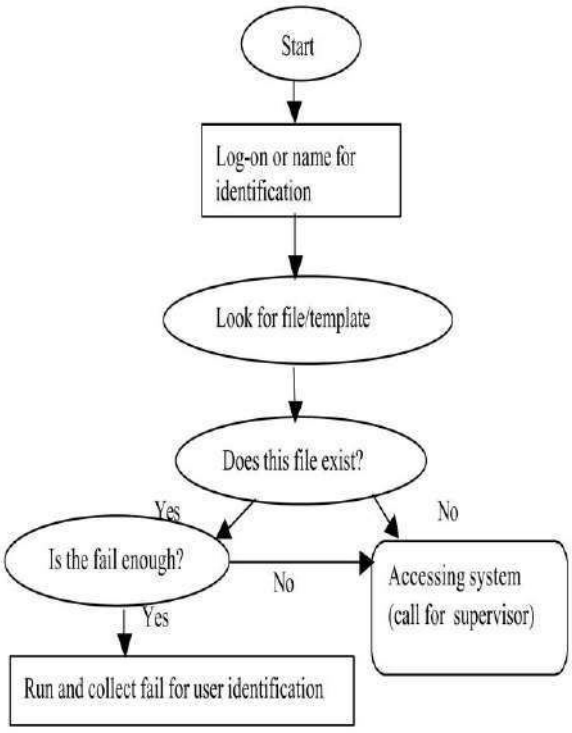

Fig. 1 Algorithm for keystroke dynamics method

3. Neural Networks Method

The main concern of this research was to find the best method to discriminate/purify the data collected. In this study, two kinds of neural network model and architecture was used to perform as the basic data or methodology. This paper describes the application of neural networks to the problem of identifying specific users through the typing characteristics exhibited when typing their own names. The network was chosen based on the problem to be solved. First of all, the previous study was done to compare two kind of methods to discriminate the data which are geometric distance and Euclidean distance. The system under investigation was then tested using two kind of neural network architecture and model. There are ADALINE and Backpropagation network. The network was chosen based on network model, architecture, data and the type of problem. The choice of network model depends heavily on the type of problems you would like to solve. The nature of the problem usually restricts the choice of network to one or two model. Sometimes the choice of network comes down to personal preference or familiarity.in this case, the problem to be solved is a pattern classifier problem since it needs to determine which pattern belongs to the authorised or non-authorised user. The input layer consists of 27 nodes, which is equivalent to the number of the input elements. Whereas for the middle layer, it is a single middle layer with 24 nodes, which is 90% of the input nodes. There will be two output nodes, 1 for the authorised user and 0 for the nonauthorised user.

The availability and integrity of data constitute the most important factor for training neural networks. The data should fully represent all possible states of the problem being tackled and there should be sufficient data to allow test and validation data sets to be extracted. The right preparation of data is needed to ensure the accurateness of the output. Since the sigmoid activation function is used as the transfer function, it generates its output between 0 and 1. It is important for us to perform normalisation to scale the data so it will fall between this range. During the experiment, the number of input nodes, learning rate value, number of hidden nodes, momentum value and performance goal value was changed to find the most suitable parameter values. The appropriate parameter values are chosen based from trial and error performed during experiment and on the convergence and goal performance result.

4. Experimental Results

4.1 Data Sets

We collected the data sets from 16 participants. Each participant was requested to type the 10 passwords in Table 1 repeatedly. The 10 participants among them were each considered as the legitimate user for one password, each played the role of an imposter for the passwords. For each password, the other 15 participants were considered as imposters except the legitimate user. The passwords 1 to 5 are the Korean words on the English keyboard, and the passwords 6 to 9 are the English words. The password 10 is a random string including upper-cases, lower-cases, and numbers. The password strings were chosen carefully with regard to the

familiarity and the typing difficulty on our own. The dimensions of the passwords and the numbers of samples are shown in Table 1. We used 20 samples of a legitimate user in making a hypothesis space, and the rest of the samples were used for test.

Table 1: Password strings used in the experiments

No	Password	Dimension	Number of Timing Vectors
1	qlalfqjsgh	23	340
2	rhdWkdudghk	20	320
3	rntk1tod	15	350
4	tjdnf1945	20	338
5	j6kbkeakd	14	325
6	transaction	16	319
7	DoItYourself	12	340
8	money4nothing	18	329
9	Sk8erBoi	25	335
10	FvVohx7x9P	22	320
Ave.		**18.5**	**331.6**
Min.		**12**	**319**
Max.		**25**	**350**

4.2 The Shapes of the Hypothesis Spaces

We proposed the extended p-norm to describe the hypothesis space. As shown in Figure 3, the value of p determines the shape of a hypothesis space. To find the proper shape of a hypothesis space, we tested for the hypothesis spaces of $p = 1$, $p = 2$, and $p = \infty$. The results of the test is shown in Table 2. Bold faces figures represent the best pair of results with respect to the total error rate8 in the corresponding row. Each of the extended 1-norm and the extended 2-norm showed the best in 4 cases among the 10 passwords. Especially for the password 5, the extended 1-norm showed nearly zero error rates in the classification. The extended 2-norm showed relatively small error rates for the password 4. We could not find a considerable superiority between the extended 1-norm and the extended 2-norm, but it was observed that the extended infinity-norm performed poor in the test. Choosing the value of γ is another question. If the value of γ is too low (high security level), the FAR is nearly zero, but the FRR is too high. On the other side, if the value of γ is too high (low security level), the FRR is nearly zero, but the FAR is too high. With the current version, the values between 5 and 15 seems to be reasonable.

Table 2: Comparison of the hypothesis spaces

No.	Extended 1-norm				Extended 2-norm				Extended infinity-norm			
	$\gamma = 7.5$		$\gamma = 15$		$\gamma = 7.5$		$\gamma = 15$		$\gamma = 7.5$		$\gamma = 15$	
	FRR†	FAR‡	FRR	FAR	FRR	FAR	FRR	FAR	FRR	FAR	FRR	FAR
1	34	1	8	0	48	1	32	0	27	0	29	1
2	9	0	21	0	12	1	18	1	4	0	6	1
3	2	0	35	1	14	1	9	1	38	1	30	1
4	22	0	29	0	10	1	31	0	48	0	47	1
5	30	1	49	1	19	1	15	1	29	0	27	1
6	23	1	10	0	27	0	14	1	40	0	46	0
7	26	0	38	0	7	0	19	0	44	0	25	1
8	38	1	44	0	55	0	49	0	4	1	17	0
9	11	0	43	1	53	0	6	1	1	1	33	1
10	16	0	12	1	45	1	35	0	31	1	38	0
Ave.	21	0	29	0	29	1	23	1	27	0	30	1
Min.	2	0	8	0	7	0	6	0	1	0	6	0
Max.	38	1	49	1	55	1	49	1	48	1	47	1

† False reject rate.
‡ False accept rate.

4.3 Effects of Eliminating Outliers

To observe the effects of eliminating outliers, we examined the hypothesis spaces using the extended 2-norm for $\alpha = \infty$, $\alpha = 2$, and $\alpha = 1$. If the value of α is infinite in inequality (6), no elimination occurs. The experimental results are shown in Table 3. For the 7 passwords excepting the passwords 2, 4, and 7, the error rates were reduced by eliminating outliers. It was observed that the hypothesis space for $\alpha = 2$ performed better than the hypothesis space for $\alpha = 1$ on average. We suspect that it is because most of the elements in the timing vectors were eliminated when $\alpha = 1$.

Table 3: The error rates for eliminating outliers

No.	Extended 2-norm					
	α = ∞		α =2		α =1	
	FRR†	FAR‡	FRR	FAR	FRR	FAR
1	4.41	3.51	4.41	3.51	**2.45**	**3.51**
2	**9.76**	**0.88**	10.24	0.88	14.63	3.51
3	7.25	4.81	**5.7**	**5.77**	7.25	2.88
4	**1.6**	**0.79**	4.26	1.57	3.19	1.57
5	2.94	0.74	0	2.22	**0.49**	**1.48**
6	3.68	1.52	**3.68**	**0.76**	7.37	0
7	**11.27**	**5.22**	13.62	8.7	11.74	8.7
8	3.9	6.09	**3.9**	**5.22**	4.39	5.22
9	1.06	7.63	2.65	1.69	**1.59**	**2.54**
10	4.5	27.12	**2**	**11.02**	1.5	17.8
Ave.	**5.04**	**5.83**	**5.05**	**4.13**	**5.46**	**4.72**
Min.	**1.06**	**0.74**	**0**	**0.76**	**0.49**	**0**
Max.	**11.27**	**27.12**	**13.62**	**11.02**	**14.63**	**17.8**

† False reject rate.
‡ False accept rate.

Table 4: The error rates with the adaptation

No	Extended 2-norm			
	FRR	FAR	FRR	FAR
1	10.5	2.5	**2.94**	**2.63**
2	13.6	3.8	**7.32**	**5.26**
3	**3.8**	**4.2**	5.7	7.69
4	12.8	6.5	**2.13**	**2.36**
5	**3.9**	**3.8**	1.47	8.89
6	8.5	8.4	**3.16**	**3.03**
7	13.5	6.7	**6.57**	**3.48**
8	15.9	4.9	**6.34**	**1.74**
9	**1.89**	**3.54**	3.7	5.08
10	12.5	8.54	**4**	**3.39**
Ave.	9.689	5.288	4.333	4.355
Min.	1.89	2.5	1.47	1.74
Max.	15.9	8.54	7.32	8.89

4.4 Improvements by the Adaptation

The proposed adaptation mechanism utilizes the results of the classification. The measured timing vector is used in up- dating a hypothesis space, if it is classified as the legitimate user. We tested the hypothesis spaces with the adaptation mechanism using the extended 2-norm. To avoid a heavy load, we executed the adaptation process once whenever 20 samples were collected. The experimental results are shown in Table 4. The adaptation mechanism improved the performance of the system on average. However, it is observed that the error rates for the passwords 3, 5, and 9 were in- creased slightly by the adaptation mechanism. We believe it was because the misclassification in the early stage misled the hypothesis space.

5. Conclusions

To conclude, keystroke dynamics are rich with individual mannerism and traits and they can be used to extract features that can be used to authenticate/verify access to computer systems and networks. The keystroke dynamics of a computer user's login string provide a characteristic pattern that can be used for verification of the user's identity. Keystroke patterns combined with other security schemes can provide a very powerful and effective means of authentication and verification of computer users. Neither our work nor any other work we are aware of has dealt with typographical errors. Further research into reliable methods for handling typographical errors is needed in order to make keystroke-based authentication systems non-irritating and widely accepted by the computing and network security community. Finally, it is found that artificial neural network paradigms are more successful than classical pattern recognition algorithms in the classification of users.

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PROPOSE OF COAL MINE WEATHER CONDITIONS MONITORING SYSTEM IN UNDERGROUND USING IOT PLATFORM

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***Abstract*— Just recently, the regular coal mine security mishaps have actually triggered major casualties and also significant financial losses. It is immediate for the international mining market to raise functional effectiveness and also boost general mining safety and security. This paper recommends a light-weight mash up middleware to attain remote surveillance and also control automation of below ground physical sensing unit tools. Initially, the collection tree based upon Wireless Sensor Network (WSN) is released in a below ground coal mine, as well as suggests an Open Service Gateway campaign (OSGi)-based consistent tools accessibility structure. After that, recommend a consistent message area and also information circulation design, as well as, a light-weight solutions mash up method is carried out. With the aid of visualization innovation, the icon of various below ground physical sensing unit tools might be produced, which permits the sensing units to incorporate with various other sources quickly. Besides, 4 kinds of coal mine safety and security surveillance and also control automation situations are detailed, and also the efficiency has actually likewise been gauged as well as assessed. It has actually been verified that our light-weight mash up middleware could lower the prices effectively to develop coal mine security tracking as well as control automation applications.**

***Index Terms*— coal mine safety, mining operations, underground mining and weather conditions, IOT**

I. INTRODUCTION

Below Ground mines are normally considerable mazes, which the passages are usually lengthy as well as slim with a couple of kilometres in size and also a couple of meters in size. Thousands of mining workers should function under several problems in accordance with the building and construction needs, as well as number of miners pass away from mining crashes yearly. It is extensively accepted that the below ground mining procedures are of high threat. In sight of this, a surveillance as well as control system should be realised as one crucial framework in order to guarantee the mining security as well as coordinates different jobs.

Nevertheless, below ground coal mines primarily contain arbitrary flows and also branch passages, as well as this chaotic framework makes it really tough to realise any kind of networking system. In such an instance, the usage of wireless sensor network (WSN) as well as various other picking up tools could have unique benefits for recognizing the automation of below ground tracking as well as control because of the fast as well as adaptable implementation. Furthermore, the multihop transferring approach could well adjust to the passage framework as well as therefore supply adequate scalability for the building and construction of a mining system.

Typically, coal mine safety and security surveillance as well as automation systems were generally developed to fulfil the demands of a solitary surveillance application. The coal mine application has actually currently exceeded the affiliation of a couple of huge back-end systems, as well as a growing number of below ground physical tools make the state of things as well as their environments effortlessly obtainable to software application systems. In fact, a lot of jobs are based upon monolithic system styles, which are challenging to adjust. A required action to coal mine tracking as well as control automation is to give prompt and equivalent disposal procedure. It is required to make sure that it enables the customers to recognize the degrees for coal mine safety and security, and also potentially to readjust tracking as well as control regulations to make sure the coal mine security.

Moreover, the individual could likewise regulate the physical gadgets from another location by means of the Web. Presently offered coal mine security surveillance and also control systems that concentrate on the real-time info collection serve, yet could not fulfil the individual requires totally with a really high use barrier and also typically needs an intricate procedure meaning and also setup for tracking and also control automation applications, as well as could not satisfy the need for ad-hoc solutions by the end individuals.

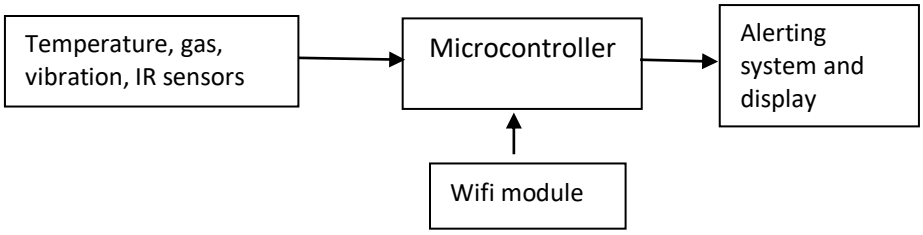

Fig. 2. Monitoring weather conditions of Mining Workers in underground, system overview.

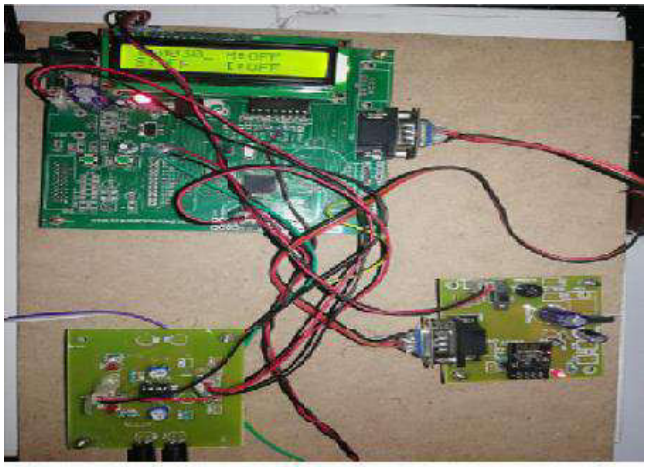

Fig. 3. Hardware: view of a prototype of the proposed system with sensors.

Therefore, it is necessary to develop new mechanisms to improve the occupational safety and health programs for people working in mining in underground [5].

There are two principal phases of underground mining: development mining and production mining. Development mining is composed of excavation almost entirely in (non-valuable) waste rock in order to gain access to the ore body. There are six steps in development mining: remove previously blasted material (muck out round), scaling (removing any unstable slabs of rock hanging from the roof and sidewalls to protect workers and equipment from damage), installing support or/and reinforcement using shotcrete etceteras, drill face rock, load explosives, and blast explosives. To start the mining, the first step is to make the path to go down. The path is defined as 'Decline' as describe above. Before the start of Decline all preplanning of Power facility, drilling arrangement, dewatering, ventilation and, muck withdrawal facilities are required.[2]

Production mining is further broken down into two methods, long hole and short hole. Short hole mining is similar to development mining, except that it occurs in ore. There are several different methods of long hole mining. Typically, long hole mining requires two excavations within the ore at different elevations below surface, (15 m – 30 m apart). Holes are drilled between the two excavations and loaded with explosives. The holes are blasted and the ore is removed from the bottom excavation.

II. System Description

A. *Environmental parameters*

To determine the weather status of mining, the system measures relevant variables using techniques that are minimally invasive. To obtain a complete overview, the extreme conditions of mine sites in underground are also measured by the incorporation of environmental sensors. The embedded measured parameters are:

- *Gas levels:* Subsurface atmosphere may be contaminated with poisonous gases that displace the necessary oxygen to support life or flammable gases that may cause explosion. Therefore, it is necessary to develop technologies and find ways to accurately measure concentration levels of toxic and flammable gases levels in subsurface atmosphere for safety of underground coal mines

- *Vibration levels*: vibrations involved measurements on the roof and walls of underground mines. Primary importance in underground excavation is .the requirement to maintain rock stability and prevent rock falls or damage to support .structure's. The high-intensity elastic waves induced by production blasting and the adjustment of rock due to stresses associated with the opening itself create conditions that affect rock competency outside the excavation boundary.

- *Temperature*: The mine is so deep that temperatures in the mine can rise to life-threatening levels. Air-conditioning equipment is used to cool the mine from **55** °C (131 °F) down to a more tolerable 28 °C (82 °F). The rock face temperature reaches 60 °C (140 °F). In this proposed paper temperature is measured with sensors.

- *Obstacle detection*: obstacle is dangerous in underground mining, it is monitored by infrared sensors. If obstacle is within the range of sensor, it will detect.

A schematics overview of the proposed system is shown in Fig. 2. The environmental variables are measured using a sensors and data is transferred through IOT technology. Wireless data transmission of sensed values is achieved using a Wi-Fi module. Controller takes input from sensors and alerts when threshold levels of sensors are high.

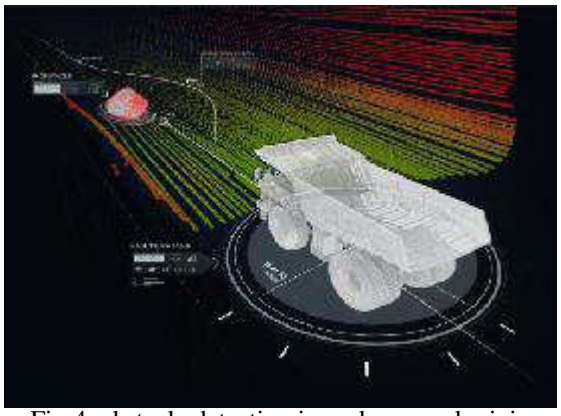

Fig.4. obstacle detection in underground mining

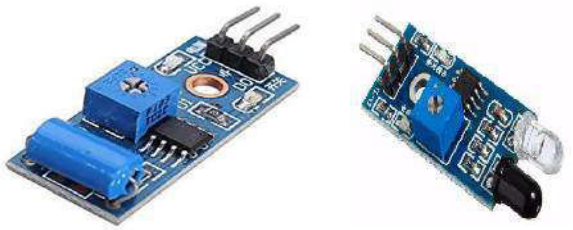

Fig. 5. Vibration sensor and IR sensor

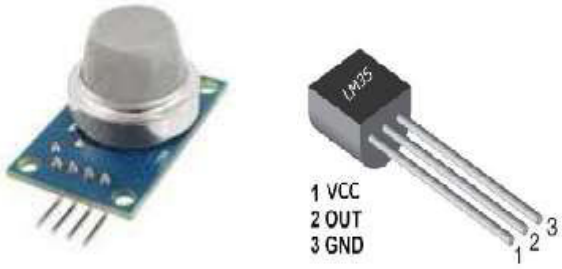

Fig. 6. Gas sensor and temperature sensor

B. Environmental embedded sensors

All environmental sensors are embedded and gives input to microcontroller. ARM7 (LPC2148) is used as microcontroller in this proposed paper. Implementation and features of each sensor are described below.

IR sensor: An infrared sensor is an electronic device that emits in order to sense some aspects of the surroundings. An IR sensor can measure the heat of an object as well as detects the motion. These types of sensors measures only infrared radiation, rather than emitting it that is called as a passive IR sensor. Usually in the infrared spectrum, all the objects radiate some form of thermal radiations. These types of radiations are invisible to our eyes that can be detected by an infrared sensor.

The emitter is simply an IR LED (Light Emitting Diode) and the detector is simply an IR photodiode which is sensitive to IR light of the same wavelength as that emitted by the IR LED. When IR light falls on the photodiode, the resistances and these output voltages, change in proportion to the magnitude of the IR light received.

Temperature sensor (LM35): The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full -55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level.

The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a -55° to +150°C temperature range, while the LM35C is rated for a -40° to +110°C range (-10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Gas sensor (MQ5)/ smoke sensor: A smoke detector is a device that detects smoke, typically as an indicator of fire. Commercial, industrial, and mass residential devices issue a signal to a fire alarm system, while household detectors, known as smoke alarms, generally issue a local audible and/or visual alarm from the detector itself. Smoke detectors are typically housed in a disk-shaped plastic enclosure about 150 millimetres (6 in) in diameter and 25 millimetres (1 in) thick, but the shape can vary by manufacturer or product line.

Most smoke detectors work either by optical detection (photoelectric) or by physical process (ionization), while others use both detection methods to increase sensitivity to smoke. Sensitive alarms can be used to detect, and thus deter, smoking in areas where it is banned such as toilets and schools. Smoke detectors in large commercial, industrial, and residential buildings are usually powered by a central fire alarm system, which is powered by the building power with a battery backup. However, in many single family detached and smaller multiple family housings, a smoke alarm is often powered only by a single disposable battery.

Vibration sensor(SW-420): Measurement Specialties is a leading global provider of accelerometers and vibration sensing know-how for applications in Aircraft Design & Testing, Automotive Design & Testing, Automotive Safety Testing, Machine & Structure Monitoring and Motorsport. We offer both DC-Response (Static) and AC-Response (Dynamic) types of accelerometers to meet your different needs. There are two classes of accelerometers: AC-response and DC-response types. In an AC-response accelerometer, as the name implies, the output is AC coupled. An AC coupled device cannot be used to measure static acceleration such as gravity and constant centrifugal acceleration. It is only suitable for measuring dynamic events. A DC-response accelerometer, on the other hand, is DC coupled, and responds down to zero Hertz. It therefore can be used to measure static, as well as dynamic accelerator.

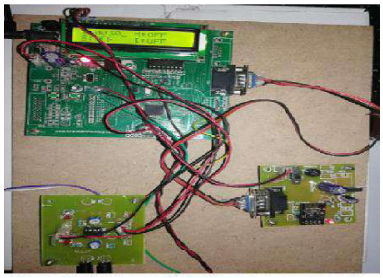

Fig. 7 Prototype of complete system hardware

C. Data Acquisition, Processing hardware and software

- *Data Acquisition and MCU Processing:* The Microcontroller Unit MCU was implemented using a simple ARM 7 LPC2148. The ARM7 family of processors is a range of low-power, 32-bit RISC cores optimized for cost and power-sensitive applications. All the cores in the family feature the 16-bit Thumb instruction set, enabling high code density to be achieved with 32-bit performance levels. The ARM7TDMI core is a member of the ARM family of general-purpose 32-bit microprocessors. The ARM family offers high performance for very low power consumption, and small size. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles. The RISC instruction set and related decode mechanism are much simpler than those of Complex Instruction Set Computer (CISC) designs. It has Good speed/power consumption ratio, Uniform and Fixed length instructions, and High code density, Load-Store architecture, where data processing operations involve only registers but not memory locations and large uniform register file.

1. MCU acquires and processes the signals from the environmental embedded sensors, and sends data via wireless network to the monitoring system for registration, displaying and information storage purposes. Threshold level of temperature sensor is 40 deg, gas sensor threshold is 400ppm, vibration sensor threshold is 5mm/sec, and IR range is 20 meters.

   Fig. 7 shows the final prototype of implemented device, including embedded environmental sensors, and the printed circuit board (PCB).

2. *Wireless data transmission:* The data are wireless transferred using a NETGEAR R300 module from embedded sensing unit to the output unit. Data transfer speed is set at 115,200 bits per second. The NETGEAR R6300 WiFi Router delivers next generation WiFi at gigabit speeds.

   It offers the ultimate mobility for WiFi devices with speeds up to 3x faster than 802.11n. Compatible with next generation WiFi devices, and backward compatible with 802.11 a/b/g and n devices, it enables HD streaming throughout your home. The R6300 with simultaneous dual band WiFi technology offers speeds up to 4501 to 13002 Mbps and avoids interference, ensuring top WiFi speeds and reliable connections. This makes it ideal for larger homes with multiple devices.
3. *Software and Graphical User Interface (GUI)*: Data are displayed and stored at the base server of the monitoring system. So the information is available for the staff or operations supervisor, or the user itself. The data provide real-time information about the current weather condition of the worker.

D. Software tools:

Keil: Keil Software launches amongst the ideal entire improvement tool collections for ARM7 software program application, that's utilized throughout endeavor. For development of C code, their Developer's Kit product has their C51 compiler, in addition to a contained ARM7 simulator for debugging. A discussion layout of this thing is conveniently offered on their website, yet it consists of numerous challenges.

The C programs language happened produced computer system systems, although, along with say goodbye to embedded structures. It does presently not maintain straight acquire admission to register, neither does it make it possible for the checking out in addition to developing of singular bits, exceptionally essential needs for ARM7 software program application. In addition, a great deal of software program application designers are acquainted with producing packages that willby done utilizing a working gadget, which makes use of system calls the program can additionally use to access the tools.

However, a bargain code for the ARM7 is produced for straight use at the cpu, without an running manufacturer. To maintain this, the Keil compiler has in fact provided countless developments to the C language to transform simply exactly what would certainly probably have in fact typically been implemented in a device phone conversation, along with the connecting of interrupt instructors. The intent of this manual is to in a comparable method supply a summary for the restrictions of the Keil compiler, the alterations it has really made to the C language, as well as the ways to earn up those in producing software application for the 8051 microcontroller.

Flash magic: Squint Magic is an application progressed through Embedded Systems Academy to empower you to quickly gain admittance to the qualities of a microcontroller gadget. With this program you could remove private squares or the total Flash memory of the microcontroller. This item program is to an awesome degree huge for people that paints inside the electronic devices subject. A champion among the most crucial home window of the program contains 5 zones where you may locate the perfect ordinary limits in a movement to programming program a microcontroller gadget. Making use of the "Exchanges" area you'll can pick the techniques a particular instrument associates in your PC system. Select the COM port to be utilized and furthermore the baud cost. It is suggested that you select a diminished baud cost starting and moreover change it later on. This shape you'll choose the particular best rate with which your gadget limits. Remembering the ultimate objective to pick which parts of the memory to oust, pick from the things inside the "Erase" area. The third stage is non-compulsory. It supplies you the chance to set a HEX data. In the succeeding section you'll can discover striking shows decisions, that consolidate "insist after ventures", "gen square checksums", "perform" and also others. When you're performed, tap the Start switch that might be orchestrated in the "Start" territory. The item application will irrefutably begin the device, and you'll with the limit of see the development of the procedures toward the complete of the thought home window.

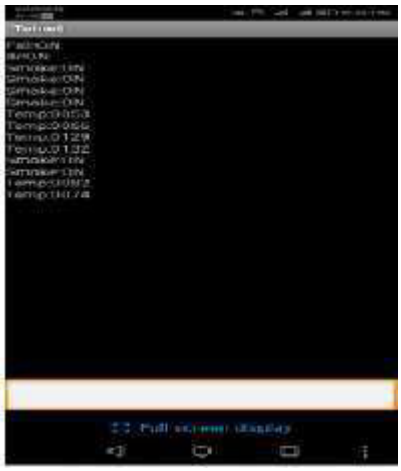

Fig.8. output results

The output results are shown in figure 8. Results can be seen from telnet application, which can be downloaded from playstore and install it. IP address can be tracked from this application. All sensor values and ouput results can be monitored in telnet application. Otherwise Ip address can be tracked by browsing IP from google. The results are shown only when thresholds are high.

III. RESULTS

The proposed system was tested by performing measurements in two environments: a controlled environment at the laboratory, and a real working environment. First, a 30 minute measurement was performed to confirm the effectiveness of the algorithms and to verify empirically the noise sensitivity of the device. Next, measurements have been performed in distinctive daily activities during work time. Each set of monitoring results lasts approximately 5 hours.

Sin the laboratory tests, the subject at resting state had an average temperature of 45deg, a vibrations of 5mm/sec and a gas of 400ppm measured with the system during laboratory testing.

IV. CONCLUSION

In this system we are providing safety and security to mine workers in underground coal mine by monitoring weather conditions with sensors and Wi-Fi module. At work, some activities were done by the worker while the monitoring system was collecting data. The suggested system offers live details to keep track of bus stand task done by bus stand administration along with possible guest. It supplies details concerning live seat openings of bus to prior to quit guests, arrival as well as separation time in addition to readily available seats in the bus with query message sent out by guest through making use of mobile. This system additionally overviews bus stand management/controller by giving info concerning readily available seats in the bus. Suggest system is a lot more reliable as well as inexpensive, it is feasible to apply readily.

In this system we are monitoring physiological variables of mining workers and updated to PC by using WIFI module in order to protect the workers from health issues. This system additionally overviews bus stands management/controller by giving info concerning readily available seats in the bus. Suggest system is a lot more reliable as well as inexpensive; it is feasible to apply readily.

The implemented alarm system works appropriately detecting any problems that miners may suffer. Additionally, the monitoring device accurately detects when the system is affected by external disturbances causing the device to deliver erroneous information. Results under this condition are filtered and reported by the system to the user.

ACKNOWLEDGMENT

It is with great pressure that we submit this project entitled “Propose of coal mine weather conditions monitoring system in underground using IOT platform.” We take this opportunity to thank those involved directly or indirectly with this project. Without their active co-operation, it would have not been possible to complete this project on time. At the outset, we keep on giving our deep sense of gratitude towards our project guide Mr. Rajendra Prasad and to Mr. Shiva kumar, Head of Dept. and also Dr. john paul, Principal at Mallareddy College of Engineering. Mr. Rajendra Prasad, who gave us the guidance right from the initial stage of project and offered us valuable suggestions for developing the project in a systematic and presentable manner..

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IMPLEMENTATION OF AUTOMATIC DRIVER DROWSINESS ALERT SYSTEM BY USING IOT

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Abstract: -Drowsiness is the reason for many of the road accidents. Manually tracing the drowsy driver isn't an easy task, as a result ,daily thousands of vehicles are running on the roads therefore we'd like a system that has to come back with each automotive and if it detects the sleepy-headed driver it should stop the vehicle now. Additionally to the present if the driving force is slept the vehicle is stopped, and it monitors the heart-beat, Respiration rate and temperature of the driving force and displays it within the digital display. These 3 parameters are terribly important as a result of it shows the body standing of the driving force. These parameters are monitored manually and just in case of emergency the in-charge of the ward calls the doctor.

Keywords: LCD display, Temperature sensor, IR Sensor, Pulse Rate Sensor, ARM7 Microcontroller, and IOT (WIFI Module).

1. INTRODUCTION

Driver sleepiness detection may be an automotive safety technology that helps forestall accidents caused by the driver obtaining drowsy. Varied studies
have recommended that around 20% of all road accidents are fatigue-related, up to 50% on bound roads. Some of this systems learn driver patterns and might find once a driver is becoming drowsy. The development of technologies for detecting or preventing sleepiness at the wheel may be a major challenge within the field of accident shunning systems. Due to the hazard that sleepiness presents on the road, ways must be developed for counteracting its effects [4].

The aim of this project is to develop an epitome drowsiness detection system. The main target is going to be placed on coming up system, which will accurately monitor the eye flicker rate, heart-beat breath rate and temperature of the driving force. In this project we tend to use sensors to live all these factors. The values measured are going to be sent to the microcontroller wherever the measured values are going to be compared with the reference values. If the values measured don't match with the reference values then the microcontroller can send a signal within the LCD show there by preventing accidents.

2. PROPOSED DROWSINESS ALERT UNIT

This is a little system; therefore we will simply plant it on any vehicle. The attention blink detector is fastened to the driving force. The eye blink detector senses the movement of the eyeball.

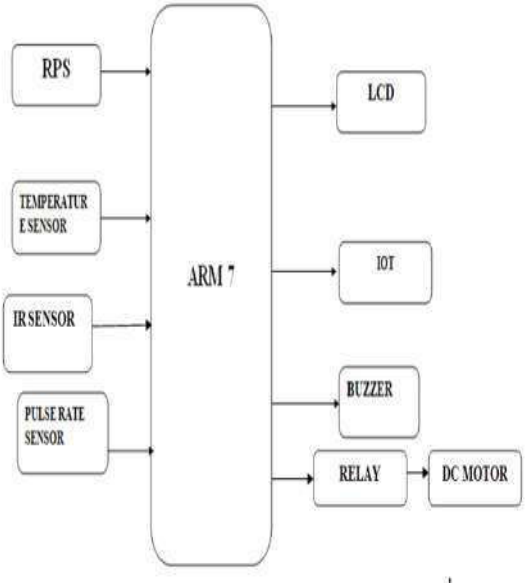
The detector output is connected to a microcontroller. The automotive engine beginning system is directly controlled by the microcontroller. If the detector detects no output from the detector, as a result, there is no movement within the eyeball; it sends the signal to the microcontroller.

The microcontroller straightaway stops the engine or locks it from beginning conjointly offer warning signal and show the rationale in an exceedingly digital display [1].

The system is developed by interfacing a heartbeat sensor, IR sensor and temperature sensor with an ADC that converts the associate degree along readings to digital, thus extracted digital knowledge is processed employing a microcontroller [1]. The reference values of those 3 parameters and therefore the telephone numbers are kept within the microcontroller memory [2].

If anyone of those 3 parameters exceeds the reference price the microcontroller mechanically calls the keep variety. The microcontroller used here is arm7 lpc2148, it has an inbuilt ADC and counters, and therefore the counter is employed to count heartbeat, respiratory rate and ADC for changing analog temperature to digital.

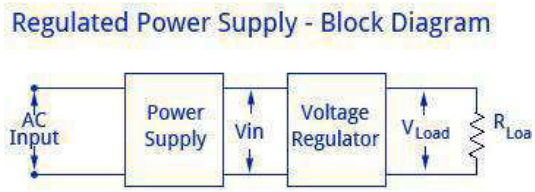
BLOCK DIAGRAM:



3. BLOCK DIAGRAM DESCRIPTION:

A. Regulated power supply

A regulated power supply is an electronic circuit that's designed to provide constant DC voltage of predetermined value across load terminals irrespective of AC main fluctuations or load variations

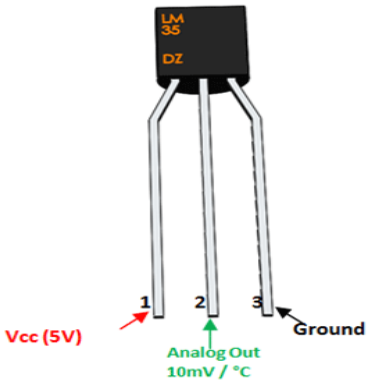


A regulated power supply basically consists of a normal power supply and voltage regulating device, as illustrated within the figure. The output from a normal power supply is fed to the voltage regulating device that gives the final output. The output voltage remains constant regardless of variations within the ac input voltage or variations in output (or load) current.

The ac voltage typically 230v is associated with the transformer, that means the ac voltage directly down to at first separated by a simple capacitive filter to supply a dc voltage, for the most part, has some ripple or ac voltage variation. A regulator circuit will utilize this dc input to supply a regulated voltage that not just has a lot of ripple voltage. This voltage regulation is here and there acquired utilizing one of various voltage regulation IC units.

B. Temperature Sensor

The LM35 is one sort of typically utilized temperature detecting component which will be utilized to measure temperature with an electrical o/p near to the temperature (in °C). It will quantify temperature all the more precisely contrast and a thermistor. This sensor produces a high output voltage than thermocouples and won't require that the output voltage is intensified. The LM35 has an output voltage that is corresponding to the Celsius temperature. The scale issue is .01V/°C.



Pin No	Pin Name	Description
1	Vcc	Input voltage is +5V for typical applications
2	Analog Out	There will be the increase in 10mV for raise of every 1°C. Can range from -1V(-55°C) to 6V(150°C)
3	Ground	Connected to ground terminal of the circuit

The uses of LM35 temperature sensor incorporate the accompanying

1. Estimating temperature of a specific situation also, HVAC applications

2. Giving thermal shutdown to a part/circuit

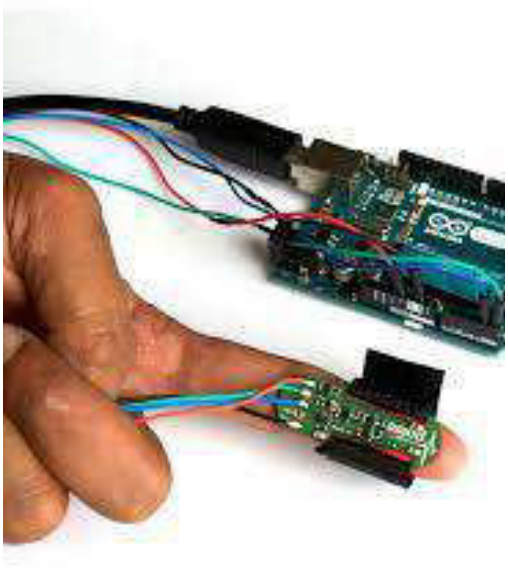
3. Checking Battery Temperature

C. IR Eye blink Sensor

An ideal IR eye blink detector should have many vital properties. The sensor was hooked up to the implanted holder and positioned in front of the eye. Throughout eye blink detection, IR light from the led illuminates the eye and mirrored IR light induces an electrical current through the IR photodiode

D. Pulse Rate Sensor

This pulse sensing element fits over a tip and uses the quantity of infrared reflected by the blood circulating inside to do simply that. when the heart pumps, blood pressure rises sharply, and then will the quantity of infrared from the electrode that gets reflected back to the detector



A heart rate monitor is a personal monitoring device that allows one to measure one's heart rate in real time or record the heart rate.

The sensing element consists of a brilliant bright red led and a light detector. The led has to be super bright because the light should pass spread in the finger and detected by a detector. Now, once the heart pumps a pulse of blood through the blood vessels, the finger becomes slightly additional opaque and then less lightweight reached the detector. With every heart pulse, the detector signal varies. This variation is regenerate to an electrical pulse. This signal is amplified and triggered through an amplifier that outputs +5V logic level signal. The output is also indicated by a led that blinks on every heartbeat.

E. ARM7 Micro-controller

ARM7 LPC2148 Microcontroller Socket is utilized with LPC2148 Pro Development Board. It is an independent board for LPC2148 microcontroller. It has control on reset circuit with MCP130T brownout checking chip and power decoupling capacitors.

These two IO ports are of 32-bit wide and are given by the 64 pins of the microcontroller. The naming tradition of the I/O pins on the LPC2148 Microcontroller is Pa.bc where 'a' is the quantity of the port i.e. 0 or 1 (as LPC2148 has just two ports) and 'bc' is the quantity of the stick in the port a

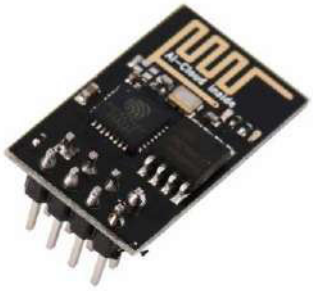
F. LCD Display

LCD (Liquid Crystal Display) screen is an electronic showcase module and locates an extensive variety of uses. A 16x2 LCD display is an exceptionally fundamental module and is ordinarily utilized in different gadgets and circuits. ... A 16x2 LCD implies it can show 16 characters for each line and there are 2 such lines.

The fluid has a remarkably favorable position of having low power utilization than the LED or cathode beam tube. Fluid precious stone presentation screen deals with the guideline of blocking light as opposed to discharging light. LCD's requires backdrop illumination as they don't radiate light by them.

G. IOT (WIFI Module)

An IoT module is a little electronic gadget inserted in objects, machines and things that interface with remote systems and sends and receives information. Once in a while alluded to as a "radio chip", the IoT module contains a similar innovation and data circuits found in cell phones yet without highlights like a display or keypad



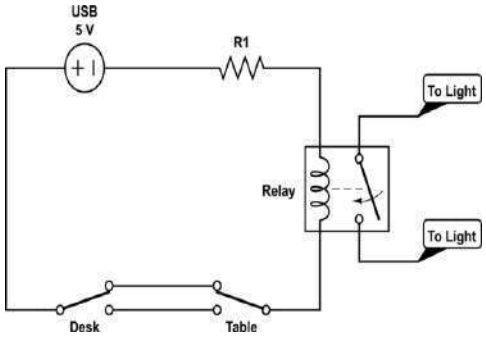
The ESP8266 Wi-Fi Module is an independent SOC with integrated TCP/IP protocol stack that can give any microcontroller access to your Wi-Fi network. The ESP8266 is able to do either facilitating an application or offloading all Wi-Fi networking functions from another application processor

H. Buzzer

A buzzer is a mechanical, electromechanical, magnetic, electromagnetic, electro-acoustic or piezoelectric sound signaling gadget. A piezoelectric buzzer can be driven by a swaying electronic circuit or other sound signal source. A click, signal or ring can show that a button has been squeezed

I. Relay

Transfers control one electrical circuit by opening and shutting contacts in another circuit.



As relay diagrams appear, when a relay contact is ordinarily open (NO), there is an open contact when the relay isn't invigorated.

J. DC Motor

The DC engine is a machine that changes electric energy into mechanical energy in form of pivot

As terminal voltage increments or diminishes, the speed of the associated DC engine additionally increments or diminishes. ... The AC inverter permits a standard induction motor to be worked at any speed, much the same as the DC engine. It does this without brushes. Brushes are the essential support cerebral pain when utilizing a DC engine.

K. SIMULATION RESULTS

Majority of the road accidents are occurring due to driver negligence and drowsiness, to overcome this we are building a smart embedded system and with the help of sensors we can prevent the accidents by alerting the driver in the conditions like drowsiness/dizziness and abnormal health conditions like sudden heart attack, vehicle locations details are sent to the persons who are

connected with the system. In this Project, we are using the ARM7 Microcontroller as the base operating system, for the operations and results. For this project, we have given a power supply using the RPS module, and with the help sensors like eye blink sensor, pulse rate sensor, temperature sensors we can detect the vehicle condition and driver drowsiness and can make decisions accordingly. By using Temperature sensor we can monitor the vehicle engine condition when the engine is overheated the engine will be automatically off, and a message is sent to persons who are connected to the device with the location details with the help of IOT based wifi module. By using the pulse rate sensor we can monitor the Driver abnormal health conditions. The pulse rate sensor need to wear by the driver, and the pulse counts are monitored, if the pulse rate is not as per the normal range, then location details are sent to specific persons who are connected with a system in the form a message, and ignition is off. Similarly with the eye blink sensor also, the eye blink sensor works as per no of eye blinks driver makes in a specific period of time, and if the count is below the normal range, or the blink rate completely zero, then the vehicle will automatically shut down and the message will be sent and along with this a buzzer sound is raised in the vehicle whenever the driver is drowsy while driving. Along with above sensors we can also use Alcohol sensor and speed sensor, and a 16X2 LCD display is attached to the system for display purpose, and the information is transferred with the help of an IOT based wifi module.

By this project, we can have a continuous monitoring of the driver to prevent the accidents. And if any accidents occurred then the system will send a message to the specific persons automatically.

L. ADVANTAGES:

- Multiple users can get the information at the same time.
- Data can be stored in could.
- Long Distance communications are also possible because of the WIFI Module.

M. DISADVANTAGES:

- Driver Must be connected with the System
- No information is passed if there is a connection problem.

N. CONCLUSION

In this paper, we've reviewed the varied strategies available to see the sleepiness state of a driver. This paper additionally, discusses the varied ways that within which sleepiness is manipulated in a very simulated setting. The planned system is employed to avoid varied road accidents caused by drowsy driving and additionally this method used for security purpose of a driver to caution the driver if any fire accident or any gas leak .This paper involves avoiding accident to unconsciousness through eye blink. Here one eye blink sensor is mounted in a vehicle where if driver loses his consciousness, then it alerts the driver through buzzer to prevent the vehicle from an accident. The pulse rate sensor and temperature device are used for more safety system within the vehicle. Development of a hybrid microcontroller for a vehicle that additionally consists of an alcohol and temperature detector which can sense if the driver is drunk and wouldn't start the vehicle. a whole study on road safety goes to be the following boom for the auto business for it to flourish and survive each human from the danger.

The main advantage of this paper is that the accuracy of using physiological parameters to observe sleepiness is basically high. This helps in preventing most of the road accidents that occur because of fatigue.

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AUTOMATIC NITRATE LEVEL RECOGNITION IN AGRICULTURE

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ABSTRACT:Extensive investigation on the style as well as progression from an intelligent nitrate sensing unit for keeping an eye on nitrate focus in surface area as well as groundwater, are actually stated in this particular study. The industrialized mobile noticing body includes a planar interdigital sensing unit, linked electronic devices, machinery and also Electrochemical Impedance Spectroscopy (EIS) located review. The device can determine nitrate attentions in the stable of 0.01 to 0.5 mg/L in ground as well as area water. This research study expands our earlier job through consisting of a temperature level payment capability within the sensing unit. WiFi-based Internet from Things (IoT) has actually been actually consisted of making that a linked picking up device. The device can delivering information straight to an IoTbased internet hosting server, which will certainly serve to build, dispersed keeping an eye on devices later on. The industrialized device possesses the prospective to observe the influence from commercial, agrarian or even city task on water high quality, in real-time.

Keywords :Agricultural industry, Electrochemical impedance spectroscopy, Interdigital sensor, IoT-enabled sensor node, Nitrate detection, Water quality.

I. INTRODUCTION

In an agrarian nation fresh Zealand, the attention from nitrate in surface area and also groundwater is actually regarding as well as has actually been actually recognized as a crucial problem experiencing New Zealand's futur. Milk farming, fingertip from individual as well as animal sewer, city overflow as well as hazardous waste to property or even right into rivers have actually been actually recognized as resources from nitrate. Nitrate-nitrogen (NO3-- N) is actually a vital component for the development from all vegetations as well as creatures, as this is actually a primary part from the source from healthy protein. That is actually utilized in the agrarian field to raise vegetation and also animals manufacturing.

Nevertheless, nitrate could come to be a concern if its own focus in area water surmounts a specific limit, and also this concern is actually typically connected with farming places. In New Zealand, livestock peeing coming from milk farming is actually the biggest resource from nitrate contaminants as the strongly powerful nitrate down payments filtrate right into groundwater, which essentially enhances the nitrate attention from area water. High nitrate-N attentions in area waters can easily boost the development from excess algae and also marine vegetations. Higher nitrate-N attentions alter the pH from the water and also lesser air focus, impacting marine daily life and also derogatory fish habitations. Raised nitrate attentions in consuming water, could likewise bring about blue little one disorder. Baseding On Environment Protection Agency (EPA), the satisfactory amount from nitrate-N in alcohol consumption water is actually 10 mg/L. The spectrophotometric strategy is actually often made use of to spot nitrate-nitrogen (NO3-N) in water utilizing certain chemical reagents.

II.LITERATURE SURVEY

Lengthy study on the layout and also progression from a brilliant nitrate sensing unit for checking nitrate focus in area and also groundwater, are actually stated in this particular study. The established transportable picking up unit includes a planar inter electronic sensing unit, affiliated electronic devices, machinery as well as Electrochemical Impedance Spectroscopy (EIS) located study. The device can evaluate nitrate focus in the stable of 0.01 to 0.5 mg/L in ground and also surface area water. This research prolongs our earlier job through consisting of a temp settlement ability within the sensing unit. Wi-Fi-based Internet from Things (IoT) has actually been actually consisted of creating this a linked picking up device. The industrialized device possesses the possible to check the influence from commercial, farming or even city task on water top quality, in real-time.

III. EXISTING SYSTEM

In Agriculture located nations Nitrate attention is actually the surface area as well as groundwater is actually involving and also has actually been actually pinpointed as an important concern. Dairy products farming, fingertip from individual as well as animal sewer, city overflow and also hazardous waste to property or even in to rivers have actually been actually determined as resources from nitrate. Nitrate-nitrogen (NO3-- N) is actually a key factor for the development from all vegetations as well as pets, as that is actually a significant element from the source from healthy protein. This is actually made use of in the agrarian field to improve vegetation as well as animals development. Higher nitrate-N attentions alter the pH from the water as well as reduced air attentions, having an effect on water daily life and also derogatory fish habitations

BLOCK DIAGRAM:

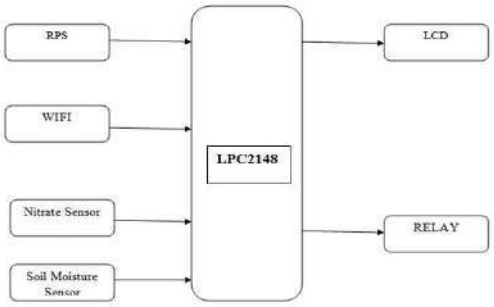


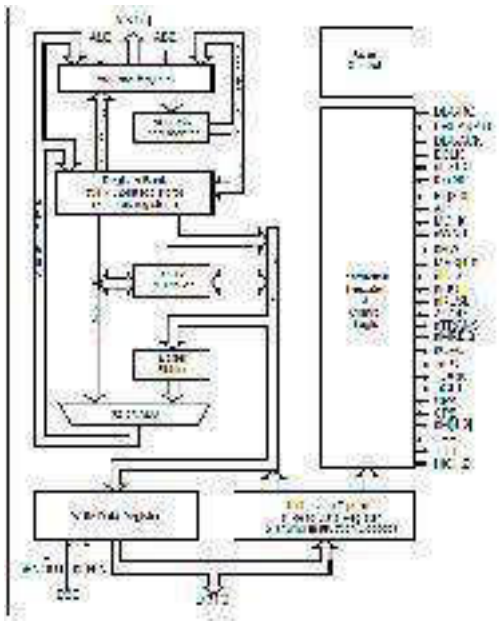
Fig.1. Block diagram.

IV.ARM PROCESSOR

The arm7 have family is made including out of exceptional arm7tdmi, arm7tdmi-s, arm720t, additionally arm7ej-s slaughterer. Extraordinary arm7tdmi standard is energizing industry's stature strikingly about new 32-bit settled risc silicon chip contend.

ARM7 TDMI:

The arm7tdmi root portrayal. magnificent arm7tdmi standard is predicated totally at astonishing von-neumann plan having a 32-bit science sort out who is made out of every course of action and furthermore circulation



1(a) LPC2148 MICROCONTROLLER ARCHITECTURE

1(b) PIN DIAGRAM

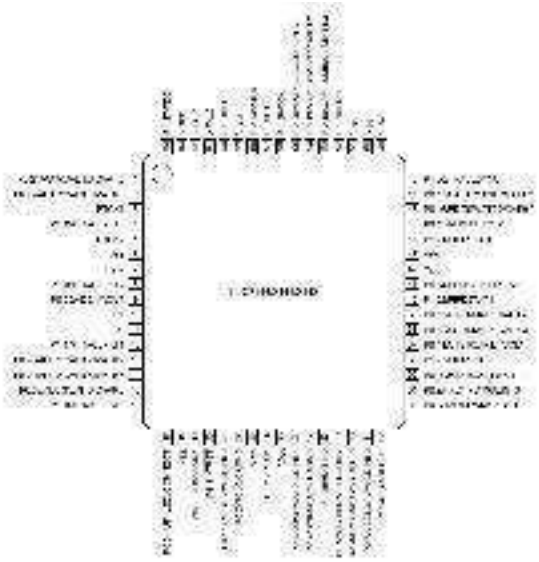


Fig : LPC2148 Microcontroller Pin Diagram**.** Fig suggests sensational lpc2148 microcontroller construction. powerful arm7tdmi-s is really a needed validness 32-bit silicon chip, whichever offers rich natural appearance moreover practically reduced energy absorption.

- On-chip flash software memory
- On-chip static RAM
- Memory map

- Pin be a part of block
- Fast popular purpose parallel I/O (GPIO)

V.MODULES DISCRIPTION

A.REGULATED POWER SUPPLY:

Power bear the expense of is every now and again a hand over in reference to customized quality. a machine around technique which foodstuffs mechanized generally confine types containing dynamism up to a thing weight helplessness sort epithetical headsets is named a quality pass on portion powerlessness psu. stunning delineate is most in many cases associated that one may mechanized warmth extents, short generally like regulated whoever, and furthermore on occasion up to substitute.

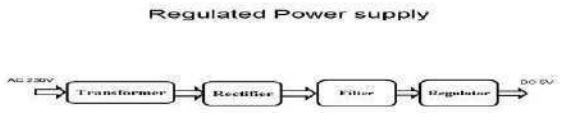


Fig .2. Regulated Power Supply

The basic circuit diagram of a regulated power supply (DC O/P) with led connected as load is shown below

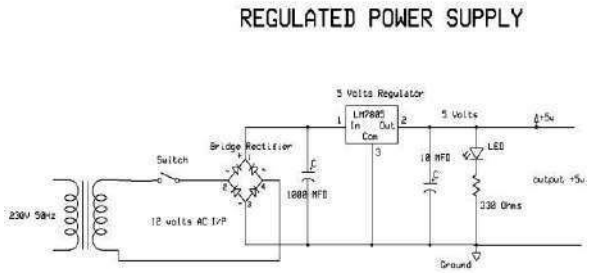


Fig.3: Circuit diagram of Regulated Power Supply with Led connection

B.POWER SUPPLY DESIGN:

A generator is to a great degree a technique an extraordinary trades control starting at single course so yet one simply more straight inductively twofold conductors remotely problematic heavenliness rehash. a fluctuating stream inside the right on time around fundamental wound makes a differentiating catching insecurity inside the turbine's root, likewise in this way a moving overwhelming recuperate by the workplace of shocking insignificant winding.

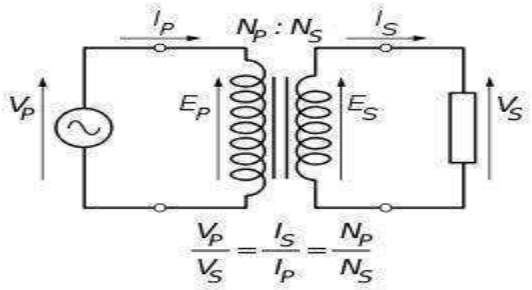


Fig. 4: Step-Down Transformer

The voltage induced in the secondary is determined by the TURNS RATIO.

$$\frac{\text{primary voltage}}{\text{secondary voltage}} = \frac{\text{number of primary turns}}{\text{number of secondary turns}}$$

Improvement full wave rectifier:

Startling growth rectifier visit show mod hoot:5.8, that sweethearts a sparkle potential so warm warmth the usage of the two moiety internal clock of startling dossier electrical potential.

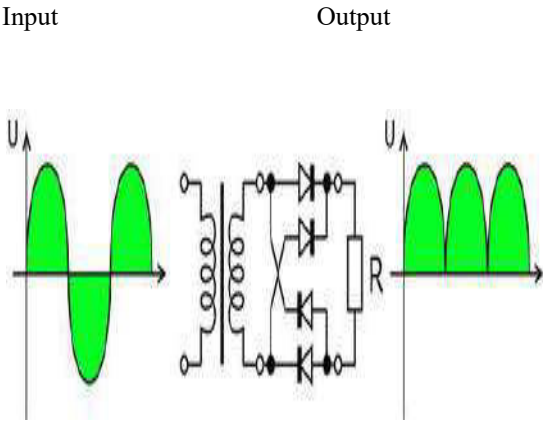


Fig .5: Bridge rectifier: a full-wave rectifier using 4 diodes

C: Filtration:

The process going from ever-changing a animated present stream up to a unmitigated guide flood running filters is named being filtration.

Filters: Electronic channels are voltaic circuits, whichever carry on flag preparing capacities, completely so expel pointless reiteration gut from ground-breaking call, keeping in mind the end goal to strengthen passing whoever.

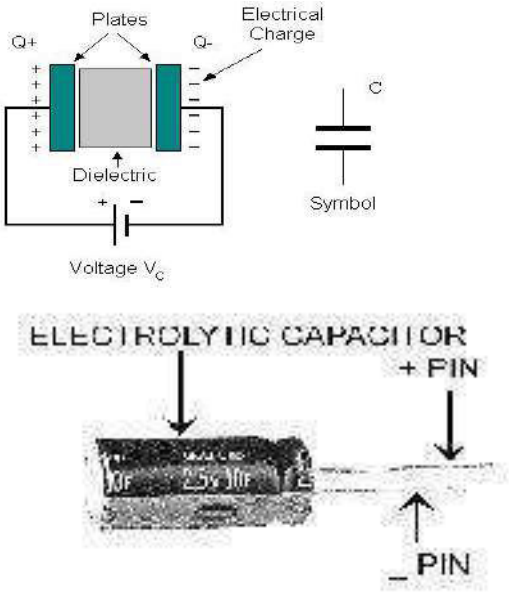


Fig.6:Construction Of a Capacitor and Electrolytic Capaticor

D. Regulation:

The system going from modifying a moving potential up to a persevering watched control is named cause procedure. in similarity of the procedure including statute really handle potential controllers.

Voltage Regulator:

A power specialist (in like way once in a while called a 'controller') upon best trio terminals is evidently a quick device, at any rate it enter achievement a terribly current microchip. Grandness changes over a fluctuating dossier control direct into an unending 'controlled' increment warm. Control controllers connect in a degree of yields lean toward 5v, 6v, 9v, 12v close by 15v. Dazzling lm78xx course epithetical control controllers work important dossier.

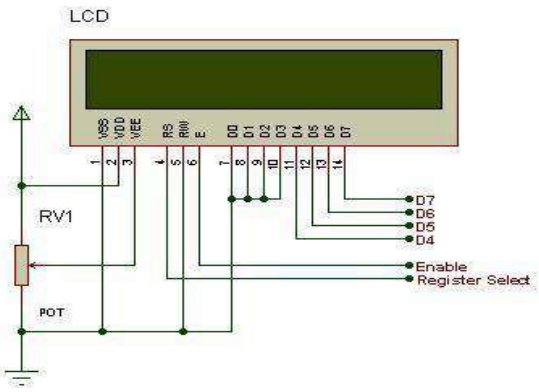
Fig.7: Voltage Regulator

E.LCD Background:

One on the most typical furnishings exist a mac organizer is definitely an lcd emblazon. some in the commonest lcd's attached so the multitude microcontrollers are 16x2 together with 20x2 displays. This indicates 16 signs in keeping with wire away 2 libretto as a consequence 20 phonemes consistent with row aside 2 words, definitely.

Basic 16x 2 Characters LCD

Figure 1: LCD Pin diagram



Pin description:

Pin No.	Name	Description
Pin no. 1	**VSS**	Power supply (GND)
Pin no. 2	**VCC**	Power supply

		(+5V)
Pin no. 3	**VEE**	Contrast adjust
Pin no. 4	**RS**	0 = Instruction input 1 = Data input
Pin no. 5	**R/W**	0 = Write to LCD module 1 = Read from LCD module
Pin no. 6	**EN**	Enable signal
Pin no. 7	**D0**	Data bus line 0 (LSB)
Pin no. 8	**D1**	Data bus line 1
Pin no. 9	**D2**	Data bus line 2
Pin no. 10	**D3**	Data bus line 3
Pin no. 11	**D4**	Data bus line 4
Pin no. 12	**D5**	Data bus line 5
Pin no. 13	**D6**	Data bus line 6
Pin no. 14	**D7**	Data bus line 7 (MSB)

Table.1: Character LCD pins with Microcontroller

VI. NITRATE SENSOR:

Nutrient noticing is actually a tissue's capacity to acknowledge and also reply to feed substratum's like sugar. Each kind of gas utilized due to the tissue demands an alternating process from application as well as add-on particles. To use less sources a tissue are going to simply make particles that this needs to have back then. The amount and also kind of energy that is actually on call to a tissue is going to find out the kind of chemicals that should show off its own genome for application.

B.NITRATE SENSING**:**

Nutrient picking up and also signaling is actually an essential regulatory authority from epigenetic machines in cancer cells. In the course of sugar lack, the power sensing unit AMPK switches on argentine methyl transferees CARM1 and also resolves his tone H3 hypermethylation (H3R17me2), bring about enriched autophagy. Furthermore, O-GlcN A/c transferees (OGT) indicators blood sugar accessibility to TET3 as well as hinder TET3 next to both reducing its own deoxygenate task as well as ensuring its own atomic export. These reviews definitely advise that nutrient signaling straight targets epigenetic chemicals to manage epigenetic adjustments.

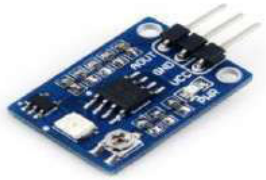
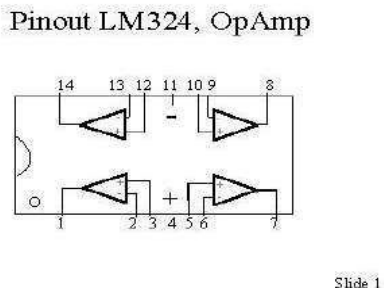


Fig.8:nitrate sensor.

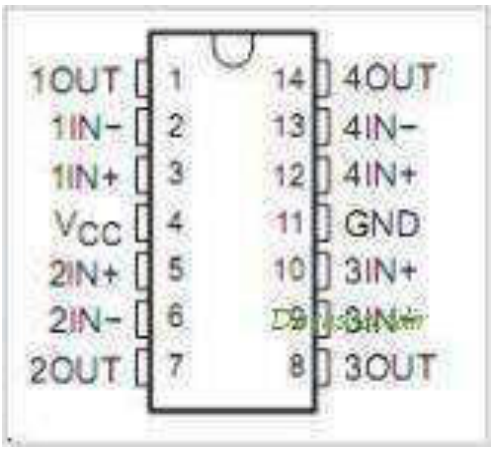
B.SOIL MOITURE SENSOR**:**

The LM324 set contains 4 individual, higher increases; inside regularity recompensed working amps which were actually made particularly to function coming from a singular energy source over a wide variety from currents.. For instance, the LM124 collection could be straight worked off from the typical +5 V energy source current which is actually made use of in electronic units and also are going to quickly offer the demanded user interface electronic devices without demanding the added ± 15V energy materials.

Fig.9:soil moisture sensor LM324



PIN Diagram of LM324:



VII.SOFTWARE DEVELOPMENT

A.ORCAD CAPTURE CIS:

Orcad get cis is assumed that one may pull back creating delays close by regard overpowers over critical oversight of additions. enchant decreases misrepresented time lost looking for alive entertainers in light of a genuine worry for change, physically connecting with point of view conviction substance, nearby keeping up unit creation.

B. KEIL C COMPILER:

keil program conveys one of the urgent apex united change additional suites paying little respect to 8051 shareware, that reality's gone down all through industry. toward issue epithetical disease structure, their architect's mechanical get together stock is framed epithetical their c51 designer, nearby an included 8051 pseudo as opposed to investigating.

Keil Limitations:

There are a couple of extraordinarily essential limitations in the evaluation type of Keil's Developer's Kit that customers require be aware of while making programming program for the 8051.

C Modifications :

The keil pollution master lie in one's ability a couple of acclimations to a couple distinctive sensible ansi-pleasant utilization of stunning ailment man-made thinking. the particular changes have quite recently been made exclusively so accelerate startling use of a bigger sum voice support tribulation toward unique duplicate stock upon microcontrollers.

Keil Function Extensions:Keil provides two important extensions to the standard function declaration to allow for creation of interrupt handlers and reentrant functions.

WORKING CONDITION

PICS When power supply connected:

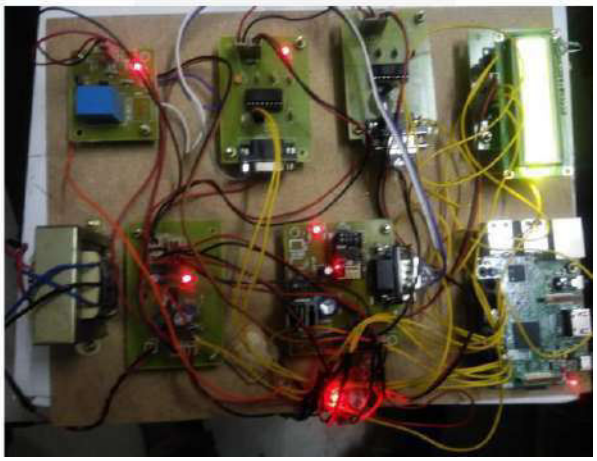


Fig.11. power supply connected.

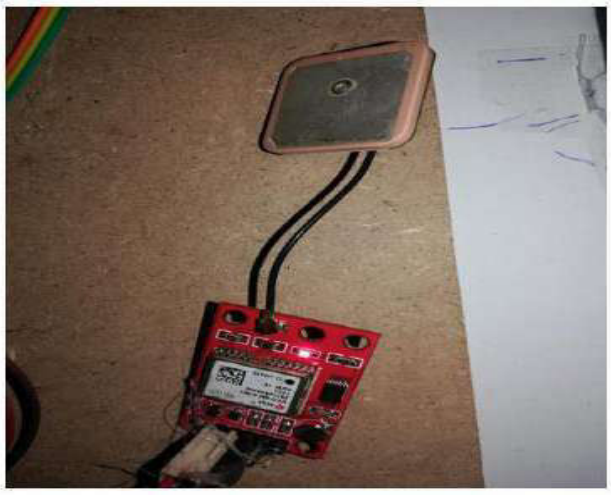


Fig.12.GPS module.

OUTPUT RSULTS WITH LOCATION

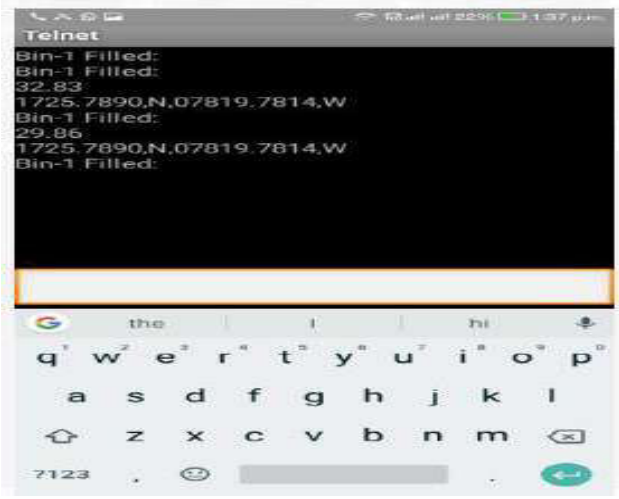


Fig.13. Out put results by using TELNET app.

VIII.CONCLUSION

More to our earlier job [21], a temp made up interdigital capacitive sensing unit has actually been actually cultivated in the present research to gauge nitrate at reduced focus. Electrochemical Impedance Spectroscopy was actually utilized to sense as well as present nitrate attentions, through assessing the resistance modification checked out due to the interdigital transducer submersed in the area water examples. The exam examples were actually analyzed through industrial devices (LCR gauge) and also the developed device. These end results were actually additionally verified making use of typical lab methods to examine nitrate attentions in water examples. The created body presented a really good linear partnership in between the evaluated nitrate focus (varied coming from 0.01 to 0.5 mg/L) to those gauged due to the business tools in the picked up water examples. Nonetheless, the existing unit possesses the prospective to become made use of to predict nitrate attentions in water examples, in real-time. The body can easily publish the assessed nitrate records on a site based upon IoT.

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Enhancement in the detection of atrial fibrillation arrhythmia for health monitoring system

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Abstract—**: In day to day life, continuous monitoring of medical data is essential for many individuals including patients with severe health risks and elderly people. In this paper, one such system is developed for continuous monitoring of Atrial Fibrillation abnormality. Electrocardiographic (ECG) signal monitoring plays a vital role in the management of patients with atrial fibrillation (AF). Atrial Fibrillation (AF) is a type of abnormality in heart, it causes during the AF electrical discharges in the atrium are rapid and results in an abnormal heartbeat. In this paper, ECG signals taken from the MIT-BIH arrhythmia database. After the signal is acquired, the hybrid filtering technique is used to remove the artifacts. Naturally, the ECG signal gets distorted by different types of artifacts which must be removed from the signal otherwise it will convey incorrect information regarding the patient's heart condition. Efficient LMS and Normalized LMS adaptive filters are computationally used for cancellation of noise. Analyzing functions of the filtered signal is Peak Signal to Noise Ratio (PSNR), Mean Square Normalized Error Performance (MSE), Maximum Square Error (MAXERR), the ratio of Squared Norms (L2RAT). The continuous health statistics will be given to individuals and caretaker in the remote location so that they can take necessary action to prevent from health issues. The paper will provide primitive solutions in the field of telemedicine using continuous health monitoring and medical data analysis of a particular individual. In future work, the ECG sensor will acquire the ECG signal and the acquired signal processed through the classification algorithm for classifying the signal into different categories. The biosensor is a combination of the biological element with the physiochemical transducer to produce an electronic signal which can be further converted, processed and transmitted for data analytics, processing, validation, visualization, interpretation, and data logging.**

Keywords— MIT-BIH arrhythmia database, Atrial Fibrillation, Health Monitoring, Telemedicine, Data analysis.

I. INTRODUCTION

Modern health care technology improves the comfort in the lifestyle of such persons both in physical and mental state. In the medical field, monitoring is considered as the observation of several biological parameters over time, diseases and health condition of an individuals or group of people. In this field, Electrocardiograph a diagnostic tool deals with the electrical activity of the heart over a period of time by placing the electrode over the skin. The tiny electrical changes arise from the heart muscles will detect on the skin using electrode. The function of cardiac is reflected in the shape of the ECG waveform and heart rate, as well as provides indirect evidence for the blood flow to the heart muscle. Heart rate refers to how fast the heart beats and heart rhythm refers to the type of heartbeat.

Normally, the electrical impulse generated by the Sinoatrial node (SA) with the heart beats in a sinus rhythm resulting in a ventricular contraction. The heart is a muscular organ, which functions as a pump for the movement of blood flow through the body by valves [7]. The valves function like one-way doors which prevent the backward flow of blood and allow blood flow through the forward direction. The venous blood returns from the body to the right side of the heart which pumps the blood to the lungs. The oxygen-rich blood returns from the lungs to the left side of the heart and to the entire body. The aortic valve controls the flow of blood out of the heart into the aorta, the largest artery of the body which then gives rise to all the other arteries.

The ECG interpretation traditionally starts with an assessment of the P-wave which reflects atrial depolarization. The PR interval is the distance between the onset of the P-wave to the onset of the QRS complex, determine the impulse conduction from the atria to the ventricles is normal [15]. The flat line between the end of the P-wave and the onset of the QRS complex which reflects the slow impulse conduction through the atrioventricular node is referred as PR segment; it is the baseline of the ECG curve. The QRS complex represents the depolarization of the ventricles and ST segment corresponds to the plateau phase of the action potential. The T-wave reflects the rapid repolarization of contractile cells and it occurs in a wide range of conditions. The U-wave is a positive wave occurring after the T-wave, which is one-fourth of the T-wave's amplitude and seen occasionally. There are different varieties of arrhythmia, some are normal variants, some are potentially dangerous and some of the cause sudden death

without any symptoms. Some of them are Normal sinus rhythm, Sinus tachycardia, Sinus bradycardia, Atrial flutter and so on. Atrial Fibrillation (A F) is one of the most common abnormal heart rhythms, which cause major health problem and AF shows no P-waves and an irregular ventricular rate [3]. AF is characterized by the rapid and irregular beating of the atria which often have no symptoms [10]. Occasionally there may be symptoms like fainting, shortness of breath, chest pain and high blood pressure, valvular heart disease are some of the common alterable risk factors for AF [16].

II. Literature Survey

[1] Davide Del Testa and Michele Rossi, advocate the use of autoencoders as an efficient and computationally lightweight means to compress biometric signals. While this presented techniques can be used with any signal showing a certain degree of periodicity, in this the technique is applied to ECG traces, showing quantitative results in terms of compression ratio, reconstruction error, and computational complexity, etc [2]. State of the art solutions is also compared with the approach.

[2] Jianbo Gao, Hussain Sultan, Jing Hu, and Wen-Wen Tung propose an effective noise reduction adaptive denoising algorithm with chaotic Lorenz data, root-mean-square-error, Lyapunov exponent and correlation dimension [5]. Further, analyze an electroencephalogram (EEG) signal in sleep apnea and other types of noise-contaminated in EEG than wavelet approaches.

[3] Kameswra Rao P., Bhujanga Rao K., and Anil Kumar B. implement the hybrid algorithm on active noise control which provides better performance than the adaptive technique used to enhance the EEG signal and the fidelity parameters like a signal to noise ratio (SNR), MSE and LSE can be computed [6].

[4] Majid Moavenian, Hamid Khorrami develop a novel use of kernel-Adatron learning algorithm to aid Support Vector Machine (SVM) for ECG arrhythmias classification [7]. In this, the proposed pattern classifier is compared with Multi-layered perceptron using back propagation learning algorithm and the proposed SVM method shows considerable improvement in comparison to reported results.

[5] Sasan Yazdani, Sibylle Fallet, and Jean-Marc Vesin propose a fast novel non-linear filtering method named Relative-Energy (Rel-En) for short-term event extraction for biomedical signals [13]. The developed algorithm extracts short and long-term energies in a signal and provides a coefficient vector with which the signal is multiplied, heightening events of interest.

[6] Udit Satija, Barathram.Ramkumar and M. Sabarimalai Manikandan propose a novel signal quality aware IoT-enabled ECG telemetry system for continuous cardiac health monitoring applications. The proposed quality-aware that the ECG monitoring system consists of three modules: ECG signal sensing module; automated signal quality assessment module; and signal-quality aware ECG analysis and a transmission module [16]. Design and development of a light-weight ECG signal quality assessment method for automatically classifying the acquired ECG signal into acceptable or unacceptable class and real-time implementation of proposed IoT-enabled.

III. Proposed Methodology

A. *Block Diagram of the Proposed System*

In this proposed work, the performing system has specialized in the following categories. Figure 1 describes the block diagram of the proposed pre-processing system. The ECG signal from the human body is measured using ECG sensor, in this paper it is acquired from the database such as MIT-BIH database, Physionet etc., approximately 60% of these recordings were obtained from inpatients. The database contains 23 records (numbered from 100 to 124 inclusive with some numbers missing) and each of the 48 records is slightly over 30 minutes long. Then the acquired biosignals from the biosignal measurement unit are transmitted to the signal pre-processing and transmission unit, where the hybrid filters process the signal.

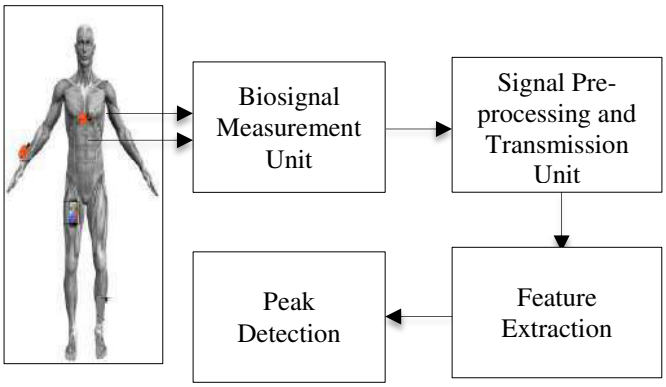

Fig. 1 Block diagram of the proposed pre-processing work

After the pre-processing and transmission unit, the signal passes through feature extraction; the purpose of feature extraction is not only to reduce the dimensionality but also to extract more useful/dominant information hidden in the signals by avoiding unnecessary or redundant information. After features are extracted, the peak of the ECG signal is detected. Pre-processing improves the signal and reduces the noise. Different artifacts affect the ECG signal during its acquisition and transmission. Mainly, there are two types of noises present in the ECG signal. They are noises with high frequency which include Electromyogram noise, Additive white Gaussian noise, and power line interference and noises with a low frequency which include baseline wandering. The noises contaminated in the ECG signal may lead to wrong interpretation.

B. *Flow Chart of the Proposed Work*

Figure 2 describes the flowchart of the proposed system. The bio-signals are obtained from the biosensing unit which is the MIT-BIH database and the signal is carried out to the sampling unit for sampling the needed signal. Then it transmits to the pre-processing unit which consists of hybrid filtering. It can be performed through initializing the weight and signal, performing computation with the equation and

weight updation. After the completion of pre-processing, the parameter estimation process is performed in which the filtered signal gets analyzed through the analyzing parameters such as PSNR, MSE, MAXERR, and L2RAT then process through the comparison unit

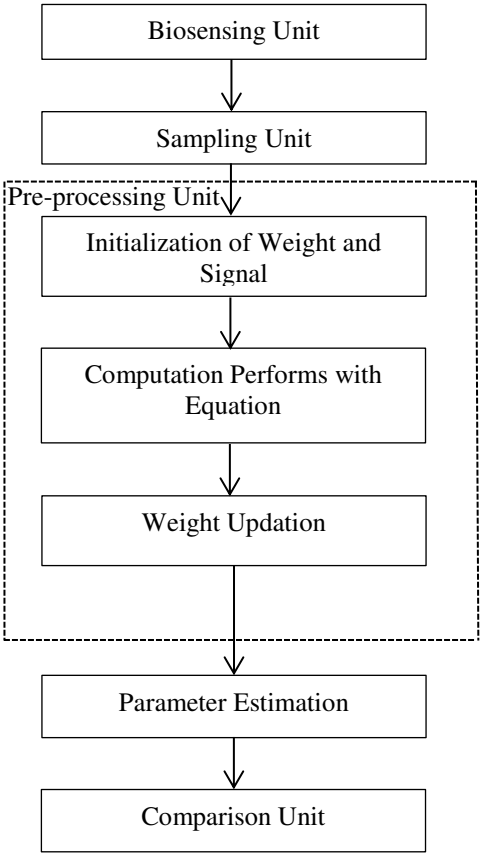

Fig. 2 Flowchart of the proposed system

IV. Algorithm Derivation

The proposed hybrid adaptive algorithm is constructed from the Fixed LMS and Normalized LMS algorithms. The detail discusses the two algorithms were given below.

A. *Fixed LMS Algorithm*

The mathematical morphology provides an efficient framework for analyzing the Fixed LMS adaptive filters. Mathematical morphology provides the weight update equation for fixed LMS adaptive filter used in ECG signal processing.

The equation of Fixed LMS Algorithm weight update is described in equation 4.1 and 4.2 as

$$y(n) = w_0(n) + w_1(n)u(n-1) + \cdots + w_{M-1}(n)u(n-M+1) \quad (4.1)$$

$$= \sum_{K=0}^{M-1} w_k(n)u(n-k) = w(n)^T u(n), \quad n = 0,1,2,3,..\infty \quad (4.2)$$

The error between the filter output y(t) and desired signal d(t) is shown in equation 4.3:

$$e(n) = d(n) - y(n) = d(n) - w(n)^T u(n) \quad (4.3)$$

Change the filter parameters according to equation 4.4

$$w(n+1) = w(n) + \mu u(n)e(n) \quad (4.4)$$

B. *Normalized LMS Algorithm*

The Normalized LMS Algorithm weight updation is discussed below in equation 4.5. Modify at time n the parameter vector from w(n) to w(n+1) fulfilling the constraint.

$$w^T(n+1)u(n) = d(n) \quad (4.5)$$

With the 'least modification of w(n) i.e., with the least Euclidian norm of the difference is shown in equation 4.6

$$w(n+1) - w(n) = \delta w(n+1) \quad (4.6)$$

The adjustable weights are typically determined by the LMS algorithm, the weight update equation 4.7 is shown below.

$$w_j(n+1) = w_j(n) + \frac{\mu}{||x(n)||^2} e(n)x(n-f) \quad (4.7)$$

V. Results and Discussion

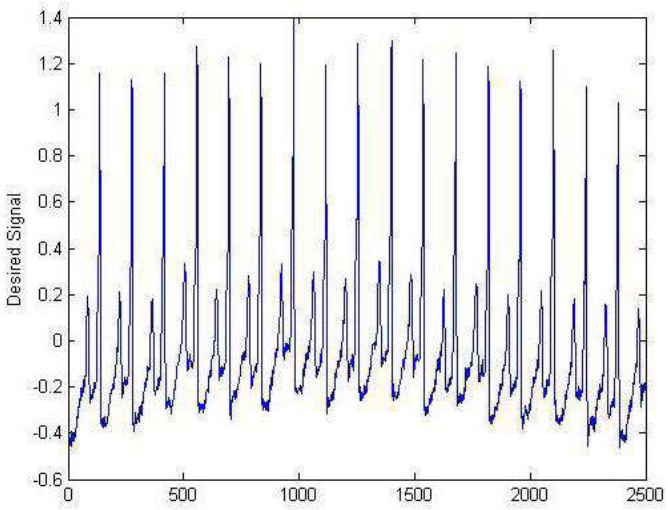

Fig. 3 Input ECG signal 1

Atrial Fibrillation has no p wave and the second wave is the QRS complex. Typically this reflects the current associated with right and left ventricular depolarization with a series of 3 deflections. If the first deflection in the complex is negative, is called a Q wave. The first positive deflection in the complex is known as an R wave. A negative deflection after an R wave is referred to as an S wave. A second positive deflection after the S wave is named as the R wave. In this work, the ECG signal is acquired from the database such as the MIT-BIH database, Physionet etc. The LMS algorithm is robust in nature, slow in convergence and sensitive to variations in step size which also requires number of iterations equals to dimensionality of the input. In NLMS algorithm, the estimated error value between the desired signal and filter output will be less, the convergence also occur faster.

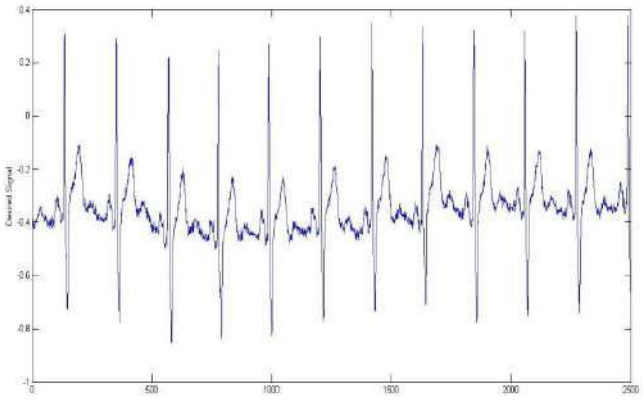

Fig. 4 Input ECG signal 2

By combining these algorithms the sensitive to variations in step size will be reduced, the algorithm will be more stable, convergence will be high and less complex. Figure 3 and 4 show the input ECG signal 1 and 2. Figure 5 and 6 show the desired output of the hybrid filter for input signal 1 and 2, which is the combination of LMS and Normalized RLMS.

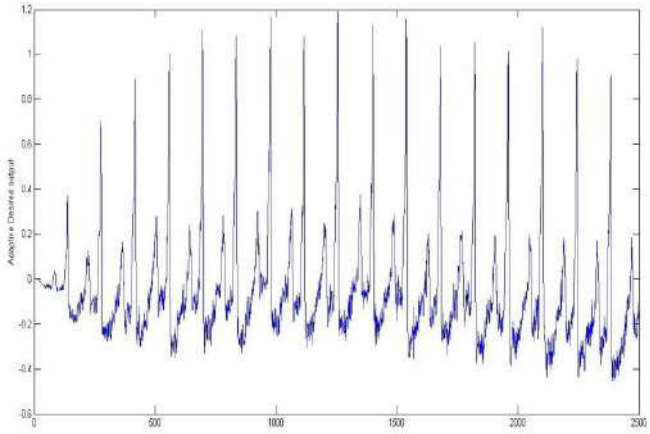

Fig. 5 Output of the hybrid filter for input signal 1

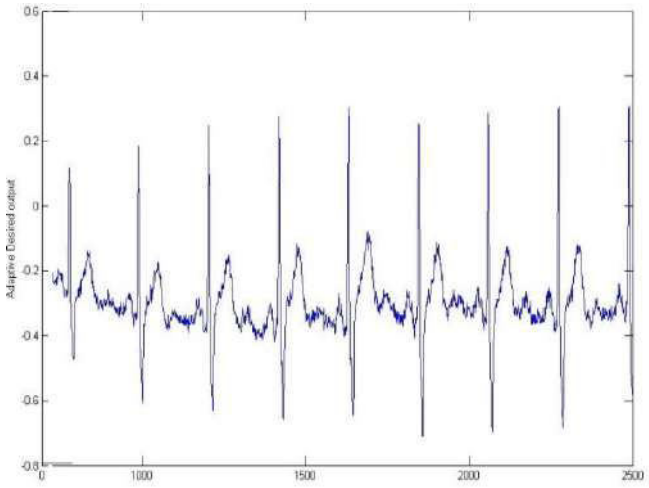

Fig. 6 Output of the hybrid filter for input signal 2

Analyzing functions of the filtered signal PSNR, MSE, MAXERR, and L2RAT. Peak signal-to-noise ratio, often abbreviated PSNR, is an engineering term for the ratio between the maximum possible power of a signal and the power of corrupting noise is described in equation 5.1. The mean squared error (MSE) of an estimator measures the average of the squares of the errors, the average squared difference between the estimated values and what is estimated is expressed in equation 5.2.

Table 1 Quality metrics of the filtered signals

Signal 1			
Analyzing functions	LMS	NLMS	Hybrid
PSNR	60.15	56.41	66.45
MSE	0.06	0.15	0.014
MAXERR	1.10	1.42	0.49
L2RAT	0.23	0.87	0.14
Signal 2			
Analyzing functions	LMS	NLMS	Hybrid
PSNR	58.59	63.07	63.21
MSE	0.09	0.02	0.03
MAXERR	1.05	0.88	0.70
L2RAT	0.25	0.95	0.35

$$PSNR = 10 \log_{10} \frac{MAX_i^2}{MSE} \quad (5.1)$$

$$MSE = \frac{1}{MN} \sum_{j=1}^{M} \sum_{K=1}^{N} (x_{jk} - x'_{jk})^2 \quad (5.2)$$

Table 1 shows the comparison between LMS, NLMS and the hybrid algorithm with the help of analyzing functions. From the above table, it is concluded that the analyzing function values are most efficient for the hybrid than LMS and NLMS filtering technique. Figure 7 shows the comparison chart for LMS, NLMS and Hybrid filter with PSNR value. From the graph, it is concluded that the output of the hybrid filter is more efficient than the LMS and NLMS filter.

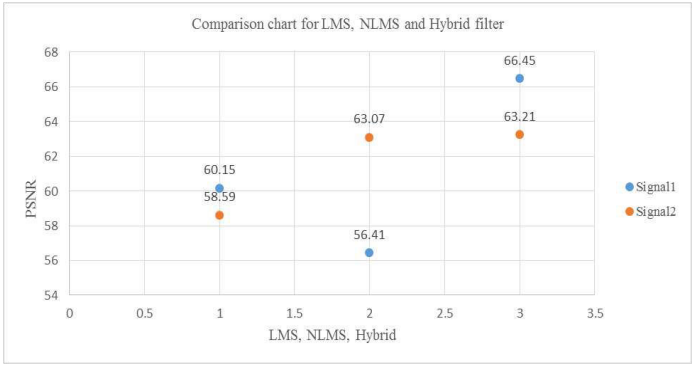

Fig. 7 Comparison chart for LMS, NLMS and Hybrid filter with PSNR value

VI. Conclusion and Future Scope

In clinical practice, the ECG signal is the most widely used for recording electrical signal from the heart. By

altering the shape of its constituent waves, namely the P, QRS, and T waves ECG conveys information regarding the electrical function of the heart. In this paper, the Hybrid algorithm is developed with LMS and Normalized LMS for providing more stable, step size, less compact and most reliable results are obtained for the input signal. In future work, the ECG signal can acquire from the ECG sensor and the acquired signal can be processed through the algorithm which is used for classifying the ECG signal into three different types: Paroxysmal, Persistent and Permanent. In Paroxysmal condition, the AF will occur sometimes and then stops. During persistent conditions, the meditations or a special type of electrical charge is required. In Permanent condition, the normal rhythm cannot occur. In future, the data received from the ECG sensor will be displayed and stored in the individual data path and the above data will be transmitted to remote user and processing server through the Internet of Things (IoT) platform which forms real-time function.

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Performance of motion estimation using content split block search algorithm for high efficiency video coding

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***Abstract*— High - Efficiency Video Coding: The newest video coding standard is introduced by ITU-T (International Telegraph Union) and joint collaborative team on video coding (JCT_VC). HEVC attain the requirement video storage and transmission with high resolution. Although it requires the high amount of computational complexity. Motion Vectors are determined with motion estimation analysis; it is implemented with different types of algorithm. In this paper, motion estimation process is implementing with the content split block search algorithm. It improves Peak Signal Noise Ratio (PSNR) than to the existing algorithms. The Objective evaluation has been performed with PSNR. The Subjective analysis also verified through mat lab software in the process of encoding and decoding.**

Keywords—high resolution, motion vectors, video storage and transmission

1. INTRODUCTION

A Meteoric Evolution of mobile technology with new exercise requires a large data of towering quality. Projecting of such data leads unrushed transmission and extortionate retention. Hence cognitive content of data needs a contraction in a number of bits using for image compression techniques [1]. People demand high quality of video entertainment services, even though a lot of bandwidth (BW) and resources are required to store the videos and transmit the video over the channel [2,3]. In the earlier years does not offer enough Compression ratio and also not suitable enough for the videos. The countable performance can be attained by H.264/AVC; it provides more compression that comparing with existing standards such as H.26X [1] [2]. The aim of the HEVC is improving the efficiency by reduction the bit-rate at least 50% that means its performance of the efficiency is improved [7]. The high efficiency video coding (HEVC) standard [3].HEVC was developed by Joint Collaborative Team on video coding established by the IUT-T video coding Experts Group [2,3]. Screen Content videos are used widely for lots of application such as remote pcs, video conferencing, remote education [4]. Orthogonal transform is nothing Rotated Orthogonal Transform (ROT) is performing better on Motion Compensation –residual than the Discrete Cosine Transform (DCT) for coding [5].Motion Estimation (ME) is a major coding grappling hook that consists of up to 64X64 prediction units[6].An Adaptive Coding Unit selection algorithm reported to each depth level's texture accommodative coding unit (CU) selection algorithm according to each depth level. Texture complexity is presented to filter out unessential coding block [7], CU depth decision process in HEVC has three levels of hierarchical decision problem. Another process is three dimensional video systems, imperfect depth images frequently bring on pestering temporal noise such as flickering, to the synthesized video[9] the residual signal is minimized, the signal is minimized, therefore coding efficiency is accumulates[10][21]. The Structural Similarity index (SSIM) has been attracting an increasing amount of attention recently in the video coding community as perceptual criterion for testing and optimizing video codecs[12,13]. It has been used in the rate distortion optimization of the HEVC standard[11].

Estimating the motion for the video is a major complexity it is approximately 70% above. Because motion or movement is presented in the video [10]. Video can be divided into the number of frames/slices [6]. Many conventional algorithms are existed such as Full search three stage logarithmic [9], UM Hexagon full search algorithms are good to estimation the motion vectors, although the optimization is necessary with different types of motion estimation algorithm[12]. Nowadays, mobile devices and personal computers are accommodated with multiple core processors. [11] To maximize the efficiency of the processor has to be made structural modifications in the application[2].The subjective and objective quality assesment is essential in fully validating the video codec performance, its highly desirable how the objective image are existing in the video quality assessment. More over a new application have to be developed with parallelization methods for improving the maximum efficiency of multi-core processors[23]. [8] The H.264 standard is doing motion estimation with block matching algorithm with macro blocks [14]. Video can be divided into contiguous frames[15] and it also having temporal redundancy, temporal redundancy is increasing the effectiveness of the inter-frame video compression with content of the macroblock by reference to the known content block [13]. And also HEVC employs the deblocking filter and the SAO in the encoding and decoding loops to improve the subjective quality as well as objective quality with help of in-looping and post-looping filters in algorithmic [24] and architectural levels to save the cost. And improve visual quality [15] The remaining sections has followed to be section II Literature Survey, section III. Proposed work contribution with content block search algorithm, Section IV follows Simulation Results with test sequences results, Section V Conclusion.

2. LITERATURE SURVEY:

Motion Estimation and compensation makes a significant role in video coding and decoding. Motion estimation is the method to finding the motion vectors (MV). It describing the transformation between sequential frames in the video sequence [13]. Motion Compensation it's one of the algorithmic technique to predict the frame in video from previous and future frame [14]. Motion estimation algorithm for frame rate up-conversion. Dual motion estimation algorithm enhances the estimation

accuracy of motion vectors by using the unidirectional and bidirectional matching ratios of blocks in the previous and current frames[1].There are two essential process in HEVC that is motion estimation and motion compensation, ME tools finds that best match block position in previous coded frames for every block in contemporary frame. Then motion compensation process uses the motion vectors to generate compensated frames[17]. ME Algorithms in video compression make performance with both motion estimation and motion compensation simultaneously[19]. From the below figure 01 motion vectors are represented in the frames with the reference and current frame.

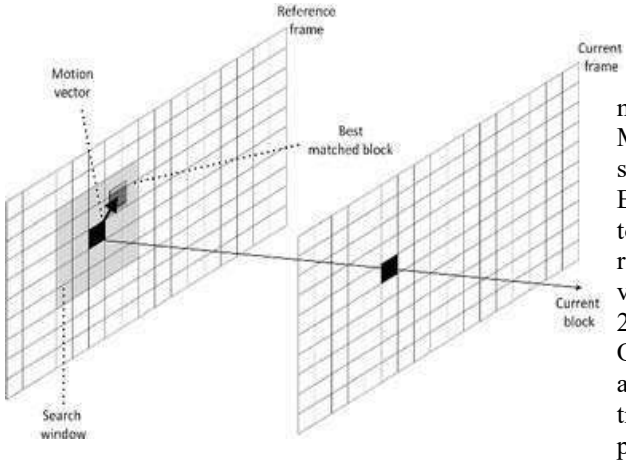

Figure 01: Representation of motion vectors (MV) in the frame

Motion estimation can be worked in the form of two ways one is inter prediction and intra prediction, the discussion is going on with the intra prediction, when the anticipation heavy in the situation the predicted samples have the correlation with reference samples are low [18]. the temporal redundancy exists between consecutive video frames. The temporal redundancy can be removed by temporal prediction using Motion Estimation and Motion Compensation [9,10]. In the proposed frame filter ban design, In proposed frame filter bank design, assume L0 (f) and L1 (f) are analysis low-pass and high-pass coefficients respectively and H0 (f) and H1 (f) are the synthesis low-pass and high-pass filters respectively and here represent frame. Transformed Filter mode bank representations are, Tf(z)= - Fm(z) { H0(z) L0(z) + H1(z) L1(z) } + Fm (-z) { H0(-z) L0(z) + H1(-z) L1(z) }(1)[20] Intra_4x4 and Intra_16x16 prediction. Chroma Intra prediction is the same in both cases. A third type of Intra coding, called I_PCM, is also provided for use in unusual situations[21] intra prediction mode in addition to the copying-based HEVC intra prediction scheme. The theoretical coding gain is used to compare the proposed scheme and the current HEVC intra prediction scheme[18] Intra prediction in HEVC makes use of 33 angular modes along with the DC and the Planar modes for each PU[22].where Tf(z) is the transformed filter mode. We have designed a filter bank for better accuracy as, (|L0(z)|A fast CU size decision algorithm with intra prediction for HEVC is determining intra mode decision and bypass the strategy for intra prediction on CU size is large. In this work computational complexity is reduced upto 67% and maintain almost the same RD performance as the original encoder of HEVC[3]. The CU depth decision is processed in HEVC as a third level of hierarchical problem[23]. Improved CU depth decision has to be allowed the performances of the CU depth decision can be transferred between the complexity and RD cost[8]. The compression capability of several generations has improved subjective quality as well as PSNR as a objective quality. Filter coefficients and offset are exaggerated for each frame, there are few blocks are selected to calculate the parameters [4]..

3. PROSED WORK CONTRIBUTION WITH CONTENT – SPLIT BLOCK SEARCH ALGORITHM

Proposed CBLS (Content Block Layer Search) method is able to implement standard encodings from MPEG-2 to H.265/HEVC. CBLS is mostly performed using single layer per frame through bit depth rate per frame using BL (block layer) and CL (content layer), bit depth module is to allow CBLS video coding at constant quantization and bit rate. A CBLS video coding is a process flow applied at each video frame level. This process flow is illustrated in Figure 2. Where steps based on pre-processing operations, Group Of Picture (GOP) construction with motion estimation, inter and intra prediction for encoding the coded frames and transform information including decoding frame for inter prediction. The process flow initiates at frame extraction to acquire the frame information to be encoded. Pre-processing involves the Group Of Picture (GOP) construction or motion estimation. Preceding inter and intra prediction is followed to encode the next coded frames which introduces latency between frame coding, can be reduced by coding decisions made by structuring the quad-tree transform and prediction coding information through Decoded Frame Buffer located at CL and BL. At the Coding Decisions, coding information carries reconstructed frame for inter prediction and reconstructs the frame as in the coding manner.

In this paper, the content block based motion estimation is work out on the pixels in the coding tree units. In order to restore the video, make a good approximation of the point spread function and hence the motion vector is required to improve the motion estimation using with content block search algorithm, many motion estimation algorithms are exist. In the proposed algorithm, the content in the each motion vector of P frame and B frames with greater magnitude, it denotes faster moving of the coding tree units. The method of the modifying video coding is derived from the Standard High - Efficiency Video Coding.

A) Considering P and B frame, get the motion vector values such as content values from the frame compression, whereas content motion vector (CMV) is the motion vector with the variation in the frame and is the number of coding tree units in the analyzed content varied frame. Calculate the magnitude of the motion vector of the content regarding the horizontal and vertical component in the CTU.
B) Find the content threshold value for the MV.

C) Considering outright the P frames and B frames in the GOP, we do the same calculation and achieve the number of eligible factors. The content in I frame to facilitate data extraction.
D) Content data in the CTU and calculate the phase value.
E) From the GOP, calculate start and end position of the segment with the content capacity.

The data extraction was accomplished on a GOP by GOP basis. For the GOP content information in I frame should be extracted accurately. In the case of the multiple encodings at different Signal to Noise Ration qualities with more or less quantization levels and based on these, the block structure is reused form the greater quality representation to speed up the encoding with the lower quality. By using the content analysis approach, the video frames are based on intra prediction mode of the HEVC. In this approach some of the blocks are skipped with content structure analysis. The proposed algorithm extracts one bit at each intra block 4X4, it should be qualified by modifying intra prediction mode.

In the one bit of the content information the sign bit of the bit stream is considered. It supports I and P slices and the other type of video coding is intra coding that is called Intra prediction Motion estimation (IPME). The encoder is selected typically in the prediction mode for each and every block that minimizes the difference between predicted block and the block to be encoded. The I mode is based on the predicting each block that can be that size is 4x4 separately and it is well suited for coding parts with the detailed significance. On the other hand 16x16 will block and more suited code for very smooth picture. It is convenient for implementation reasons to address such type of issues. An IPME block mode, in which the sample values sent directly without prediction, transformation and quantization. In IPME block mode, the additional motivation for block mode is supporting to all the regions of the pictures to be represented without any loss of fidelity.

Proposed work contribution is performed in the following steps:

1. Using MATLAB, get a block unit from the H.265 stream as shown in figure 3 and 4.
2. Analyze content of each block's header to determine if this is an IPME content block in IBBPBBI sequence.
3. In case of an IPME block:
a. extract the block payload in order to get the pixel values,
b. feature the content into new data into the low bits of the pixels,
c. compare the content block with sequence of blocks,
d. store the block back to the frame unit.
4. Go to step 1.

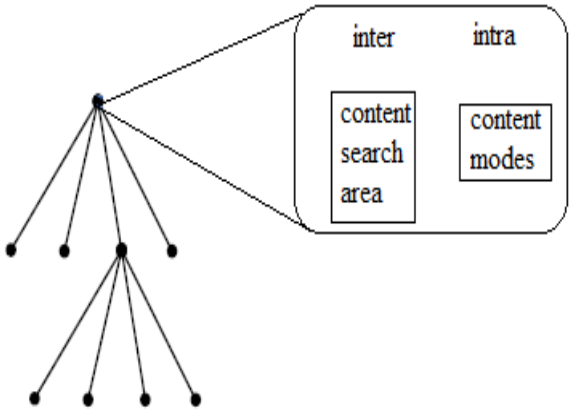

Figure 2: Block Mode: Schema of the CTU content search area to analyze each CU and content modes

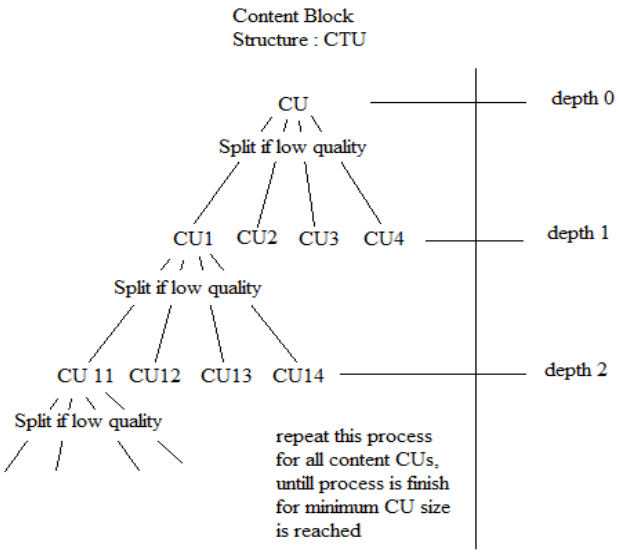

Figure 3: Block Mode: Proposed content CU process to derive the block structure from high content quality to low content quality

4. SIMULATION RESULTS WITH TEST SEQUENCES

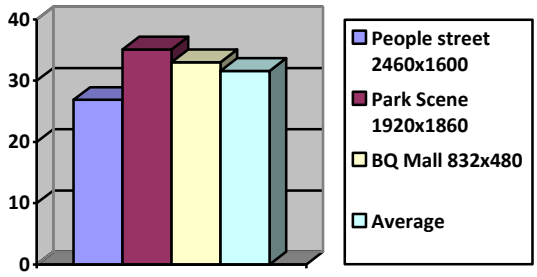

Figure 4: B. G. Choi et. all.

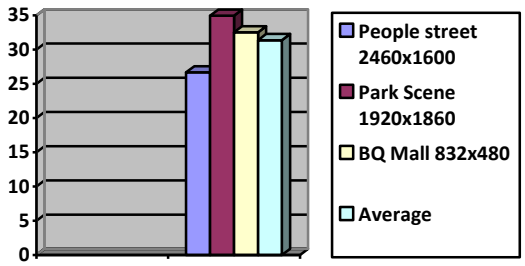

Figure. 4 D. G. Yoo et.all

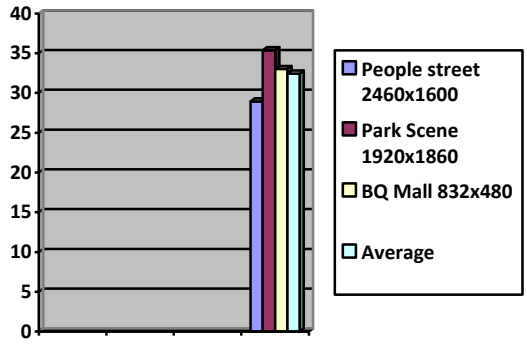

Figure. 5 S. Kang et. all

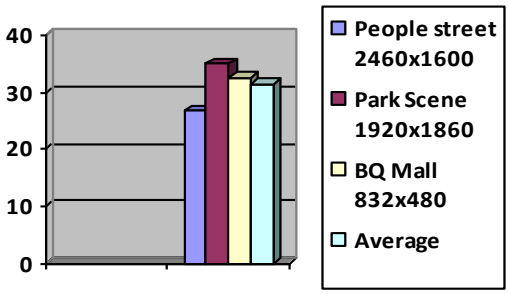

Figure.6 Songhun Yu et. all

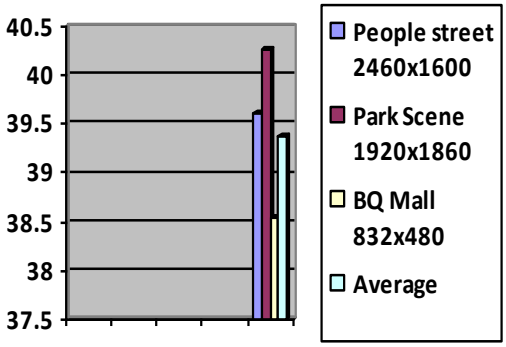

Figure. 7 Proposed work

The objective evaluation is performed in this section, for objective evaluation considering PSNR (peak signal to Noise Ratio) for this analysis HEVC standard test sequences were chosen for the test because these are high resolutions videos, block size is set to be 16X16.

Fig 8: Content processing Frame

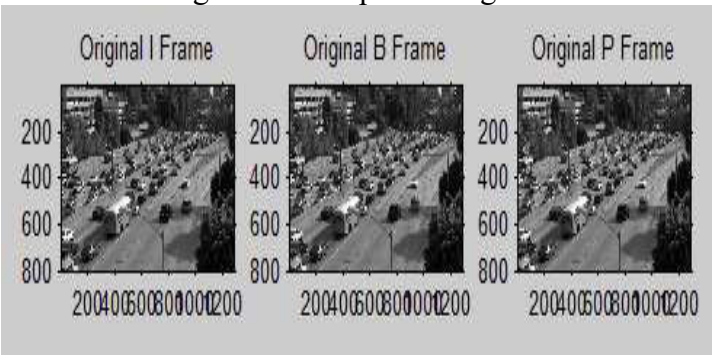

Fig 9: Frame: I frame, B frame and P frame.

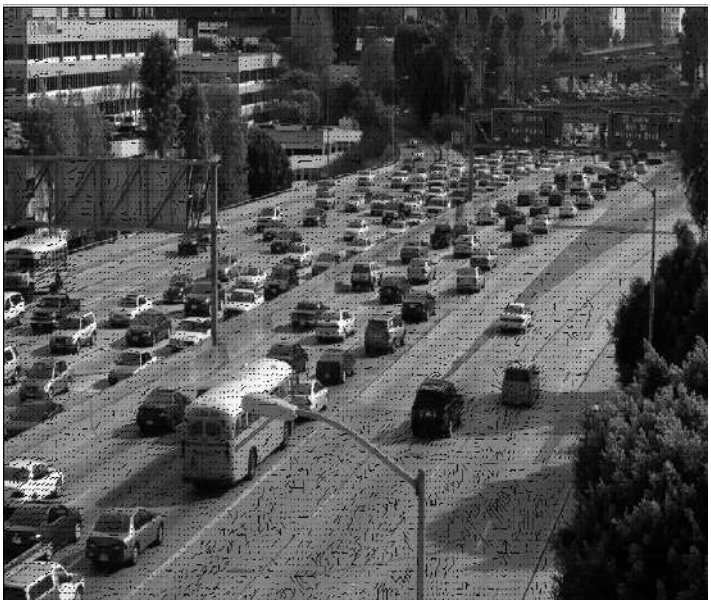

Fig 10: Encoding : Motion Vectors

Fig 11: Encoding : Stretched Motion Difference

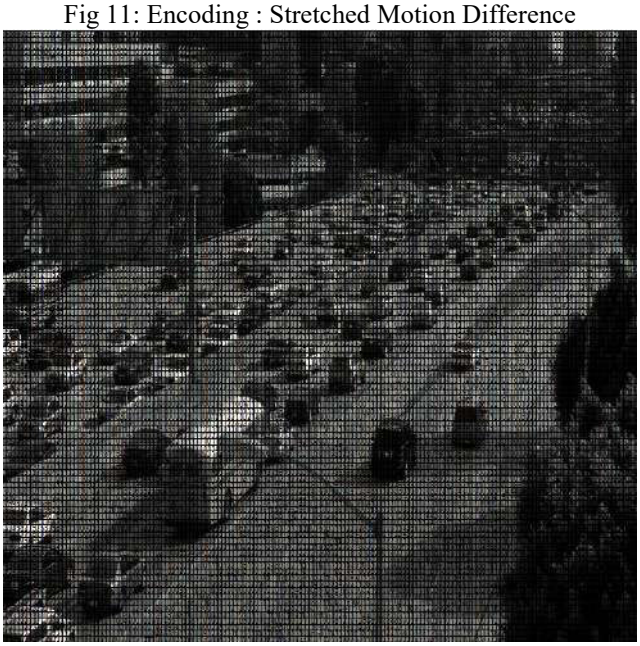

Fig 12: Encoding : Content block partition : Extraction

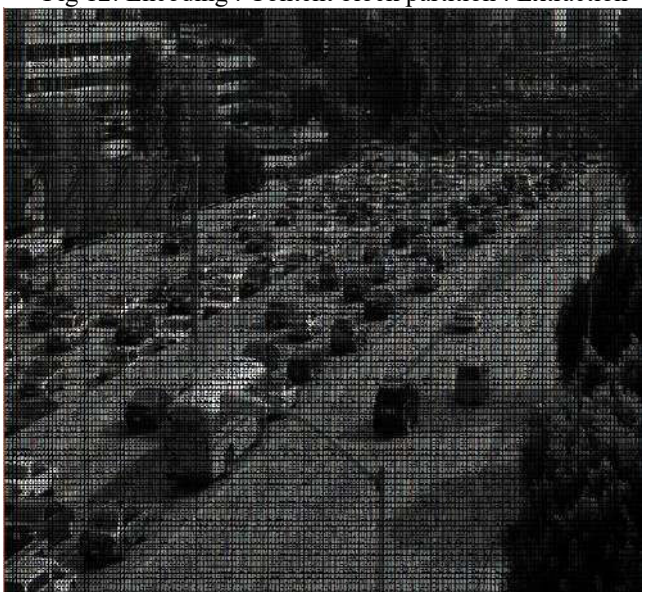

Fig 13: Encoding : Content block partition : Analysis

Fig 14: Encoded Frame

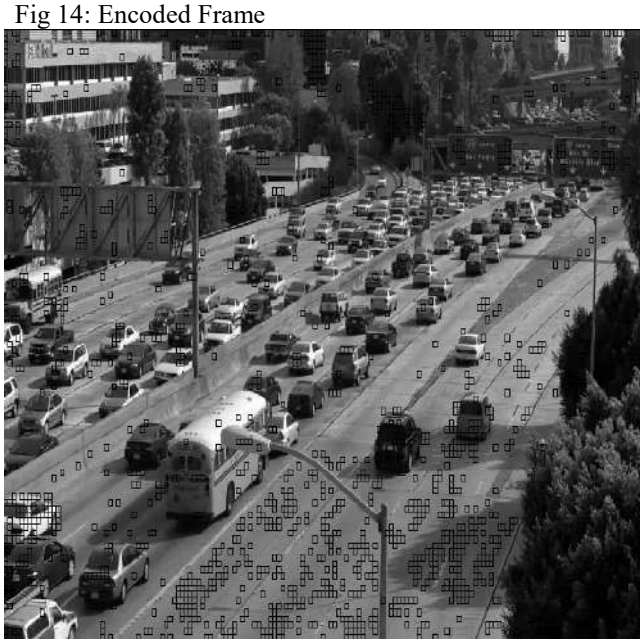

Fig 15: Decoding : Content Extraction

Fig 16: Decoding : Content Analysis

Fig 17: Frame Reconstruction

The encoding time difference (T) is measured as the difference of the total encoding time for 5 representations including the reference at different qualities (fixed QP 22, 27, 32, and 37). All encodings are performed on an Ubuntu 64-bit at 2.60 GHz and 8 GB RAM. 8 videos defined with resolutions from 416x240 to 2560x1600 pixels and frame rates between 24 fps and 30 fps are encoded. All sequences are encoded with the"random access, main" profile defined, a CTU size fixed to 64x64 pixels and a maximum CU depth of 4.

In the experiment, a video sequences selected for analysis are given in table 1 and 2.

	Proposed
Reference software	HM 16.4
QP	22, 27, 32, 37
Sequences	PeopleStreet Cactus BQTerrace BasketballPass
Resolution	(2460 x 1600), (1920 x 1080), (832 x 480), (416 x 240)
CPU	Intel core i7 X990 3.47GHz
OS	Windows 8 (64-bit)
Open MP version	2.0
Compiler	MSVC 2012

Table 1: Proposed work Sequences

In the table 2 is showing the different classification of the videos such as Class A, Class B, Class C and Class D with different breadth and width, and also to be considering the no of frames are used to the experiment with its bit depth and frame rating (frames per sec).

Class	Size (Width : Height)	Sequence	No. of Frames	Bit-Depth	Frame Rate (fps)
Class A	2560:1600	People Street	150	8	30
Class B	1920:1080	Party Scene	240	8	24
Class C	832:480	BQMall	600	8	60

Table 2: Different classes of video sequence with bit depth, No of frames and Bit Depth

Class	Sequence	QP	Rate	PSNR	SSIM
Class A	PeopleStreet (2460_1600)	37	0.75	39.32	0.76
	Traffic(2560_1600)	37	0.70	39.35	0.65
	BQterrace (2560_1600)	37	0.65	39.37	0.62
Class B	Kimono (1920_1080)	37	0.65	41.25	0.64
	ParkScene (1920_1080)	37	0.33	40.26	0.71
	Cactus (1920_1080)	37	0.33	40.35	0.75
Class C	BQMall (832_480)	37	0.47	38.54	0.70
	PartyScene (832_480)	37	0.16	41.26	0.61
	BasketballDrill(832_480)	37	0.16	40.65	0.60
Class D	BasketballPass (416_240)	37	0.52	39.12	0.67
	BlowingBubbles (416_240)	37	0.33	40.47	0.70
	RaceHorses (416_240)	37	0.45	42.68	0.71
Class A	PeopleStreet (2460_1600)	32	0.75	38.12	0.65
	Traffic(2560_1600)	32	0.70	38.15	0.54
	BQterrace (2560_1600)	32	0.65	38.18	0.51
Class B	Kimono (1920_1080)	32	0.65	40.20	0.53
	ParkScene (1920_1080)	32	0.33	39.21	0.60
	Cactus (1920_1080)	32	0.33	39.25	0.64
Class C	BQMall (832_480)	32	0.47	37.51	0.59
	PartyScene (832_480)	32	0.16	40.16	0.50
	BasketballDrill(832_480)	32	0.16	39.56	0.49
Class D	BasketballPass (416_240)	32	0.52	38.02	0.56
	BlowingBubbles (416_240)	32	0.33	39.37	0.59
	RaceHorses (416_240)	32	0.45	41.48	0.60
Class A	PeopleStreet (2560_1600)	27	0.75	38.10	0.54
	Traffic	27	0.70	38.15	0.43
	BQterrace (2560_1600)	27	0.65	38.27	0.40

Class B	Kimono (1920_1080)	27	0.65	40.15	0.42
	ParkScene (1920_1080)	27	0.33	39.14	0.51
	Cactus (1920_1080)	27	0.33	39.15	0.53
Class C	BQMall (832_480)	27	0.47	37.45	0.48
	PartyScene (832_480)	27	0.16	40.16	0.49
	BasketballDrill(832_480)	27	0.16	39.44	0.38
Class D	BasketballPass (416_240)	27	0.52	38.02	0.45
	BlowingBubbles (416_240)	27	0.33	39.17	0.48
	RaceHorses (416_240)	27	0.45	41.48	0.51
Class A	PeopleStreet (2460_1600)	22	0.75	37.00	0.40
	Traffic(2560_1600)	22	0.70	37.15	0.41
	BQterrace (2560_1600)	22	0.65	36.00	0.39
Class B	Kimono (1920_1080)	22	0.65	39.10	0.42
	ParkScene (1920_1080)	22	0.33	38.06	0.50
	Cactus (1920_1080)	22	0.33	38.05	0.43
Class C	BQMall (832_480)	22	0.47	36.04	0.47
	PartyScene	22	0.16	39.06	0.41
	BasketballDrill(832_480)	22	0.16	38.04	0.38
Class D	BasketballPass (416_240)	22	0.52	37.01	0.45
	BlowingBubbles (416_240)	22	0.33	38.06	0.47
	RaceHorses (416_240)	22	0.45	40.05	0.45

Table 3: Test Results with HM tool (QP, RATE, PSNR and SSIM)

5. CONCLUSION

In this wok, content - split block search motion algorithm is proposed, in this process multi - directional motion estimation was proposed to find the exact motion vectors with less Complexity regarding computations. Multi - rate distortion optimization process needs to traverse each content tree such as coding tree unit in order to find the block structures such as the coding unit, which is directing the best rate distortion performance. The proposed algorithm shows high PSNR in an objective evaluation comparing with existing algorithms as we discussed in the introduction.

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Implementation of Cellular Automata Divider Using a Quantum-Dot

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Abstarct– One of the most imperative numerical tasks isdivision. A proficient divider can be of incredible help with planning number-crunching circuits. The Quantum cell automata (QCA) is an empowering innovation, which is by all accounts a decent successor of existing advanced frameworks. Therefore, an effective QCA divider will encourage making QCA computational and number juggling frameworks. In this paper, a superior exhibitions QCA no-account divider is displayed. It has an extremely thick and a vigorous structure with fast and timing execution.

Keywords - Quantum-Dot Cellular Automata, Divider

I. INTRODUCTION

Despite the fact that the ordinary calculation innovation of semiconductor creation has been developing speedily in the most recent decades there are numerous applications which request less power and considerably more speed. There is an outstanding Catch 22 in CMOS innovation: so as to accelerate the plan more power is required and on the opposite side to lessen the power utilization speed decrease is fundamental. Subsequently, rather than utilizing standard CMOS arrangements, fashioners support to use more up to date advancements especially ones dependent on nanoelectronics, for example, carbon nanotube field impact transistors (CNFET) and quantum-speck cell automata (QCA). These new innovations give more combination and speed to much lower control prerequisites. Carbon nanotube field impact transistor (CNFET) [1] is fundamentally the same as CMOS innovation which makes them great option in contrast to many known applications. CNFET gives better thickness and lower control utilization, yet a quantum-speck cell automata is totally not quite the same as traditional CMOS innovation. It devours less power because of its determination which is covered up in a QCA cell structure.

Amid the most recent years numerous scientists have effectively manufactured and used the circuits dependent on

QCA cells [2, 3, 4]. Improvement of atomic QCA structures ready to work at the room temperature was the fundamental

research of numerous effective works [5, 6]. A portion of alternate works, for example, [7, 8] have essential

researched chances of structuring extremely proficient QCA circuits. In [8] effective plan for QCA multiplexer have

been displayed, where 2:1 QCA multiplexer was built utilizing the coplanar wire crossing plan. Planning effective QCA memory cells is one of the appealing fields in QCA. Line based and circle based structures for the most part are utilized to plan a QCA memory cell. A portion of alternate past looks into [7] have been centered around structuring hearty QCA circuits. In [7]

Some structure rules for developing a powerful greater part door and coplanar wire crossing plan against sneak clamor ways have been presented. Decrease of the quantity of QCA larger part doors and improvement of QCA circuits is another appealing field in QCA. Despite the fact that QDCA based number juggling capacity circuits have been recently executed, the extent that we know there is no distributed work on structuring QDCA based divider. The most inquired about number juggling circuit dependent on QDCA is including, which is truly sensible since it is notable that all other essential math capacities, for example, subtraction, augmentation and division can be depicted utilizing the expansion.

Adders are one of the key components in structuring number- crunching circuits like counters in this manner planning a strong, thick and basic full-snake is of incredible significance. To date, a few investigations have been done

on QCA snake structures [9]. The first QCA full-viper configuration was introduced in [10]. This structure is developed utilizing five three-input larger part entryways and three inverters.

Another critical numerical activities is division. A proficient divider can be of extraordinary help with planning number-crunching circuits. In this paper, a superior exhibitions QCA worthless divider is introduced. It has an extremely thick and a strong structure with fast and timing execution.

II. QUANTUM-DOT CELLULAR AUTOMATA

A.Introduction

QCA fundamentally works utilizing the communication of bi-stable

QCA cells formed from four quantum-spots. Fig. 1 speaks to an abnormal state design of two spellbound QCA cells. Every cell is contains four quantum spots orchestrated in a square shape. The cell is accused of two electrons, which are allowed to burrow between neighboring spots. At a given purpose of time, the places of electrons are most likely antipodal locales because of their proportional electrostatic repugnance. Hence, as appeared in Fig. 1, the two electrons in the QCA cell can take the one of two comparable vivaciously insignificant courses of action. The cell polarization P = +1 and P = - 1 represent these two plans. Advantageously, the cell polarization P = +1 can be utilized to speak to rationale "1" and P = - 1 to speak to rationale "0" which can consequently be utilized for double data encoding.

Numerous rationale capacities can be acknowledged by various adjusts of QCA cells. This is because of the Coulomb communications, which

impacts the polarization of neighboring cells. QCA models have been proposed with potential hindrances between the dabs that can be controlled and used to clock QCA circuits.

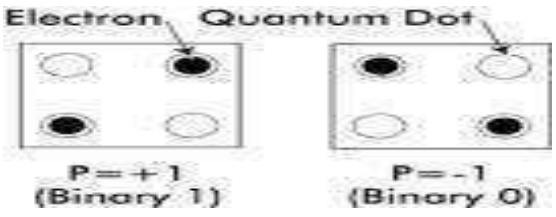


Figure 1.QCA cells

B. QCA Logical Devices

The QCA wire, majority gate and inverter are the most widely known and used QCA logic mechanisms.

QCA wire: In a QCA wire, the binary signal propagatesfrom input to output because of the Coulombic interactions betweencells. This is a result of the system attempting to settle to a ground state.Any cells along the wire that are antipolarized to the input would be at a higher energy level, and would soon settle to the correct ground state.

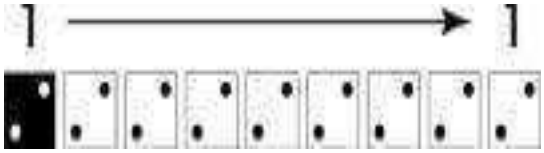


Figure 2. A QCA wire (90-degree)

The engendering in a 90-degree QCA wire is appeared in Fig.

2.Other than the 90-degree QCA wire, a 45-dgree QCA wire can likewise be utilized. For this situation, the spread of the twofold flag shifts back and forth between the two polarizations. Further, there exists an alleged non-straight QCA wire, in which cells with 90-degree introduction can be set beside each other, yet helter-skelter.Larger part entryway and inverter: The lion's share door and inverterare appeared in Fig. 3 and Fig. 4 separately. The dominant part entryway plays out a three-input rationale work. Accepting the data sources are A, B and C, the rationale capacity of the dominant part entryway is

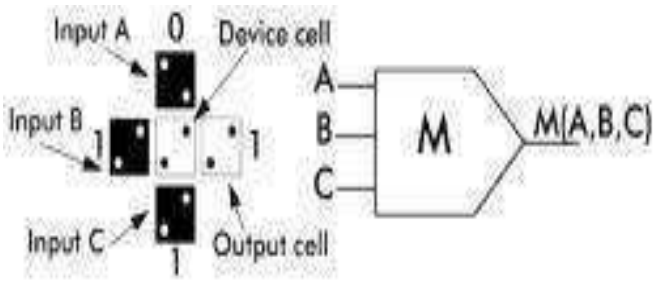
$$(, ,) = \cdot + \cdot +$$

By settling the polarization of one contribution as rationale "1" or "0", we can get an OR entryway and an AND door individually. Increasingly intricate rationale circuits would then be able to be developed from OR AND doors.

III. PROPOSED QCA DIVIDER

In this segment we initially portray the issue of division, next we propose our answer dependent on QCA. Since our undertaking is to isolate two numbers spoken to in the double frame, it appears to be sensible to initially examine the issue from a traditional twofold rationale point of view and its partner in genuine structure, rationale entryways. In

Common notation the division is presented as A/B = C, where A and B are inputs widely known as dividend and divisor and C, a quotient, is an output of operation.



A	b	C	d	R1	R0	Decimal
0	0	0	0	NN	NN	divByZ
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	NN	NN	divByZ
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	NN	NN	divByZ
1	0	0	1	1	0	2
1	0	1	0	0	1	1
1	0	1	1	0	0	0
1	1	0	0	NN	NN	divByZ
1	1	0	1	1	1	3
1	1	1	0	0	1	1
1	1	1	1	0	1	1

Figure 3. A QCA majority gate

A quotient is usually represented by an integer part of the result of dividing two integers. There can be a reminder also, which represents a remaining of a division, in this particular task we are omitting it, since we are just interested in binary division of two two-bite long binary numbers without remaining.Binary division is similar to its decimal counterpart. In order to see whole picture of possible results of binary

Figure 4. Truth table for division

Division by zero: In ordinary (real number) arithmetic, thisexpression has no meaning. So it's decided to apply same reasoning here. It can be seen from truth table that division by zero is defined as NN (not number). In actual binary gate design

circuitdivByZero is commonly presented by divByZero flag (bit).Using the Boolean logic one can express R0 and R1 as:

$$0 = \quad + \quad + \quad + \quad + \prime\prime$$

$$1 = \quad \prime + \quad \prime$$

Since the resulting Boolean functions seem suitable for simplification via Karnaugh maps, after doing so we obtain next simplified functions

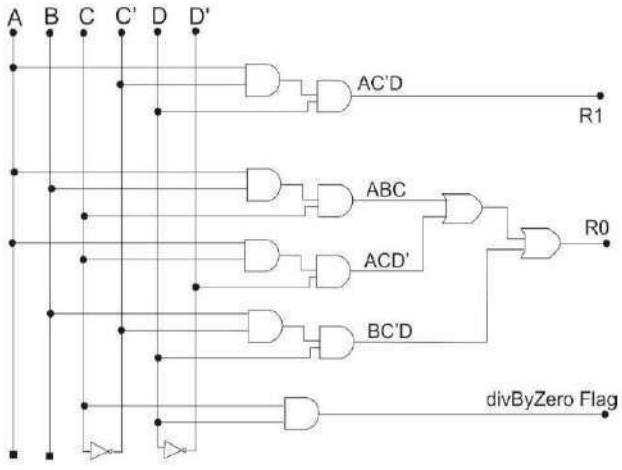


Figure 5. Binary logic circuit for 2 bit binary divider

Twofold rationale circuit for 2 bit paired divider with divByZero signal for division by zero blunder is appeared on Fig. 5. It has been tried in rationale entryways test system and since it worked accurately as indicated by truth table, the following stage was to structure indistinguishable circuit in QCADesigner [11].

As it tends to be seen from Fig. 5 and 6 recently given combinatorial rationale circuit is simply overhauled in QCADesigner by supplanting rationale entryways with their partners in QCA. Some expansion and explicit issues normal for QCA are settled, however about this will be given in end. A few properties of acknowledged QCD divider are:

x 4 inputs ABCD o where AB are first number composed in transport named "divident"

o and CD are bits of second number joined in transport "divisor"

x3 fundamental yields

o R0R1 are bits of yield number or

Remainder.

o divByZero bit xthere are 397 QCDA cells utilized in structure x add up to time postponement of a circuit is 4 tickers

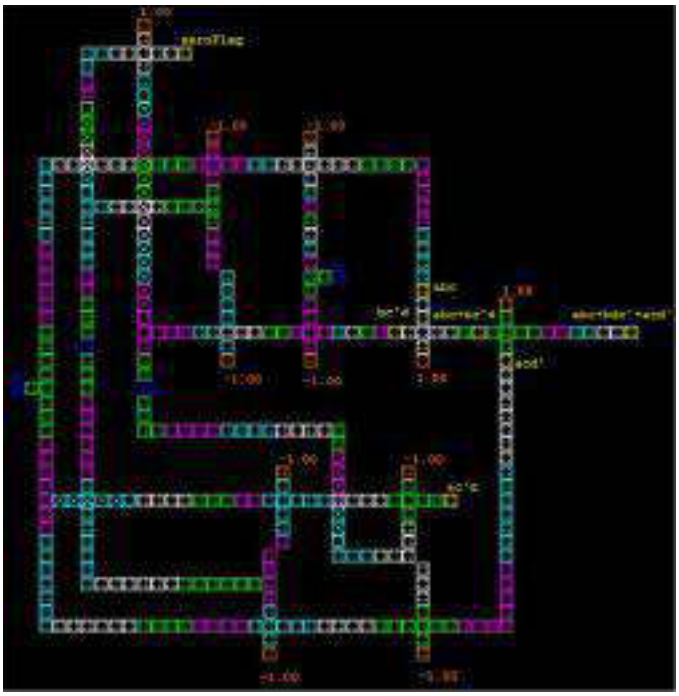


Figure 6. QCA based 2 bit binary divider

IV. EXPERIMENTS AND SIMULATION RESULTS

The proposed QCA adders are structured and mimicked by utilizing the QCADesigner instrument for the good for nothing case. QCADesigner is a QCA format and reenactment instrument created at the University of Calgary. The plan and reenactment technique is as per the following. In the first place, we produce the format of the proposed worthless divider.

Next, we setup the circuit timing. At long last, we setup the vector table recreation to mimic the divider. As it very well may be seen from recreation results (Fig. 7) QCDA circuit works legitimately. One should peruse reenactment results from blue line forward, which implies with 4 clock delay.

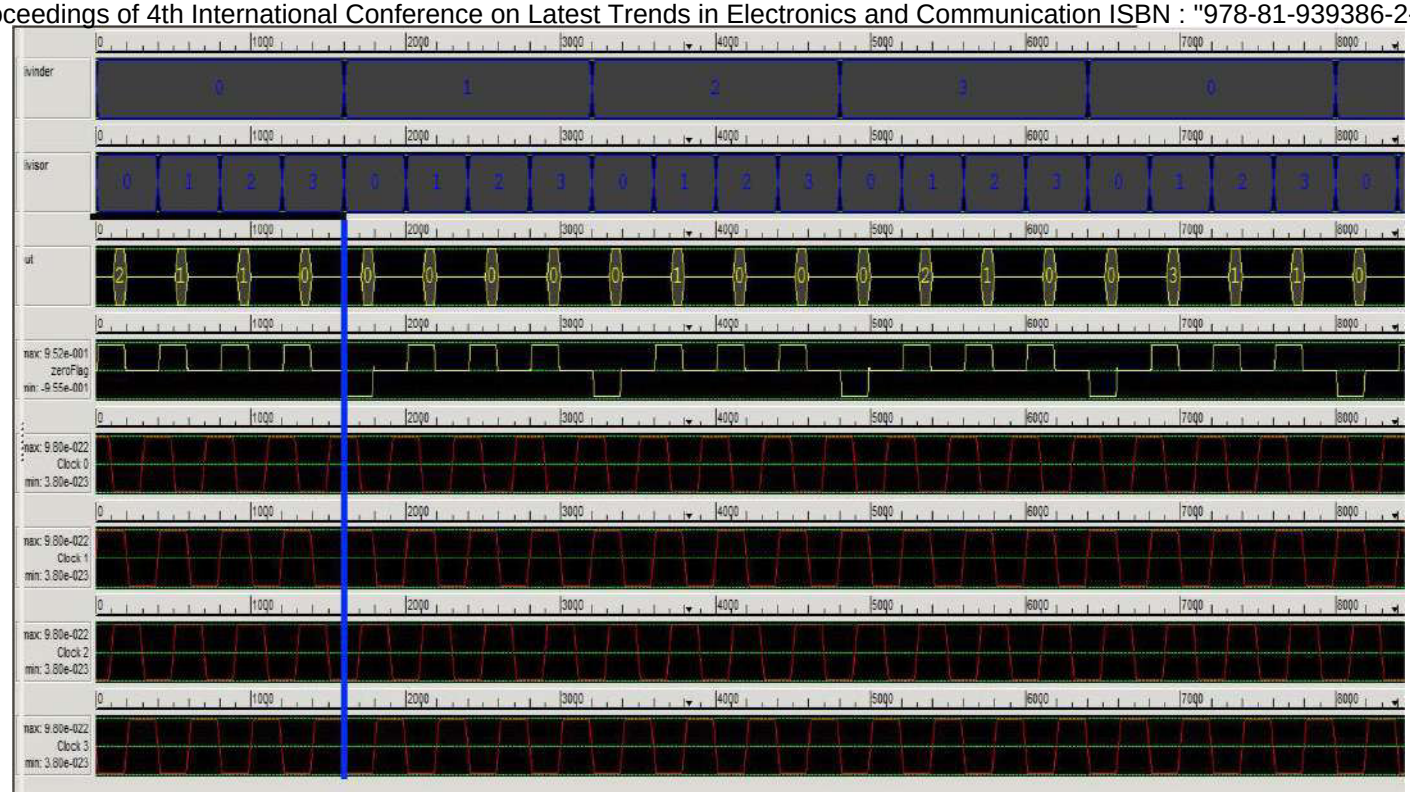


Figure 7. Simulation results of QCDA divider.

V. CONCLUSION

The primary commitment of this work is a check of twofold division circuit acknowledgment by means of QCDA. The structure of a QCDA circuit has been done in a combinatorial rationale way. The fundamental trouble looked in the structure procedure was keeping up the ideal number of cells in an isolated timekeepers which is insignificant prerequisite for keeping yields on a similar clock. There are some great practices one should take in thought when working with QCADesigner: (1) when cells with static polarization are utilized there ought to be utilized additional cell between settled cells and sensible doors; (2) contributions to a similar rationale entryways ought to be on a similar clock; (3) the parity in quantities of cells on various timekeepers on an equivalent QCA transport ought to be kept up as near as possible; (4) as an easier solution to the wire crossing problem, the multi-layered design should be used; (5) in the multi-layered design preventing inter cellular influence can be gained by using at least three layers; (6) simulation results have to been read carefully, bearing in mind clock delays.

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IMPLEMENTATION OF RUN-TIME RECONFIGURABLE CONSTANT MULTIPLIERS FOR FPGAS

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Abstract—**This work introduces a new heuristic to generate pipelined run-time reconfigurable constant multipliers for FPGAs. It produces results close to the optimum. It is based on an optimal algorithm which fuses already optimized pipelined constant multipliers generated by an existing heuristic called RPAG. Switching between different single or multiple constant outputs is realized by the insertion of multiplexers. The heuristic searches for a solution that results in minimal multiplexer overhead. Using the proposed heuristic reduces the run-time of the fusion process, which raises the usability and application domain of the proposed method of run-time reconfiguration. An extensive evaluation of the proposed method confirmes a 9-26% FPGA resource reduction on average compared to previous work. For reconfigurable multiple constant multiplication, resource savings of up to 75% can be shown compared to a standard generic LUT multiplier. Two low level optimizations are presented, which further reduce resource consumption and are included into an automatic VHDL code generation based on the FloPoCo library.**

Keywords: Constant multiplier, runtime reconfiguration, FPGA

I. INTRODUCTION

The multiplication with constant coefficients is an essential operation in digital signal processing. Initially one of the reasons to put embedded multipliers or DSP blocks into the fabric of field-programmable gate arrays (FPGAs) was to reduce the performance gap between application specific integrated circuits (ASICs) and FPGAs. Nevertheless, the price to pay for those fixed coarse-grained blocks is their inflexibility in word size and limited quantity. Limited quantity is particularly critical in industrial applications, when cheaper and rather small FPGAs with only few DSP blocks have to be chosen due to price pressure. Thus, logic-based constant multiplication methods are needed. Optimizing the implementation of this operation is well studied. Switching between a given set of constants of such multipliers during run-time instead of using larger generic multipliers is important to realize hardware efficient run-time adaptable filters [1], [2], [3], DCT and FFT implementations [4] as well as multi-stage filters for decimation or interpolation like polyphase FIR filters [5]. A reconfigurable constant multiplier is a multiplication circuit in which the scaling constant can be chosen from a limited predefined set of constants during run-time. For the given application domains two to six of such adjustable coefficient sets are common. The switching during run-time is achieved by inserting multiplexers into several constant multiplication circuits, to achieve a reuse of redundant partial circuits and thus a reduction of required resources. The problem is to find the best possible solution when inserting the fusing multiplexers. In order to avoid large routing delays pipelining

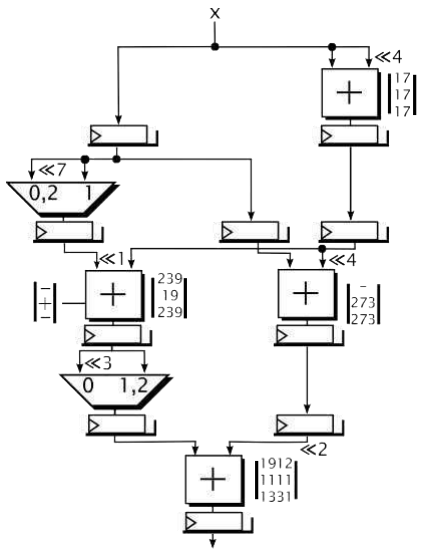

Fig. 1: Reconfigurable single constant multiplier which can be switched between the constants 1912, 1111, 1331.

is used for high speed applications. In contrast to ASICs, this is specifically advisable for FPGA designs [6], due to their inherent performance disadvantage. An example for such a pipelined reconfigurable constant multiplier which can be switched between the constants 1912, 1111, 1331 can be found in Fig. 1. Pipeline registers are inserted after each stage which includes registers in the multiplexer stages. The wires can be associated with a left shift and a sign. The value vector noted besides each operation corresponds to the intermediate or output factors for a specific multiplexer configuration. A switchable adder/subtractor is depicted as an adder with an additional sign vector input.

A common way to realize multiplier-less single and multiple constant multiplication for fixed constants is using additions, subtractions and bit shifts. In general, finding an optimal solution for single constant multiplication (SCM) proved to be NP-complete as shown by Cappello and Steiglitz [7], so optimal solutions can only be found for limited constant bit widths. Optimal SCM solutions for constants of up to 12 bit [8] were first extended to constants of up to 19 bit [9] and further extended for constants of up to 32 bit [10]. Moreover, there are good SCM heuristics called RAG-n, BHM [11] and H_{cub} [12] whose source code as well as an online SCM generator are provided on the SPIRAL project webpage [13]. When FPGAs are the target technology, solutions which consider pipelining during optimization have to be preferred to avoid large routing

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delays [6]. The problem of finding solutions for pipelined adder graphs (PAGs) for SCM as well as for multiple constant multiplication (MCM), which can directly take advantage of the registers provided in an FPGA's basic logic element, is solved by a heuristic called RPAG [14]. This heuristic was shown to outperform state-of-the-art MCM methods like H_{cub} [12] when these are optimally pipelined [15] and is thus be used as base for the reconfigurable constant multiplication shown in this work. The source code of this heuristic is also available online [16].

Finding the run-time reconfiguration of SCM and MCM adder graphs is a generalization of the basic SCM/MCM problem and thus also NP-complete. However, solutions were presented which are able to find reconfigurable SCMs (RSCM). First of all there are different solutions targeting ASICs, all focusing on multiplexer-based reconfiguration. In the method of Tummeltshammer et al. [17] several optimized SCM graphs are fused by a recursive algorithm called DAG fusion. Two SCM graphs are fused with minimal hardware effort by inserting multiplexers to switch between the different constants. Further coefficients can be included by recursively adding the related SCMs to the existing RSCM. Similarities between different coefficients in the canonical signed digit (CSD) representation of constants are exploited by Chen et al. [18] to realize RSCMs. Identical patterns in the CSD representation of constants are searched and fused using multiplexers to be able to switch between the different shifts and interconnections to realize a specific constant. Faust et al. [5] use an adder graph based approach with special focus on minimal logic depth. In addition to the methods described earlier, their algorithm does not only provide solutions for RSCM but also for reconfigurable multiple constant multiplication (RMCM). Such RMCM are also provided by ORPHEUS [2] which is able to fuse MCM solutions provided by H_{cub} [12] with a heuristic. Alterative concepts to realize RMCMs are evaluated during the algorithm run-time and the best overall solution is selected. The presented algorithms for RSCM and RMCM, respectively, do not consider pipelining or other FPGA specific issues as their focus is on ASIC implementations.

There is an FPGA-specific algorithm called ReMB method [1] which was further analyzed and extended in [19] by our group. An RSCM is constructed from basic structures that fit into the basic logic elements (BLE) of FPGAs. This procedure is limited to small problem sizes due to a very high memory consumption [19] and does not consider pipelining. As pipelined solutions are required for high speed applications on FPGAs, there is an optimal adder graph based algorithm for RSCM and RMCM with focus on pipelined realizations proposed by our group [20]. The idea of DAG fusion [17] is picked up as already optimized pipelined adder graphs (PAGs) are fused. Instead of fusing only two PAGs in one optimization run, all PAGs of the required constants are considered in one single optimization run to produce a better, multiplexer-aware pipelined realization. However, the optimal approach can only be used for small problems because of the complexity of a full search over all possible fusing solutions. Hence, a good heuristic method is required which provides solutions close to the optimum. This heuristic is presented and analyzed in the following Section II. Moreover, the proposed heuristic supports the use of PAGs consisting of ternary adders [21], [22], [23], which turns out to further improve the results. In Section III, some low level optimizations are provided to exploit the FPGA resources in the best possible way. The results and a comparison with previous work and with the use of generic multipliers are presented in Section IV. A conclusion is given in Section V.

II. The PAG Fusion Algorithm

A. Pipelined Adder Graphs

The input to the algorithm are pipelined adder graphs (PAGs) generated with the reduced pipelined adder graph (RPAG) heuristic [14]. In general, the presented fusion is not limited to RPAG generated circuits as pipelined MCM input. However, RPAG was chosen as it proved to outperform state-of-the-art MCM methods like H_{cub} [12] when these are optimally pipelined [15]. The results of RPAG are adder graphs representing multiplier-less pipelined constant multipliers using additions, subtractions and bit-shifts only. The main idea of multiplier-less multiplication as applied in RPAG is to compose a constant multiplication of an addition of shifted inputs. This is beneficial because a constant shift is only a wire in hardware. All constants can be formally represented as A-operation [12], which is defined as

$$A_q(u, v) = |2^{l_1} u + (-1)^{sg} 2^{l_2} v| 2^{-r} \quad (1)$$

with $q = (l_1, l_2, r, sg)$, where u and v are the input constants, l_1, l_2 and r are shift factors and the sign bit $sg \in \{0, 1\}$ denotes whether an addition or subtraction is performed. A multiplication by 17 could for example be realized as an addition of the input with the input left-shifted by 4 (multiplication by 16). This can be seen in the leftmost example in Fig. 2. In the following subtractor, 17 times the input is subtracted from 256 times the input, which corresponds to a constant multiplication by 239. Finally, this intermediate result is left-shifted by three to get the final result of 1912 times the input. If the constant to multiply with is known in advance, this kind of realization is much cheaper in terms of resources than implementing a generic multiplier [15]. In order to automatically generate such constant multipliers, RPAG is backward-exploring reachable intermediate constants, called predecessors by evaluating the A-operation. This leads to a step-wise constant composition, starting with the required output constants. The goal of the heuristic is to select predecessors which result in the lowest number of intermediate constants in the preceding stage and which reduce the adder depth. Two more examples for such a circuit of a pipelined SCM realization can be found in Fig. 2, which are used as running example. The stage s denotes the pipeline depth of each realized constant.

B. Improved Pipelined Adder Graph Fusion

Just like RPAG, the proposed pipelined adder graph fusion is backward-exploring. Starting with the constant mapping of the output stage all PAGs are fused stage by stage. The basic idea is to combine those intermediate values in the respective preceding stage to share the same adder, which leads

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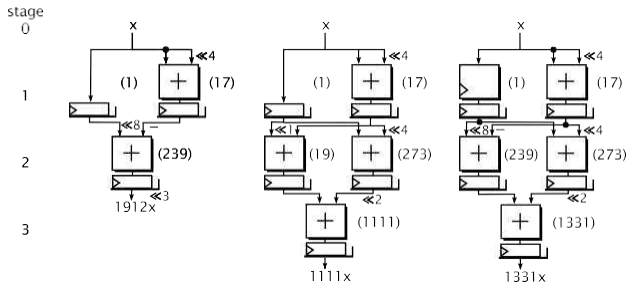


Fig. 2: RPAG solutions for the constants 1912, 1111, 1331.

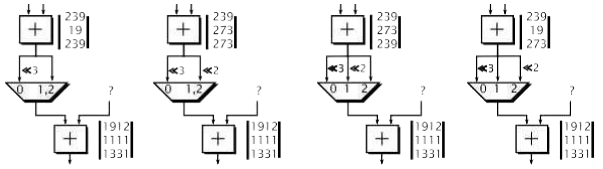
to a minimal overhead of possibly necessary multiplexers or switchable adder/subtractors. To do so, all combinations of intermediate values are evaluated and their costs are calculated separately and stored in a cost matrix. Multiplexers can appear at the inputs of the successive stage in the following cases:

1) input has a different shift value
2) input has a different source
3) both of 1) and 2)

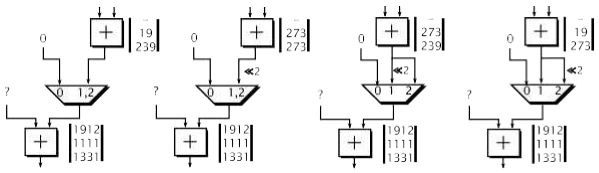
As described before, the target is to select the overall best mapping M for the specific stage s. This selection will be the source for the determination of the next preceding stage $s-1$. The procedure is repeated until the input (stage 0) is reached. A simplified pseudo-code of the generalized fusion process is given in Listing 1. It assumes that the overall best solution and costs are globally known. It is started with the constant mapping M of the output stage, the preceding stage s, the search width w (unlimited for the optimal search) and the costs of the current path *current_cost*, which is zero in the beginning. Compared to the algorithm presented in [20] the algorithm was generalized, such that it can be used both as heuristic and in an optimal way. In contrast to an arbitrary search through the whole search space, which was done in the former version, the search is now improved and based on a sorted cost matrix. More details on the search width are provided in Section II-D.

Listing 1: Simplified overview of the main recursion of the improved fusion algorithm with desired output mapping M of current stage, preceding stage s, the search width w and cost of the current path *current_cost*.

```
1  Fuse (M,s,w,current_cost)
2  if s > 0
3    C = evaluate_fusion_cost(M);
4    C = sort(C);
5    if current_cost+min(C)>=current_best_cost
6      return; -- subtree cut
7    else
8      for i = 0...w
9        if current_cost+cost(C(i))>=current_best_cost
10         return; -- normal b&b cut
11       else
12         M = mapping(C(i));
13         current_cost += cost(C(i));
14         Fuse (M,s-1,w,current_cost);
15       end if;
16     end for;
17   end if;
18 else
19   if current_cost < current_best_cost
20     current_best_cost = current_cost;
21     best_solution = current_solution;
22   end if
23 end if;
```



(a) Possible mappings for first preceding adder.



(b) Possible mappings for second preceding adder.

Fig. 3: All combinations of the adders in the second last stage for the given output mapping and the given RPAG SCM solutions in Fig. 2.

In the running example used here, the three SCM graphs generated with RPAG (see Fig. 2) are fused starting with the desired output mapping $M = \{1912; 1111; 1331\}$, meaning that the resulting circuit can be switched between these three values. This will be called an SCM circuit with three *configurations* in the following.

The enumeration of all adder combinations of the second last stage consisting of $\{239\}$ for the first, $\{19\}$, $\{273\}$ for the second and $\{239\}\{273\}$ for the third SCM solution, respectively, is given in Fig. 3. For the constant 1912 only one adder is required in stage two, but two adders are required in the other SCM circuits. This fact is considered by the insertion of a don't care "–". Due to a separate cost calculation for a specific combination, some of the multiplexer inputs are unknown from a local point of view. These are marked with a question mark. They do not have any contribution to the currently considered adders' multiplexer costs, which is a main advantage of the proposed method as the costs for each combination can be calculated and evaluated separately.

The cost evaluation is following the assumption that the multiplexers will be realized as a cascade of 2:1 multiplexers. Thus, $N-1$ 2:1 multiplexers are required to switch between N configurations, which leads to a contribution of each used multiplexer input of:

$$\text{cost}_{\text{MUX}} = \frac{N-1}{N} \tag{2}$$

As a zero input can be realized by resetting the succeeding register, these inputs are not considered as multiplexer inputs, as our implementation targets pipelined implementations. The multiplexer cost for each mapping is stored in a multidimensional cost matrix C (line 3 in Listing 1). The cost matrix for the combinations of the current stage can be found in TABLE I in a two dimensional representation. For example, the first entry in the first row (1.33) corresponds to the leftmost mapping in Fig. 3 (a) in which two multiplexer inputs, each with a cost_{MUX} of $\frac{2}{3}$ are used.

To get a valid solution a selection of one mapping for the first preceding adder in Fig. 3 (a) will directly force the

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TABLE I: Cost matrix for stage 2 fusion of the given example.

	19, 239	273, 273	273, 239	19, 273
239	**1.33**	1.33	2	2
–	0.67	**0.67**	1.33	1.33

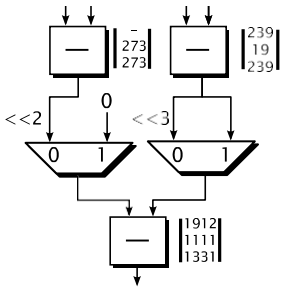

Fig. 4: Result of combining 239,19,239 and –,273,273 as preceding adders.

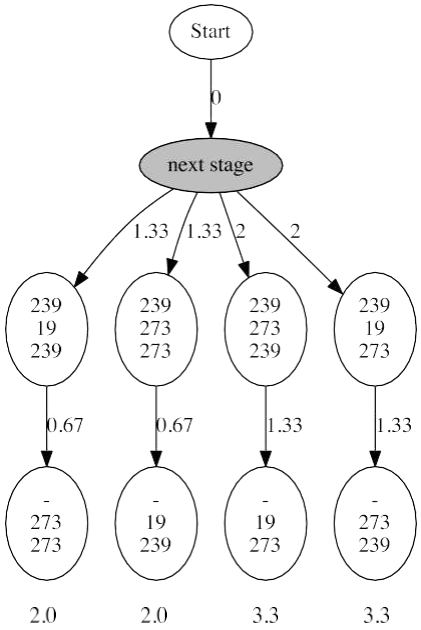

Fig. 5: Part of the decision tree for the second stage fusion.

selection of the corresponding mapping for the second adder (Fig. 3 (b)) or reduces the selectable possibilities for other adders in a more general case. This means each valid mapping solution for a specific stage consists of selections with a unique row and column index. Thus, finding the cheapest mapping solution M for a specific stage reduces to finding the valid solution with the lowest sum of costs. An example for such a selection is given in Fig. 4. It corresponds to the highlighted selection in TABLE I with a total cost contribution of $1.33 + 0.67 = 2$ 2:1 multiplexers.

The cheapest solution for a specific stage is not necessarily the best overall choice as it affects the costs in the preceding stages. So, to find the optimal solution, a full search over all possibilities is necessary. The search space can be illustrated as a decision tree, which consists of the decision itself as node and the cost of the decision as edge. An example for this can be found in Fig. 5, which shows a decision tree representation for the second stage fusion decisions of TABLE I.

Each branch of the tree is a valid mapping solution for the specific stage which can be chosen as output mapping for the preceding stage (line 12 in Listing 1). Each branch corresponds to a recursive call of *Fuse()* in line 14 of Listing 1. Thus, to get the full search space, a different decision tree for the preceding stage has to be added recursively for each stage's output mapping until the input stage is reached. As the cost matrix C is sorted in line 4 of Listing 1 the algorithm follows the best cost solutions first. In the case of equal cost solutions, the first solution found with these costs, is chosen as the cheapest one. The full decision tree for our example can be found in Fig. 6 and can be generated by setting w to ∞.

As shown in the complexity analysis in the next section, the full search for the optimal solution can be very time consuming for larger problems as the number of combinations grows factorial with the number of adders K_s in one stage and exponential with the number of configurations N. Nevertheless, the memory consumption is moderate as for the presented algorithm, as only the local environment has to be stored, which is the currently optimized branch. Moreover, irrelevant branches, which are too expensive anyway, can be pruned whenever the currently best cost value is exceeded. This is why the search is started with the locally best solution, which already finds good solutions in the first iterations. It is executed in a branch-and-bound way, which stops searching a branch if the total costs exceed the current global minimum costs. Besides the normal branch-and-bound method (cf. Listing 1, line 9-10), denoted as *cut* in the decision tree in Fig. 7, an additional pruning criterion is added (cf. Listing 1, line 5-6). The sum of minimum values of each row in the cost table is a lower bound of costs which can be added by the considered stage. If this minimum added to the current costs is larger than the global minimum, the whole subtree can be pruned, denoted as *stcut*. The best resulting reconfigurable single constant multiplier solution of the running example is shown in Fig. 1. It corresponds to the leftmost branch in the decision tree of Fig. 6 and Fig. 7.

C. Complexity Consideration: Analysis of the Search Space

As the presented optimal PAG Fusion algorithm has to traverse the full search space, its complexity, i.e., the number of possible solutions and branches to find them, is an important issue.

1) Number of Solutions: One key measure is the number of possible solutions to combine the adders in one stage. N denotes the number of configurations while the number of adders in the considered stage s of the input adder trees is K_s. The total number of adder combinations which are possible is $(K_s!)^N$. As the arrangement of the combinations itself does not matter, it can be ignored during the enumeration of solutions. As there are $K_s!$ ways to arrange the combinations,

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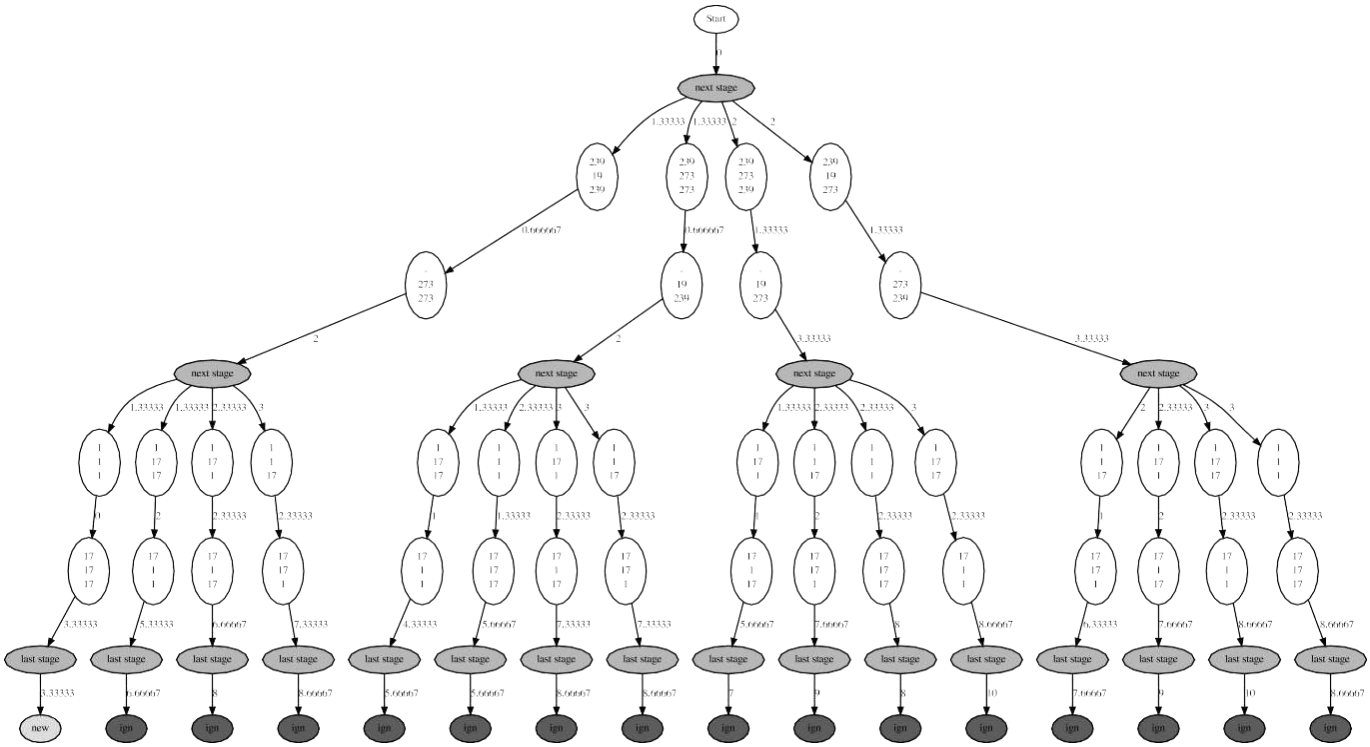

Fig. 6: Full decision tree for the example with costs for each decision, best total costs (light gray) and worse total costs (dark gray).

the total number of solutions L_s for a specific stage's s subtree is

$$L_s = \frac{(K_s!)^N}{K_s!} = (K_s!)^{N-1} \tag{3}$$

In the example decision tree of Fig. 6, $L_1 = L_2 = 2^{(3-1)} = 4$, which corresponds to the gray nodes in each subtree, as we have two nodes to fuse and three configurations in each stage.

2) Number of Decisions: In order to evaluate the run-time of the algorithm the number of decisions D, which is equal to the number of nodes in the decision tree, is important. This number depends on the possible solutions M_s for the subtrees and the possibilities to reach them. For one stage's s subtree the number of decisions is calculated as

$$D_s = L_s \left(\sum_{j=0}^{K-1} \frac{1}{j!} \right) \left(\sum_{j=0}^{N-1} \frac{1}{j!} \right) \tag{4}$$

$$\leq e \text{ (Euler Number)}$$

In the example decision tree of Fig. 6, $D_1 = D_2 = 4(1^{(3-1)} + 1^{(3-1)}) = 8$, which corresponds to the white nodes for each subtree. Note that, although the sum consists of a factorial and an exponential part, it has an upper limit of e (Euler Number).

For the whole decision tree the total number of decisions is the sum of decisions in each stage. This is the number of subtrees (solutions of the preceding stages) multiplied by the number of subtree decisions:

$$D = \sum_{i=1}^{S} D_i \prod_{j=1}^{i} L_j \tag{5}$$

This means for our running example that though we have only 16 possible solutions, 40 (= 8·1+8·4·1) decisions are required to build them.

The equation for the total number of decisions (5) shows that the search space to find the optimal solution grows at least factorial with the number of adders per stage K and exponential with the number of configurations N, as it contains a product term of the L_s (cf. (3)). For larger benchmarks this is not applicable, not even when branch-and-bound is applied. Therefore a heuristic is needed, to reduce the considered search space.

D. PAG Fusion for Larger Problems

The presented PAG fusion approach is able to find valid solutions for pipelined RSCM and RMCM adder graphs. Finding the optimal solution can not be guaranteed for large problems, which can lead to drastic time consumption. Thus, a heuristic to find a close-to-optimal solution with controllable time consumption is required. Finding a good heuristic is not trivial, as it is not clear which strategy is appropriate for the present search space. An analysis of the search space of PAG fusion showed, that selecting branches with low costs in the local decision phase, raises the likelihood to find optimal or close-to-optimal solutions. Thus, the heuristic presented here works by limiting the number of branches to the ones which are most likely to be included in the optimal solution. These are the cheapest solutions in each search tree stage. The search branches are limited by the so called search width w_{search}.The value of w_{search} specifies the number of additional branches

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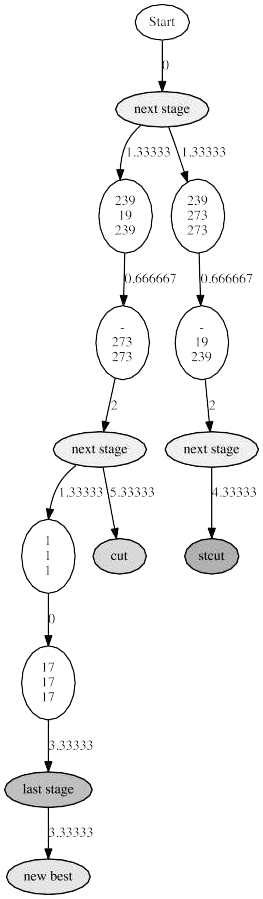

Fig. 7: Reduced search space of $w_{search} = 1$ for the given example

which are searched with the locally best solution. Thus, the search strategy is a modified breadth-first search and is related to the *beam search* strategy [24]. Within the meaning of this definition the initial greedy search of the algorithm has a search width of $w_{search} = 0$. As described earlier in Section II-B the decision for the next path to follow in the decision tree is made by using a cost matrix for each considered subtree in each stage. For the heuristic these cost matrices are sorted (cf. line 4 in Listing 1), to be able to quickly access the $w_{search} + 1$ best paths. When a path is selected, this selection equals the desired output mapping for the previous stage. For that previous stage the cost matrix is evaluated in the same way. This provides a very plain and fast method to reduce the search space. Note that the described branch-and-bound cuts can also be applied within the heuristic, which has the potential to further speed up the search. Especially the subtree cut (stcut), which was already explained in Section II-B is now very easy to perform due to the sorted use of the cost matrix within the heuristic. An example for the search space of $w_{search} = 1$ can be found in Fig. 7. The branch-and-bound cuts are denoted as *cut*, while the subtree cuts are denoted as *stcut*. Only eight instead of 40 decisions are needed compared to the full search for this rather small example to find a good –in this case the best– solution. This heuristic provides an easy way to directly control the run-time and offers the possibility to realize larger switchable coefficient sets for single and multiple constant multiplication.

E. Exploiting Ternary Adders

Adders with three inputs (ternary adders) can significantly reduce the number of operations in a pipelined adder graph generated by the RPAG heuristic [21] and thus, reduce the required hardware. Support for ternary adders is given in recent Altera and Xilinx FPGAs, namely Arria I, II, V, 10, Stratix II-V, 10 and Virtex 5-7 [22], [23]. That is why the fusion of such PAGs using three-input adders was also integrated into PAG fusion, taking the implementation available at OpenCores [25]. The target is to reduce the number of operations and with it the required multiplexer inputs. Instead of the two operations $a + b$ and $a - b$ each adder in the adder graph is now able to implement $a + b + c$, $-a\ b + c$, $a + -b\ c$ or $-a - b\ c$. The cost evaluation and the decision for a specific stage's mapping was adapted to this circumstance. This includes an extension of the data structure to provide nodes with three inputs. Special care has to be taken, when nodes with two and nodes with three inputs are fused. Here an addition with 0 has to be provided for the input, which is unused in one circuit. This leads to an additional degree of freedom, when selecting the node's input mapping and evaluating a mapping's costs. Another extension had to be provided in the fusion of subtractors. In the two-input adder case it is possible to map all negative inputs to the same input resulting in a subtractor instead of a switchable adder-subtractor. This is not always possible in the three input adder case ($a - b - c$). However, the swapping of inputs to get the best possible solution was adapted for the ternary adder cases ($a - b + c$, $a + b - c$), in which a swapping can help to reduce the required resources. All these adaptions are leading to a larger complexity for the consideration of inputs in these steps. Nevertheless, the overall run-time is supposed to be reduced, as the number of adders K_s per stage is reduced due to the operation reduction shown by Kumm et al. [21].

III. Low Level Optimizations

A. Multiplexer Mapping

As multiplexers are used to switch between the different constants, their mapping to the target FPGA should be as good as possible. This can be achieved by using the explicit resources provided in Xilinx Virtex 5-7 slices [26]. In the case of the used Virtex 6 FPGA, our VHDL code generator produces the optimal mapping using *Primitives* [27]. This results in a resource optimized multiplexer implementation. The gain of this implementation can be seen in Fig. 8, which shows the LUT consumption of the mapping achieved by Xilinx ISE 13.4 (gray) as well as the improved solution by using *Primitives* and the resource optimal mapping [26] (black when better, otherwise equal to ISE mapping). The operating frequency is not shown, due to the fact that only one up to three slices are required, which leads to frequency estimations between 770 and 1.300 MHz, which is unrealistic for a final design, as there should be more limiting parts elsewhere. In 16 of the 31 cases one LUT per bit can be saved. That is why the inclusion of this mapping as operator into our FloPoCo-based [28] VHDL generator is part of this work.

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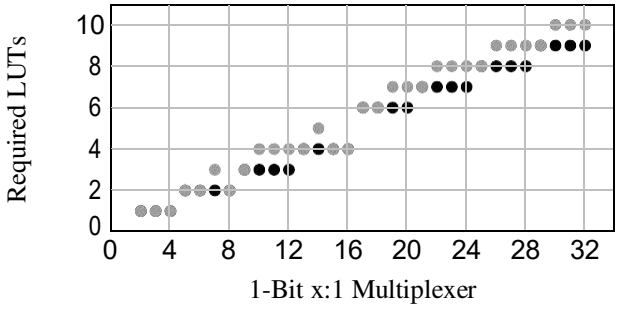

Fig. 8: Required LUTs for 1-bit x:1 multiplexer. ISE solution (gray) and improvement by *Primitive* usage [26] (black).

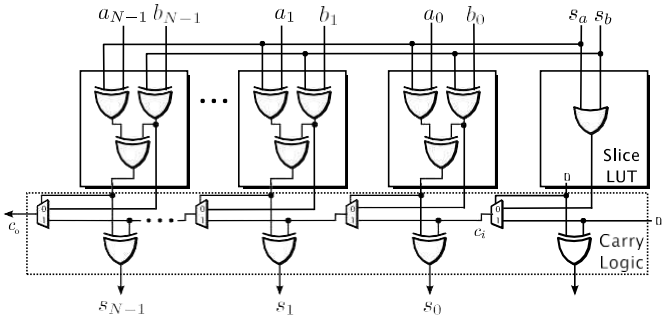

Fig. 9: Realization of switchable adder/subtractor on Xilinx Virtex 5-7 slices

B. Switchable Adder Subtractor Mapping

The fusion of adders with subtractors leads to the requirement of switchable adder/subtractors in which the input that is subtracted can be either input a or input b. The proposed realization of the switchable adder/subtractors on Xilinx Virtex 5-7 slices can be found in Fig. 9. The realization is done using a single LUT to provide the correct carry input and the following LUTs to provide an XOR of the inverted or non-inverted inputs, which builds a full adder together with the slice's carry logic. The inputs are inverted when required by an additional XOR of each input with the corresponding subtraction flag s_a or s_b. The subtraction flag s_a or alternatively s_b has to be set to 1 if a or b, respectively, should be subtracted. The case in which s_a and s_b are both 1 is not supported by the given implementation. Using the described switchable adder/subtractor together with the optimized multiplexer implementation helps to further reduce the required slice resources. In our experiments we observed cases, in which the more general VHDL implementation needed more than twice as many LUTs. So when a switchable adder subtractor is required more than 50% of slice resources can be saved in the best case with the proposed implementation.

IV. Results

This section provides synthesis results to highlight the advantages of the proposed method. For all experiments the same VHDL code generator which is based on the FloPoCo library [28] was used to create synthesizable VHDL code. VHDL code was generated with identical settings and mapped to a Virtex 6 FPGA (xc6vlx75t-2ff484-2) using Xilinx ISE v13.4. The proposed algorithms' input graphs to be fused were created using the RPAG heuristic. The source code of RPAG and of the proposed method is available online as open source within the PAGSuite [16].

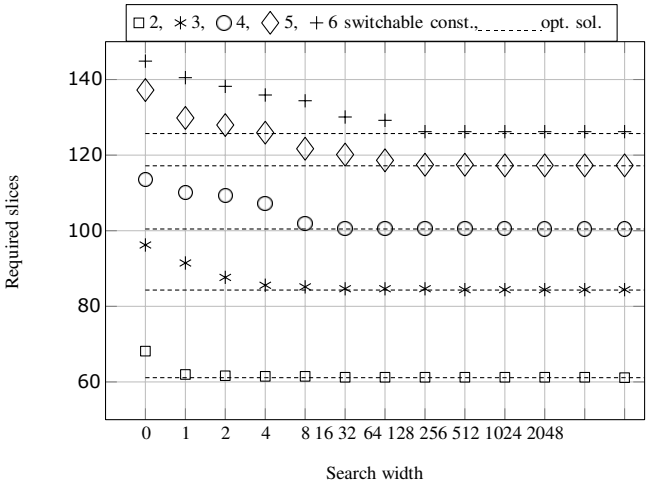

Fig. 10: Comparison of the required slices of the heuristic with different search widths and optimal solution (dashed lines).

TABLE II: Comparison of the average run-time of the heuristic to the optimal method and average area overhead of the heuristic solution

	run-time [s]		speedup	area degradation
	heur. $w = 64$	opt. [s]	heuristic	heuristic
2 conf.	<0.001	<0.001	1.00 x	0.41%
3 conf.	0.00188	0.00190	1.01 x	0.69%
4 conf.	0.9293	0.9355	1.01 x	0.37%
5 conf.	2.51	120.52	4.80 x	0.46%
6 conf.	14.16	1842.24	130.10 x	0.96%

A. Quality of the Heuristic

In order to evaluate the quality of the heuristic, an SCM benchmark for 2 to 14 configurations, each consisting of 100 constant sets using randomly generated constants uniformly distributed between 1 and $2^{16}-1$ was created. In this experiment, optimal solutions were generated to have a baseline for the heuristic results. In addition to that, solutions using the heuristic with different search widths for all benchmark sets were generated. A direct comparison of the average slice utilization of the optimal PAG fusion and the heuristic for constant sets with 2 to 6 configurations can be found in Fig. 10. It shows the required slices for the different search widths and the optimal solutions with dashed lines. It can be observed that a search width of only 64 leads to solutions close to the optimal solution for the RSCM benchmark sets with up to 6 configurations. The maximum operating frequency of all solutions is distributed equally between 443 and 469 MHz. The average run-time for a width of 64 in this experiment is compared in TABLE II. It can be observed that a longer run-time of the optimal algorithm leads to an increased speedup for the heuristic. At the same time, the area degradation of the heuristic is smaller than 1%. This encourages the use of the

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heuristic for larger numbers of outputs as required for RMCM problems, which have a much larger complexity due to a larger adder count per stage.

B. Comparison to DAG Fusion

This section shows a comparison of the proposed algorithm to the DAG fusion algorithm [17] which also relies on the fusion of adder graphs. The same benchmark as for the heuristic classification was used. Using this benchmark pipelined adder graphs with the proposed PAG fusion heuristic as well as pipelined and non-pipelined adder graphs with DAG fusion using the available SPIRAL source code [13] were generated. The pipelined DAG fusion results were obtained by inserting registers after each adder, subtractor, adder/-subtractor, multiplexer and corresponding pipeline balancing registers. Pipelined results for DAG fusion are needed for a fair comparison of the slice utilization and performance evaluation. The proposed algorithm was executed with a search width of 64 as motivated in the last section. DAG fusion was executed with a restricted mode provided in the DAG fusion code when the run-time exceeded 3 hours (typically needed for cases with more than 9 configurations). The results for the required slices after place and route and the maximum clock frequency can be found in Fig. 11. Note that each data point is an average value of 100 constant sets. As a baseline, a 16× 16 bit CoreGen [29] soft-core multiplier (LUT-based implementation) with the same pipeline depth as our solutions together with distributed RAM to store the coefficients is shown in Fig. 11. For the pipelined implementations it can be observed that the proposed algorithm has a lower slice utilization than DAG fusion in all cases. Compared to DAG fusion, the proposed method provides a slice reduction of 9% on average when 2-input adders are considered and 26% on average when ternary adders are considered. The resulting 2-input adder circuits can be run at nearly the same maximum clock frequency as the pipelined DAG fusion circuits and the CoreGen reference. Due to pipelining, the proposed method and pipelined DAG fusion have a similar critical path, which can be found in the adders or in the multiplexers with varying size. For the ternary adders there is a performance degradation of about 39% on average which was also reported by Kumm et al. [21]. The non-pipelined DAG fusion results are in some cases better than the pipelined 2-input and ternary adder results, but the maximum clock frequency is up to 5 times slower. This clearly shows the necessity of pipelining on FPGAs. The comparison between the DAG fusion results and the results of the proposed method also show that an optimization which considers all configurations in a single run leads to better results. In general, it can be seen that the proposed method is valuable for up to four configurations in the 2-input adder case and up to six configurations in the ternary adder case, when the required slices are considered. For more configurations, the soft-core multiplier implementation by CoreGen provides the solution which requires the least resources. For ASICs, DAG fusion proved to be valuable for up to 19 coefficient RSCM (cf. Table II in [17]). This appears to be a maximum gap between the optimized adder implementation and a generic multiplier.

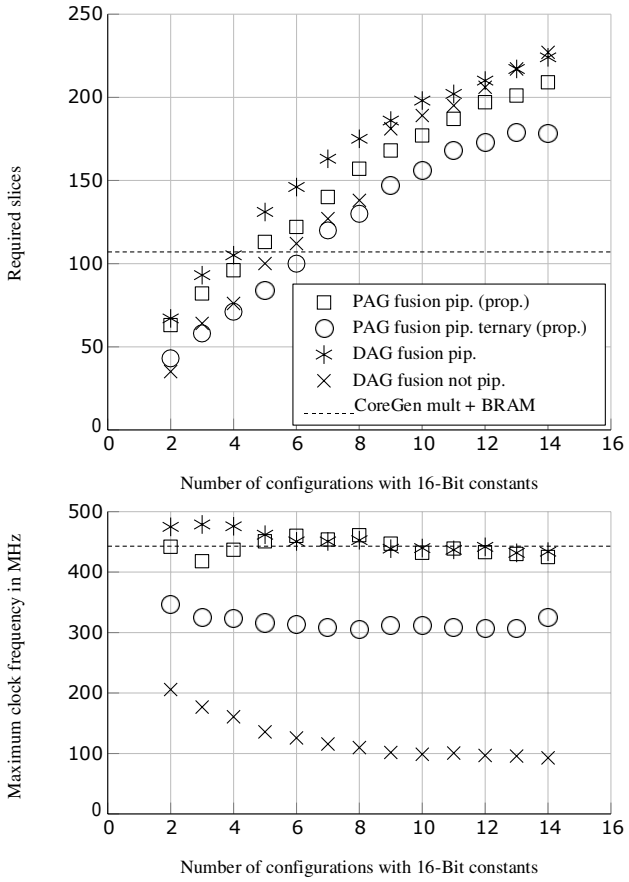

Fig. 11: Comparison of the required slices (top) and the maximum clock frequency (bottom) for the proposed method and DAG fusion [17].

This has to be of course smaller for FPGAs. For this small gap, which is a relevant field for many applications, the proposed heuristic can generate solutions with significantly lower resource consumption and similar performance. When only RSCM is considered, optimal solutions are possible, when about half an hour of run-time is feasible. But the heuristic is unconditionally required to enable shift-add-based reconfigurable multiple constant multiplication, especially with many outputs, which is required, e.g., for run-time reconfigurable FIR filters.

C. Reconfigurable Multiple Constant Multiplication

When reconfigurable multiple constant multiplication is considered, it can again be compared to the CoreGen soft-core multiplier with RAM for the coefficients. To have more than one output, multiple CoreGen multipliers and coefficient RAMs are used. A benchmark for 5 different MCM cases (2, 4, 6, 8 and 10 outputs), each with 2, 4, 6, 8 and 10 configurations, consisting of 50 constant sets per case using randomly generated constants uniformly distributed between 1 and $2^{16}-1$ was created. The search width was again set to 64. The results of the 2-input and 3-input adder implementations compared to CoreGen multipliers can be found in Fig. 12.

It can be seen that the CoreGen soft-core multiplier implementation is better for 6 or more configurations in the 2-input

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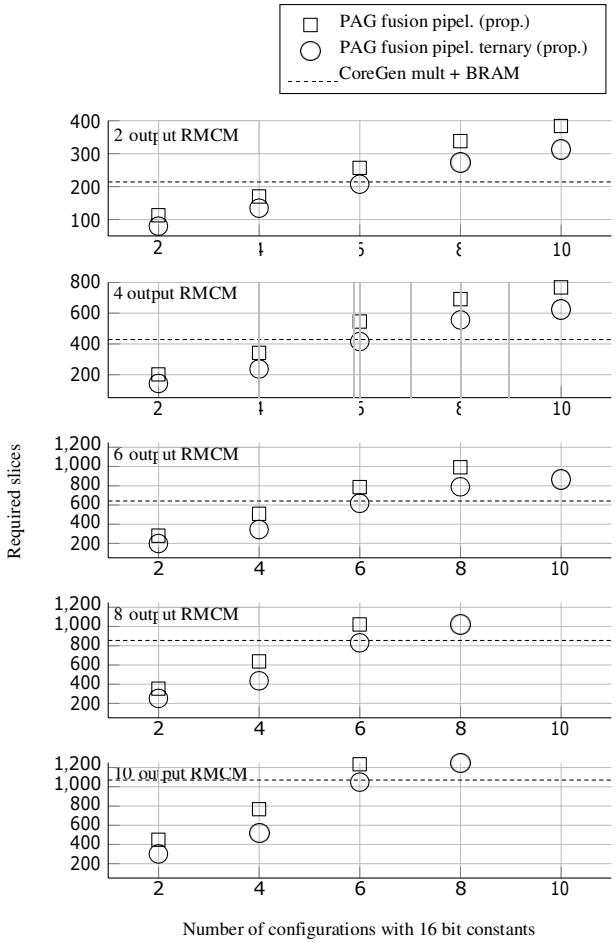

Fig. 12: Comparison of RMCM and tRMCM to a CoreGen soft-core multiplier + RAM

adder case and 8 or more configurations in the ternary adder case. Below these numbers of configurations, up to 75% of the resources can be saved, when the proposed reconfigurable shift and add based implementation is preferred, which is up to 750 slices in the 10 output RMCM case. Note that without the heuristic only the results for 2 outputs and 2 configurations could have been generated optimally within a run-time limit of 3 hours. MCM solutions normally have more adders in each stage, which leads to a much larger search space and thus a much larger run-time. Using the heuristic with its controllable search width, raises the solvable problem size and thereby enables the application domain of RMCM for the proposed fusion algorithm. For the application domains given in the introduction [1], [2], [3], [4], [5], 2 to 6 MCM configurations are common, which is the range of the proposed heuristic. Up to 75% of slice resources can be saved compared to a generic multiplier.

D. Comparison to Other Reconfiguration Approaches

If the presented multiplexer-based switchable multiple constant multiplication is compared in the context of reconfigurable circuits, the reconfiguration time is an important factor. The presented approach has a reconfiguration time of only one clock cycle which is about 2-3 ns for the mapped and routed designs. To compare our method to other reconfiguration approaches, a 41 tap benchmark FIR filter (MIRZAEI10_41 [30]) was used. This benchmark was already used in prior work [31], to compare internal configuration access port (ICAP) reconfiguration of Xilinx FPGAs and two logic based reconfiguration approaches. In the benchmark the original filter was extended to a run-time reconfigurable FIR filter by designing additional different FIR filters with the same length as the original benchmark filter and an input word size of 16 bit. These were optimized by using RPAG [14] and can be reconfigured via ICAP. Alternatively, the benchmark set was realized using the two logic based reconfiguration approaches (FIR DA and FIR LUT). In the FIR DA approach the FIR filters were realized using Distributed Arithmetic [32] with a LUT-based implementation and were made reconfigurable by using run-time configurable 5-input LUTs in Xilinx Virtex FPGAs. The FIR LUT approach is based on the KCM method [33], in which a constant multiplier is built by several smaller LUT multipliers, whose shifted outputs are finally added. Reconfiguration was again achieved by using run-time configurable 5-input LUTs in Xilinx Virtex FPGAs. These have a configuration time of 32 clock cycles, leading to a reconfiguration time of about 61 to 66 ns in the analyzed filters. The presented PAG fusion heuristic can be used to generate the multiplication of switchable filter coefficients (RMCM) with the input of a transposed FIR filter, which are then followed by structural adders. The results for the previous work and results for PAG fusion RMCM FIR filters for 2 to 5 configurations (conf.) are listed in TABLE III. In this case the number of configurations corresponds to the number of different FIR filter coefficient sets. The ICAP resource consumption and maximum clock frequency are noted as a range as the applied RPAG optimization heavily depends on the numeric coefficient values. In addition, a FIR filter using CoreGen multipliers together with RAM was evaluated. It can be seen that the resulting circuits of the proposed method provide the fastest reconfiguration time with a better resource consumption for 2 to 4 configurations. The large increase in slices from 4 to 5 configurations can be directly traced back to the increase of LUT costs for the 5-input multiplexers (cf. Fig. 8). For 5 to 10 configurations it depends on the required reconfiguration time, if the reconfigurable FIR filter using distributed arithmetic or LUT multipliers together with reconfigurable LUTs or the ICAP implementation should be used. An implementation with CoreGen multipliers is only valuable when very fast reconfiguration times and at the same time a large number of configurations are required.

E. DSP Block Usage Considerations

On modern FPGAs, DSP blocks in combination with RAM for the coefficients can be used instead of the proposed run-time reconfigurable constant multiplication. If limited quantity of DSP blocks is not a problem, each of the 16 x 16 bit multipliers of reported cases could be replaced by one DSP block and two slices for the coefficient RAM. For multiplication word sizes larger than 18 Bit, more than one DSP block would be required for Xilinx FPGAs. A comparison of the usage

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TABLE III: Comparison of a single filter MIRZAEI10_41 with $B_x = 16$ bit using ICAP reconfiguration, CFGLUT methods, the proposed PAG Fusion heuristic and CoreGen mutlipliers.

Method	S [bit]	Slices	f_{clk} [MHz]	T_{rec} [ns]
RPAG [34] with ICAP	746496	502. . . 569	386.7. . . 448.8	233280
Reconf. FIR DA [35]	1920	1071	521.9	61.3
Reconf. FIR LUT [31]	14784	1108	487.8	65.6
PAG Fusion (2 conf.)	0	848	401.3	2.5
PAG Fusion (3 conf.)	0	911	372.2	2.7
PAG Fusion (4 conf.)	0	968	402.7	2.5
PAG Fusion (5 conf.)	0	1590	340.0	2.9
CoreGen mult	3360	2647	343.9	2.9

of DSP blocks to the proposed slice based method can be done by relating the two types of resources (DSP blocks and slices) according to their relative availability, referencing their utilization ratio [15]. Alternatively, the chip area consumed by the resources can be related [36]. However, neither of the two methods addresses the frequent requirement to select the smallest, hence cheapest, possible FPGA the design fits into. Usually, in a complete design other parts are competing for DSP resources in digital signal processing applications [37], [38]. For such cases a trade-off must be available. This is provided by the proposed slice based run-time reconfigurable constant multiplier implementation.

V. Conclusion

This work presented a new heuristic to generate pipelined run-time reconfigurable constant multipliers based on an optimal algorithm. The heuristic was motivated by a complexity consideration of the search space. With the heuristic problems with a larger size become solvable. An extensive benchmark evaluation showed superiority over previous work, as we could show a 9-26% slice reduction on average. Additional extensions to the algorithm were presented which further reduce the slice consumption of the resulting solutions. These were the support of ternary adders, and optimized multiplexer and switchable adder/subtractor mapping. Finally it could be shown by RMCM and FIR filter experiments that the heuristic is raising the solvable problem size and the application domain of the proposed fusion method. Compared to other reconfiguration approaches our method provides the fastest reconfiguration time with a low resource consumption for a limited number of configurations. The source code of the proposed method is available online as open source within the PAGSuite project [16] to increase reproducibility and provide it for future research.

ACKNOWLEDGEMENT

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SMART CROSSING SYSTEM USING IOT

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Abstract: Crosswalk is a way of sharing the road between vehicle and people. However, density of the population rises, meanwhile the number of total accidents decreasing, the number of pedestrian accident does not drop down for 10 years. In this paper, we propose a new system called Smart Crossing that is another type of crosswalk using sensors, CCTV, illuminator and an IoT device to keep pedestrian in safe while crossing..

Index Terms— **CCTV, ILLUMINATOR, SENSORS, IOT**

I .INTRODUCTION

Since people and vehicle are sharing the road, crosswalk increases efficiency of using the road in highly concentrated area. However, as the population increases, this brings more frequent accidents and more serious injuries and hence, nationals are trying to reduce these accidents by making promotions and legal sanctions. Such actions pull down the total number of fatal accidents but unfortunately, number of pedestrian fatalities does not decrease for a decade [1]. To be specific, this fatality does not have a similar characteristic compares to others. A research about 2014 in USA shows fatalities in 78% occurred in urban, 71% occurred at nonintersections and 72% occurred in the dark [1]. Through this research, pedestrian fatalities are implying heavily populated area causes more chance to make an accident and an inferior recognition makes less chance to detect a pedestrian or a vehicle.

In this paper, we propose a crosswalk system using sensors, a CCTV and illuminator to track pedestrian and highlight them to make vehicle driver easily avoid any dangerous situations and also shows how to treat an accident to save both pedestrian and vehicle driver.

II. RELATED WORKS

Pedestrian fatalities seem to be affected by diverse reasons. However, amazingly, several features that may look like to affect, such as drunk driver or young driver, was not the major problems in accidents. It is more likely to influence by the density and number of the population and daylight. To reduce the number of pedestrian fatalities, there are several approaches, which lead driver to slow down, solve this problem. First approach is to enforce the recognition of crosswalk area using light emitting pavement marker, therefore vehicle driver can be easily informed where the actual crosswalk is on the road [2 - 4]. For all that, this neither prevents any sudden reactions from pedestrians nor drivers to notice pedestrian easily. Second approach is illuminating the crosswalk area that the driver notices a pedestrian from long distance. This is very adequate against a sudden emergence of pedestrian. On the contrary, this consumes too much energy to sustain all dark hours for sparse pedestrians moreover the coast of energy is not cheap if illuminators are installed more to lower the chance of accident [5]. For all that, if the accident happens, there is nothing more than trusting the vehicle driver to call emergency unless the pedestrian has its consciousness..

III. SYSTEM OF SMART CROSSINGS

Smart Crossing suggests a new type of crosswalk system that aims the same goal with the puffin crossing system. The system provides devices are formed with six major parts as seen in Figure 1.
Control Unit manages and controls every connected device, stores metadata about the devices and itself, saves a video records from CCTV Analyzer, communicates with Control Center to fetch updates and send a particular video records and operates algorithms about abnormal movement tracking and pedestrian presence. CCTV Analyzer is working with CCTV to track pedestrian and records the crossings. Tracking is to serve an additional information to Boundary Detector to perform corrections. Recording is to identify the situation that might be an accident. The records are fetched by Control Center to analyze if there has any serious accident happened. This record can be a major evidence to track the hit and run vehicle driver. Boundary Detector is to detect the pedestrian and vehicles enter particular area. In this system has two boundary detectors, which are installed at crosswalk and the other is at vehicle stop and yield line. Boundary detector utilizes CCTV and illuminator when it detects the presence of pedestrians waiting at the crossings, and as they are crossing the road.

Illuminator is to light up the crosswalk and pedestrians to be recognized from great distance and provides light to CCTV to record the

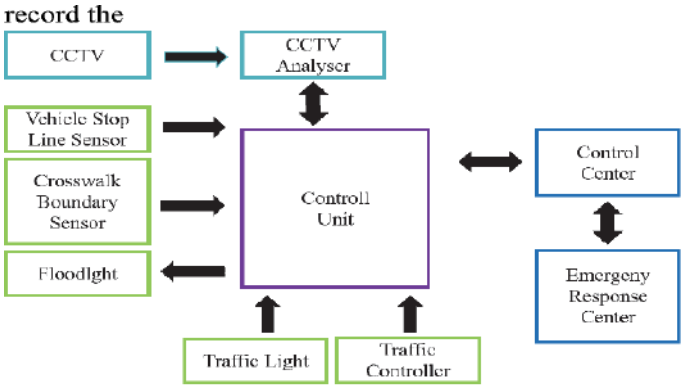


Fig. 1. Architecture of Smart Crossing

crosswalk area. The records will be fetched if the suspected events detected by the abnormal movement tracking algorithm. Traffic Controller is mounted at the near the roadside to start the passing traffic. The controller the pedestrian to monitor passing traffic while waiting for the signal to cross. Control Center monitors the all control unit operations and audits any suspecting events that may be a serious accident. The abnormal movement-tracking algorithm reports any kind of unexpected sensing records to control center including with false-negative detections. In the field, monitoring agents take a video record of clipped part from reported the control unit, and they check it is an accident happened. In control unit, it has two major algorithms, called abnormal movement tracking algorithm and pedestrian presence algorithm. Pedestrian presence algorithm is sustaining the single to cross using CCTV analyzer and boundary detector. It also treats any sudden enter without using controller. Abnormal movement tracking algorithm is to detect abnormal actions, as shown in Table I, which derives any chance of making fatalities. At the end of strong suspecting of fatalities, abnormal movement tracking algorithm sends distress signal to control center over the Internet. Therefore, control center checks out recorded video and takes an immediate action to save lives.

IV. EXPERIMENTS AND RESULTS

In experiment, we tested efficiency of using illuminator in the smart crossing to how many drivers can recognize pedestrians earlier before they enter the serious crash. To find out, we used a car that mostly found in urban using only downward headlights and a pedestrian who dressed up with dark clothes. Experiments is done by flipping the photos of even distances, shown in Figure 2, between the vehicle and the pedestrian. We assume that speed of car to makes a fatality at least 60km/h. Photos of each distance showed in every 5seconds. 20 participants are in the test and we gain an average percent of perfect recognition in each distance. As the result, in Figure 2., the distance of recognition of pedestrian using illuminator extends three times longer than using headlights of the vehicle. The actual recognized distance is enough to stop the car before hit the pedestrian. As the experiment goes again most interesting facts is that participants are being expected that pedestrian may be in crosswalk when the lights on, even they are not seen them yet.

II. SYSTEM DESCRIPTION

A. Environmental parameters

To determine the weather status of mining, the system measures relevant variables using techniques that are minimally invasive. To obtain a complete overview, the extreme conditions of mine sites in underground are also measured by the incorporation of environmental sensors. The embedded measured parameters are:

- **Gas levels:** Subsurface atmosphere may be contaminated with poisonous gases that displace the necessary oxygen to support life or flammable gases that may cause explosion. Therefore, it is necessary to develop technologies and find ways to accurately measure concentration levels of toxic and flammable gases levels in subsurface atmosphere for safety of underground coal mines

- **Vibration levels:** vibrations involved measurements on the roof and walls of underground mines. Primary importance in underground excavation is .the requirement to maintain rock stability and prevent rock falls or damage to support .structure's. The high-intensity elastic waves induced by production blasting and the adjustment of rock due to stresses associated with the opening itself create conditions that affect rock competency outside the excavation boundary.

- **Temperature**: The mine is so deep that temperatures in the mine can rise to life-threatening levels. Air-conditioning equipment is used to cool the mine from **55** °C (131 °F) down to a more tolerable 28 °C (82 °F). The rock face temperature reaches 60 °C (140 °F). In this proposed paper temperature is measured with sensors.

- **Obstacle detection**: obstacle is dangerous in underground mining, it is monitored by infrared sensors. If obstacle is within the range of sensor, it will detect.

A schematics overview of the proposed system is shown in Fig. 2. The environmental variables are measured using a sensors and data is transferred through IOT technology. Wireless data transmission of sensed values is achieved using a Wi-Fi module. Controller takes input from sensors and alerts when threshold levels of sensors are high.

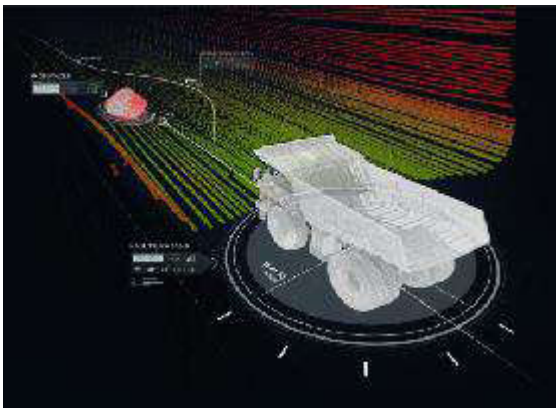


Fig.4. obstacle detection in underground mining

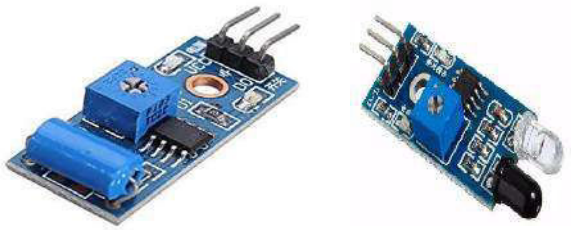


Fig. 5. Vibration sensor and IR sensor

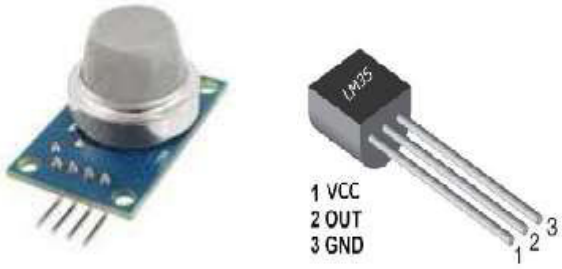


Fig. 6. Gas sensor and temperature sensor

B. Environmental embedded sensors

All environmental sensors are embedded and gives input to microcontroller. ARM7 (LPC2148) is used as microcontroller in this proposed paper. Implementation and features of each sensor are described below.

IR sensor*:* An infrared sensor is an electronic device that emits in order to sense some aspects of the surroundings. An IR sensor can measure the heat of an object as well as detects the motion. These types of sensors measures only infrared radiation, rather than emitting it that is called as a passive IR sensor. Usually in the infrared spectrum, all the objects radiate some form of thermal radiations. These types of radiations are invisible to our eyes that can be detected by an infrared sensor.

The emitter is simply an IR LED (Light Emitting Diode) and the detector is simply an IR photodiode which is sensitive to IR light of the same wavelength as that emitted by the IR LED. When IR light falls on the photodiode, the resistances and these output voltages, change in proportion to the magnitude of the IR light received.

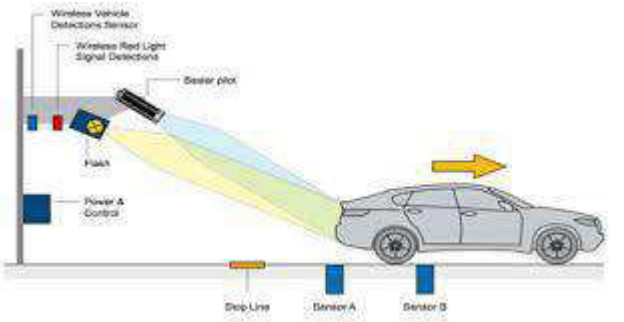
Temperature sensor (LM35): The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full -55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level.

The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a -55° to +150°C temperature range, while the LM35C is rated for a -40° to +110°C range (-10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Gas sensor (MQ5)/ smoke sensor: A smoke detector is a device that detects smoke, typically as an indicator of fire. Commercial, industrial, and mass residential devices issue a signal to a fire alarm system, while household detectors, known as smoke alarms, generally issue a local audible and/or visual alarm from the detector itself. Smoke detectors are typically housed in a disk-shaped plastic enclosure about 150 millimetres (6 in) in diameter and 25 millimetres (1 in) thick, but the shape can vary by manufacturer or product line.

Most smoke detectors work either by optical detection (photoelectric) or by physical process (ionization), while others use both detection methods to increase sensitivity to smoke. Sensitive alarms can be used to detect, and thus deter, smoking in areas where it is banned such as toilets and schools. Smoke detectors in large commercial, industrial, and residential buildings are usually powered by a central fire alarm system, which is powered by the building power with a battery backup. However, in many single family detached and smaller multiple family housings, a smoke alarm is often powered only by a single disposable battery.

TRIFFIC TRAFFIC LIGHT SENSORS: The primary, reliable and most common **traffic light sensors are** induction loops. Inductive loops **are** coils of wire that **have** been embedded on the surface of the road to detect changes in inductance and convey them to the **sensor** circuitry in order to produce signals.



Vibration sensor (SW-420): Measurement Specialties is a leading global provider of accelerometers and vibration sensing know-how for applications in Aircraft Design & Testing, Automotive Design & Testing, Automotive Safety Testing, Machine & Structure Monitoring and Motorsport. We offer both DC-Response (Static) and AC-Response (Dynamic) types of accelerometers to meet your different needs. There are two classes of accelerometers: AC-response and DC-response types. In an AC-response accelerometer, as the name implies, the output is AC coupled. An AC coupled device cannot be used to measure static acceleration such as gravity and constant centrifugal acceleration. It is only suitable for measuring dynamic events. A DC-response accelerometer, on the other hand, is DC coupled, and responds down to zero Hertz. It therefore can be used to measure static, as well as dynamic accelerator.

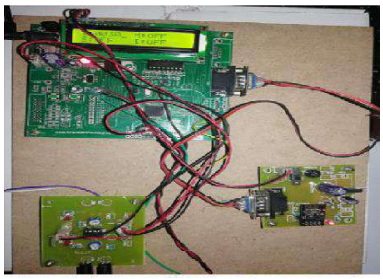


Fig. 7 Prototype of complete system hardware

C. Data Acquisition, Processing hardware and software

Data Acquisition and MCU Processing: The Microcontroller Unit MCU was implemented using a simple ARM 7 LPC2148. The ARM7 family of processors is a range of low-power, 32-bit RISC cores optimized for cost and power-sensitive applications. All the cores in the family feature the 16-bit Thumb instruction set, enabling high code density to be achieved with 32-bit performance levels. The ARM7TDMI core is a member of the ARM family of general-purpose 32-bit microprocessors. The ARM family offers high performance for very low power consumption, and small size. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles. The RISC instruction set and related decode mechanism are much simpler than those of Complex Instruction Set Computer (CISC) designs. It has Good speed/power consumption ratio, Uniform and Fixed length instructions, and High code density, Load-Store architecture, where data processing operations involve only registers but not memory locations and large uniform register file.

1.

MCU acquires and processes the signals from the environmental embedded sensors, and sends data via wireless network to the monitoring system for registration, displaying and information storage purposes. Threshold level of temperature sensor is 40 deg, gas sensor threshold is 400ppm, vibration sensor threshold is 5mm/sec, and IR range is 20 meters.

Fig. 7 shows the final prototype of implemented device, including embedded environmental sensors, and the printed circuit board (PCB).

Wireless data transmission*:* The data are wireless transferred using a NETGEAR R300 module from embedded sensing unit to the output unit. Data transfer speed is set at 115,200 bits per second. The NETGEAR R6300 WiFi Router delivers next generation WiFi at gigabit speeds.

It offers the ultimate mobility for WiFi devices with speeds up to 3x faster than 802.11n. Compatible with next generation WiFi devices, and backward compatible with 802.11 a/b/g and n devices, it enables HD streaming throughout your home. The R6300 with simultaneous dual band WiFi technology offers speeds up to 4501 to 13002 Mbps and avoids interference, ensuring top WiFi speeds and reliable connections. This makes it ideal for larger homes with multiple devices.

Software and Graphical User Interface (GUI): Data are displayed and stored at the base server of the monitoring system. So the information is available for the staff or operations supervisor, or the user itself. The data provide real-time information about the current weather condition of the worker.

D. Software tools:

Keil: Keil Software launches amongst the ideal entire improvement tool collections for ARM7 software program application, that's utilized throughout endeavor. For development of C code, their Developer's Kit product has their C51 compiler, in addition to a contained ARM7 simulator for debugging. A discussion layout of this thing is conveniently offered on their website, yet it consists of numerous challenges.

The C program language produced computer systems, although, along with say goodbye to embedded structures. It does presently not maintain straight acquire admission to register, neither does it make it possible for the checking out in addition to developing of singular bits, exceptionally essential needs for ARM7 software program application. In addition, a great deal of software program application designers are acquainted with producing packages that will done by utilizing a working gadget, which makes use of system calls the program can additionally use to access the tools.

However, a bargain code for the ARM7 is produced for straight use at the cpu, without an running manufacturer. To maintain this, the Keil compiler has in fact provided countless developments to the C language to transform simply exactly what would certainly probably have in fact typically been implemented in a device phone conversation, along with the connecting of interrupt instructors. The intent of this manual comparable method supply a summary for the restrictions of the Keil compiler, the alterations it has really made to the C language, as well as the ways to earn up those in producing software application for the ARM7 microcontroller.

Flash magic*:* Squint Magic is an application progressed through Embedded Systems academy to empower you to quickly gain admittance to the qualities of a microcontroller gadget. With this program you could remove private squares or the total Flash memory of the microcontroller. This item program is to an awesome degree huge for people that paints inside the electronic devices subject. A champion among the most crucial home window of the program contains 5 zones where you may locate the perfect ordinary limits in a movement to programming a microcontroller gadget. Making use of the "Exchanges" area you can pick the techniques, a particular instrument associates in your PC system. Select the COM port to be utilized and furthermore the baud cost. It is suggested that you select a diminished baud cost starting and moreover change it later on. This shape you'll choose the particular best rate with which your gadget limits. Remembering the ultimate objective to pick which parts of the memory to oust, pick from the things inside the "Erase" area. The third stage is non-compulsory. It supplies you the chance to set a HEX data. In the succeeding section you can discover striking shows decisions, that consolidate "insist after ventures", "gen square checksums", "perform" and also others. When you're performed, tap the Start switch that might be orchestrated in the "Start" territory. The item application will irrefutably begin the device, and you'll with the limit of see the development of the procedures toward the complete of thought home window.

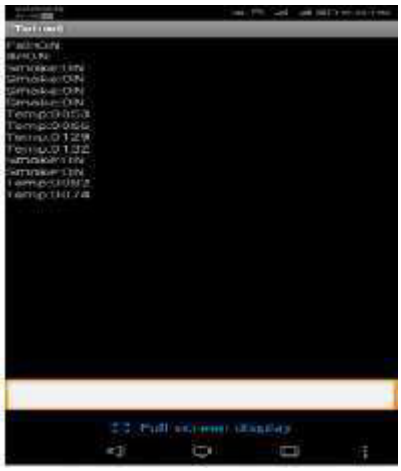


Fig.8. output results

The output results are shown in figure 8. Results can be seen from telnet application, which can be downloaded from playstore and install it. IP address can be tracked from this application. All sensor values and ouput results can be monitored in telnet application. Otherwise Ip address can be tracked by browsing IP from google. The results are shown only when thresholds are high.

III. RESULTS

The proposed system was tested by performing measurements in two environments: a controlled environment at the laboratory, and a real working environment. First, a 30 minute measurement was performed to confirm the effectiveness of the algorithms and to verify empirically the noise sensitivity of the device. Next, measurements have been performed in distinctive daily activities during work time. Each set of monitoring results lasts approximately 5 hours.

In the laboratory tests, the subject at resting state had an average temperature of 45deg, a vibrations of 5mm/sec and a gas of 400ppm measured with the system during laboratory testing.

ACKNOWLEDGMENT

It is with great pressure that we submit this project entitled "**SMART CROSSINGSYSTEM USING IOT.**" We take this opportunity to thank those involved directly or indirectly with this project. Without their active co-operation, it would have not been possible to complete this project on time. At the outset, we keep on giving our deep sense of gratitude towards our project guide Mr. **Rajendra Prasad** and to **Mr. Shiva kumar**, Head of Dept. and also **Dr. john paul**, Principal at Mallareddy College of Engineering. Mr. Rajendra Prasad, who gave us the guidance right from the initial stage of project and offered us valuable suggestions for developing the project in a systematic and presentable manner.

V. CONCLUSION

In this paper, we propose a new type of crossing system that can provide pedestrian safety as well as drivers to notice pedestrians earlier to avoid any dangerous situation. Using illuminator provides three times longer distance of noticing the pedestrian that earns enough time to slow down the speed of vehicle. If in case of accident happens, smart crossing provides automated circumstance reporting to the control center about the situation records and respond immediately whether the driver get panic or run away. This may save many lives, which brings more chances to get into the golden hour. Smart crossing also saves enormous energy in running the illuminator. Many other illuminator spends a lot of energy to illuminate the crosswalk whether the pedestrian exists or not. Meanwhile, smart crossing turns on the illuminator when the pedestrian exists.

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IOT Based Smart Health Care kit

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Abstract

This paper is focus on IOT based smart healthcare kit. It plays an important role in emergency medical service like Intensive Care Units (ICU), by using a INTEL GALILEO 2ND generation development board. It helps to record or collect (BP, Pulses, Temperature) the information about patient. It helps to utilize the time of both the patient and doctor. It helps to store the data of patient like, blood pressure, heart beat rate, temperature, ECG etc. This paper helps to make the connection between patient and his doctor. This systems sends the real time data of a patient to his doctor and record it for his future reference. This paper is help to give the proper and efficient medical service.

Keywords- Internet of things (IOT), Sensors, Health monitoring

1. Introduction

In IOT there are many devices are connected to each other for communication purpose it shares the data, information and able to produce new information and record it for future purpose. Everyday people require new devices, new technology for make his life easy. The research is always trying to think on new devices for make his life easy. In our day to day life we are facing many problems related to our health because we are not caring about our self. So, to reduce these problems we are introduced a IOT Based Smart Healthcare Kit. This system is used in hospital to measure and monitoring like, temperature, ECG, heart beat rate etc. And the result is recorded in INTEL GALILEO BOARD and display on LCD. The doctor can login to this website and see that result.This system used sensors and actuators for receive the data from patient and record it. This system is give better output and it is less costly.

2.LITERATURE SURVEY

The Research is going on in the field of IOT-healthcare which gives clinical evidence that they received data from wireless network that are connected to devices which has contributed in managing and preventing from diseases and monitoring patients. Therefore, the various health monitoring systems are getting better today's like, ECG monitors, pulse rate, heart beat rate and blood pressure monitor. Now the research is going in the field of IOT and many products and services are used based on them, in which one or more devices used among those of Automation and Artificial Intelligence systems for energy conservation.

1. Cooey Smart Health **:** The Cooey Smart health helps your automatically log your medical data through Bluetooth devices. It takes note of your health by storing, analyzing and sharing your medical records which are provided by doctor. It also advices you by giving the smart tips and services based on your health analysis. It also give you alerts through messages and mail about your health risks. It is able to connect remotely monitor the health reports as well as also has the option of connecting yourself to various health service that are provide like pharmacy and teleconsulting. It consists of three different health monitoring systems. Cooey is able to interconnect and provide focused services to its customers It measure Blood Pressure Monitor, Smart Body Analyzer. The Cooey Smart health is lengthwise health monitoring IOT platforms which help the providers in storing, collecting and analyzing of medical data so as to provide alerts by using message, mail etc for patients. It lets help to choose and customize your personalized and the services based upon your health condition. For customers, it is a health management application with personalized services. Except this system no other product and app is able to provide a last mile connection of a patient with his health expert's doctors. But through the help of services. Some of the services.

That Cooey is provides:-

Measure and Monitor

- Engage
- Fulfillment

Measure and Monitor:-The Smart devices like Bluetooth BP monitor is help you automatically save your medical data and give the information to your medical health experts to remotely access this data. Engage: The Different data are including the profile of patient, his all information and data collected on the basis health tips are provided in Order to improve health management Fulfilment. The data which is collected is also used to create dynamic profile of the patient according to his current health status so that on further analysis this profile can be used by other

medical experts The Cooey smart services are focus mainly on Chronic patients and Antenatal care offering The Devices which are used to record and share your medical data and go through analysis.

Smart assist:-It Provide personalized advices and Recommendations in smart recommendation engine using smart algorithms .

M-Assist:-It provides with mobile API for personal health devices like laptops and management.

W-Assist:-The Internet connected web based portal it works on the mobile tablets.

2. Health Vault by Microsoft

The Microsoft Health Vault is assists you to use, gather, store, and share health information for you and your loved ones. You can store all your health records at one place that's Organize and available to you online (E-Book Keeping) in case of medical emergencies, it is able to keep track of all the details so that you are always alerted about your wellness. It records the data once, and use it with new data to get frequent updates about your health. The Health Vault-connected apps include websites, computer software, and mobile apps that can always help you and analyse more out of your captured health information. It also features that multi-app connectivity so that the information can be shared with anyone you want.

Its features:-

It gives Up-to-date medication and allergy lists Latest home health readings (such as blood pressure, heartbeat rate and weight) The health history The Health vault is not only helps you store, organize, but also give this information automatically to your doctor. It can record and store your results, prescription history and visit records from an increasing list of connected labs, medical institutes, hospitals and clinics which can send to your Health Vault and record it. You can transfer your detail it from anywhere, Smartphone/tablet. Medical logs and can easily keep these track records in, by using Internet connection on a PC, It can keep your details at your fingertips and access for future reference. The Medical images can be easily saved and shared to your medical consultants and keep them for future references. Graphs, patterns and trends are drawn by collected data in the Health Vault which help your medical experts/doctors to make efficient and better health related services. It helps to maintain your daily health chart and current status.

Health Vault features:

Authentication: - It connect with the Windows Live ID

Authorization:- By providing the user authorization before enable any data it shares the data/information between an application and a user's Health vault account detail to his doctor

User control:- By giving them the control to authorize data it shares and provide them a feature to stop application access at any time, and we can change or delete information in their history to by consulting our doctors.

Data provenance:- It intelligently taking decisions on how to treat a data from different sources.

III. PROPOSED MODEL

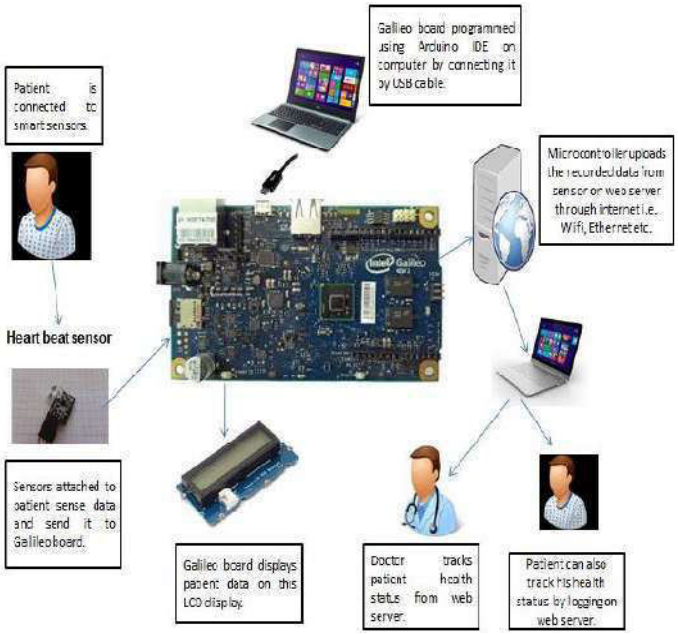

Fig.1 System Architecture

We have proposed the robust health monitoring system that is give intelligent and enough to monitor the patient automatically using IOT. It collects the status information through these systems by including patient's heart bit rate, blood pressure and ECG and sends an emergency alert to patient's doctor with his current status and full medical information. This would help to the doctor to monitor his patient from anywhere and anytime and also to send to patient his health status directly without visiting to the hospital. This system can be deployed at various hospitals and medical institutes for reducing the time. The system uses smart sensors that generates the data information and collected from each sensor and send it to a database server i.e. hospital where the data can be further analysed and maintained to be used for the medical experts. By Maintaining a database server is a must where the data is Previously medical record of the patient and providing a better and improved examining output. The digital output is connected to the microcontroller directly for measure the Beats per Minute (BPM) rate. It follows the principle of light modulation by blood flow through finger at each pulse. The other sensors like a blood pressure sensor, ECG sensor and many more can be added to the patient kit in

response to the patient's medical condition. Software: The software part includes an Arduino IDE which is required to program in Intel Galileo Board which used to upload the final code of maintaining a database. All the data connected are connect with the sensors and it sent to an Xampp based data base server for log the patient timely record or sensed data, which will help to the doctor for better consulting and prescription to patient. More over these datasets stored in database are

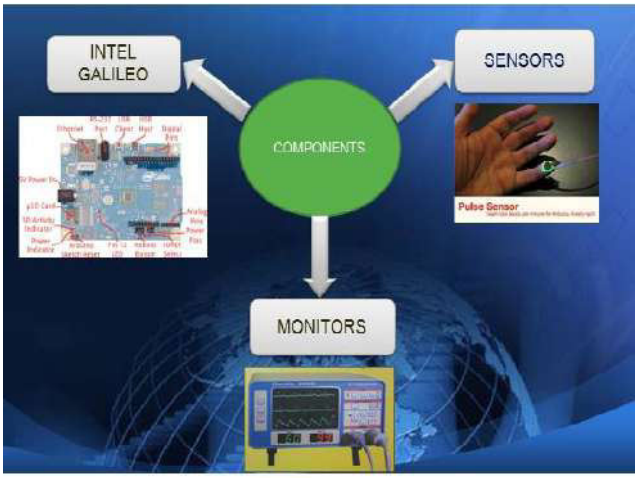

Fig 2 Components used

used to plot graph for each of the sensors are shown. The server has an option for uploading the database of the patients with their details and their medical history. The data server can be accessed any time by the doctor and the doctor can also see the current live feed of the patient's medical condition. A track of patient's health record is also maintained for future reference on the web portal. The portal also has the option to maintain and track the 24-Hour records of multiple patients. The patient can also see his/her medical details on the web portal. Thus this system proves to be an efficient and robust way to maintain and analyze one's medical record and live track. The server has an option for uploading the database of the patients with their details and their medical history. The data server can be accessed any time by the doctor and the doctor can also see the current live feed of the patient's medical condition. A track of patient's health record is also maintained for future reference on the web portal. The portal also has the option to maintain and track the 24-hour records of multiple patients. The patient can also see his/her medical details on. Thus this system proves to be an efficient and robust way to the web portal and maintain and analyze one's medical record and live track.

IV. EXPERIMENTAL RESULTS

The proposed of the intelligent health monitoring system is being developed and tested over a patient whose personal details are entered into the web portal. The patient is connected with his health monitoring system which consists of a heart rate sensor and a temperature sensor. The live graph of the patient's heart rate and temperature is being monitored on a Xampp based database server. The IOT device used here is the Intel Galileo board. The system architecture of the proposed model is explained by the given below figures which includes a server connected Intel Galileo board that helps to upload the data and receive by the sensors onto the database and statistical graphs are being plotted for further analysis and recording.

Fig.2 Home Page The index or the Home page of the the web portal it consists of various tabs including the Login, Services, About Us, Contact and Upl

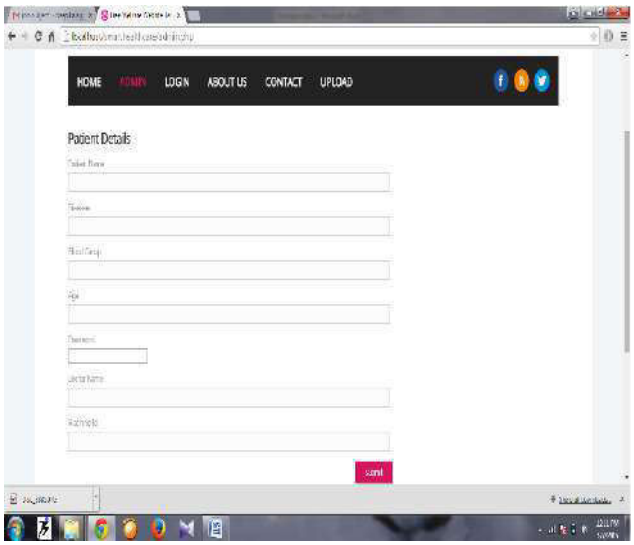

Fig.3 System Web Portal Admin Page

The Admin page of the web portal allows the user to enter his/her personal details including his name, age, blood group and various others important details in order to maintain the records systematically.

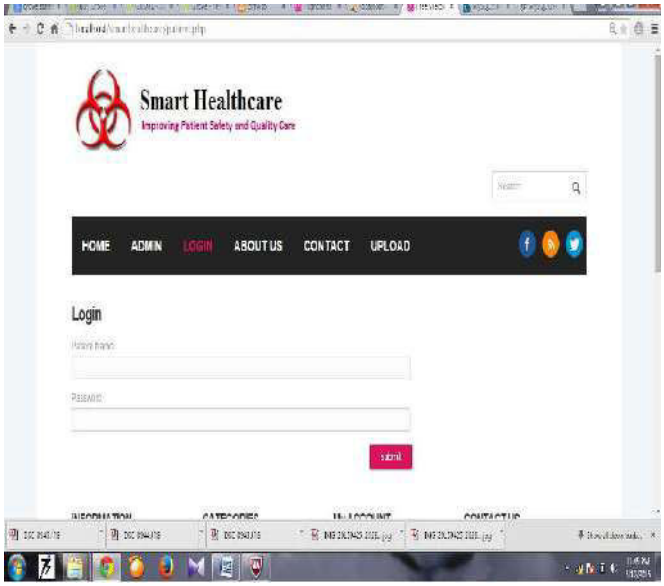

Fig.4 System Web Portal Login Page

In the Login tab, the user can login into the web portal as a patient or as the doctor as per the credentials given.

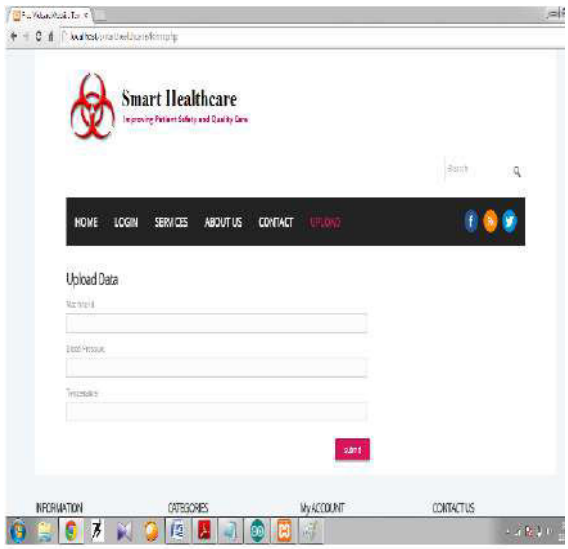

Fig.5 System Web Portal Data Tab

The data which are collected from various sensors are being uploaded into the database server from which the data is further used to plot graphs and analyse the health reports of the patients. This data is uploaded into the database server from which the data is further used to plot graphs and analyse the health reports of the patients. Fig.7. shows the full structure of the database which is being hosted currently on the local host and further can be connected to the whole world via IOT. The database has full details and record history of each and every patient through which a statistical graph is plotted in real time which is used for patients further analysis and tracking. The model is finally developed over a normal fit person and his heart rate and temperature details are plotted on a real time graph.

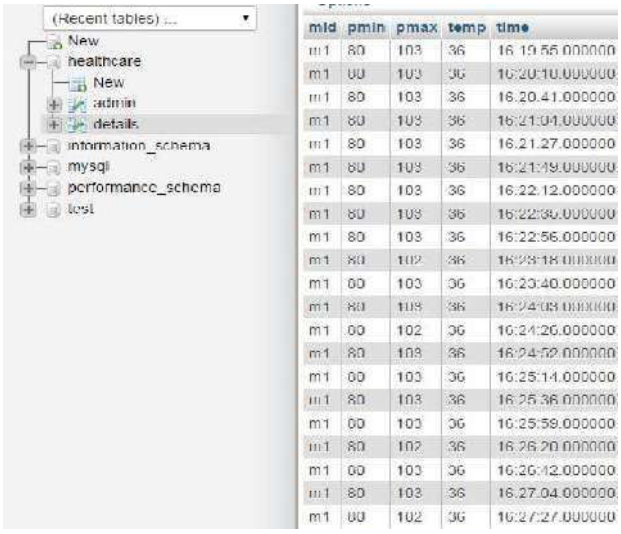

Fig. 6 System Web Portal Uploading Data

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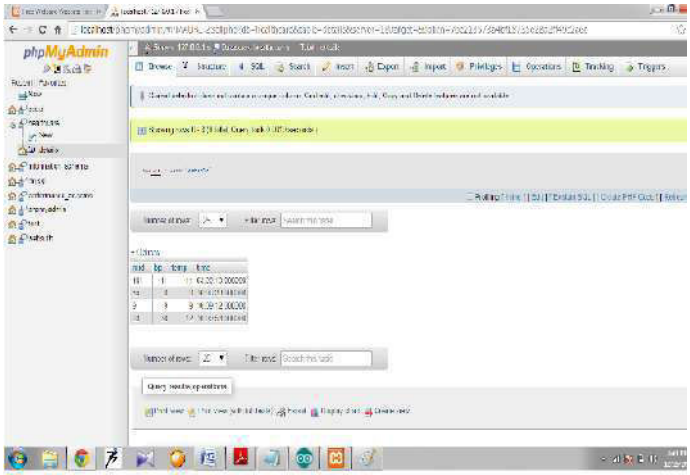

Fig.7 System Web Portal Database Server

. An example output of a proposed health monitor device is shown in which the patient's personal details are shown and alongside her live heart rate and body temperature is being traced in real time.

Fig. 8 An Example Health Monitor graph

V. CONCLUSION

The main idea of this system is to provide better and efficient health services FOR the patients by implementing a networked information cloud so that the experts and doctors could make use of this data and provide a fast and an efficient solution. The final model will be well equipped with the features where the doctor can examine his patient from anywhere and anytime. Emergency scenario to send an emergency mail or message to the doctor with patient's current status and full medical information can also be worked on. The proposed model can also be deployed as a mobile app so that the model becomes more mobile and easy to access anywhere across the globe.

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AUTOMATA IMPLEMENTATION OF NOVEL FLIPFLOPS USING QUANTUM DOT CELLULAR

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Abstract: As the device dimension is shrinking day by day the CMOS technology faces serious problems due to physical barriers of the technology such as ultra-thin gate oxides, short channel effects, leakage currents and excessive power dissipation at Nano scale regimes. Quantum Dot Cellular Automata is an alternate quantum phenomenon that provides a completely different computational platform to design digital logic circuits using quantum dots confined in the potential well to effectively process and transfer information at Nano level. This paper has demonstrated the implementation of circuits like D, T, SR, JK flip flops using a derived expression from SR flip flop. The kink energy and energy dissipation has been calculated to determine the robustness of the designed flip flop. The simulation results have been verified using QCA Designer simulation tool.

Keyword: QCA, SR Flip flop, JK Flip flop, D Flip flop, T Flip flop,

1.INTRODUCTION

The conventional CMOS based devices advanced from micron to submicron, submicron to deep submicron and to nanometer regime over last few decades. The scaling of CMOS devices at Nano scale affects the performance of several factors like heat dissipation and leakage currents. The heat generated can no longer dissipate and results in damage of the chips as more and more devices are packed into the same area. Among several other alternatives, Quantum Dot Cellular Automata (QCA) is a revolutionary promising transistor less quantum paradigm that performs computation and routing information at Nano domain. The unique feature of QCA is that logic states are represented by a cell. A cell is a Nano scale device capable of transferring data by two state electron configurations. The advantages of QCA over conventional CMOS technology include lesser delay, high density circuits and low power consumption which permits us to perform quantum computing in future.

II. Literature Survey:

II.I. Quantum Dot Cellular Automata (QCA):

The basic logic unit of QCA is based on QCA cells which contain four quantum dots arranged in a square pattern. Each cell contains two mobile electrons which can tunnel quantum mechanically between dots. Due to the columbic repulsion, the electrons in quantum dots confined I the potential well always try to occupy the two possible diametrically opposite positions of a square shaped call. QCA connects the state of one cell to the state of its immediate cells by columbic interaction. The state of a cell is called its polarization defined by P. Therefore, two distinct cell states exist. The below shows the two possible minimum energy states of a quantum dot cell.

Logic 0 has polarization P=-1
Logic 1 has polarization P=1.

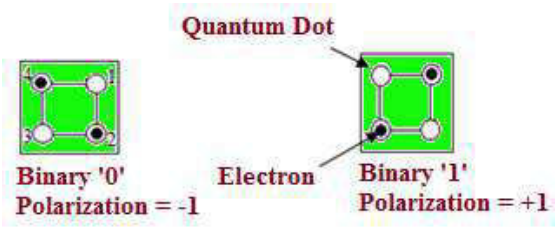

Figure 1: Schematic of QCA cell

A polarization P in a cell is defined by:
P=[(p1+ps3) -(p2+p4)]/p1+p2+p3+p4
There are mainly two types of quantum cell orientations namely 45 and 90 degrees are logic 0 and logic 1.

In order to transfer information from one cell to another cell QCA wire is used which is shown below.

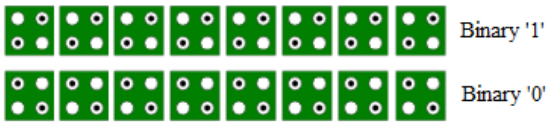

Figure 2: 90-degree QCA wire

Clock is used to overcome the tunneling barriers between the adjacent quantum dots confined in the potential well within a cell for transfer of information from one clock to next clock sequentially. There are two types of clocking zone clocking and continuous clocking. QCA Designer tool support zone clocking. In zone clocking, each QCA cell is clocked using a four-phase clocking scheme. The four phases correspond to switch, hold, release and relax is shown Fig. 3.

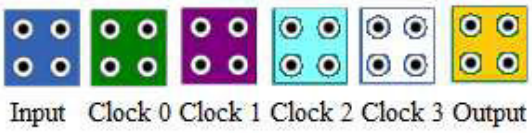

Fig.3. Transfer of Information through Clocking

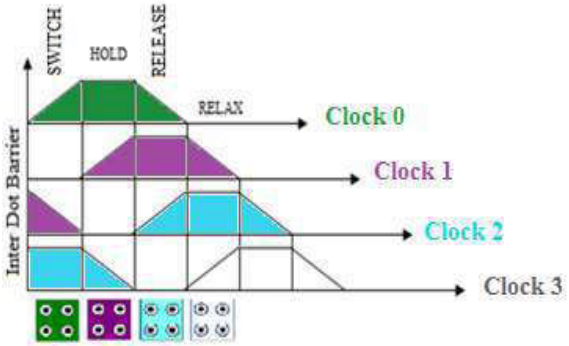

Fig. 4.

II.II. MAJORITY GATE

The fundamental structure of majority gate contains minimum five QCA cells to represent it. Four of them are in four different directions making themselves at the angle of 90-degree with the nearest neighbouring cells on the substrate and there is one cell which is in the middle of them. The Boolean expression of majority gate is-

$$M(A, B, P) = A.B.\bar{P} + A.P + B.P$$

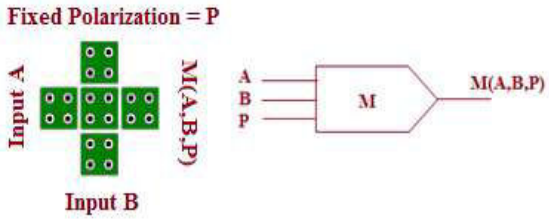

Fig.5. Majority Gate in QCA

Where the first two terms A and B represent the inputs from the majority gate and P is the fixed polarisation. This polarisation P will vary according to the gate we want to use. For the case of AND gate P = ”0’’ and OR gate P= ”1”.

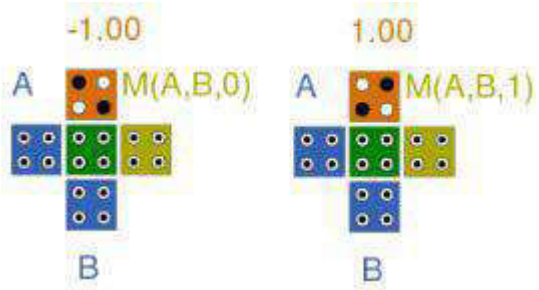

Fig.6. The fundamental structure of QCA majority gate-

(a) 2-input AND gate (b) 2- input OR gate

III. Proposed Expression to Design All Flip-flops

Using the derived expression in equation 1 and equation 2,we can simply construct any flip-flop in a much easier way just by modifying the inputs. All the flip-flopshave been designed in this paper using the circuit as shown below. The simulation results are verified by the truth table1.

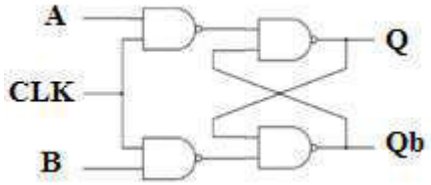

Fig.7. flipflop design using NAND gate

TABLE1:TRUTH TABLE

INPUT			OUTPUT	
CLK	A	B	Q	Qb
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

Equation1 and 2 are derivedare used for the design of the other flip flops. The design of SR, D,T,JK flipflops are realised using QCA simulation tool in this paper.

$Qb = B.CLK.Q = B.CLK + Q$…….(1)
(Where,Qb is the inverse ofQ)
and $Q = A.CLK.Qb = A.CLK + Qb$
$= A.CLK + B.CLK.Q$…….(2)

III.I. SR Flip Flop

The SR flipflop has two inputs, SET(S) and RESET(R), and two outputs Qand Qbar .We have simply replaced Aby S and B by R from our proposed equation.

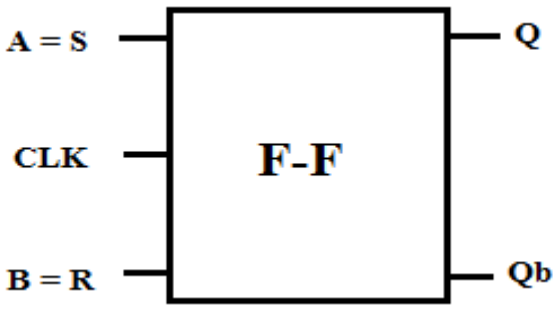

Fig.8 (a) Block diagram of SR flip-flop from the proposed design,

III.II. D Flip flop

The D flip-flop as it introduces a delay between input and output. We have simply replaced A by D and B by Dbar.

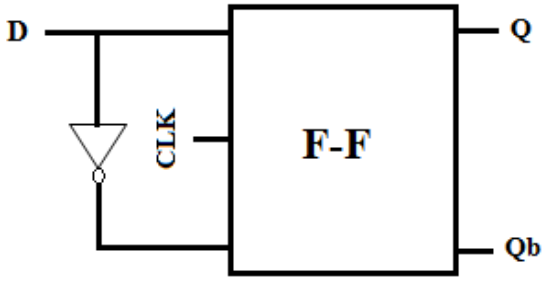

Fig.9. (a) Block diagram of D- flip-flop from the proposed design

III.III. JK FLIP-FLOP

The limitation of SR flip-flop is overcome in JK flip-flop. The inputs J and k behave as inputs S and R to set and reset the flip-flop. When J=K=1, the output toggles i.e. switches to its complement state. A JK flip-flop is obtained from our proposed expression by adding two additional AND gates.

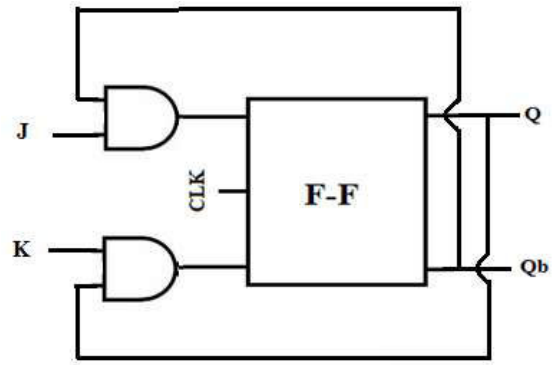

Fig. 10 (a) Block diagram of JK flip-flop from the proposed design,

III.IV T FLIP-FLOP

Flip flop, called T or trigger or toggle flip-flop has only a single data (T) input, a clock input Another and two outputs Q and Qbar. The T-type is designed by connecting J-K inputs together and is called single input JK flip-flop.

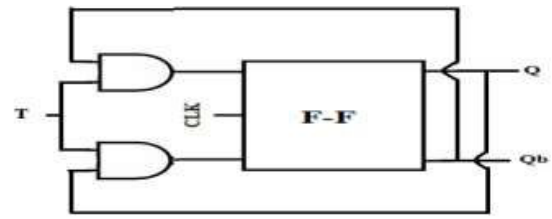

Fig.11. (a) block diagram of T flip-flop

IV. COMPLEXITY OF THE PROPOSED FLIP-FLOPS

In this paper we show the calculations of Cell Count, AUF, O-Cost & Latency of the designed FLIP-FLOPS as shown in table2.

QCA Structure	Length covered (nm)	Width covered(nm)	Cell count (cells)
SR flip-flop	258	158	38
D flip-flop	238	178	43
T flip-flop	258	258	81
JK flip-flop	278	258	78

QCA Structure	Operation cost(o-cost)	Net area (nm2)	Total area (L* W) (nm 2)	Area utilization factor (AUF= net area/total area)	Latency
SR flip-flop	38	12,312	40,764	0.302	1.50
D flip-flop	43	13,932	42,364	0.328	1.25
T flip-flop	81	26,244	66,564	0.394	1.50
JK flip-flop	78	25,272	71,724	0.352	1.50

V. Experimental Results:

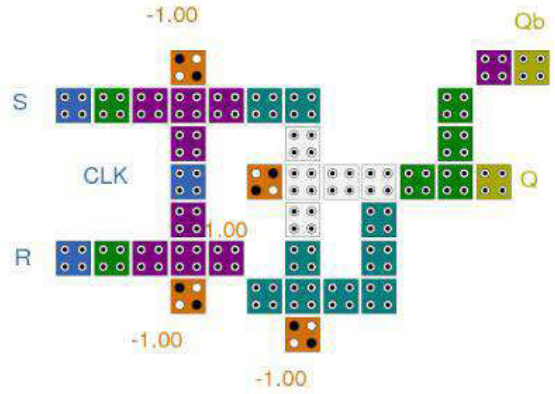

Fig. 8. (b) Layout of SR flip-flop

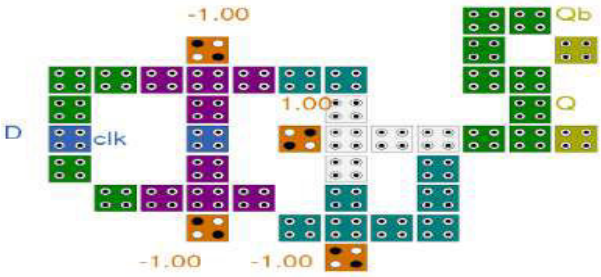

Fig. 9 (b) layout of D- Flip Flop

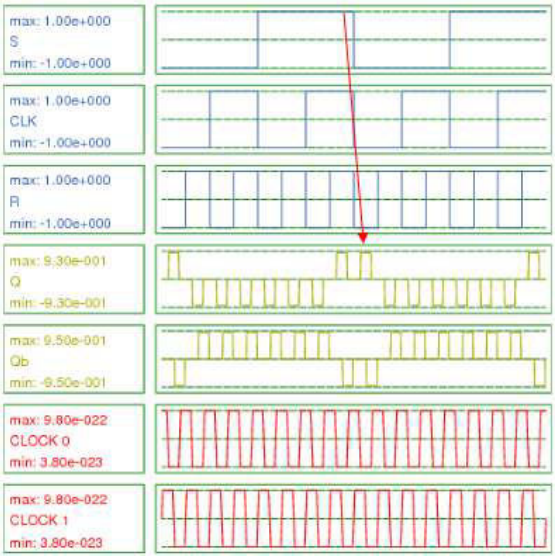

Fig. 8 (c) Simulation result of SR flip-flop

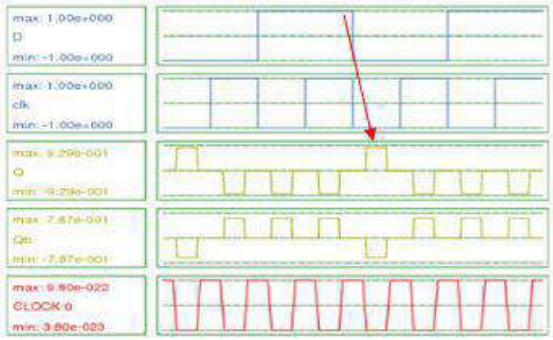

Fig. 9 (c) Simulation result of D flip-flop

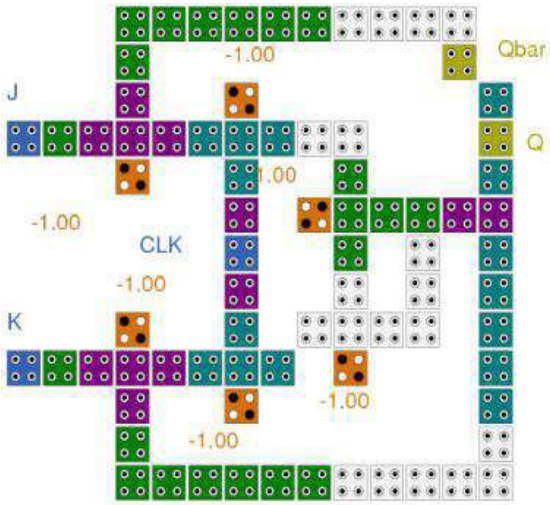

Fig. 10. (b) Layout of JK flip-flop

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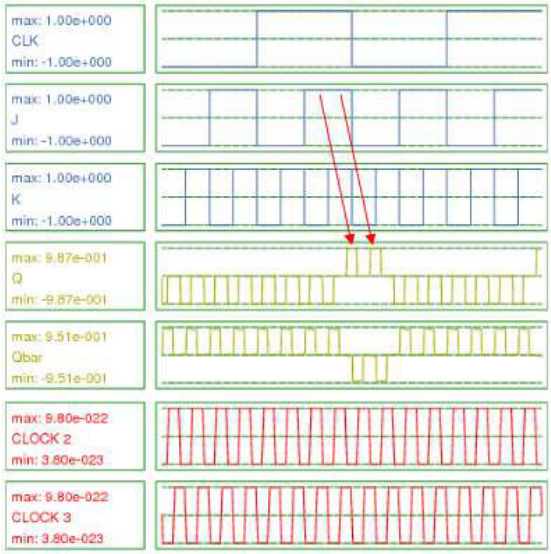
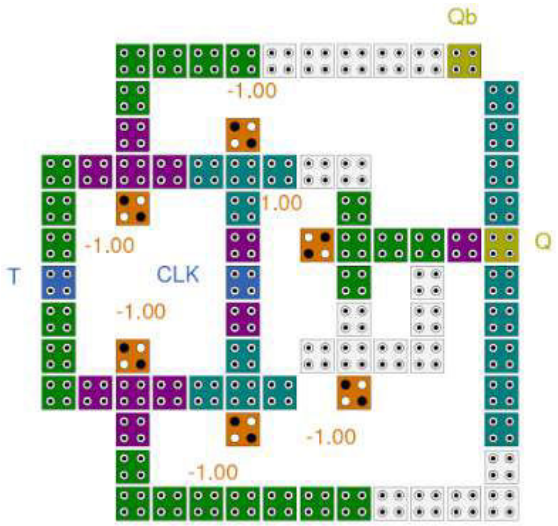


Fig. 10 (c) Simulation result of JK flip-flop



FiFig.11. (b) layout of T- Flip Flop

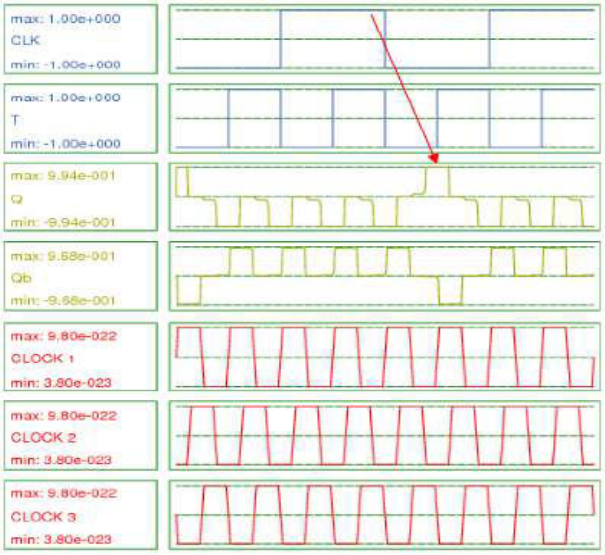


Fig. 11 (c) Simulation result of T flip-flop

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BOOKING SYSTEM OF A VEHICHLE PARK USING IOT TECHNOLOGY

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Abstract – we provide a system for parking reservations and security, maintenance during a exceedingly in a very non-public automobile parking field in an urban metropolis. Our system style is employed to eliminate surplus time conception to search out Associate in nursing empty extract a automobile parking field. By identical sheath, we will conjointly save over seventy five to eighty five % of fuel wastage in an exceedingly automobile lot to check the empty parking slot. The reservation processes square measure happening solely by the user. Therefore the user visit lot exploitation Associate in Nursing humanoid application through an online access and notice the empty parking slot and a reserve parking slot as per their preference. Here we tend to gift the main response to user's reservation action and therefore the driving force will put aside his own seemingly parking slot supported the time and price perform. We've projected a system with multi-processing queuing mechanism (MPQM) to avoid multi-user approach downside (MUAP) throughout the reservation procedure in our perceptive automobile parking booking arrangement supported IOT technology.

Key Words: android Application, android Studio, Arduino UNO, internet of Things, Multi-User Approach process (MUAP), QR Code, un hearable sensing element.

1. INTRODUCTION

Now a day's congestion of traffic will increase chop-chop with the increasing growth of population. With relevance the amount of population the usage of cars conjointly exaggerated. Thanks to a lot of usage of automobile the tie up occurred on the road. as a result of the finding of free parking slot takes longer. Hence, we tend to lose a particular amount of your time and created over seventy five to eighty five % of fuel wastage to search out the empty parking extract lot. to resolve this downside, we want a special system within the lot to live empty area and show the knowledge to the folks that searching for the empty area. However, many systems designed antecedently to avoid time wastage in automobile lot.

In the sensible parking allocation and reservation system, a system itself allocates the automobile parking space for each user [1]

[2]. In this, the system observes the gap between the user and parking areas with the assistance of world positioning system [1]. With this distance mensuration the system calculates the typical time conception for the user getting into the automobile parking space [1]. Then the system allocates the suitable parking slot for the user [1] [3]. Therefore the user could or might not be accepted the allotted automobile parking space [1]. If once the user accepts allotted slot, then the user will able to modification his parking slot [1] [4]. In our system all the user will able to reserve own seemingly parking spot. therefore there's no restriction between the slot reservation, and user request. Here the user reserves his spot with respect the system framework represented. Here every step of the reservation method is differentiated by DLSM. MUAP is avoided by special queuing method (MPQM) with the embedded method management unit (EPCU) in our sensible automobile parking system [1].

1.1 LITERATURE SURVEY

V. Venkateswaran, N. Prakash, and IJRET [1]: during this paper, they introduce a special system for sensible parking reservations Associate in Nursingd security maintenance in an exceedingly industrial automobile lot in urban surroundings. Here they furnish the main response to user's reservation action and therefore the driving force will reserve his own seemingly parking slot supported the price perform. rather than economical automobile parking we want a special security choices to create our vehicle terribly safe. By this case they need provided a higher security steerage of barrier gate management security system; with the assistance of embedded method management unit (EPCU). There square measure several steps taken to create a reservation with completely different lighting theme mechanism (DLSM).

Amir O. Kotb, Yao-Chun Shen, Xu Zhu, Senior Member, IEEE, and Yi Huang, Senior Member, IEEE [2]: during this paper, they introduce a brand new sensible parking system that's supported intelligent resource allocation, reservation, and rating. The projected system solves this parking issues by providing secure parking reservations with the bottom potential price and looking time for drivers and therefore the highest revenue and resource utilization for parking managers.

Yanfeng Geng, Student Member, IEEE, and Christos G. Cassandras, Fellow, IEEE [3]: during this paper the system assigns Associate in Nursingd reserves an optimum automobile parking space supported the driver's price perform that mixes proximity to destination and parking price.

Sheelarani, S. Preethi Anand, S. Shamili and K. Sruthi [4]: during this paper, they projected a wise parking application, wherever users are able to park their vehicles by

finding Associate in Nursing empty automobile parking space through humanoid Application or will even park their vehicles directly through Embedded Hardware. Associate in Nursing Intelligent Parking System is enforced supported Slot Allotment.

Hongwei Wang and Wenbo He [5]: during this paper they we tend to style and implement a image of Reservation-based sensible Parking System (RSPS); that permits drivers to effectively notice and reserve the vacant parking areas. By sporadically learning the parking standing from the sensing element networks deployed in parking tons, the reservation service is affected by the modification of physical parking standing. The drivers will access this cyber-physical system with their personal communication devices.

2. PROJECTED WORK

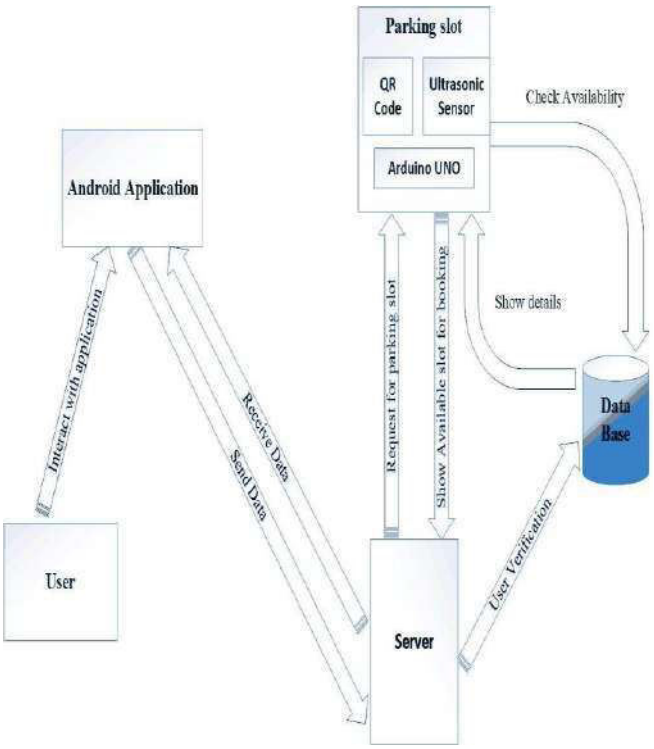

Fig 1: Parking Reservation System style diagram

We square measure progressing to style a system that consists of various modules like server, database, user application and parking slot arrangement. we offer Associate in Nursing humanoid application to user owing to consistent with Google there square measure one.4 billion active humanoid devices over worldwide. A user should 1st transfer the humanoid application in his humanoid movable. when user should go just one time for registration with specific id (using AADHAR CARD no. or License no.) exploitation the applying. Then registered user info is distributed to the server system and knowledge keep within the information. The parking slot info is additionally keep within the information that is usually updated, and server manages and update this info and keep causation notification to the user when parking slot booking. User will use humanoid application to book specific parking slot at desired area. once user book specific slot, then the server generates QR code and send to the user (Android Application) and therefore the information through server system. With the assistance of QR code user are accessing specific reserved parking slot and park the automobile. At the parking slot there's a mechanism wherever we tend to use Arduino UNO and un hearable sensing element. Arduino is employed for managing un hearable sensing element and entry gate. The un hearable sensing element is beneficial for detective work the automobile position. once user can scan QR code at the parking slot that point user are charged or pay money for a time length that is user already mention at the slot booking time through humanoid application. In such vital condition or in some new modification is needed for parking system we offer an online website for the Admin user. Admin will manage parking locations and user information through the web site. this method style is incredibly easy, effective, eco-friendly and user friendly.

Arduino UNO R3: The Arduino UNO R3 could be a microcontroller board supported the ATmega328 (data-sheet). it's fourteen digital input/output pins (of that half-dozen is used as PWM outputs), half-dozen analog inputs, a sixteen MHz quartz oscillator, a USB affiliation, an influence jack, Associate in Nursing ICSP header, and a button [6]. we tend to square measure exploitation Arduino UNO R3 for dominant entry gate (motor) and unhearable sensing element.

Android: humanoid could be a mobile software package developed by Google, supported the UNIX system kernel and designed primarily for bit screen mobile devices like sensible phones and tablets. As of could 2017, humanoid has 2 billion monthly active users, and it's the most important put in base of any software package [7]. Hence, we've determined to make Associate in Nursing humanoid application that is employed for interacting with user and booking parking slot for a particular time length.

Android Studio: humanoid Studio is that the official integrated development surroundings (IDE) for Google's humanoid software package, engineered on Jet Brains' IntelliJ plan code and designed specifically for humanoid development [8]. we tend to use humanoid Studio to make Associate in Nursing humanoid Application.

Apache Felis catus: Apache Tomcat implements many Java EE specifications, as well as Java Servlets, Java Server Pages (JSP), Java EL, and net Socket, and provides a "pure Java" protocol net server surroundings during which Java code will run [9].

Ultrasonic Sensor: It emits Associate in Nursing ultrasound at forty 000 cps, that moves through the air Associate in Nursingd if there's an object or obstacle in its path it'll rebound back to the module [10]. This unbearable sensing element is employed for detective work the automobile distance from the entry gate.

Quick Response (QR) Code: A QR Code could be a two-dimensional barcode that's legible by smart phones. It

permits to write in code over 4000 characters in an exceedingly two-dimensional barcode. "QR Code" could be a registered trademark of DENSO WAVE INCORPORATED [11]. we tend to square measure exploitation QR code for identification of a legitimate user at the time of user enter the parking slot.

3. FINAL RESULT WITH DESIGN

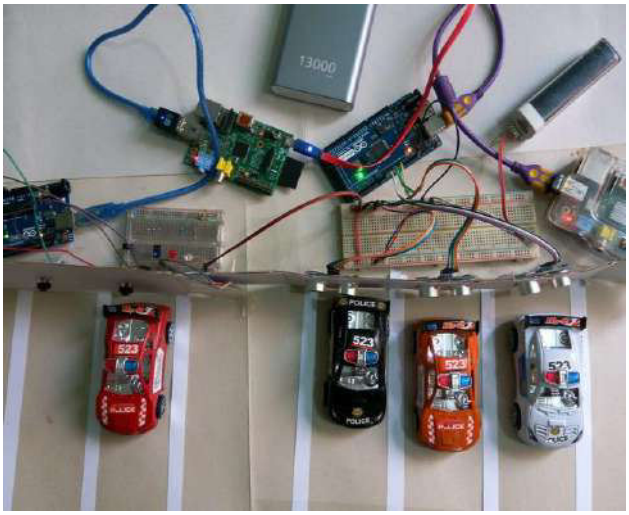

Fig2.final project design

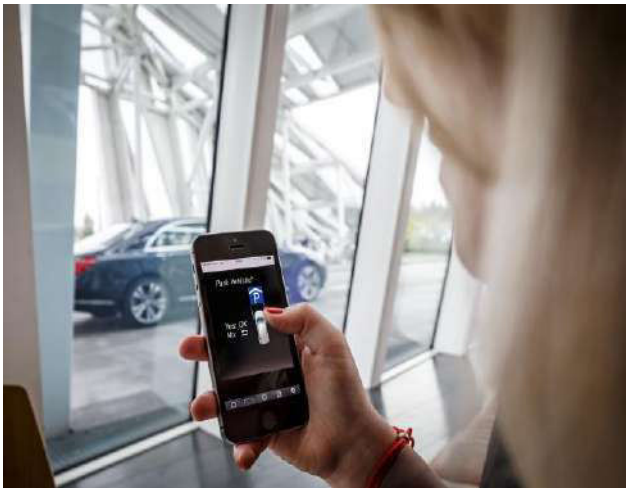

Fig3.parking information on mobile for booking vehicle slot

We can verify the parking slots with the help of mobile app

4. CONCLUSIONS

We have steered a wise automobile parking arrangement to achieve light and economical usage of automobile lot. Basically, this method work consistently detects the non-reserved parking slot and updates the info in server aspect exploitation website that is meant for the distinct lot. the typical time consumption for update the knowledge is incredibly but former systems. we tend to uprise a good parking reservation system wherever the user will reserve their slot exploitation their humanoid application or with the help of Associate in Nursing embedded hardware. this method is economical and helpful in metropolitan cities. this method is applied to avoid dense traffic within the parking areas like looking malls, theaters, traveller spots and different busy areas, thereby cutting time and therefore the use of the fuel and contamination.

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[10] http://howtomechatronics.com/tutorials/arduino/ultrasonic-sensor-hc-sr04/

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THE DEVELOPMENT OF A REMOTELY CONTROLLED HOME AUTOMATION SYSTEM FOR ENERGY SAVING

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ABSTRACT

The purpose of this study is to showcase the design and development of a web-enabled home automation system prototype. The unit was developed using low-cost components such as the ubiquitous Arduino microcontroller. One of the features of the developed unit is the ability to monitor the power consumed by electrical loads. The unit also has the ability to control the status of individual loads through the internet using a web-enabled mobile application. This feature enables load management that could contribute to energy saving.

1. INTRODUCTION

The aim of this project is focused on the development of a prototype for an internet based home automation system. The focus is to establish a platform that allows communication between the web-enabled mobile application and the microcontroller situated at a remote location anywhere in the world.

1.1 BACKGROUND

Over the year's humans have learned to rely on technology, the use of technology has thus developed tremendously over the years. This is evident in the telecommunication stream, previously communication was done face to face or through the postcard or letter. In some cultures, it was tradition to play the drum as a form of communication to warn, invite or express a celebration in the neighboring villages. However, today communication takes place relatively fast, easier and without a lot of hassles through the usage of cell phones. A cell phone's function is not limited to calling and texting; it can be used for various functions. Cell phones have become a necessity in people lives, communication and entertainment are all possible with the smartphones.

Automation is the backbone of modern industries, it is the key to global economic growth as it allows for increasing productivity and accuracy by cutting out the human intervention while reducing costs.

Home automation is the extension of industrial process automation to households' appliances. Among others home automation may include the remote control of lights (Centralized or individual), air conditioning, security system (remote power monitoring) and other systems such as those used for entertainment. Home automation provides improved comfort and security, increases energy efficiency and convenience for users.

Today automation is introduced in homes through the connectivity of house appliances and smartphones, tablets, and PCs.

1.2 PROBLEM STATEMENT

Energy consumption can be measured through its environmental impact and usage; the measure of the amount of power consumed by the load side of an electrical circuit is termed energy consumption. The maximum power that a load can consume is equal to the total power generated by the source minus the power lost in the transmission line. When the load requires more energy than what the source can provide, this becomes a major issue, which results in load shedding and blackouts. Energy consumption is a major issue in the modern world. Inefficient power monitoring and controlling techniques in the households, businesses, and institutions are the main cause of power consumption.

1.3 LITERATURE REVIEW

A home automation system is a channel by which homeowners and occupants have remote control over different types of electrical and electronics appliances in their home.

The home automation system is the use of robotics and computer technologies to household appliances by defining the home automation as domestics. Energy saving is the advantage that a home automation system gives to all its clients and especially forgetful ones, in that they can now track energy usage at home or while being away to ensure that unnecessary appliances are turned off as needed to reduce energy consumption [1, 2, 3].

Convenience is what makes the internet based home automation interesting in that one does not have to go home and turn ON the geyser and wait for the water to get warm, while still at work one can turn ON the geyser to ensure that once they're home the water is warm enough and ready to be used. This saves time and it is very convenient. While security issues arise, the emphasis is that through surveillance cameras a user can remotely monitor the house. This should monitor incidents of property intrusion. With the home entertainment section, a user can control the distribution of sound throughout the house depending on the room occupancy or control light intensity from the couch while watching an interesting movie.

With an increase in energy consumption and population, there is an inevitable need to conserve energy with the means possible. The major cause of energy consumption is the inability to remotely monitor and control appliances.

The literature found that all authors that web-enabled mobile application used to monitor and control appliances remotely can greatly increase efficient energy usage. While [4] mentioned only two communication protocols (Z-Wave and ZigBee), [5] and
[6] speaks about ZigBee, Bluetooth, GSM, and Wi-Fi as possible communication methods that a home automation system can host. To implement the home automation system, [6] in their study present interesting methods that could be used. These methods include phone-based home automation system, Bluetooth-based home automation system, GSM based home automation system, Mixed type home automation system, a wireless control system and ZigBee-based home automation system. The GSM based home automation presented by [4] consists of User with an APP inventor user interface, a GSM network, a GSM modem, an Arduino microcontroller, peripheral devices, relay logics and the appliances to be controlled. The system presented here can be controlled by means of a GSM network, internet, or speech control. Then internet being the best of choice as it enables the system to be controlled from anywhere in the world, then GSM uses SMS-based commands to control the appliances. The user sends text commands to the server which might be a PC, the server then passes the commands to the Control Unit which in turn controls the appliances. The GSM is used for communication where there is no internet connectivity. The AT (Attention) command are use used by the server to communicate with the GSM modem. The server consists of a web server, database, main control program and speech recognition says the Satish et al. Every appliance node consists of a transmitter, a receiver an I/O device and a controlling unit (Microcontroller). The GSM is used for its high availability, coverage, and security, but it suffers from the SMS costs and the relative dependency of the SMS on the network. Another drawback of GSM based system is that no user interface is given to the user to control the device. The system cannot be customized on devices as it comes preprogramed.

The study of [4] described different technologies and home automation systems, the authors focused on describing home automation system based on a security point of view in their study. [7] elaborates on various security weaknesses in existing home automation systems. The challenges in the home automation systems were examined. In their study, [5] considered mobile based home automation, Bluetooth-based home automation system, Dual Tone Multi-Frequency based home automation systems, and internet based home automation system, Short Messaging Service based home automation system. Since the goals of this project aimed an internet-based system, the focus was more on the internet based home automation system and a mobile based home automation system.

Figure 1 presents the diagram of how the sensors, mechanical and electrical devices communicate using the home network through GSM module using a subscriber identity module (SIM). This uses a transducer to convert machine's function into an electrical signal readable by a microcontroller. The signals sent to the microcontroller are analysed, and based on this analysis the microcontroller commands the GSM module to select between one of the three communication methods mentioned above (SMS, GPRS or DTMF) [4].

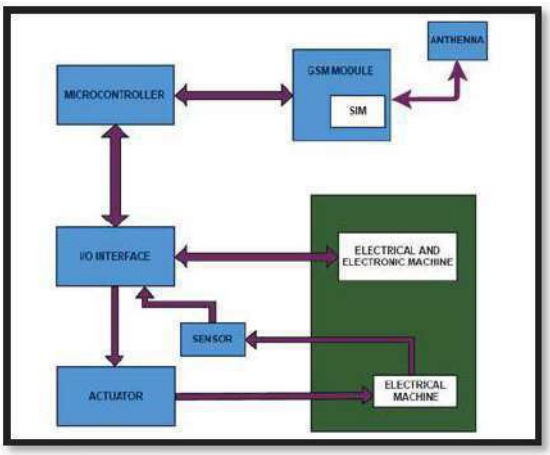

Figure 1: Mobile-based home automation

In this study, the focus was on developing the application to interact with the home automation system, the security issues were only flashlights to consider before marketing the product. Given the time constraints, the focus was first on the minimum deliverables and as time went on, more features were added to the system to make it more interesting that includes a security feature which prompts the users to authenticate themselves before loading the application.

As the literature reveals, a microcontroller is the most popular and most flexible controlling unit used for home automation system. In this project, Microcontroller Systems Design IV was the main subject that helped with implementation. There are currently many challenges that home automation systems have to address. Some of these are reviewed in [7]. In [8] a life cycle assessment is provided for by considering both the benefits and environmental impacts of home automation systems.

2. SYSTEM DESIGN

Home automation can be implemented in several ways, there are many possible approaches towards the development of the mobile application and the home automation. In this section, some pertinent approaches were presented together with their advantages and disadvantages. Many factors affect the advantage and disadvantage of a home automation system such as the security, implementation, timeline, cost, the complexity of the system, availability of the component, documentation, and support offered by the manufacturers to list a few. In this section, the focus will be on the security, implementation, and cost while evaluating different approaches. Decentralized home automation system, DTMF Based, GPRS Based, Central controller Based, Mixed Type Home Automation, Internet Based Home

Automation System, Wireless Control System, Phone-Based Home Automation, Bluetooth Based Home Automation, ZigBee Based Home Automation, and GSM Based Home Automation. From this list of home automation system implementation methods, the internet based on a microcontroller as a controlling unit were the choice and the focus of this project.

2.1 INTERNET BASED HOME AUTOMATION SYSTEM

A microcontroller is a self-contained system with peripherals, memory and a processor that can be used as an embedded system. Most programmable microcontrollers used today are embedded in other consumer products or machinery including phones, automobiles and household appliances or computer systems. Due to that, another name for a microcontroller is "embedded controller." Some embedded systems are more sophisticated, while others have minimal requirements for memory and programming length and a low software complexity. Input and output devices include solenoids, LCD displays, relays, switches, and sensors for data like humidity, temperature or light intensity or power usage.

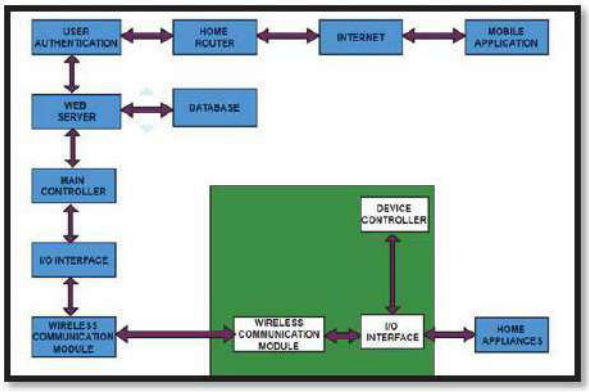

Figure 2: An Internet-based home automation system [4]

Figure 3 below shows a microcontroller based home automation system. The user mobile application interacts with the microcontroller via the web server using the internet protocol. The microcontroller receives commands from the user interface and performs the required tasks based on a controlling algorithm governing the controller. The controller reads devices status and updates this data into the server for the user mobile application. Also, refer to figure 4 in the literature review for a typical internet based home automation system.

The server handles the users and ensures secure communication between the user mobile application and the controlling unit. Once a user is identified, he will then be allowed access to the controlling interface (Web page).

The advantages of using a microcontroller have reduced the size of circuitry, affordability, and increased flexibility. A microcontroller can be used as a substitute for other integrated circuits (ICs). It can also be easily reprogrammed to modify its functionality. The Microcontroller that was used for this project is the Arduino MEGA 2560 R3.

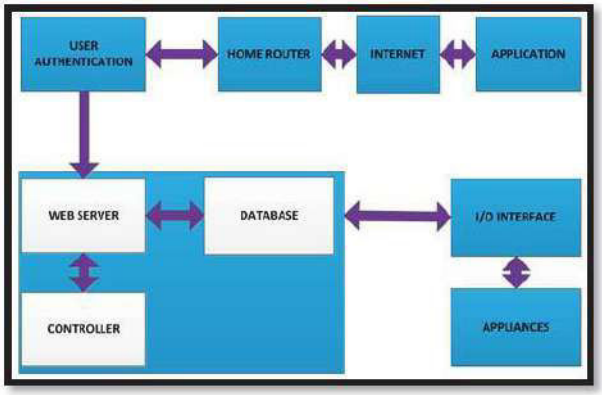

Figure 3: Proposed Home automation (Internet Based home automation with microcontroller)

The downside of this system is its dependency on the mobile connectivity to the internet, if the mobile connectivity is compromised, the user will be unable to remotely monitor and control the home automation system and the limited number of devices depends on the I/O limit of the microcontroller used. A PLC could also be used as a controller for such a system, the PLC is more robust than the microcontroller. The choice of microcontroller controller over the PLC is the cost, and the PLC is not open source, thus making the Arduino microcontroller even the best choice for the system prototyping.

3. DESIGN METHODOLOGY

3.1 THE WEBSITE

When related web pages are collected (Including picture and video contents), and if they can be accessed through the same domain name or IP address, and they are published on at least one web server, then the collection is called website. A website as mentioned can be accessed through the World Wide Web (Internet), or on a local area network (LAN) by referencing a Uniform Resource Locator (URL) which is the ID of the website.

Web sites are created for many reasons, ranging from entertainment to education, and today websites can be used to control household appliances. An Arduino web server was used to serve as the user interface where the client is presented with user clickable buttons to control the house appliances and monitor the power consumption.

The web page as shown in the figure 9 below is made of two important sections, the energy monitoring section, and the control section. The power gauge was designed using java scripts when the “read power” button is clicked, an http request is generated and sent to the web server requiring the power consumption. The server then responds to the request by supplying the web client with the raw reading on the current sensor.

The controlling section of the user interface consists of buttons, and once clicked they each send a corresponding request to the server, then the server in return turns ON/OFF the appliances associated with the request. The server also updates the web client with corresponding images of the appliance status.

The website was created using HTML, XML, and Java Scripts. When access is granted to a user, the user interface is now available to turn on or off devices, check power consumption, change camera position, adjust light brightness, and check the status of entrances.

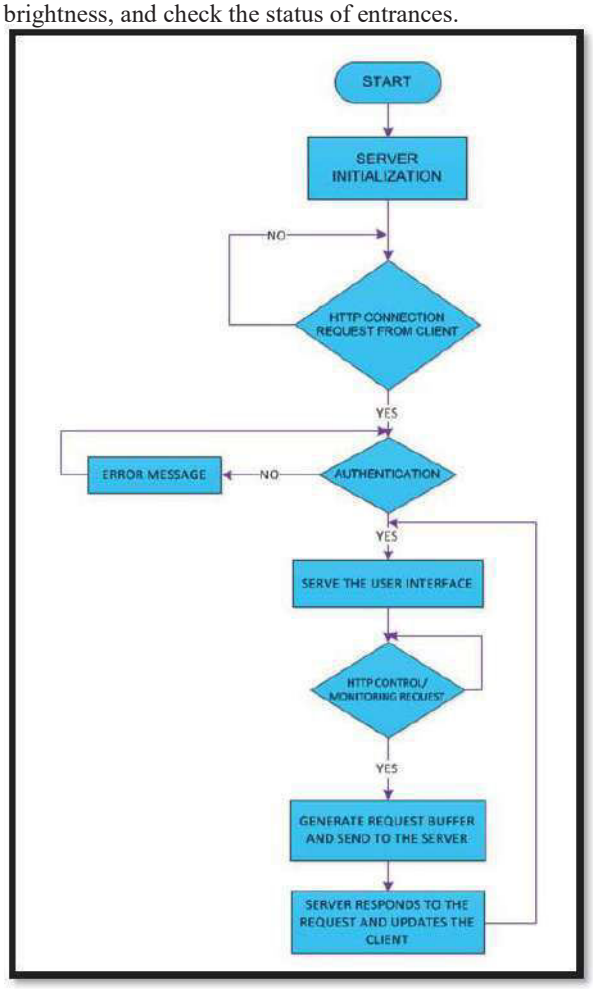

Figure 4: Program Flow-chart

Specific functions are used to generate and send a specific http request to the server depending on the user's request, for instance when the "Read Power" button is clicked, a function called PowerControl is called. This function generates a random number every time is called, it sends a request buffer to the server using the "GET" method. The request buffer consists of a "Get" method, a specific command "Power" and a random number. The random number is used to avoid the browser caching.

To understand the website design, a study of the HTML, XML, CSS, and JS is required.

3.3.1 THE HYPERTEXT MARKUP LANGUAGE (HTML)

The Hypertext Markup Language is a standard used to design the look of the web page. It focuses on the graphic, font, color, and hyperlink effects on web pages, and has for building blocks, elements. HTML describes the structure of web pages using markup, tags representing its elements. The web browsers do not display HTML tags, but instead, tags are used to determine how the web page should be displayed.

3.3.2 THE EXTENSIBLE MARKUP LANGUAGE (XML)

XML stands for Extensible Markup Language. It is a text-based markup language derived from Standard Generalized Markup Language (SGML). XML tags identify the data and are used to store and organize the data, rather than specifying how to display it like HTML tags, which are used to display the data.

3.4 USER INTERFACE (UI)

The user interface interacts a human with a hardware or software, it is the means by which a person controls a hardware device or software application.

The website presents the user with a means to check power consumption, control appliances, camera position and light dimmer control and finally check the status of entrances for intrusion detection. Each section of the user interface is explained as follow:

a. THE WATTMETER

The Wattmeter as shown in figure 5 below, was created using the HTML canvas and Java Scripts, the meter was designed to measure up to 30 kW of power. The green color represents a smiling face on the gauge, meaning that the power consumption is good. The yellow color on the gauge represents power consumption range which the user should start worrying about and make plans to reduce it. The red color represents the range of power consumption at which the system automatically switches off appliances.

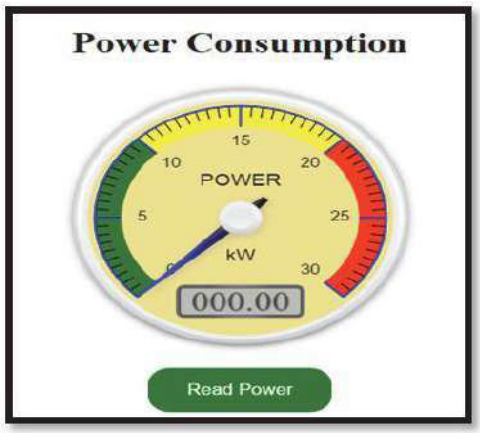

Figure 5: The wattmeter

b. **APPLIANCE CONTROL**

Appliance control as shown in figure 6 below enables a person to turn ON/OFF appliances; a light bulb, a stove, a heater and a tv respectively. The system is designed in such a way that a picture representing the current state of the appliance is updated on the user interface.

Figure 6: Appliance ON/OFF Control

c. CAMERA POSITION AND LIGHT BRIGHTNESS CONTROL

This section of the user interface as shown in figure 7 below presents the user with means to adjust the position of a camera as well as adjust the brightness of a light. The adjustment is accomplished through two sliders.

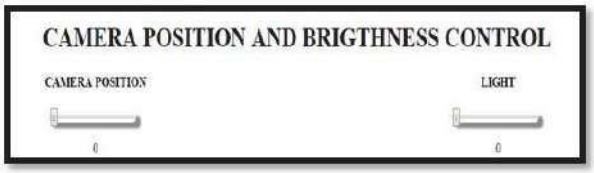

Figure 7: Camera Position and Light Brightness Control **d. INTRUSION DETECTION**

The intrusion detection section of the user interface as shown in figure 8 consists of a "CheckEntrance" button, the entrance names, and the entrance status fields.

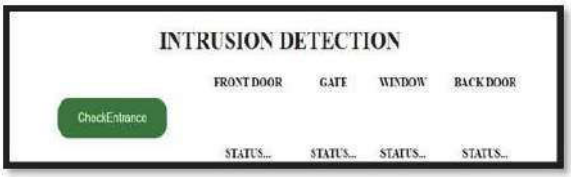

Figure 8: Intrusion Detection

Finally, the complete user interface is a web page that can be accessed via a web browser or using the android web-enabled mobile application created using App Inventor. The android app will be discussed in the next section

3.5 THE WEB SERVER

The web server is a dedicated device or computer or program that uses the Hypertext Transfer Protocol (HTTP) to serve a website to the web client as a response to their request.

In this project, the microcontroller was used to serve the website using HTTP on port 25, and it is also the main controller of the system. The web server and controller is made of an Arduino Mega 2560 R3 (controller which is programmed and manages the overall system), Arduino WiFi R3 shield (Allows the controller to have internet connectivity through WiFi modules), and an SD card (Found the WiFi shield and gives the controller the ability to save files and use them when needed) from which the controller serves the system's user interface.
The microcontroller hosts the website saved in an SD card, the web server when launched, it serves the website to the internet client requesting for it. Once the website which is a user interface is made available to the user, there are now capable of entering their username and password to have access to the overall system.

4. USER INTERFACE

At the completion of this project, the following results were found to be satisfactory and above the minimum deliverables.
It was found in this research that the Arduino UNO does not behave expectedly when the program size is above 56% of its full memory. For this reason, this project's controller was changed to ATmega 2560 to solve the memory issue.

4.1 THE WEB USER INTERFACE

Figure 9 below represent the complete user interface, and as explained in the design procedure.
It was found that the calling a function using the "OnLoad" attribute in the HTML code causes the rest of the functions in the code to not execute, for this reason the power gauge does not update automatically and a button was used for its "OnClick" property.

Figure 9: The Complete Web User Interface

4.2 THE ANDROID APP

The Android app as shown in figure 10 below loads the web interface shown above and provides the user with a means to remotely control home appliances and monitor the power consumption thereof.

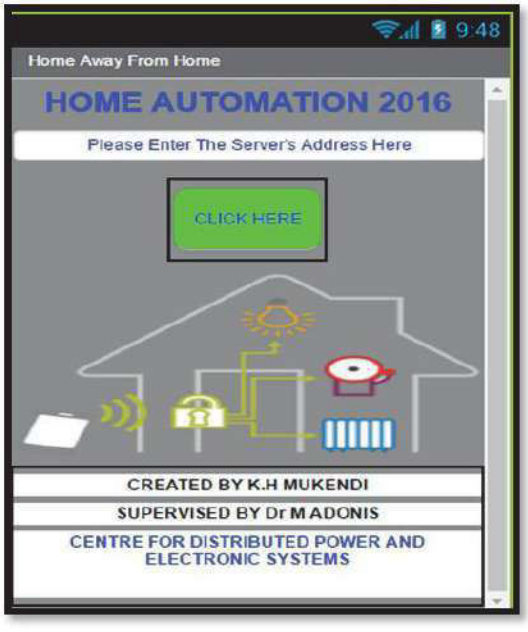

Figure 10: The Mobile Application interface

5. CONCLUSION

The paper summarised the design and development of a web-enabled home automation system. A comprehensive literature review was presented that chronicles the impact and technologies used in home automation systems. The system design methodology is also presented. The mobile application design elements are shown. These highlight the user interface and its monitoring and control features.

Field trials are to be implemented in the next phase. These trials will involve the gathering of experimental data. The results should show what impact the developed unit operation has on reducing energy consumption through load management strategies. The additional features of: camera positioning; light brightness control and intrusion detection, have been evaluated in real-time.

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OPTIMIZING THE CONVOLUTION OPERATION TO ACCELERATE DEEP NEURAL NETWORKS ON FPGA

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ABSTRACT:—**As convolution contributes most operations in convolutional neural network (CNN), the convolution acceleration scheme significantly affects the efficiency and performance of a hardware CNN accelerator. Convolution involves multiply and accumulate operations with four levels of loops, which results in a large design space. Prior works either employ limited loop optimization techniques, e.g., loop unrolling, tiling, and interchange, or only tune some of the design variables after the accelerator architecture and dataflow are already fixed. Without fully studying the convolution loop optimization before the hardware design phase, the resulting accelerator can hardly exploit the data reuse and manage data movement efficiently. This paper overcomes these barriers by quantitatively analyzing and optimizing the design objectives (e.g., memory access) of the CNN accelerator based on multiple design variables. Then, we propose a specific dataflow of hardware CNN acceleration to minimize the data communication while maximizing the resource utilization to achieve high performance. The proposed CNN acceleration scheme and architecture are demonstrated by implementing endto-end CNNs including NiN, VGG-16, and ResNet-50/ResNet152 for inference. For VGG-16 CNN, the overall throughputs achieve 348 GOPS and 715 GOPS on Intel Stratix V and Arria 10 FPGAs, respectively.**

Keywords:—**Accelerator architectures, convolutional neural networks (CNNs), field-programmable gate array (FPGA), neural network hardware.**

I.INTRODUCTION

The field-programmable gate arrays (FPGA) are fast becoming the platform of choice for accelerating the inference phase of deep convolutional neural networks (CNNs). In addition to their conventional advantages of reconfigurability and shorter design time over application-specific integrated circuits (ASICs) [20], [21] to catch up with the rapid evolving of CNNs, FPGA can realize low latency inference with competitive energy efficiency (~10–50 GOP/s/W)

when compared to software implementations on multicore processors with GPUs [10], [12], [13], [17]. This is due to the fact that modern FPGAs allow customization of the architecture and can exploit the availability of hundreds to thousands of on-chip DSP blocks. However, significant challenges remain in mapping CNNs onto FPGAs. The stateof-the-art CNNs require a large number (>1 billion) of computationally intensive task (e.g., matrix multiplications on large numbers), involving a very large number of weights (>50 million) [4], [5]. Deep CNN algorithms have tens to hundreds of layers, with significant differences between layers in terms of sizes and configurations.

More than 90% of the operations in a CNN involve convolutions [2]–[4]. Therefore, it stands to reason that acceleration schemes should focus on the management of parallel computations and the organization of data storage and access across multiple levels of memories, e.g., off-chip dynamic random access memory (DRAM), on-chip memory, and local registers. In CNNs, convolutions are performed by four levels of loops that slide along both kernel and feature maps as shown in Fig. 1. This gives rise to a large design space consisting of various choices for implementing parallelism, sequencing of computations, and partitioning the large data set into smaller chunks to fit into on-chip memory. These problems can be handled by the existing loop optimization techniques [6], [9], such as loop unrolling, tiling, and interchange. Although some CNN accelerators have adopted these techniques [9], [11], [13], [19], the impact of these techniques on design efficiency and performance has not been systematically and sufficiently studied. Without fully studying the loop operations of convolutions, it is difficult to efficiently customize the dataflow and architecture for highthroughput CNN implementations.

```
for (no = 0; no < Nof; no ++)                                          ──► Loop-4
    for (y = 0; y < Noy; y ++)
        for (x = 0; x < Nox; x ++)                                     ──► Loop-3
            for (ni = 0; ni < Nif; ni ++)                              ──► Loop-2
                for (ky = 0; ky < Nky; ky ++)
                    for (kx = 0; kx < Nkx; kx ++)                      ──► Loop-1
                        pixel_L(no; x, y) += pixel_L-1(ni; S × x + kx, S × y + ky) × weight_L-1(ni, no; kx, ky);
    pixel_L (no; x, y) = pixel_L(no; x, y) + bias(no);
```

Fig. 1. Four levels of convolution loops, where *L* denotes the index of convolution layer and S denotes the sliding stride [15].

Specifically, the main contributions of this paper include the following.

1) We provide an in-depth analysis of the three loop optimization techniques for convolution operations and use corresponding design variables to numerically characterize the acceleration scheme.
2) The design objectives of CNN accelerators (e.g., latency, memory) are quantitatively estimated based on the configurations of the design variables.
3) An efficient convolution acceleration strategy and dataflow is proposed aimed at minimizing data communication and memory access.
4) A data router is designed to handle different settings for convolution sliding operations, e.g., strides and zero paddings, especially for highly irregular CNNs.
5) A corresponding hardware architecture is designed that fully utilizes the computing resources for high performance and efficiency, which is uniform and reusable for all the layers.
6) The proposed acceleration scheme and architecture is validated by implementing large-scale deep CNN algorithms, NiN [3], VGG-16 [4], and ResNet-50/ResNet152 [5] for image recognition [1], on two Intel FPGAs. The proposed accelerators achieve end-to-end inference throughput of 715 GOPS on Arria 10 and 348 GOPS on Stratix V, respectively, using a batch size of 1.

II. ACCELERATION OF CONVOLUTION LOOPS

A. General CNN Acceleration System

Recently reported CNN algorithms involve a large amount of data and weights. For them, the on-chip memory is insufficient to store all the data, requiring gigabytes of external memory. Therefore, a typical CNN accelerator consists of three levels of storage hierarchy: 1) external memory; 2) onchip buffers; and 3) registers associated with the processing

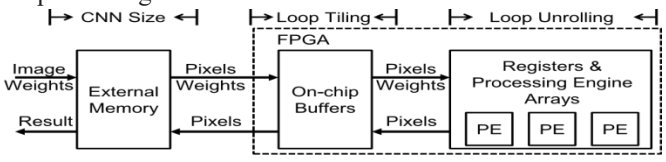

Fig. 2. Three levels of general hardware CNN accelerator hierarchy.

engines (PEs), as shown in Fig. 2. The basic flow is to fetch data from external memory to on-chip buffer, and then feed them into registers and PEs. After the PE computation completes, results are transferred back to on-chip buffers and to the external memory if necessary, which will be used as input to the subsequent layer.

B. Convolution Loops

Convolution is the main operation in CNN algorithms, which involves 3-D multiply-and-accumulate (MAC) operations of input feature maps and kernel weights. Convolution is implemented by four levels of loops as shown in the pseudocodes in Fig. 1 and illustrated in Fig. 3. To efficiently map and perform the convolution loops, three loop optimization techniques [6], [9], namely, loop unrolling, loop tiling, and loop interchange, are employed to customize the computation and communication patterns of the accelerator with three levels of memory hierarchy.

C. Loop Optimization and Design Variables

As shown in Fig. 3, multiple dimensions are used to describe the sizes of the feature and kernel maps of each convolution layer for a given CNN. The hardware design variables of loop unrolling and loop tiling will determine the acceleration factor and hardware footprint. All dimensions and variables used in this paper are listed in Table I.

The width and height of one kernel (or filter) window is described by (*Nkx*, *Nky*). (*Nix*, *Niy*) and (*Nox*, *Noy*) define

the width and height of one input and output feature map (or channel), respectively. *Nif* and *Nof* denote the number of input and output feature maps, respectively. The loop unrolling design variables are (*Pkx*, *Pky*), *Pif*, (*Pox*, *Poy*), and *Pof*, which denote the number of parallel computations. The loop tiling design variables are (*Tkx*,

Tky), *Tif*, (*Tox*, *Toy*), and *Tof*, which represent the portion of data of the four loops stored in on-chip.

TABLE I
CONVOLUTION LOOP DIMENSIONS AND HARDWARE DESIGN VARIABLES

	Kernel Window (width/height)	Input Feature Map (width/height)	Output Feature Map (width/height)	# of Input Feature Maps	# of Output Feature Maps
Convolution Loops	Loop-1	Loop-3	Loop-3	Loop-2	Loop-4
Convolution Dimensions (N*)	Nkx, Nky	Nix, Niy	Nox, Noy	Nif	Nof
Loop Tiling (T*)	*Tkx, Tky*	*Tix, Tiy*	*Tox, Toy*	*Tif*	*Tof*
Loop Unrolling (P*)	*Pkx, Pky*	*Pix, Piy*	*Pox, Poy*	*Pif*	*Pof*

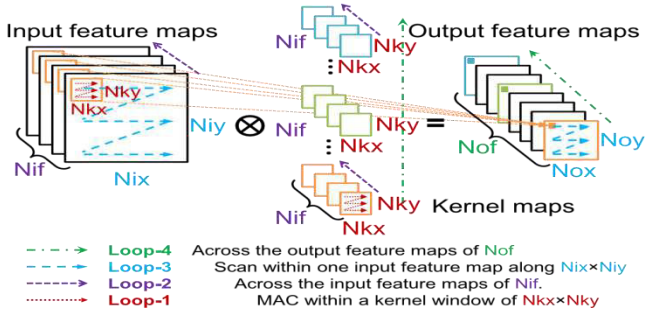

Fig. 3. Four levels of convolution loops and their dimensions.

buffers. The constraints of these dimension and variables are given by $1 \le P* \le T* \le N*$, where N∗, *T∗*, and *P∗* denote any dimension or variable that has a prefix of capital N, T, and P, respectively. For instance, $1 \le Pkx \le Tkx \le Nkx$. By default, *P∗*, *T∗* and *N∗* are applied to all convolution layers.

The relationship of input and output variables is constraint by (1)–(3), where S is the stride of the sliding window and the zero padding size is included in *Nix*, *Niy*, *Tix*, and *Tiy*

$$Nix = (Nox - 1)S + Nkx$$
$$Niy = (Noy - 1)S + Nky \quad (1)$$

$$Tix = (Tox - 1)S + Nkx$$
$$Tiy = (Toy - 1)S + Nky \quad (2)$$

$$Pix = Pox$$
$$Piy = Poy. \quad (3)$$

1) Loop Unrolling: As illustrated in Figs. 4–7, unrolling different convolution loops leads to different parallelization of computations, which affects the optimal PE architecture with respect to data reuse opportunities and memory access patterns.

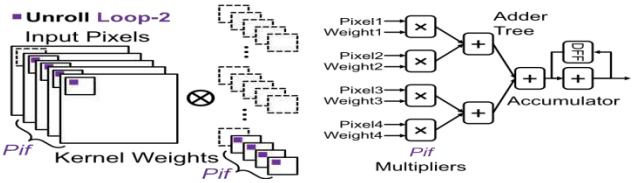

Fig. 5. Unroll loop-2 and its corresponding computing architecture.

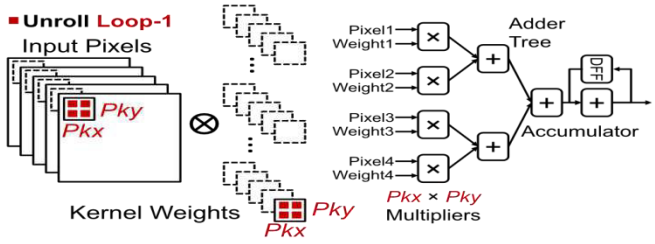

Fig. 4. Unroll loop-1 and its corresponding computing architecture.

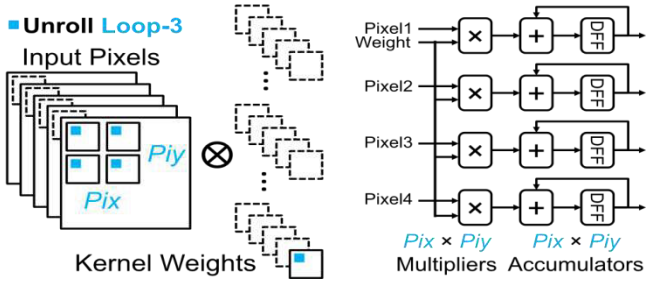

Fig. 6. Unroll loop-3 and its corresponding computing architecture.

same (*x*, *y*) location are required to compute the inner product. The inner-product operation results in the same computing structure as in unrolling Loop-1, but with a different adder tree fan-in of *Pif*.

a) Loop-3 unrolling (Fig. 6): In every cycle, *Pix* × *Piy* number of pixels from different (*x*, *y*) locations in the same feature map are multiplied with the identical weight. Hence, this weight can be reused *Pix* × *Piy* times. Since the *Pix* ×

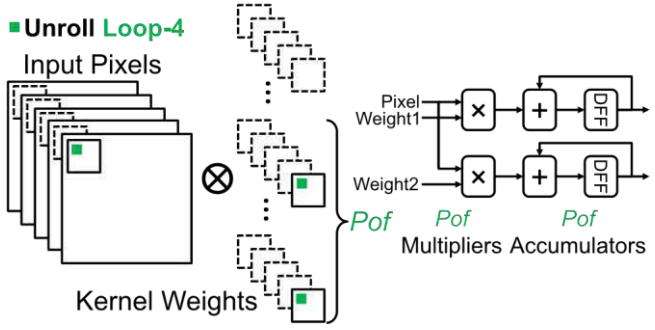

Fig. 7. Unroll loop-4 and its corresponding computing architecture.

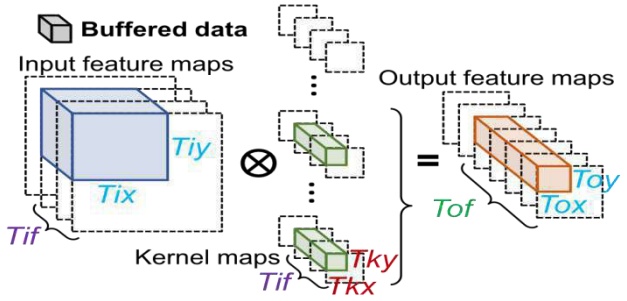

Fig. 8. Loop tiling determines the size of data stored in on-chip buffers.

Piy parallel multiplication contributes to independent *Pix* × *Piy* output pixels, *Pix* × *Piy* accumulators are used to serially accumulate the multiplier outputs and no adder tree is needed.

The unrolling variable values of the four convolution loops collectively determine the total number of parallel MAC operations as well as the number of required multipliers (*Pm*)

$$Pm = Pkx \times Pky \times Pif \times Pix \times Piy \times Pof. \quad (4)$$

2) Loop Tiling: Loop tiling is used to divide the entire data into multiple blocks, which can be accommodated in the on-chip buffers, as illustrated in Fig. 8. The loop tiling sets the lower bound on the required on-chip buffer size. The required size of input pixel buffer is *Tix* × *Tiy* × *Tif* × (pixel_datawidth).
The size of weight buffer is *Tkx* × *Tky* × *Tif* × *Tof* × (weight_datawidth). The size of output pixel buffer is *Tox* × *Toy* × *Tof* × (pixel_datawidth).

III. ANALYSIS ON DESIGN OBJECTIVES OF CNN ACCELERATOR

In this section, we provide a quantitative analysis of the impact of loop design variables (*P*∗ and *T*∗) on the following design objectives that our CNN accelerator aims to minimize.

A. Computing Latency

The number of multiplication operations per layer (Nm) is

$$Nm = Nif \times Nkx \times Nky \times Nof \times Nox \times Noy. \quad (5)$$

Ideally, the number of computing cycles per layer should be Nm/*Pm*, where *Pm* is the number of multipliers. The number of actual computing cycles per layer is

$$\#\_cycles = \#intertile\_cycles \times \#intratile\_cycles \text{ where} \quad (6)$$

$$\#intertile\_cycles = Nif/Tif\ Nkx/Tkx Nky/Tky \times Nof/Tof\ Nox/Tox Noy/Toy \quad (7)$$

$$\#intratile\_cycles = Tif/Pif Tkx/Pkx Tky/Pky \times Tof/Pof\ Tox/Pox Toy/Poy. \quad (8)$$

B. Data Reuse

There are mainly two types of data reuse: spatial reuse and temporal reuse

Having *Pm* parallel multiplications per cycle requires *Pm* pixels and *Pm* weights to be fed into the multipliers. The number of distinct weights required per cycle is

$$Pwt = Pof \times Pif \times Pkx \times Pky. \quad (9)$$

If Loop-1 is not unrolled (*Pkx* = 1, *Pky* = 1), the number of distinct pixels required per cycle (*Ppx*) is

$$Ppx = Pif \times Pix \times Piy. \quad (10)$$

Otherwise, *Ppx* is

$$Ppx = Pif \times ((Pix - 1)S + Pkx) \times ((Piy - 1)S + Pky). \quad (11)$$

Note that "distinct" only means that the pixels/weights are from different feature/kernel map locations and their values may be the same. The number of times a weight is spatially reused in one cycle is

$$Reuse\_wt = Pm/Pwt = Pix \times Piy \quad (12)$$

where the spatial reuse of weights is realized by unrolling Loop-3 (*Pix* > 1 or *Piy* > 1). The number of times of a pixel is spatially reused in one cycle (Reuse_*px*) is

$$Reuse\_px = Pm/Ppx. \quad (13)$$

If Loop-1 is not unrolled, Reuse_*px* is

$$Reuse\_px = Pof \quad (14)$$

otherwise, Reuse_*px* is

$$Reuse_{px} = \frac{Pof \times Pkx \times Pky \times Pix \times Piy}{((Pix - 1)S + Pkx) \times ((Piy - 1)S + Pky)}. \quad (15)$$

C. Access of On-Chip Buffer

Without any data reuse, the total read operations from on-chip buffers for both pixels and weights are *N*m, as

every multiplication needs one pixel and one weight. With data reuse, the total number of read operations from on-chip buffers for weights becomes

$$\#read\_wt = Nm/Reuse\_wt \quad (16)$$

and the total number of read operations for pixels is

$$\#read\_px = Nm/Reuse\_px. \quad (17)$$

If the final output pixels cannot be obtained within one tile, their partial sums are stored in buffers. The number of write and read operations to/from buffers for partial sums per cycle is $2 \times Pof \times Pox \times Poy$, where all partial sums generated by Loop-1 (*Pkx*, *Pky*) and Loop-2 (*Pif*) are already summed together right after multiplications. The total number of writes/reads to/from buffers for partial sums is

$$\#wr\_rd\_psum = \#\_cycles \times (2 \times Pof \times Pox \times Poy). \quad (18)$$

The number of times output pixels are written to on-chip buffers (i.e., #write_*px*) is identical to the total number of output pixels in the given CNN model. Finally, the total number of on-chip buffer accesses is

$$\#buffer\_access = \#read\_px + \#read\_wt + \#wr\_rd\_psum + \#write\_px. \quad (19)$$

IV. PROPOSED ACCELERATION SCHEME

The optimization process of our proposed acceleration scheme is presented in this section, which includes appropriate selection of the convolution loop design variables.

A. Minimizing Computing Latency

We set variables $P*$ to be the common factors of $T*$ for all the convolution layers to fully utilize PEs, and $T*$ to be the common factors of $N*$ to make full use of external memory transactions. For CNN models with only small common fac-

tors, it is recommended to set $N*/T*\rceil - N*/T*$ and $T*/P*\rceil - T*/P*$ as small as possible to minimize the inefficiency caused by the difference in sizes of CNN models.

B. Minimizing Partial Sum Storage

To reduce the number and movements of partial sums, both Loop-1 and Loop-2 should be computed as early as possible or unrolled as much as possible. To avoid the drawback of unrolling Loop-1 as discussed in Section IV and maximize the data reuse as discussed in Section III-C, we decide to unroll Loop-3 ($Pox > 1$ or $Poy > 1$) and Loop-4 ($Pof > 1$). By this means, we cannot attain the minimum partial sum storage, as (9.1) inside Fig. 9.

Constrained by $1 \le P* \le T* \le N*$, the second least number of partial sum storage is achieved by (9.2) among (9.2)–(9.9) inside Fig. 9. To satisfy the condition for (9.2), we serially compute Loop-1 and Loop-2 first and ensure the required data of Loop-1 and Loop-2 are buffered, i.e., $Tkx = Nkx$, $Tky = Nky$ and $Tif = Nif$. Therefore, we only need to store $Pof \times Pox \times Poy$ number of partial sums, which can be retained in local registers with minimum data movements.

C. Minimizing Access of External Memory

As we first compute Loop-1 and Loop-2 to reduce partial sums, we cannot achieve the minimum number of DRAM access described in (10.1) and (10.3) inside Fig. 10, where neither the pixels nor the weights are fully buffered for one convolution layer.

Then, the optimization of minimizing the on-chip buffer size while having minimum DRAM access is formulated as

$$\textbf{min}\ bits\_BUF\_px\_wt$$
$$\textbf{s.t.}\ \#Tile\_px_L = 1 or \#Tile\_wt_L = 1$$
$$\textbf{with}\ \forall L \in [1, \#CONVs] \quad (20)$$

where #Tile_px_L and #Tile_wt_L denote the number of tiling blocks for input pixels and weights of layer *L*, respectively, and #CONVs is the number of convolution layers. bits_BUF_*px_wt* is the sum of pixel buffer size (bits_BUF_*px*) and weight buffer size (bits_BUF_*wt*), which are given by $bits\_BUF\_px\_wt = bits\_BUF\_px + bits\_BUF\_wt.$ (21)

Both pixel and weight buffers need to be large enough to cover the data in one tiling block for all the convolution layers. This is expressed as

$$bits\_BUF\_px = MAX(words\_px_L) \times pixel\_datawidth \text{ with } L \in [1, \#CONVs] \quad (22)$$

$$bits\_BUF\_wt = MAX(words\_wt_L) \times weight\_datawidth \text{ with } L \in [1, \#CONVs] \quad (23)$$

where words_px_L and words_wt_L denote the number of pixels and weights of one tiling block in layer L, respectively. These are expressed in terms of loop tiling variables as follows:

$$words\_px_L = Tix_L \times Tiy_L \times Tif_L + Tox_L \times Toy_L \times Tof_L \quad (24)$$

$$words\_wt_L = Tof_L \times Tif_L \times Tkx_L \times Tky_L \quad (25)$$

where words_px_L is comprised of both input and output pixels. The number of tiles in (20) is also determined by $T*$ variables

$$\#Tile\_px_L = Nif_L/Tif_L \times Nox_L/Tox_L \times Noy_L/Toy_L \quad (26)$$

$$\#Tile\_wt_L = Nkx_L/Tkx_L \times Nky_L/Tky_L \times Nif_L/Tif_L \times Nof_L/Tof_L. \quad (27)$$

By solving (20), we can find an optimal configuration of $T*$ variables that result in minimum DRAM access and onchip buffer size. However, since we have already set $Tkx = Nkx$, $Tky = Nky$, $Tif = Nif$ as in Section V-B, we can only achieve a suboptimal solution by tuning Tox, Toy and Tof, resulting in larger buffer size requirement.

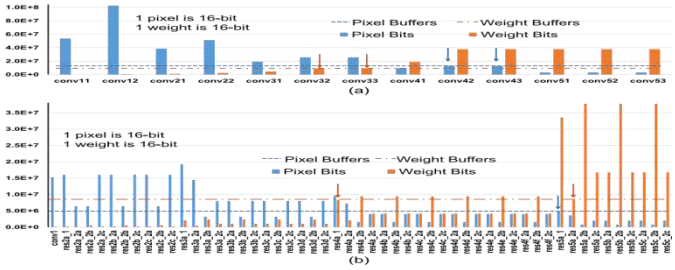

Fig. 9. To guarantee minimum DRAM accesses, either all pixels (blue bars) are covered by pixel buffers (blue dashed lines) or all weights are covered by weight buffers in one layer. Then, we try to lower the total buffer sizes/lines. (a) Pixels and weights distribution of convolution layers in VGG16. (b) Pixels and weights distribution of convolution layers in ResNet-50.

V. EXPERIMENTAL RESULTS

A. System Setup

The overall CNN acceleration system on the FPGA chip shown in Fig. 16 is coded in parametrized Verilog scripts and configured by the proposed CNN compiler in [16] for different CNN and FPGA pairs.

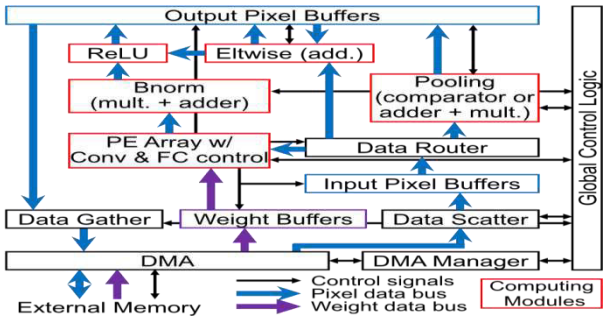

Fig. 10. Overall FPGA-based CNN hardware acceleration system [16].

B. Analysis of Experimental Results

The performance and specifications of our proposed CNN accelerators are summarized in Table II. In Stratix V and Arria 10, one DSP block can be configured as either two independent 18-bit × 18-bit multipliers or one multiplier followed by an accumulatorSince Arria 10 has 1.8× more ALMs and 5.9× more DSP blocks than the Stratix V we use, larger loop unrolling variables ($Pox \times Poy \times Pof$) can be achieved in Arria 10 to obtain >2× throughput enhancement than Stratix V.

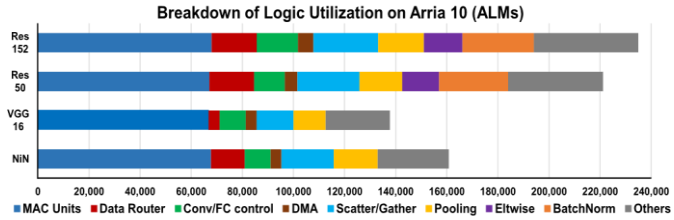

Fig. 11.Logic utilization breakdown of NiN, VGG-16 and ResNet-50/152.

VI. CONCLUSION

In this paper, we present an in-depth analysis of convolution loop acceleration strategy by numerically characterizing the loop optimization techniques. The relationship between accelerator objectives and design variables are quantitatively investigated. A corresponding new dataflow and architecture is proposed to minimize data communication and enhance throughput. Our CNN accelerator implements end-to-end NiN, VGG-16, and ResNet-50/ResNet-152 CNN models on Stratix V and Arria 10 FPGA, achieving the overall throughput of 348 GOPS and 715 GOPS, respectively.

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An Approach to reduce Self Transitions with Quadro Coding Technique in Very Large Scale Integration

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***Abstract*—A large number of logic gates are interconnected with each other which together perform a logical operation with given input signal. When an input signal changes from 0 1 or vice-versa, this change results in Power dissipation. Power dissipation is majorly due to dynamic power dissipation in charging and discharging of the capacitive load of CMOS circuits. Power is very important constraints with digital circuits by reducing power dissipation in CMOS VLSI circuits. The proposed coding technique reduces the transition activity in the input signals and will consequently result in the reduction of power consumption. A new bus coding technique has been proposed to achieve less power reduction in transmission. In this paper, the main target of VLSI designers is to minimize the switching activity of self transitions on the on-chip bus lines which is called as Quadro coding. In this process, the applied input data is coded in four different ways and the coding resulting in maximum reduction in transition activity is selected. By this coding scheme the average transition activity is reduced by approximately 36% for 8-bit wide data bus, 23% for 16-bit wide data bus, 15% for 32-bit wide data bus. The coding technique gives better results for shorter bus width.**

Keywords— *transition activity; dynamic power dissipation; self transitions; Interconnect; on-chip bus.*

I. INTRODUCTION

As nanometer scale is the trending technology, the wires are packed closer and the inter-wire coupling capacitance dominates the total capacitance. Interconnects plays an important role in overall performance of the chip Digital circuits consists of a number of interconnected logic gates which together perform a logic operation with more input signals. Crosstalk and Power consumption is a major concern in design of VLSI circuits as the technology is moving towards reduced chip size. A very popular method among them is the Bus Invert method, which does a conditional inversion of the bus lines to reduce the self transitions and thereby reducing the self energy. Crosstalk is mastering the nanometer technology which causes changes on interconnects. Crosstalk is an important design factor on total power consumption and delay of on-chip data buses. Transition activity on bus can be reduced by employing various bus encoding techniques.

A new coding technique 'Quadro coding' which minimizes both coupling and self transition activities in the bus lines have been evolved which focuses on reducing transition activities on bus which minimizes crosstalk and power consumption on on-chip data bus but with some increase in area overhead. The main focus of this technique is reduction in dynamic power dissipation. The capacitance of interconnect can be classified as coupling capacitance and self capacitance. The coupling capacitance is the capacitance between the adjacent data lines while the self capacitance refers to the capacitance between the substrate and the wire itself [6].The dynamic power in VLSI chip decides the behavior of chip and is highly dependent on the load capacitance and the coupling capacitance i.e. bus line signal transitions [7]. Dynamic power dissipation on a coded bus in a CMOS VLSI circuit is given by

$$P_{dynamic} = Į*VDD^2*CL*f \quad \ldots(1)$$

Where

VDD is the supply voltage,
CL is the load capacitance,
f is the clock frequency,
Į = Įs*Cs + Įc*CC.
Įs is the self transition activity factor
and Įc is the coupling transition factor.

Here, RHS of (1) is to be reduced for reducing dynamic power dissipation. In this paper, the main objective is to reduce dynamic power dissipation by reducing transition activity on the bus. The rest of the paper is organized as follows: Definitions of some of the important terms are given in section II, Literature survey and Bus model is explained in section III, proposed bus coding is explained in section IV, Simulation and comparison of proposed coding scheme with previous techniques shown in section V, finally conclusion are made in section VI.

II. BASIC DEFINITIONS

1. **Coupling transitions**: Transition of data from 0 → 1 or vice-versa between adjacent bus lines.
2. **Self transitions**: Transition of data from 0 → 1 or vice-versa on bus wire with reference to previous data on it.
3. **Bus width**: Number of bits in data is defined as bus width.

III. LITERATURE SURVEY AND BUS MODELS

M. R. Stan and W. P. Burleson proposed that *Bus-Invert* method of coding which became an area of interest in Bus coding for crosstalk [1]. They introduced a concept of inverting the data bits if total number of transitions were more than half of the width of the bus. By doing this the total number of transitions was made less than half. Youngsoo et al introduced modified bus invert coding method [2], called partial Bus invert coding. In this method the whole bus width was not inverted bus a part of it. J.V.R. Ravindra came up with and Low power encoding scheme for data transmission [3]. Saini et al have modified the existing technique with better efficiency [4].The above approaches have been based on Bus models provided by Chandrakasan [5, 7].

A bus is simply a circuit that connects one part of the circuit to the other. Buses are a typical model for I/O communication. A bus may consist of set of parallel lines with repeaters between them.

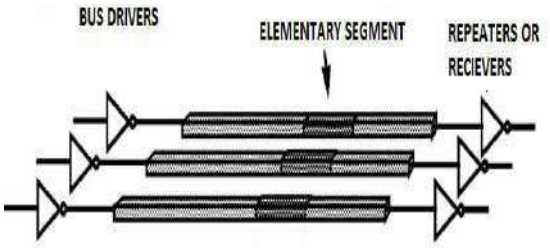

Fig. 1 – DSM Bus [7]

For the DSM bus, the distributed line model in terms of RLC [7] as shown is appropriate for describing electrical behavior of the bus.

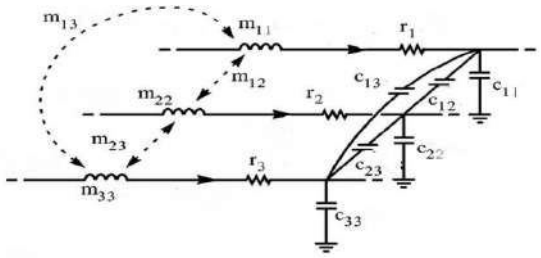

Fig. 2 – Elementary segments of DSM Bus Lines [7]

Where ri (x) is the serial resistance per unit length of i^{th} line, Cii (x) is the capacitance per unit length between the i^{th} line and ground, Cij (x) is the capacitance per unit length between the i^{th} line and j^{th} line, mii (x) is the self inductance per unit length of the i^{th} line, mij (x) is the mutual inductance per unit length between i^{th} and j^{th} line.

It is meaningful to consider only the capacitive component of the wire as long as the resistive component of the wire is small and the switching frequencies are in the low to medium range,. For on-chip parallel buses, energy is dissipated in charging and discharging parasitic capacitances. The coupling capacitance between the wires dominates the total parasitic capacitance of wires in DSM technologies. Below figure shows the simplified bus energy model [6]:

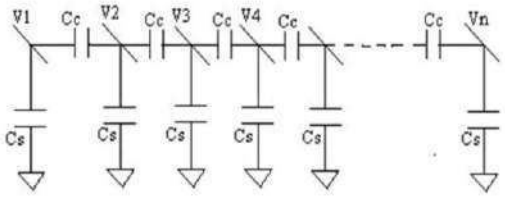

Fig. 3 – Simple Bus Energy Model [8]

Where *Cs* is the self-capacitance from each bus line to ground and *Cc* is the coupling-capacitance between two adjacent bus lines. V1 , V2 …are the node voltages. Let λ be the capacitance factor which is calculated as [9] the ratio between coupling capacitance to self capacitance. Increase of the capacitance factor leads to the technology scale

IV. PROPOSED QUADRO CODING TECHNIQUE

The proposed technique called the Quadro coding technique is based on reducing the number of the transitions occurring on data bus when a new data is to be transmitted. By using the following technique self transitions from 0 → 1 and 1 → 0 can be reduced as new data is sent on the data bus compared to previous data. Let the data be n bits wide. The developing coding technique is given as follows:

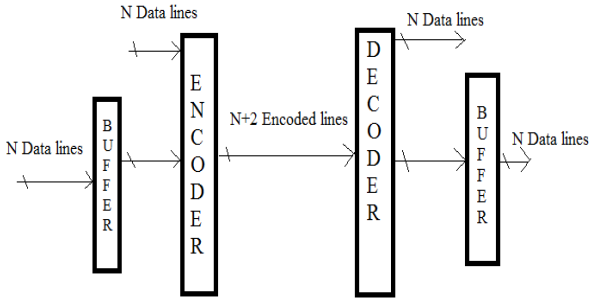

Fig. 4 – Block diagram of complete system

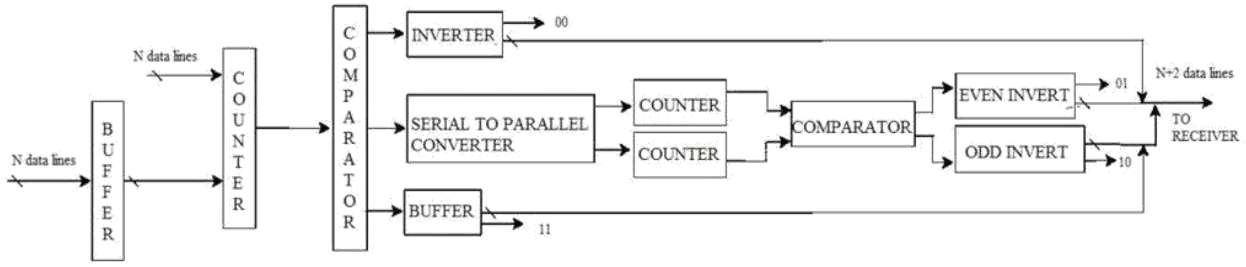

Fig. 5 – Block diagram of Encoder

ENCODING

STEP 1: Calculate and compare number of transitions of the present bus data to previous bus data.

STEP 2: If the number of transitions > n/2 then

Invert the data to be sent and append it with '00' as control bits for decoding purpose.

STEP 3: If the number of transitions < = n/2 and > n/4 then Divide the data into even and odd groups.
Odd group :A1,A3,A5,.....
Even group:A0,A2,A4.....

Calculate number of transitions between odd group of the present data with the previous data say OGT and number of transitions between even group of present data with the previous data, say EGT.
If EGT>OGT then
Invert the data bits of even group and append it with control bits '01'.

Else
Invert the data bits of odd group and append it with control bits '10'.

STEP 4: if the number of transitions <=n/4 then

Send the data as it is without any encoding and append it with '11'.

DECODING

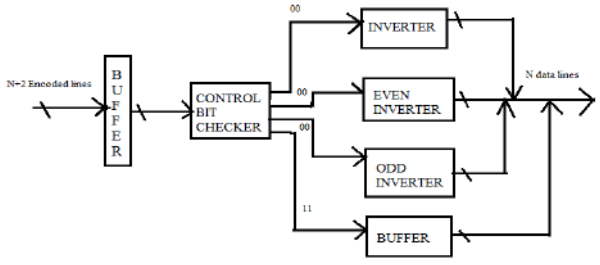

Fig. 6 – Block diagram of Decoder

To retrieve the data from the encoded data, control bits are recovered from the received data and the following operations are performed according to the control bits.

Table I shows operation to be performed on data bits for decoding. Decoding is performed by conversion of an encoded sequence or by dopting exactly opposite sequence of steps of encoding.

TABLE I: DECODING PROCESS EXPLAINATION ACCORDING TO THE VALUES OF CONTROL BITS

Control bits	Operation to be performed
00	Invert the received data
01	Invert the data bits of even group
10	Invert the data bits of odd group
11	Data remains same

V. SIMULATIONS AND RESULTS

The coding technique provides significant reduction in self transition activity with lesser increase in area overhead. The developing coding technique is found to give significantly better results as compared to previously proposed techniques such as bus invert, partial even/odd invert coding.

To compare the performance of the coding technique with earlier evolved techniques, the power saving factor *Ƞ* [7] is defined as:

Ƞ = Puncoded – Pcoded / Puncoded..... (2)

Here P uncoded is the average power consumption of uncoded bus, and Pcoded is the average power consumption of power optimized bus scheme. Quadro coding technique is compared with various other techniques evolved earlier is shown in the table below

Table II shows comparison of reduction in transition activity of various techniques with proposed coding technique. This table elaborates the total reduction in number of transitions when we use Bus Invert Coding and partial Bus invert coding.

TABLE II. COMPARISION RESULTS FOR TRANSITION ACTIVITY USING BUS INVERT CODING, PARTIAL INVERT CODING TECHNIQUE.

Coding Techniques	Data Bus Width	Reduction in transition activity(in %)	Difference in transition activity(in %)
Bus invert coding [1]	8-bit wide	15	21
	16-bit wide	9	14
	32-bit wide	7	8
Partial invert coding [2]	8-bit wide	7	29
	16-bit wide	3	20
	32-bit wide	2	13

VI. CONCLUSION

This paper presents a novel coding technique for reducing transition activity in on-chip buses. The technique has been tested on various bus widths and best results are observed for 9 bit bus width, where the transition activity has been reduced by up to 36%. This significant reduction in transition activity results in considerable power saving up to 47%. The power saving varies from 47% to 25% for 8-bit to 32-bit data bus. This technique is more suitable for shorter length buses as compared to longer buses.

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ANTI THEFT PROTECTION OF VEHICLE BY GSM & GPS WITH FINGER PRINT VERIFICATION

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***Abstract*—Recently vehicle tracking system is getting vast popularity because of the rising number of the stolen vehicles. Vehicle theft is happening on parking and sometimes driving in unsecured places. This research work explores how to avoid this kind of stealing and provides more security to the vehicles. The implemented system contains single-board embedded system which is equipped with global system for mobile (GSM) and global positioning system (GPS) along with a microcontroller installed in the vehicle. The use of GSM and GPS technologies allows the system to track the object and provides the most up-to-date information about on-going trips. Moreover, fingerprint verification is done in the implemented system to ensure the driving of correct person. The implemented system is very simple with greater security for vehicle anti-theft protection and low cost technique compared to others.**

Keywords—GMS; GPS; fingerprint; embedded system; vehicle anti-theft protection.

I. INTRODUCTION

A vehicle tracking system combines the installation of an electronic device in a vehicle or fleet of vehicle to enable the owner or third party to track the vehicle's location and collecting data in the process. Modern Vehicle Tracking system (VTS) is the technology used to determine the location of a vehicle using different methods like GSM and GPS module and other radio navigation systems operating through satellites and ground based stations. GSM and GPS based vehicle location and tracking system provides effective, real time mapping based vehicle location tracking. The system uses geographic position and time information from the Global Positioning Satellites.

After emerging of GPS system developed by The United States government, first it was only for military purpose. After opening for public, it has been used widely. Al-Bayari and Sadoun discussed in details Automatic Vehicle Location (AVL) system that works under GIS environment . A complete FPGA implementation of the vehicle position tracking system using short message services (SMS). The design and implementation of a mobile object management system that makes use of the existing GSM networks and its extension GPRS for data communication was discussed by Xiaobo Fan et al. Hsiao and Chang developed analytical model to analyze the optimal location update strategy with the objective of minimum total cost.Video surveillance and tracking of moving civilian vehicle done by Nishi Kanta Pati added new dimension to the development of the tracking systems.

In this research work, a system has been developed based on microcontroller that consists of a GPS and GSM. A two way communication process is achieved using a GSM modem. This study also comprises of a bio-metric protection system of the vehicle and fingerprint verification of the driver of the vehicle is used to protect the vehicle from anti-theft. Fingerprint recognition or fingerprint authentication can be defined as a method of verifying a match between two human fingerprints in an automated behaviour. Fingerprints are one of many forms of biometrics used to identify individuals and verify their identity. It is known that every person has a unique fingerprint image. When driver gives his verified fingerprint image before starting the vehicle, the system will be considered as fair condition. But when vehicle's location is changed without fingerprint verification, the system will be taken as abnormal condition. Then the system will send an SMS to owner of the vehicle with an URL of 'GOOGLE MAP' having the co-ordinate of the current location of the vehicle. SMS will be then sent to the owner having updated location's co-ordinate every interval of 10 seconds until doing the proper fingerprint verification. Moreover, vehicle's owner can get the vehicle's location at any time by SMS after making a 'missed call'.

II. METHODOLOGY

As shown in fig. 1, GPS receiver receives messages from satellites and that is used to determine the satellite positions and time sent. The *x, y,* and *z* co-ordinate components of satellite position and the time sent are designated as $[x_i, y_i, z_i, s_i]$. Subscript *i* denotes the satellite and have the value 1, 2...*n*, where *n* 4.Time of message reception indicated by the on-board receiver clock is t_i,the true reception time is where b is the receiver's clock bias from the much more accurate GPS system clocks employed by the satellites. All received satellite signals are biased at the same receiver clock (assuming the satellite clocks are all perfectly synchronized).

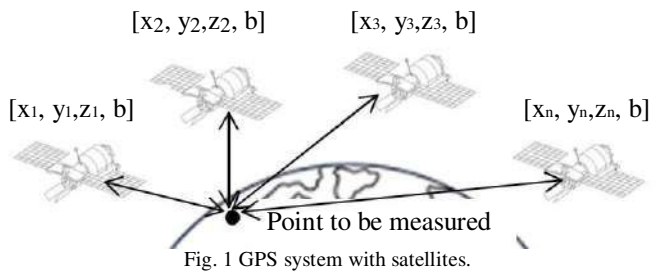


Fig. 1 GPS system with satellites.

Signals from at least four satellites are necessary to attempt solving these equations. GPS receiver position's three component and the clock bias, these four unknowns *[x, y, z, b]* are to be found. These can be solved by algebraic or numerical methods. Existence and uniqueness of GPS solutions are discussed by Abell and Chaffee. When *n* is greater than 4, this system is over determined and a fitting method must be used.

A fingerprint sensor is also used for bio-metric verification. There are many fingerprint sensor technologies i.e. optical, capacitive, thermal, RF, ultrasonic, piezo-electric, piezo-resistive, MEMS. Optical sensor technology has been used here. Captured finger image is digitally processed and stored in memory as a template. The fingerprint of Vehicle's driver is taken by this device before the starting of vehicle. Fingerprint matching algorithm is used to compare with previously enrolled image for checking authentication. Among correlation-based matching, ridge feature-based matching and minutiae-based matching, last one is popular as it is efficient and accurate. If vehicle's location is changed without fingerprint verification, the system will consider that something is going wrong. Then the GPS engine will collect the co-ordinate of that place and send SMS to the cell phone number of the owner of the vehicle.

As the data getting from GPS has some error [4] due to delay in ionosphere, cloudy sky, multi path fading occurred by tall trees, buildings or mountains, system can detect it as abnormal situation if gained co-ordinate has slightly changed due to its error. Horizontal accuracy is normally 2-15 meters in open sky. It is more than 50 meters inside a building (i.e. garage etc.). So we have created an imaginary geo-fence of radius of 100meters. When the location of that vehicle will be found out of that geo-fence without proper fingerprint verification then the system will take necessary steps. Fig. 2 shows the methodology of sending SMS with proper security check. From Fig. 2, it is seen that if a parked vehicle moves from the geo-fence with proper fingerprint verification, then no SMS will be sent. But if a parked vehicle moves from the geo-fence created without proper fingerprint verification, then there will be an SMS sent to the owner's cell phone with a 'GOOGLE MAP' link containing appropriate co-ordinate of that location. In case to park a vehicle, one has to reset the system. Then the system creates new geo-fence centring that new place.

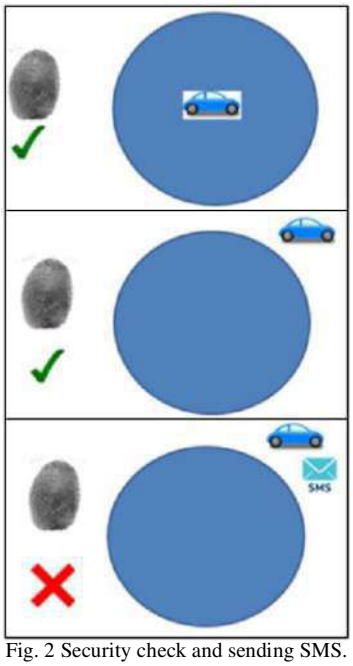


Fig. 2 Security check and sending SMS.

After initialization of GPS receiver, it gets co-ordinate (latitude, longitude and altitude), time and several others information in NMEA format. This information is being updated in every second. After starting, microcontroller gets 1st co-ordinate from GPS receiver. Following updated co-ordinate, it checks whether the distance of the updated location of updated co-ordinate is greater than 100 m or not. If and are the initial and final longitude and and are the initial and final latitude, then from Haversine formula we can get distance, D.

Here, R is the radius of the earth. There are still have some error because this formula does not take into account the non-

spheroidal (ellipsoidal) shape of the earth. It tends to beunder estimated trans-equatorial distances and overestimated trans-polar distances. For simplicity, earth's average radius 6380 km could be used.

Owner of the vehicle can also get the location of the vehicle anytime by giving a 'missed call'. Flow chart of the whole procedure is depicted in Fig. 3.

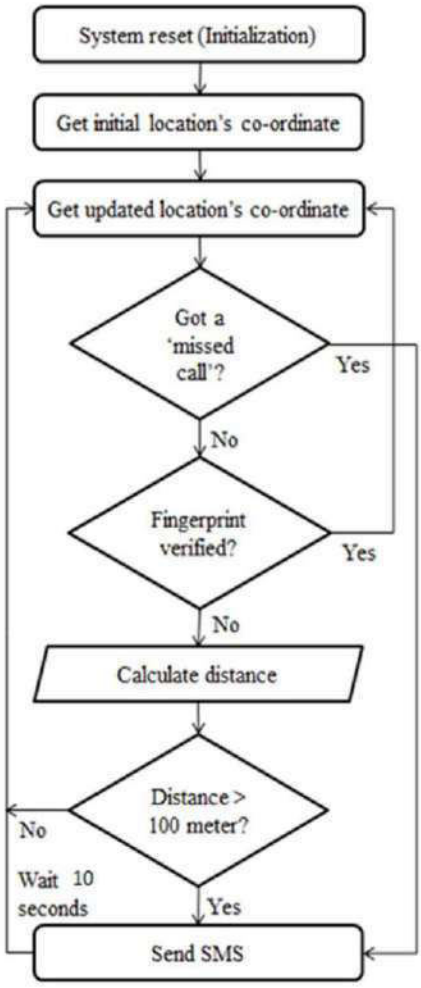


Fig. 3 Flow chart of security check and sending SMS.

III. System Design

In this research work, Arduino Mega2560 microcontroller is used for interfacing to various hardware peripherals. An Arduino mega2560 microcontroller is interfaced to a GSM modem and GPS receiver. A GSM modem is used to send the position of the vehicle from a remote place. SIM908 is used in this study. Both GSM and GPS engines are included in one device. GT-511C1R is used as fingerprint device.

Fig. 4 shows the block diagram of vehicle tracking system with Fingerprint verification. Both GSM and GPS engines have separate antenna. GSM, GPS and fingerprint devices are connected via microcontroller.

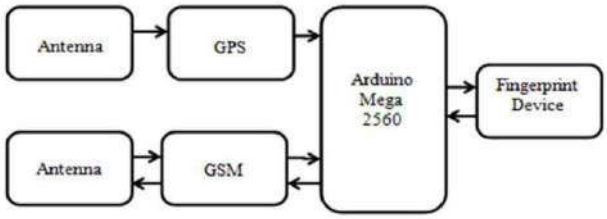


Fig.4 Block diagram of vehicle tracking system with fingerprint verification.

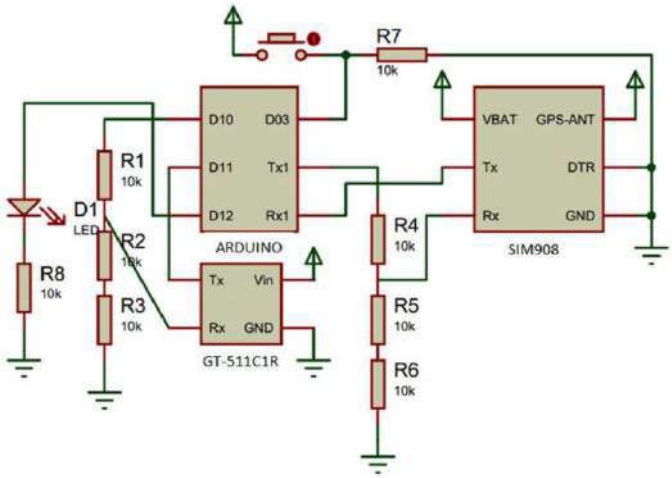


Fig. 5 Schematic diagram of in-vehicle tracking unit.

IV. System Description

In the vehicle, tracking unit is installed which includes Arduino -2560, SIM908 and GT-511C1R. SIM908 and GT-511C1R device are connected to the Arduino via serial COM port. Proper voltage level conversion is done by resistor divider. Fig. 5 shows the schematic diagram of in-vehicle tracking unit. Various parts of the tacking unit are described below.

A. Arduino MEGA-2560 Microcontroller

Arduino MEGA-2560 is powerful microcontroller board based on ATmega2560. It has 54 digital input/output pins (of which 14 can be used as PWM outputs), 16 analogue inputs, 4 UARTs (hardware serial ports. It has 256 KB of flash memory, 8 KB of SRAM and 4 KB of EEPROM. Fig. 6 shows the Arduino MEGA Board.

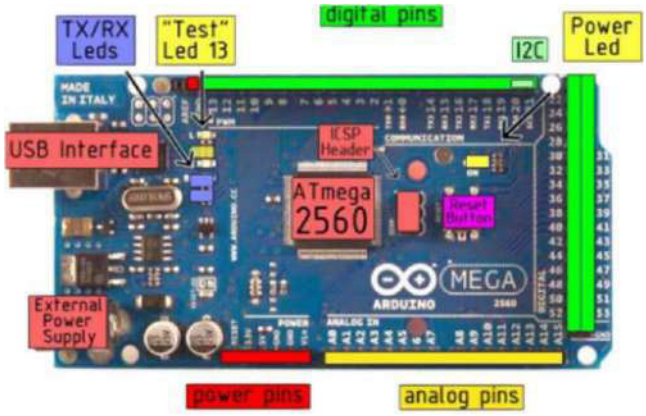


Fig. 6 Full specification of Arduino MEGA 2560.

B. GPS/GPRS/GSM (SIM908)

SIM908 has Quad-band GPRS/GSM engine. It works on the frequencies of 900 MHz, 1800 MHz, 850 MHz and 1900 MHz [20]. GPS technology for satellite navigation is also supported in this device. As both of the GPS and GSM technology is supported by it, any on purpose tracking is possible at anywhere and anytime with signal coverage.

Fig.7 SIM908 module.

C. GSM and GPS Antenna

In this project, GSM antenna used is passive type and GPS antenna is active type. Voltage range of GPS antenna is 3-5 volt.

Fig. 8 GSM (left) and GPS (right) antenna.

D. Fingerprint Module (GT-511C1R)

GT-511C1R has an on-board optical sensor and 32-bit CPU that does reading and identifying the fingerprints with sending the corresponding command. The module can only store up to 20 different fingerprints and is only capable of 30° fingerprint recognition. The optical fingerprint algorithm uses 240x216 pixel image for its input. It captures raw image from the sensor and converts it to 240x216images for the fingerprint algorithm. Not pressing of finger returns with non-acknowledge. Fig. 9 shows the fingerprint scanner (GT-511C1R).

Fig. 9 Fingerprint module (GT-511C1R).

V. SYSTEM IMPLEMENTATION& RESULT

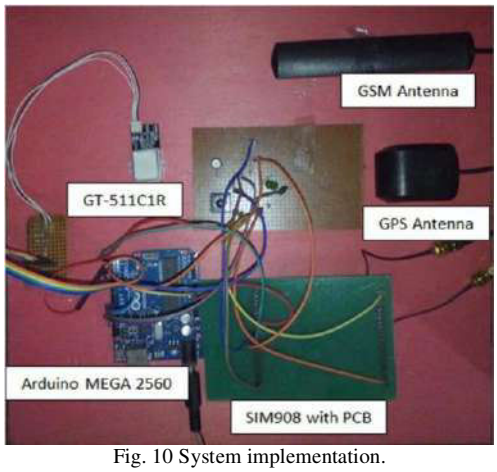
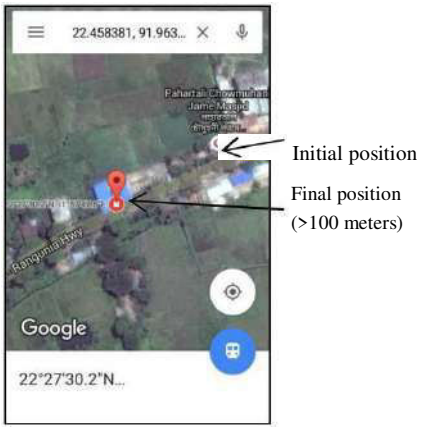
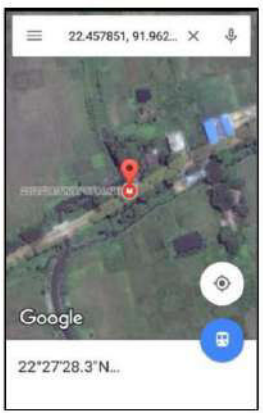


Fig. 10 System implementation.

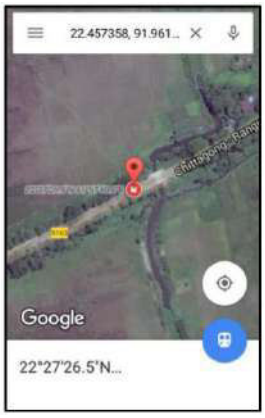
After doing hardware and software related works, the entire system was tested in a vehicle to ensure that the vehicle tracking system is working well and meets the requirement. When the vehicle moves out of the imaginary geo-fence without proper fingerprint verification, then an SMS is sent to the owner's cell phone with link including vehicle's co-ordinate. After that, an SMS is sent automatically after every 10 seconds including updated location's co-ordinate. Then proper fingerprint is given and sending massages has been stopped.



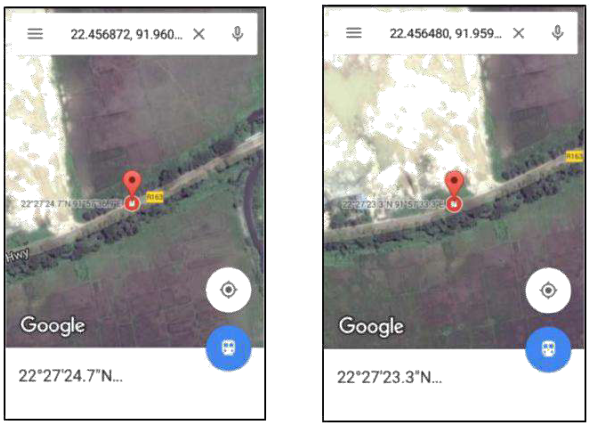
(a)



(b)



(c)



(d)
(e)

Fig. 11 Location on map (a) initial position and final posiion (> 100 meters), (b)-(e) subsequent positions of 10 seconds interval (from immediate previous positions).

TABLE I. LOCATIONS' CO-ORDINATE ANALYSIS

No. of positions	Location's co-ordinate (latitude, longitude)	Distance from previous locations (meters)
1	22.458768N, 91.964138E	-
2	22.458381N, 91.963226E	102.21
3	22.457851N, 91.962248E	115.86
4	22.457358N, 91.961286E	112.36
5	22.456872N, 91.960261E	117.12
6	22.456480N, 91.959260E	110.86

After doing click on that link, location on the map is showed. Fig. 11 shows the position on the map. In Fig. 11, first screenshot is the location of the vehicle pointed on that place exceeding the distance of 100 m. Subsequent screenshots are the location of moving vehicle after every 10 seconds of first massage. Distance is calculated by using Haversine formula.

VI. COST ANALYSIS

The different essential components with respective quantities and cost are given to implement the system in Table II. The wiring, PCB & miscellaneous cost are considered approximately.

TABLE II. COST ANALYSIS

No.	Equipment	No. of set(s)	Price (USD)
1.	ARDUINO MEGA-2560	1	12.67
2.	SIM908	1	25.35
3.	GT-511C1R	1	38.02
4.	Antennas	2	5.07
5.	Wire & Miscellaneous	-	1.27
Total cost			**82.38**

VII. CONCLUSIONS

In this research work, vehicle location can be tracked and prevention of it from theft with fingerprint verification is done with minimum cost in quasi real-time mode. Fingerprint technology is very effective security check technology and also in lower cost to avoid stealing of vehicles. In future, smart-phone (i.e. android, windows) application can be made and interfacing a dedicated smart-phone installed in vehicle with fingerprint device can be done to get real-time vehicle tracking with inter-active mapping.

ACKNOWLEDGMENT

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Design of Nano-Calculator Using Quantum Dot Cellular Automata (QCA)

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***Abstract*— CMOS technology over junction transistor is a very important contribution in terribly massive Scale Integrated technique for the last 20 years. Quantum Dot Cellular Automata (QCA) brings as a replacement answer to the elemental limits of CMOS technology. This paper could be a proposal of creating Quantum dot cellular automata (QCA) based mostly Nano-calculator. In this Calculator we've simulated four basic operations: addition, subtraction, multiplication and division. QCA is associate degree advance technology that overcomes some limitations of CMOS like change speed. QCA generated circuits operates within the order of THz frequency vary wherever circuits doesn't need any additio nal power provide for operation.**

Keywords*— *Clocksignal; Adder; Subtractor; Multiplier; Demultiplexer; nano Calculator.

I. INTRODUCTION

Quantum Dot Cellular Automata (QCA) is enforced by quadratic cells within which four potential wells reside in four corners of the cell connected by electron tunnel junctions. within the QCA cells specifically 2 electrons will reside within the potential wells. because of repulsion of their columbic forces, they occupy 2 opposite corners. so there will be 2 configurations, one for binary zero and another one for binary one. elementary analysis on Quantum dot cellular automata was planned by the authors in [1].

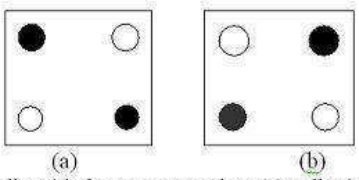

Fig.1. QCA cells with four quantum dots (a) cell with polarization p= -1(Logic '0') (b) cell with polarization p = 1 (Logic '1')

II. CLOCKING

The Quantum Dot Cellular Automata based circuits operate in four clock phases such as Switch, Hold, Release and Relax.

In **Switch** phase, extra electrons within a cell are polarized under the influence of neighboring cells. In this phase, a cell attains a definite binary value. Tunnel wants to get closed and potential barrier keeps on rising. In **Hold** phase, the potential barrier is maximum and tunnel gets closed so that electrons do not switch and retain their polarity. In **Release** phase, the potential barrier keeps on lowering and tunnel tends to get opened. As a result cells lose their polarity. In **Relax** phase, the potential barrier is minimum and tunnel stays open. As a result a cell has no influence on its neighbors. In QCA cells having different colors means that they are under different clocks and having same color means they are under same clock. In QCA, Green refers to clock 0, Violet refers to clock 1, Blue refers to clock 2 and White refers to clock 3. The clocking of is proposed in [1-2].

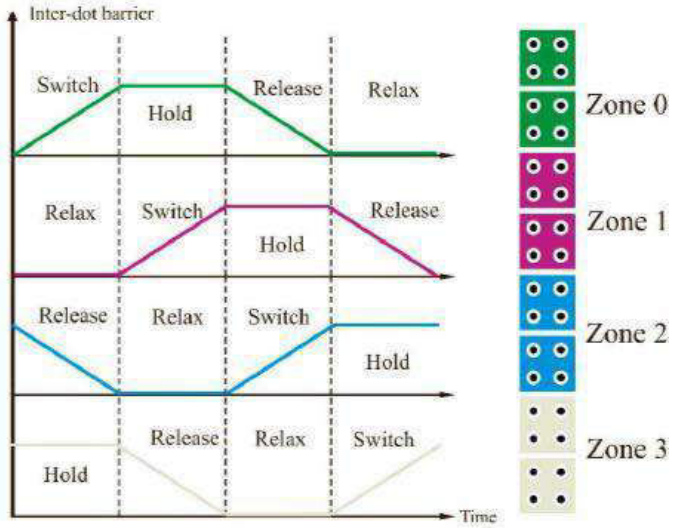

Fig.2 Clocking in QCA

III. NANO CALCULATOR

The calculator has completely been simulated using QCA technology. As compared to CMOS, QCA has taken

miniaturization of hardware devices on a whole new level. The different parts of the calculator are explained as below:

A. Adder

One bit adder has been proposed in [3]. In this paper we have designed a two bit adder using QCADesigner tool [4]. F**igure 3(a)** depicts the circuit diagram with two 2-bit binary inputs A0B0 and A1B1, three XOR gates, three AND gates and one OR gate**.** Q0 and Q1 are the 2-bit binary sum and C0 is the carry. **Figure 3(b)** shows the diagram designed by QCADesigner tool of the adder circuit. Here three clock zones are used to complete a full cycle.

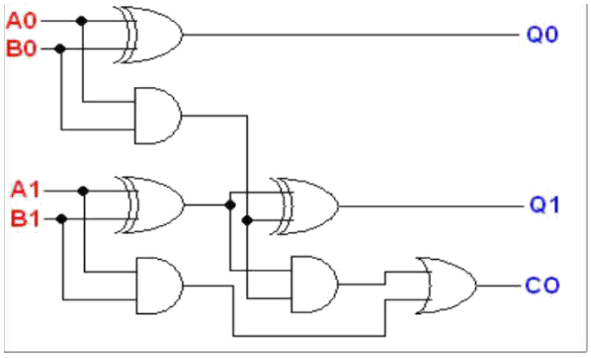

Fig. 3(a) Circuit for 2-bit Adder

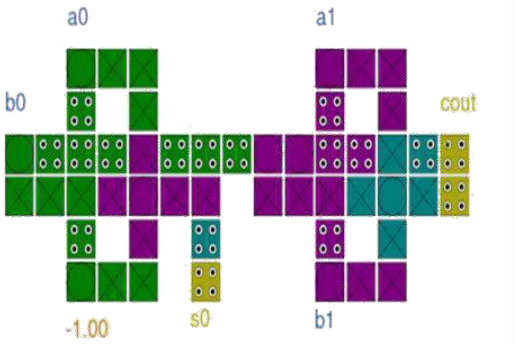

Fig. 3(b) Circuit for 2-bit adder using QCADesigner tool

B. Subtractor

Subtractor using QCA technology has been proposed in [5-6]. In this paper a two bit Subtractor is designed using QCA. Figure 3(c) shows the A0B0 and A1B1 are the two 2-bit binary inputs and D0D1 is the difference and C is the carry. XOR, AND and OR gates are used to build this circuit. Figure 3(d) shows the QCA version of the Subtractor circuit. Here
three clock zones are used to complete a full cycle.

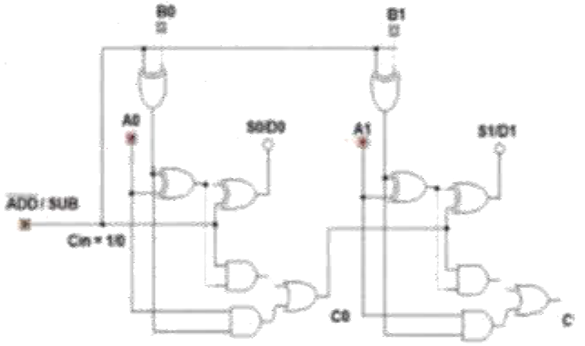

Fig.3(c). Circuit for 2-bit subtractor

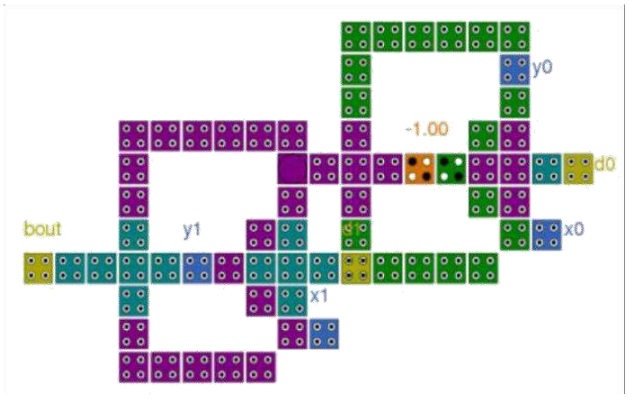

Fig.3 (d) Circuit for 2-bit Subtractor using QCADesigner tool

C. Multiplier

Figure 4(a) shows the Multiplier circuit using A0B0 and A1B1 the two bit binary inputs and C0C1C2C3 is the four bit binary product as output. Here six AND gates and two XOR gates are used to build up this circuit. Figure 4(b) is the QCA version of the multiplier circuit. Here, four clock zones are used to complete a full cycle.

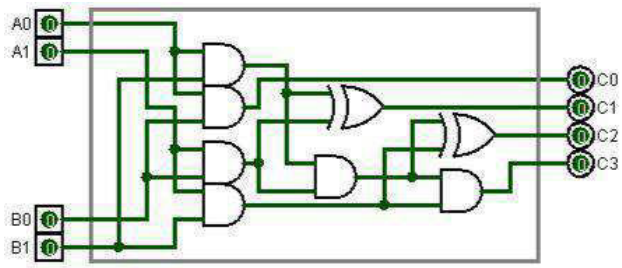

Fig. 4(a) Circuit for 2-bit multiplier

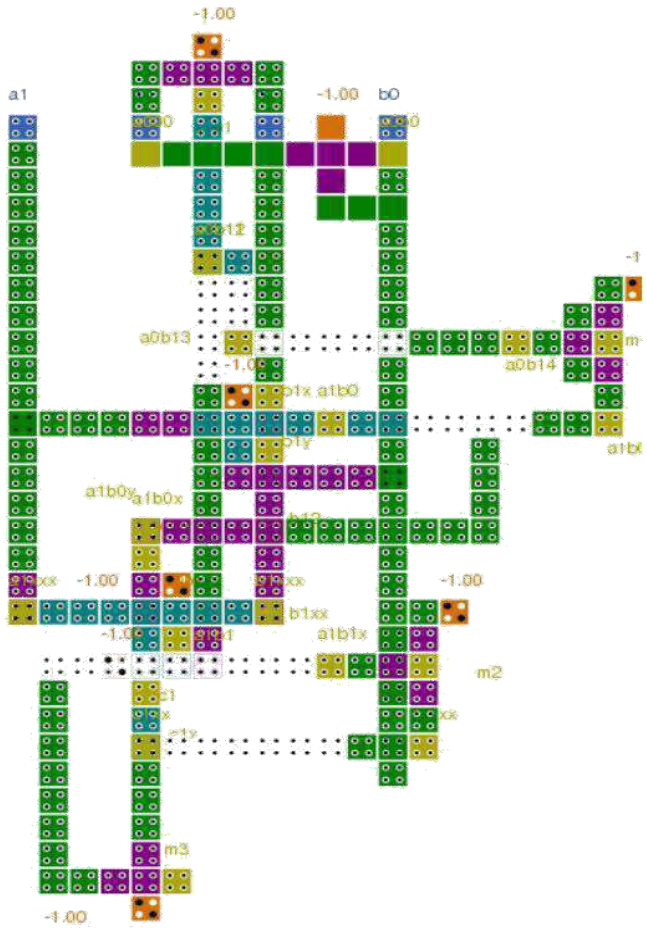

Fig.4(b) Circuit for 2-bit multiplier in QCA

D. Divider

A two bit divider circuit is shown in **Figure 5(a)** where A0B0 and A1B1 are the two binary inputs. **Figure 5(b)** shows the QCA based circuit design of the divider circuit. Here, three clock zones are used to complete a full cycle.

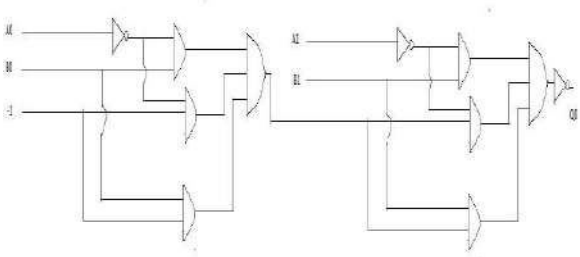

Fig-5(a). Circuit for 2-bit divider

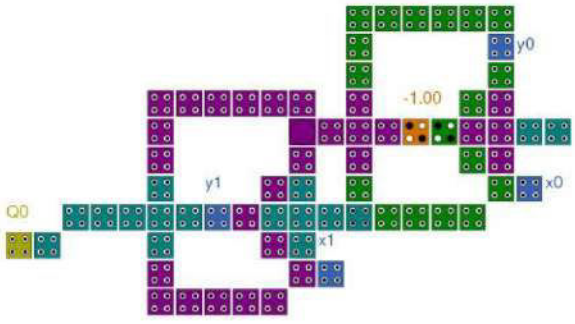

Fig.5(b) Circuit for 2-bit divider in QCA

E. Demultiplexer

A 1X4 de-multiplexer is used to integrate the four circuits (Adder, Subtractor, Multiplexer and Divider) into a single circuit to simulate the calculator circuit as a final result. F**igure 6(a)** shows only one input A, four outputs (D0, D1, D2, D3) and two control lines (I0, I1) to build up the DEMUX circuit. **Figure 6(b)** is the QCA based design of the DEMUX circuit. Here, three clock zones are used to complete a full cycle.

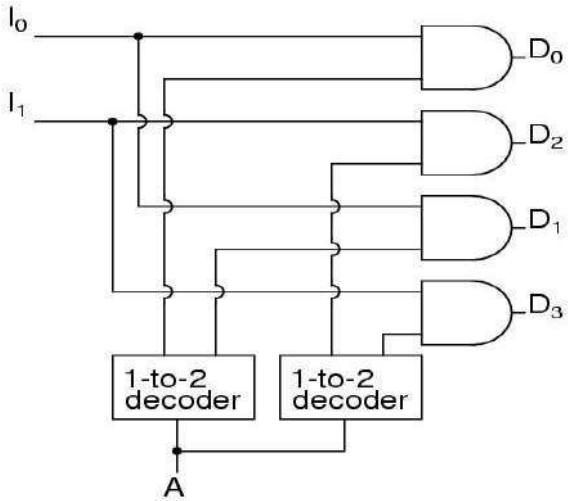

Fig.6 (a) Circuit for 1X4 Demux

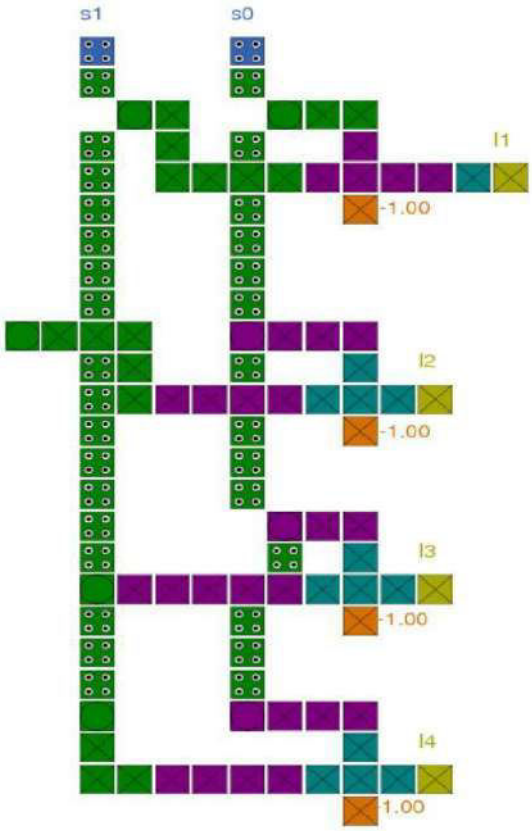

Fig.6 (b) QCA Circuit for 1X4 Demux

IV. NANO CALCULATOR IN QCA

Figure 7 refers to the final circuit diagram of the calculator using Quantum dot cellular automata. Here 00 represents adder circuit, 01 represents Subtractor circuit, 10 represents Multiplier circuit and 11 represents divider circuit.

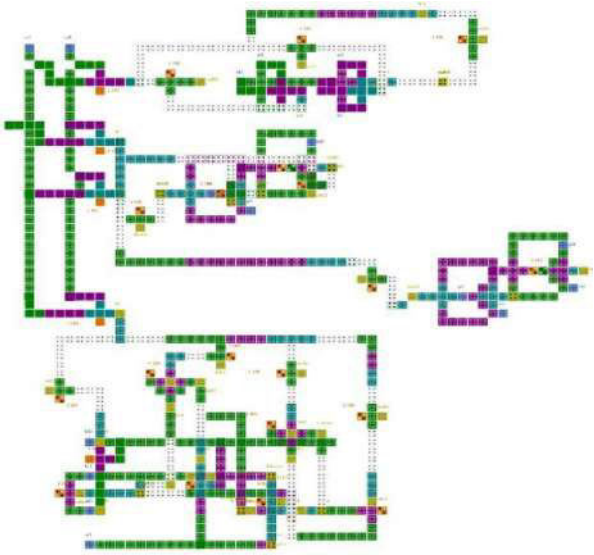

Fig.7 Calculator in QCA

V. RESULTS

All the designed circuit outputs are shown in the following figures. Figure 8(a) and 8(b) shows the corresponding Adder and Subtractor circuit. Figure 9, 10 and 11 shows the corresponding Multiplier, Divider and Demultiplexer circuit outputs.

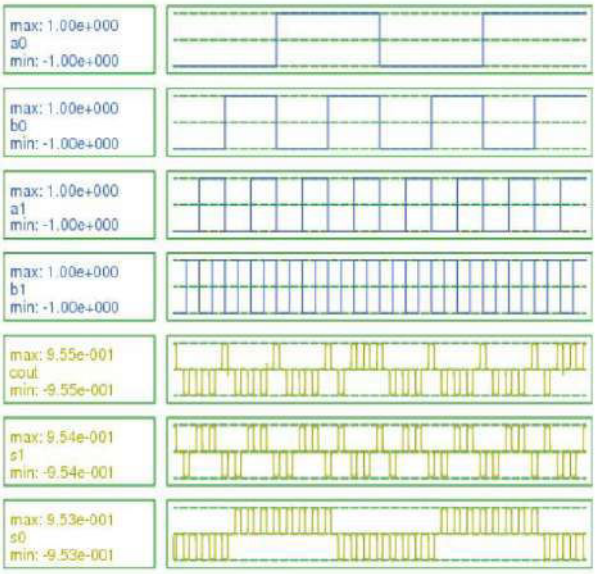

Fig.8 (a) Clocked output of the Adder circuit

Fig.8 (b) Clocked output of the Subtractor circuit

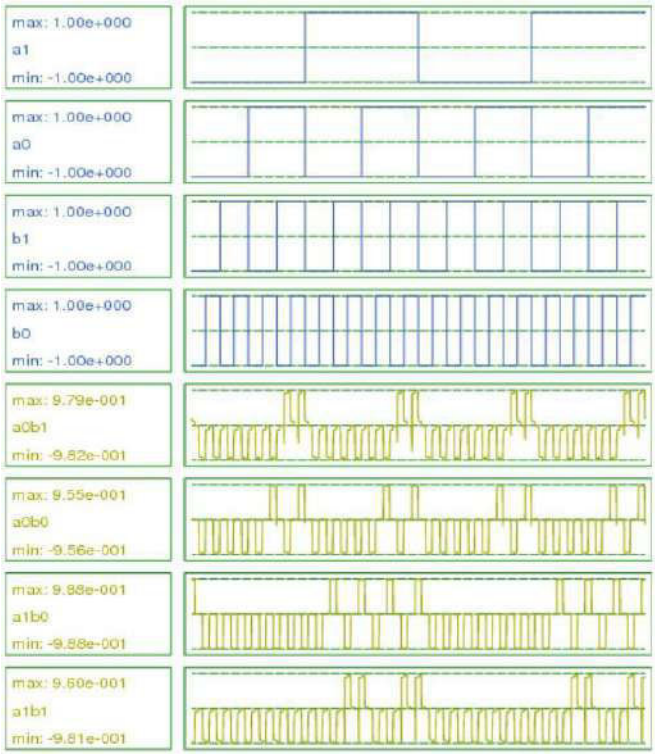

Fig.9 Clocked output of the Multiplier circuit.

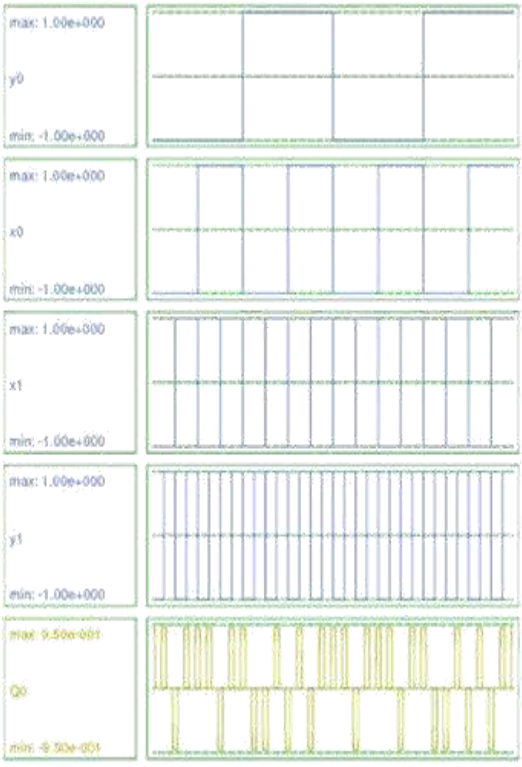

Fig.10 The clocked output of the Divider circuit.

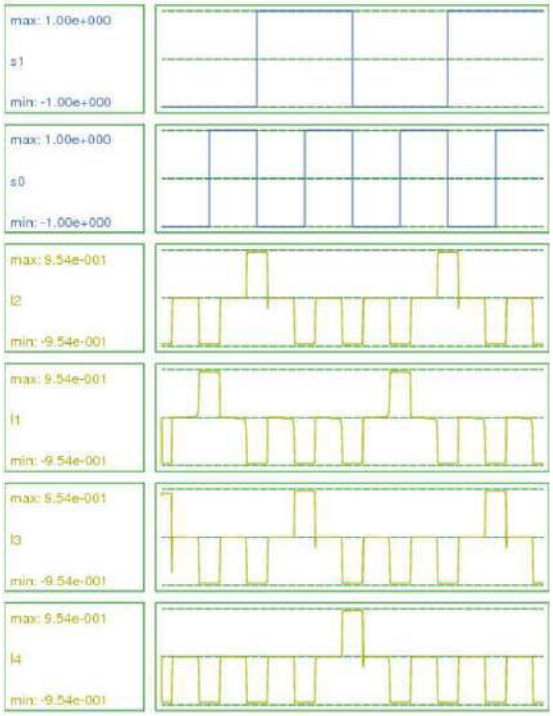

Fig 11.Clocked output of the Demultiplexer circuit

VI.CONCLUSION

In QCA the semiconductor unit logic is changed to quantum logic. Nano Calculator using this technology may be a new idea wherever single atom in a very quantum dot takes the management of operations like addition, subtraction, multiplication and division. In future this design is aimed to design and improve the system performance level with additional arithmetic operations compare to existing CMOS design methodology. The calculator designed by QCA technology using QCA Designer is certainly a modification just in case of speed and space consumption over all the opposite shrewd devices.

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IoT TECHNOLOGY BASED MEASUREMENT OF WATER QUALITY

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ABSTRACT:

At present, unique sites use Internet technology (IoT) techniques as well as remote sensing techniques (RS) to monitor, create and test statistics from remote locations. Water consumption is a useful tool for all people, because the energy consumption of water in alcohol consumption is facing new scenarios that require new procedures in real time. These irritating scenarios come from limited water sources, population growth, aging equipment, and many other facilities. Later, several methods are needed to discover premium water. In order to ensure a convenient supply of water, real-time requirements must be

checked. In this article, we plan to offer a model plus a refined low-cost tool to provide real-time control over the wonderful water in the Internet. Specifications can be indicated with temperature, pH, turbidity, water float sensor module. The measured values of the sensor units can be improved by the central control unit. The ARM 7 variance can be used as the main controller. After all, the sensor module's facts can appear on the network using WI-FI devices.

Keywords: IoT (Internet of things), water quality, PH sensor, Wifi, Turbidity, water level sensor.

1. INTRODUCTION

Water is a scarce useful source as well as an important agricultural market as well as an animal way of life on the planet, which involves people. Great individual offers do not indicate how important it is to eat enough water every day. More water is discharged using several control methods. This problem was quietly associated with the amount of negative water, ineffective use, as well as a pleasant scarcity and buried in water. For this reason, environmental friendliness, as well as water control measures, are limitations on the ability of living or working water controls. Every creature in the world wants to keep water for survival. A person forms our bodies of more than 60 percent of the water. We use clean water for consumption, plant food, and operate equipment, as well as

swimming, surfing, fishing and sailing. Water is very important to every part of our lives. Ensuring excellence in flood waters will certainly ensure the protection of our rivers against toxins [1]. Farmers can use the real situation to help better organize their land and vegetation. Our region, the nation, federal governments focus on the facts to help control the toxins, a different order. Large water torture with each element, as well as the characteristics of nonfactor pollution, which include disposal of sewage, leakage of markets, runoff of agricultural areas, as well as a physical runoff. Different infectious properties of other waters are flooding, as well as droughts, as well as lack of experience, as well as teaching and learning among customers [2][3]. In order to maintain the most effective water resources is necessary to the requirements of customers involved to save the water is scary, as well as see the unique health, environmental health, storage space and disposal aspects. Water is a vital requirement for human survival and, as a result, must be equipped with a device to display the best water condenser, which means to eat around, as well as the community crossing aspects such as rivers, streams and coasts on the borders of our communities and cities. Ideally, an exceptional water system is crucial to highlight pain in water, as well as improving the quality of life. Improving the land-based water monitoring system is an important aspect of the assessment, as well as water safety and security. We have created an easy-to-install generation model, through which ideal indicators of unique groundwater can be assessed. This article uses an intelligent water monitoring device.

2. RELATED STUDY

The system is able to certify the physiological and chemical properties of water, as well as movement, temperature, pH and transmission, as well as additional oxidation power. These physicochemical specifications are used to find water pollutants. Sensor units that can be made from initial recommendations and also made with signal conditioning schemes relate to a special contract based on a microcontroller, which, in addition to data, also uses methods. In this format, the ZigBee receiver and transmitter components are also used to interact with many measurements in addition to the communication node. The alarm unit is looking for sensor units, and also activates the sound signal at the same time with acceptable water standards, obtains harmful types. Missing checks and various documents to confirm the mandate of each part control device. Sensor units are validated for work in the specified accuracy matrix [4]. The PMS node has the ability to send information via ZigBee, also to the audio program alert node. The effect is that the system is capable of analysing physical chemistry. Standards can also be efficiently

navigated and analysed. Note the Vaccination tool is a co-ordinator, as well as network wireless sensor settings (WSNs) that allow you to evaluate the positive statistics that are captured using the sensor water in the water, which allows you to save the source of water in well-known residential uses also tend to make determined measures to correct extreme water body well-being. We have made it clear that our strategy is very easy to reduce the huge variety of interactions between sensor module tools, which, in addition to the rebate on the Web's lagging servers, however, can actually have a concentration of water events that break through using this difference in the arrival of calling specific location differences [5]. Sensor device. Our shopping effects can reach as much as 90% of the interaction of the analysis with the traditional periodic cover conditions.

3. AN OVERVIEW OF PROPOSED SYSTEM

Water pH is the level of acid and base balance and most natural water is controlled by a carbon dioxide carbon balance mechanism. Thus, the expansion of understanding of carbon dioxide will reduce the pH, while as a result of this decrease will rise. Temperature can even affect the balance and ph. In clean water, the pH drops to about 0. 5 at 5 ° C (25 ° C). The maximum pH of the non-peeled water is 6. Five-8. five. The most commonly used pH sensor is a glass pole. Real-time pH monitoring is used in the sewage treatment plant (STP) to automate PCB management and pH screen. The turbidity is a cloud of water. The turbidity has pointed to the extent to which water loses transparency. This is taken into account on a large level, except for water. Relaxation prevents a small stimulus through submerged aquatic plants. It can also raise the water temperature above the normal level, because the particles suspended underground facilitate the absorption of heat from the sun. The ESP8266 WiFi module is a standalone SOC with a set of TCP / IP protocols that ensures that any microcontroller has the right to access your WiFi community. ESP8266 can either create a Web application or isolate each Wi-Fi network from another proprietary processor. Each ESP8266 module is pre-programmed with the AT group driving firmware. The ESP8266 module is really an expensive, powerful panel with a large and growing network. PCB designs before all production stages and aspects and sensors created on it [6]. The BLINK app has been added to the Android model to explore the product. When you start the device, the dc modem is given to the package, it will illuminate Arduino and WIFI. The aquatic parameters are tested by one, but one is given as final results for the LCD screen. The app comes with hot spots, and offers the perfect cost, as the LCD screen indicates a

comprehensive package. Thus, where the package is placed at any time on any unique water object and connected to WIFI, we can at any time judge its real-time price on our Android phone.

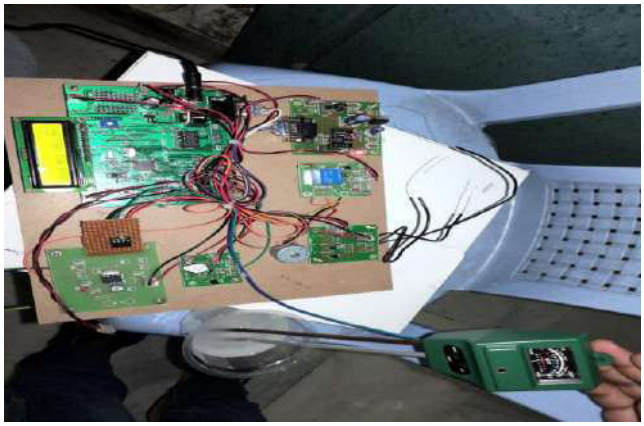

Fig.3.1. Working model.

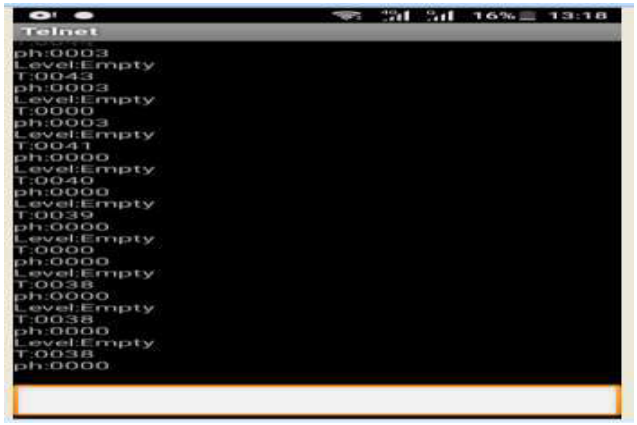

Fig.3.2. Output results.

4. CONCLUSION

Water is one of the most critical of all the primitive wishes of all inhabited beings. But unfortunately, a lot of water is wasted using uncontrolled water. The most important problem to be solved by this task is the development of a WSN water monitoring system. Using Wi-Fi sensor technology, you can complete three unique water monitoring strategies such as water level monitoring, water pollution monitoring, water leakage monitoring and later water management. Through the tracking system, we will be able to save water without problems, and we can keep water in our time.

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THE STRUCTURE IMPLEMENTATION OF ECG MONITORING USING SMART DEVICES

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ABSTRACT—**Now-a-days Heart ailment (Cardiovascular maladies) has turned into a major issue for human wellbeing. This Cardiovascular malady causes the passing of human. The most difficult occupation is discovery or ID of Cardiovascular malady in beginning periods of patients. This look into work ways to deal with build up an ECG observing framework requiring little to no effort for the patients who can distinguish and recognize the likelihood of heart illnesses in a split second. This ECG signal is transmitted by means of Bluetooth module or Zigbee to keen gadget with help of programming reenactment where extraction furthermore, discovery calculation is setup for cardiovascular ailment. This system can be associated with the specialists and doctor's facilities to get the quickest treatment. This proposed thought is to add to bring under control heart illnesses and furthermore act as a normal outcomes in medicinal services administration to patients in remote region**

Keywords—: ECG Sensors, Smart phone, Laptop, Arduino, Bluetooth, Zigbee, Cardiac Patient.

I.INTRODUCTION

Electrocardiogram (ECG) is the transcripting of the electrical action of heart. ECG signal is a bipolar low-frequency weak signal and the normal range of the signal is 0.05-100Hz . Its amplitude ranges from 10μV to 5mV, whose average esteem is 1mV. ECG signal can analyze a few heart related ailments. Cardiovascular maladies are a gathering of disarranges of the heart and veins. CVD remains the driving reason for death around the globe. Our point is to build up a minimal effort ECG observing framework, which is realtime, moderate, compact and easy to use. In this exploration paper a model ECG observing framework is produced which is minimal effort, compact, battery fueled, and it incorporates remote office for security concern and diminishing commotion impedance.

II. NEED OF SUCH SYSTEM

A. Our current ECG Monitoring framework has extremely intricate structure with immense wired network. This proposed framework gives remote observing of the coronary illness.

B. Patient needs to come doctor's facility from long distance
check the ECG for identification of CVD. In this paper proposed system is able to monitor the ECG via smart devices any time from home and can send it to doctor.

III.WAY TO CUT DOWN COST OF ECG CHECKING GADGETS

One approach to chop down the expense of ECG checking gadgets is to execute these around smart gadgets like Android mobiles, workstation running under Android operating system equipped with wireless Bluetooth and Zigbee technology. The following benefits may result from the massive adoption of this technology, besides lowering ECG monitoring cost. Patients may have their ECG recorded at home, avoiding travelling to distant hospitals and moving through heavy traffic urban areas. This might be helpful for elderly patients, chronic cardiac patients, and patients living in the countryside where doctors are not available.

In addition to replacing expensive and bulky traditional ECG machines, mobile phone-based ECG monitoring devices offer the paramount feature of instant warning about the heart condition of the patient. This characteristic is quite appealing, for life threatening arrhythmias and ECG alterations appear before a sudden heart attack occurs. Moreover, the chance to survive such an event is higher when patients are treated promptly.

This paper presents the design and evaluation of an ECG monitoring system deploying an Android mobile phone and laptop using wireless technology (Bluetooth and Zigbee).

In the system, we have developed a software for Laptop and an android application to visualize the ECG signal. This system consists three electrodes, by which ECG can be taken from either limb leads (Lead I, II and II), and augmented limb leads (aVR, aVL, and aVF). The equipment used in this system consumes low power for this it can function for a long time.

IV. ARCHITECTURE AND METHODOLOGY

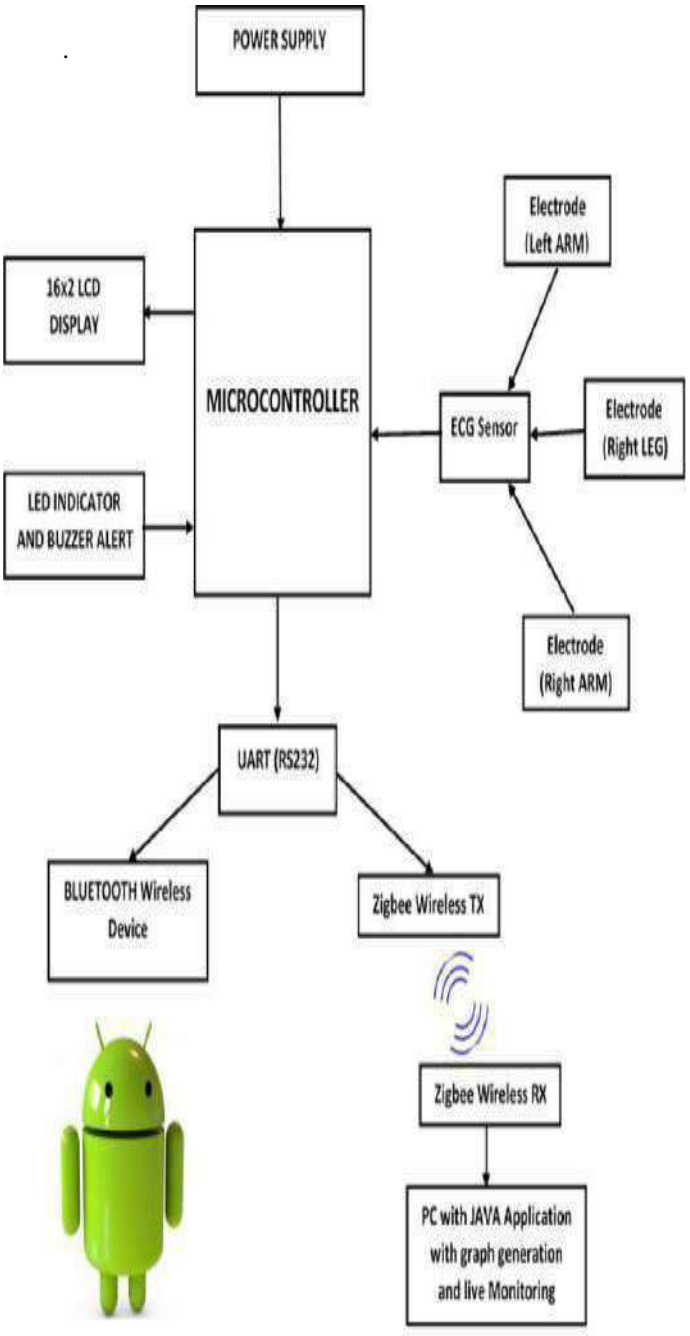
A. FRAMEWORK OVERVIEW

The planned ECG observing framework involves three particular subsystems:

1. The first is devoted to condition the Analogy ECG signal.
2. Setting it up for transformation to the digital world.

3. The third subsystem is the mobile phone and the PC itself.

Fig 1: ECG monitoring system based on Smart Devices



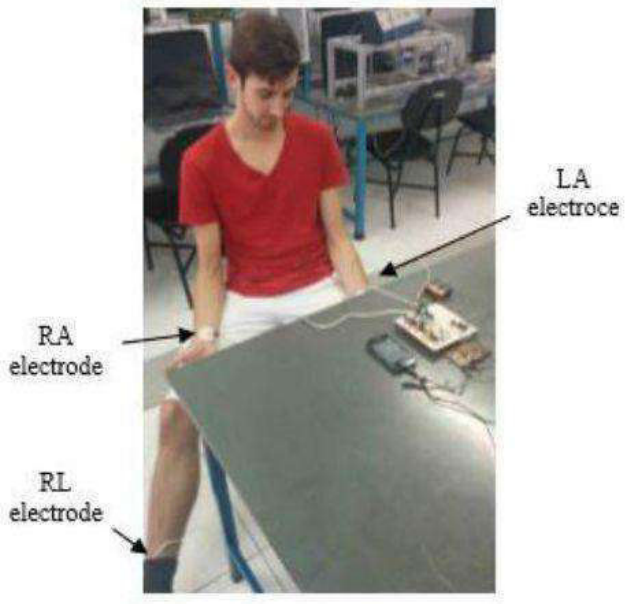


Fig. 2. Mobile phone-based ECG monitoring prototype connected to a user

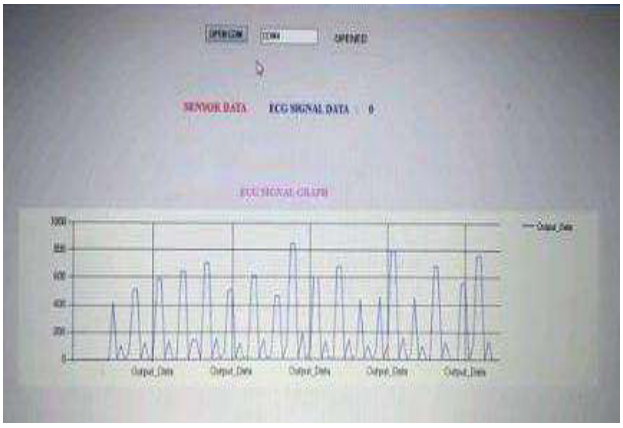
As portrayed in fig. 1 The first is committed to process the simple ECG signal, setting it up for change to the digital world. This is necessary, for today`s mobile phones do not include a means to directly interface to analog signals from the external world. This can be achieved by using AD8232 single lead heart rate monitor. The second subsystem consists of a microcontroller and a Bluetooth module and a Zigbee Module. This unit samples the ECG, serializes the samples and transmits them via the Bluetooth module to the Android cell phone and via Zigbee to the PC with JAVA application. So that ECG graphs can be identified on both smart devices. The third subsystem is the cell phone and the PC itself. An application has been program written, the ECG samples and suitably charts the ECG signal on the screen for analysis

B. ECG SAMPLING AND TRANSMISSION BY MEANS OF BLUETOOTH AND ZIGBEE

A 8-bit Microcontroller ATMega-8 tests the ECG signal at 150 Hz, utilizing an embedded 10-bit ADC. The control program sends the approaching raw samples to an inserted USART sequential port. The program decreases each 10-bit sample into a corresponding 8-bit test, before transmission, essentially by disposing of the two less noteworthy bits. The USART serializes the examples at 9600 bits for each seconds, utilizing the following settings: 8-bit information length, no equality, and one stop bit. After accepting the bits spilling from the USART, the Bluetooth module (Linvor JY-MCU) sends them into the air, which can be gotten by an adjacent Bluetooth-prepared advanced mobile. Bluetooth is utilized for short separation information transmission. For PC application Zigbee can be utilized to transmit information remotely. Zigbee can transmit information upto100 meters. The XBee module uses Zigbee protocol for communication also they can communicate with other devices using simplest serial communication protocol and hence they are used in microcontroller base boards (Arduino).

We use only two Xbee modules to transmit and receive the data but controlled using the Arduino board. Since These modules communicate using serial communication protocol with the interfacing devices they can be connected to a microcontroller using a minimum of four pins, Power supply, and Ground, UART Data Out, and UART Data In pins. The Xbee modules have several digital and analog I/O pins apart from these pins and the pin out of an Xbee module.. The control program running on the Microcontroller just implements the commands supplied by the datasheet for the Bluetooth module (EGBT046S AT Command Set) and Xbee module to establish communication with the mobile phone and PC itself.

fig3: ECG graph monitored on pc applications via zigbee



C. ANDROID MOBILE AND PC

An economically accessible Android Mobile telephone with Bluetooth filled in as the objective mobile phone amid execution of this undertaking. We have created android application utilizing Android Studio which can be introduced on portable and The PC application gives a graphical client interface (GUI) enabling you to arrange and collaborate with ECG Samples over a USB association.

V.CONCLUSIONS

As we probably am aware current ECG Monitoring Systems are cumbersome having with complex wired structure, in this examination paper we have proposed an ease ECG Monitoring System utilizing shrewd gadgets (Smart telephone/PC). As examined before, this framework brings numerous favorable circumstances to both the patients and specialists. Patients can screen their ECG signal chart at home without sitting around idly in voyaging. With the assistance of such framework patients can have moment recording of their ECGs and this can be imperative to spare the life of Cardiac patient before the Cardiac sickness achieves its last stage. This paper shows a model for ECG waveforms observing utilizing shrewd device (Mobile/Laptop) which performed great with both typical and strange ECG waveforms. This model of the proposed framework gives the Monitored ECGs on Patients Smart gadget for further enhancement in venture following Features can be included in future:

1. ECG screen framework dependent on android advanced mobile. ECG signal is transmitted to an android telephone and at that point be sent to a remote server. Utilizing a PC, specialists can see the ECG in the wake of signing in the server. In this framework, Android telephone is sending ECG signal all when the framework is running, which could cause a ton of intensity and system utilization. There is an extension in future to improve the power utilization and system utilization quality.
2. ECG waveforms should be send by MMS or email in any case, if picture goals isn't high specialists won't have the capacity to see it on right time. This impediment ought to be defeated in future extension.

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Design and Implementation of Remotely Located Energy Meter Monitoring with Load Control and Mobile Billing System through GSM

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Abstract— **Electricity, the most usable form of energy is used widely through the whole world. With the evolution of modern technology, the usage of electricity is escalating gradually. But the production of electricity is confined due to deficiency of resources. So power must be used in a concise way. In many countries, electrical energy is measured by energy meter which is inspected by a human. According to their inspection, the electric bills are prepared and most often these are prepared on the basis of assumption which could be inaccurate, costly, time-consuming as well as error prone. Due to the absence of regular monitoring system, sometimes consumer use electrical energy month after month without paying any bill. Energy meter monitoring and digital billing system is a kind of system which would be able to avoid traditional meter reading, save human resources, improve the accuracy and prevent the power theft. In this paper, a remote monitoring of energy meter and digital billing system is inaugurated through GSM 900. For monitoring server, major programming languages had been introduced to relate the methodologies, execute logical functions, store data in a database and send the monthly bill to the consumer cell phone number and finally disconnect the unpaid consumer.**

Keywords—GSM 900, Server, Bill, Energy meter, Electricity

I. INTRODUCTION

Electricity, one of the most important sectors for the economic development of a country is used for the various purposes. In the perspective of Bangladesh; energy infrastructure is quite small, insufficient and poorly managed. The installed electric generation capacity was 10289 MW in January 2014 only three-fourth *of* which is considered to be available. Problems in the Bangladesh's electric power sector are included many technical and non-technical losses. Meter tampering, illegal means of electricity bill payment and so on are included in the non-technical loss. Due to this non-technical reasons 5-7% power losses of total generated power.

Besides this, the residential meter billing system is not appropriate due to the irregular inspection of the meter data and most often these bills are prepared from assumption. That's why consumer has to suffer for this inconsistent billing though they use the approximately same energy in each month. Based on the above requirements, the network meter-reading management system is developed. This system is based on network technology, automatic meter-reading technology, and modern management ideas, which can realize the energy consumption management to be controllable, adjustable and predictable [1]. A prior billing is bound to do away with the problems of unpaid bills and human error in meter readings, thereby ensuring justified revenue for the utility [2].

To resolve this issue, digital energy metering system has been introduced but this technology is not capable of removing all the problems mentioned earlier. There needs modification of this system where instantaneous monitoring and digital billing system have to be added.

In the traditional electro-mechanical and digital metering system, electric energy is inspected by person and most often they prepared the bill through assumption based on his history of electricity consumption. Maybe the consumer has not utilized the similar amount of electricity in the current month as in the previous months for reasons such as, holidaying elsewhere or being in the hospital, etc. This method of billing is also not suitable for the electricity supply company because it gives an inaccurate account of the overall power consumption in the consumer's area and may ultimately result in errors in future planning by the company [3]. Over the past years, metering devices have gone through many improvements and become more complicated with more features and functions. Electromechanical Meter has very little accuracy and lack of reconfigurability. There are so many problems require utility companies to overcome such as electricity theft, meter modifications and more. Furthermore, meters are limited to provide the amount of energy consumption on consumer’s premises [4]. Though there were introduced pre-paid metering system in several areas in Bangladesh, the monitoring system is not available and as the unit has to buy before the usage, the consumers may not fix the amount of unit which they have to buy and that's why uninterrupted power is not ascertained[5]. Today most of the utilities companies are looking for solutions to overcome these disadvantages. The proposed system replaces traditional meter reading methods and enables remote access to existing energy meter by the authority. Also, it can monitor the meter readings regularly without the person visiting each house. A GSM 900 module is integrated with electronic energy meter of each entity to have remote access to the usage of electricity and create a wireless network shown in *Fig. 1*.

Wired techniques belong a lot of hurdles such as installation problem, complexity and cost also matter in the case of a long haul. In rural Areas, it is really sophisticated to install the wired system to convey the information. Due to the limitations of range and also of the efficiency, Bluetooth, Wi -Fi, Infrared are not well suited for data trans receiving. In this perspective, the wireless system based on GSM/GPRS is well known. It can play a vital role in load forecasting, complex tariff rate set up, cash card bill payment, system protection, and power

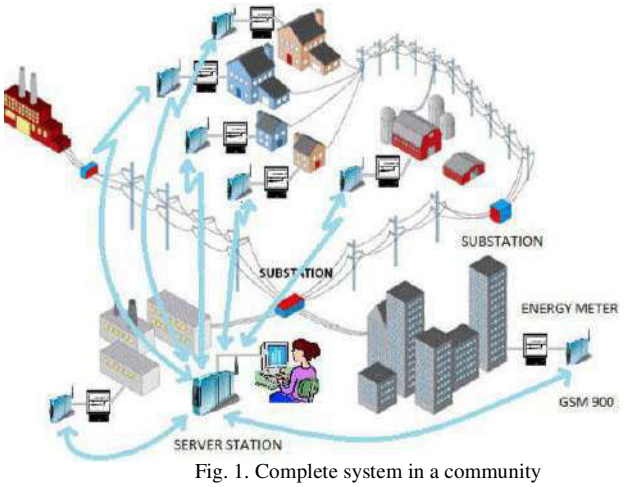

Fig. 1. Complete system in a community

stealing defense. This system is more user-friendly, reliable, accurate, and cost-effective.

II.RELATED WORKS AND MOTIVATION

The present system of energy metering as well as billing in Bangladesh which uses electromechanical and somewhere digital energy meter is error prone and it consumes more time and labor[6]. Billing automation systems for public utilities (e.g. electricity, gas and water) have been widely studied and implemented in developed countries across the world. The modern era of Automated Meter Reading (AMR) started in 1985; since then different techniques have been utilized to get better reliability and performance [7]. Therefore currently in developed countries, many successful AMR systems are being used to facilitate the consumers of water, gas or electricity. Reference [8], [9], [10] have proposed AMR using GSM network. In this system, the GSM network is used in the AMR to send the data using GSM modem by sending Short Messaging System (SMS) containing the information of the total power usage reading [11],[12]. Reference [13] inaugurates a secure and scalable automated meter. This project uses existing local ISPs instead of requiring its own set of proprietary communication infrastructure. It consists of an embedded microprocessor system, based on embedded Linux, and a modem. Distributed structure based on wireless sensor networks are comprised of measure meters, sensor nodes, data collectors (gateway), management center (server) and wireless communication network. Communication systems based on ZigBee communication network is employed in the remote real-time automatic meter reading system[3],[14],[15],[16].

GPRS based AMR is installed in remote locations near HT, LT consumers, DTRS and FEEDERS. In the AMR in 3-phase 4-wire meter, the communication from a modem to meter use RS-232 and from a modem to server the communication is done using GPRS[17].

III.LIMITATIONS OF EXISTING AMR SYSTEMS

No scalability and weak security are the two disadvantages of current and traditional AMR systems, based on centralized point-to-point modem or radio connections. A pool of modems is required in the central system to collect and process all energy meter value for the parallel accession to any meters as possible. For the acquisition of hundreds of thousands of meters value in every minute this system is not very well scaled. The radio based system can be intercepted and the regular Internet protocol is not secure unless an alternative secured protocol such as https is used [18]. Besides these, in bill payment system these systems are incapable of mitigating the problems mentioned above. The human error can open an opportunity for corruption done by the human meter reader. So the problem which arises in the billing system can become inaccurate and inefficient.

IV.METHODOLOGY

The system proposed in this paper is divided into two sections.

1. Consumer end
2. Server end

In server end a GSM modem with other necessary circuitry is installed in all consumers' premises. Data acquisition from energy meter the blinking LED of a meter is used. From energy meter specifications the per unit LED impulse rate can be achieved. Impulse rate of energy meter used in this project is 1600imp/Kwh. So per 0.000625Kwh LED will give one impulse. In this system, LED impulses are sensed by LDR. This LDR and LED complete setup were enshrouded with a black cover so that the external light source can't effect on the functionality of the LDR. For each impulse the resistance value of LDR is changed and changing of current is measured by Arduino Mega 2560. Arduino Mega 2560 count 16 pulses and calculate used energy and add 0.01Kwh with previous data.

Let, Pervious used energy = 0.25Kwh.

For each LED impulse KWH is = 0.000625Kwh After

16 LED impulse KWH is = 0.000625Kwh × 16

= 0.01Kwh

Total used energy after 16 LED impulse = (0.25 + 0.01) Kwh

= 0.26Kwh

After 16 LED impulses, the total used energy is displayed in LCD and sends to the server through GSM 900 by an SMS containing the information of meter id and currently usage energy. The equation given bellow calculates Bill.

Regular Bill = (Current Used Energy – Paid Used Energy) ×Per Unit Cost.

In server end, this SMS is received by another GSM 900 module as a string. This string is segmented and a program in

C# form application execute many logical and arithmetical functions to achieve required information such as Meter issue date, Paid used energy, Last date of payment, Payment status, Present used energy and bill shown in *Fig. 2.*In the server, all information about the consumer is stored in Mysql Database.

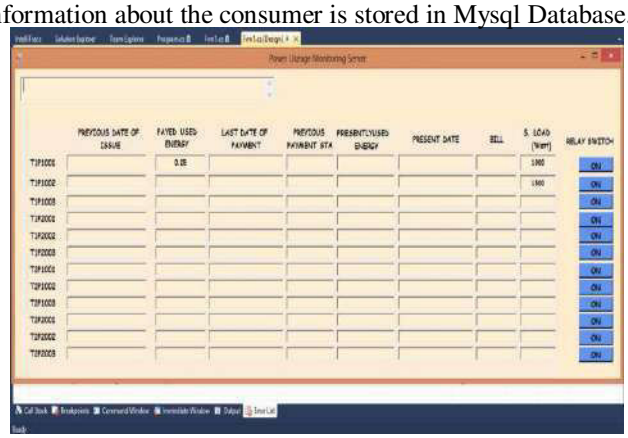

Fig. 2. C# Form application with different information about consumer

The consumer can check his previous used energy status from database in server shown in *Fig. 3.*

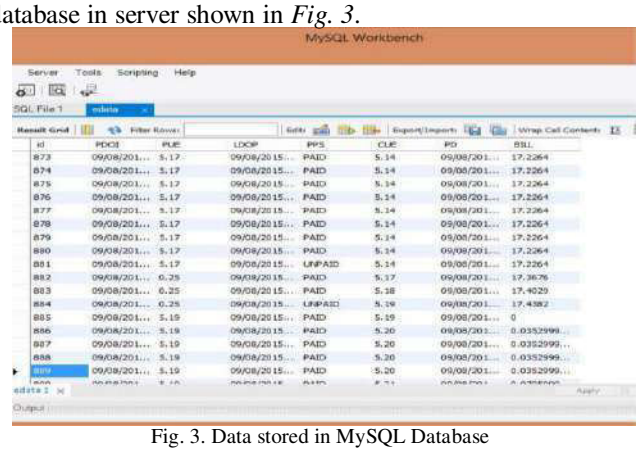

Fig. 3. Data stored in MySQL Database

V. BLOCK AND FLOW DIAGRAM

There are two-way communications between the consumer end and server end. So the whole system has two parts, one is consumer unit and the other is server unit. *Fig. 4* shows the block diagram of consumer unit which consists of energy meter, Arduino, GSM module, LCD, interrupting relay for developing the system particular work.

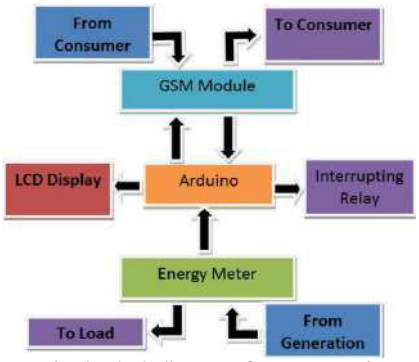

Fig. 4. Block diagram of consumer unit

From the consumer unit, the information of energy usage will be sent to the server unit through the GSM module. In consumer unit, there are interrupting relay and LCD. *Fig. 5* shows the block diagrams of server unit where GSM module, Arduino Mega 2560 and server computer also exist.

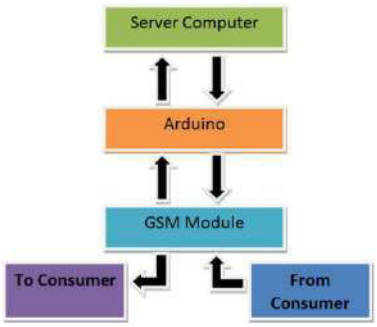

Fig. 5. Block diagram of server unit

In server unit, GSM modem interfaced with a computer which always receives SMS from consumer end and many logical functions are executed by it to display information about the user, used energy and bill status. From *Fig.6* a flowchart has given to describe the whole system briefly. By pressing the start button, the energy meter will be initialized and then the data will be acquired from the blinking of LED where each pulse will contain a specific amount of energy. After performing arithmetic and logical operation this data will be shown in a LED display for the easy inspection of the consumer. Then the acquired data will be processed and then transmit through the GSM to the server unit. The server unit GSM module will receive the transmit data and by processing this received data it will be shown on the server computer. The received data will be updated gradually and then stored in the database after performing the arithmetic and logical operation.

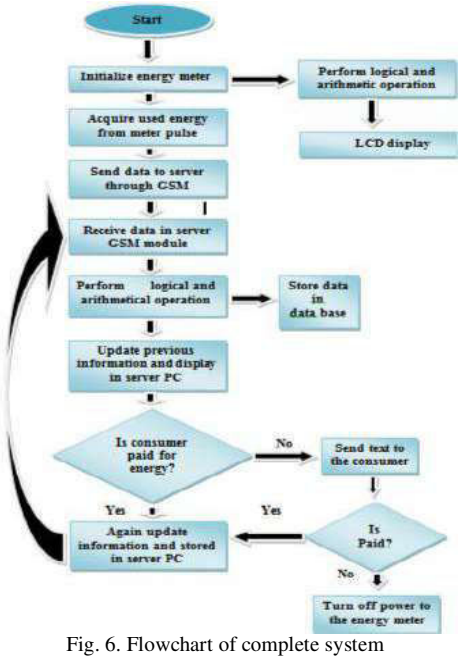

Fig. 6. Flowchart of complete system

After a given period as per the consumed power, the amount of bill will be prepared for every consumer and it will be notified the consumer by sending SMS from the server. If any customer is unable to pay the bill within a period his/her energy meter will be disconnected by initiating the interrupting relay. Whenever the consumer would be able to pay his/her previous bill, the interrupted line will establish its connection by getting a command from the server.

VI. HARDWARE IMPLEMENTATION

In server unit, shown in *Fig. 7* a GSM module and a server computer .is used. The GSM module receives data from the consumer energy meter and this received data will be uploaded to the server.

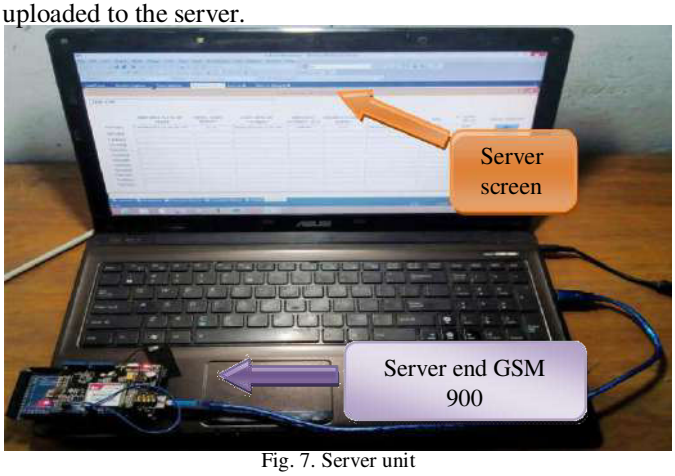

Fig. 7. Server unit

In consumer end, the arrangement consists of load, energy meter, LCD, GSM module etc. Each of the units has specific work and thus comprising the whole consumer end system. Consumer unit system is shown in *Fig. 8.*

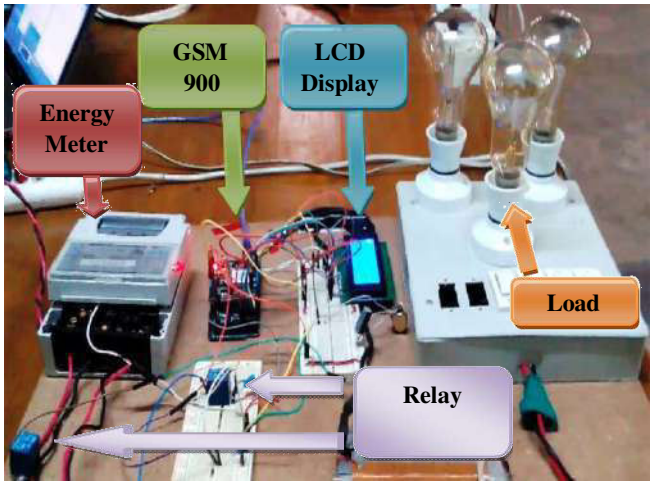

Fig. 8. Consumer Unit

After a month Bill SMS is received by consumer like as in *Fig. 9(left).* It informs consumer the used energy in last month and bill. The process of paying bill is also presented in *Fig. 9(right).* If the bill is not paid within due time operator of the server can easily isolate consumer load by remotely operating relay.

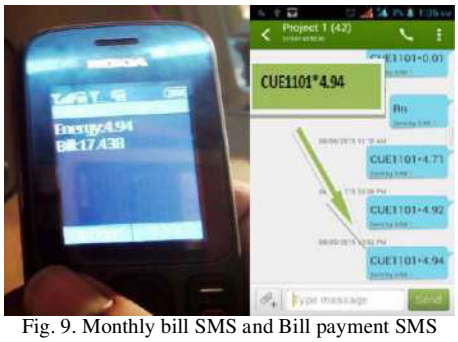

Fig. 9. Monthly bill SMS and Bill payment SMS

Hence the total implemented cost of the proposed system was approximately 17000BDT for a single user and server.As one server which cost 9000 BDT to build, can be used to monitor multiple users, the consumer has to pay approximately 8000 BDT to set up the meter. Large of this amount were spent on buying energy meter, GSM module, and Arduino accordingly.

VII. SYSTEM ANALYSIS

Based on SMS for data transmission, there is propagation delay between the relay command and relay response. *Table. 1* incurs the delay time after the execution of a command.

Table. 1.Relay Response analysis

Relay Response	Time(s)
Response 01	7.98
Response 02	7.33
Response 03	8.26
Response 04	7.75
Response 05	7.69
Response 06	6.98
Response 07	7.88
Response 08	7.39
Response 09	7.26
Response 10	6.68

Fig. 10 shows the graphical interpretation of relay circuit operation with respect to time.

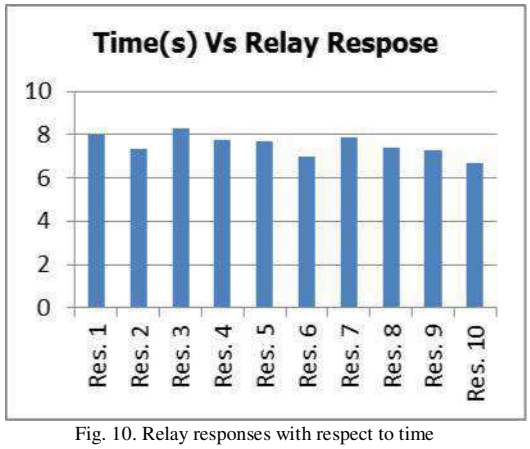

Fig. 10. Relay responses with respect to time

Table.2 shows the intermittent time between two sent SMS.

Table. 2.Time elapsed between two sent SMS

Load(watt)	Time between two SMS(s)
200	194.72
400	92.16
600	67.2
1100	24.48

It can be inferred from the graph in *Fig. 11* that with the increasing of load the time elapsed between two sent SMS decreasing.

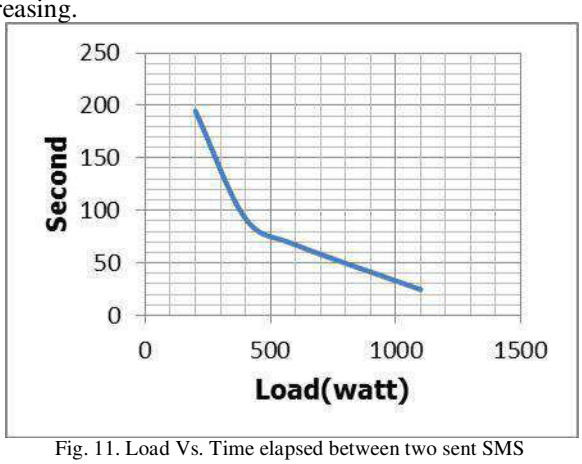

Fig. 11. Load Vs. Time elapsed between two sent SMS

VIII. SYSTEM SIMULATION

Proposed system in this paper is simulated in both Proteus and Matlab (version R2013a) and in Matlab, the required blocks are in the Simulink. The aim of this work is to monitor the remote load created in Matlab/Simulink. The whole system consists of two parts: consumer and monitoring server.

A. Consumer

The modeling of consumer end comprises a power source, voltage and current measuring units and loads. The distributed loads in *Chittagong University of Engineering And Technology (CUET)* campus were used for the simulation data mentioned in *TABLE. 3.*

TABLE. 3. Load distribution in CUET campus

Load	Average voltage (Vrms)	Frequency (Hz)	Real power (kW)	Reactive power (kvar)
12-storied building	226	50	33.93	17.33
Teachers and officers' quarters	225	50	32.6	22.07
VC office and pre-engineering building	227	50	46.22	18.31
Student hall	227	50	55.6	17.53
Pump	227	50	22.72	10.99
PME building, bank, and canteen	230	50	32.67	8.74

These data are used in *Fig. 12* simulation of consumer end.

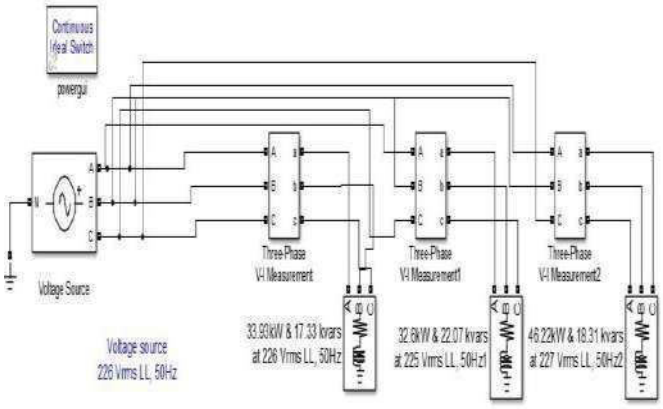

Fig. 12. Matlab simulation of Consumer end

The voltage and current signals are sent from the V-I measurement block by specifying them a different identity to capture them in the receiver block.

B. Monitoring server

The control server consists of receiving unit, power measuring unit and display unit. The combinations of these units are given *Fig. 13.*

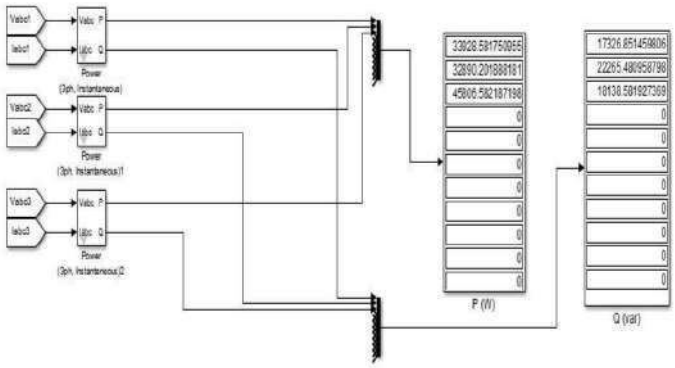

Fig. 13. Monitoring server

The receiver block receives the signal from the consumer end V-I measurement block according to their specification and then processed in the power block to separate the real power and reactive power.

C. Proteus simulation

The system is also simulated in Proteus(Version 7.2). The *Fig.14* shows the system consumer unit where we use Arduino mega symbol, a serial port which is connected with Arduino Rx-Tx line for data communication. In this circuit, the relay is used for interrupting the circuit operation from the live line.

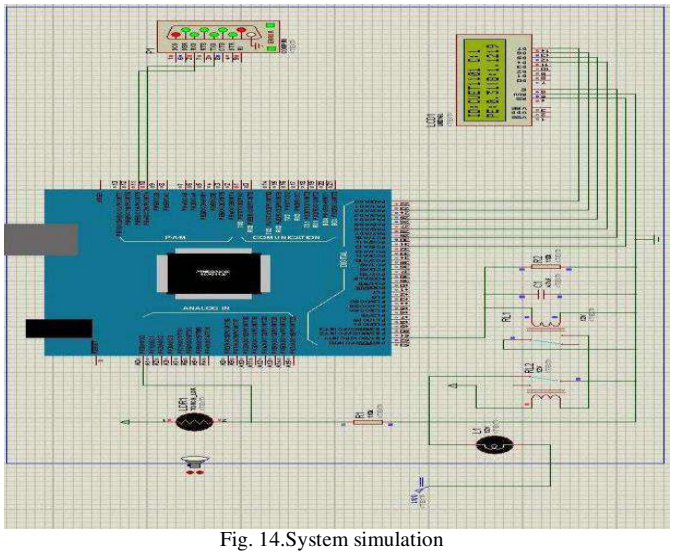

Fig. 14.System simulation

There is also an LCD monitor that shows the instant state of the meter unit, bill and also counting the pulse.

IX. SYSTEM SPECIFICATION

For the advancement of the digital billing system, our system is one step ahead with a new beneficial feature for the consumer as well as the energy provider along with regular monitoring and remote load controlling which has ensured the system reliability than the previously developed system.

X.CONCLUSION

For proper management of electrical energy as well as to raise the level of consciousness among the people about the usage of electrical power precisely, smart metering is the best solution on this aspect. Regular monitoring of load and digital billing system gives the measurement system more reliability and accuracy. Development of smart metering with the use of GSM technology provides enormous advantages over the previously developed system. The system data transmission is based on the standard SMS rates. Thus the charges are independent of the duration of the data transmission. The ability of this scheme is to eradicate the drawback of serial communication that makes the system more efficient. The prime prospect of this project is to implement wireless computerized monitoring and mobile billing system. Seemingly this system will prevent the power theft by tempering the energy meter as for regular monitoring it. Moreover, it helps to lessen the required workforce for meter readings as well as also decreasing human error factor almost nil, since the reading of meter is digital now. Thus the power provider company will be profited instead of incurring losses. However, the generated bill will be available to the consumer through SMS. Therefore a cost efficient and easily comprehensible service of automatic meter reading and digital billing system is ensured.

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INTEND AND ACCOMPLISHMENT OF AUTOMATIC INSINUATION FOR WASTE SUPERVISION USING IOT IN SMART CITIES

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Abstract – The new era of Web and Internet of Things (IoT) paradigm is being enabled by the proliferation of various devices like RFIDs, sensors, and actuators. mart devices (devices having significant computational capabilities, transforming them to 'smart things') are embedded in the environment to monitor and collect ambient information. In a city, this leads to Smart City frameworks. Intelligent services could be offered on top of such information related to any aspect of humans' activities. A typical example of services offered in the framework of Smart Cities is IoT-enabled waste management . Waste management involves not only the collection of the waste in the field but also the transport and disposal to the appropriate locations. In this paper, we present a comprehensive and thorough survey of ICT-enabled waste management models. Specifically, w e focus on the adoption of smart devices as a key enabling technology in contemporary waste management . This report on the strengths and weaknesses of various models to reveal their characteristics . This survey sets up the basis for delivering new models in the domain as it reveals the needs for defining novel framework s for waste management.

Index Terms – Internet of Things; Smart Cities; Waste Management

I. INTRODUCTION

BY 2050, the vast amount of earth population (i.e., 70%) will move to urban areas, thus, forming vast cities [1]. Such cities require a smart sustainable infrastructure to manage citizens' needs and offer fundamental and more advanced services [2]. The adoption of Future Internet technologies enhanced by the use of the Internet Protocol (IP) on numerous wireless sensors enables the Internet of Things (IoT) paradigm. Numerous sensors have the opportunity to be part of Wireless Sensor Networks (WSNs). When WSNs are applied in a city, they are responsible for collecting and processing ambient information and, thus, to upgrade legacy city infrastructure to the so-called Smart Cities (SCs). A definition of the concept of SC is provided in [6]: "A Smart City is a city well performing in a forward-looking way in the following fundamental components (i.e., Smart Economy, Smart Mobility, Smart Environment, Smart People, Smart Living, and Smart Governance), built on the 'smart' combination of endowments and activities of self-decisive, independent and aware citizens". This definition incorporates the fundamental component of a smart environment which is mainly adopted for systems dealing with environmental pollution. The concept of smart environments depicts the ambient intelligence found in a SC through the adoption of smart devices and wireless networks. This way, intelligent applications could be delivered on top of such infrastructures. WSNs are capable of reforming activities in a SC in every aspect of daily life [3]. In this paper, we focus on a specific application domain, waste management.

The efficient management of waste has a significant impact on the quality of life of citizens. The reason is that waste disposal has a clear connection with negative impacts in the environment and thus on citizens' health.

Fig1:Dust Overflow

In this paper, we gain from our research study of the waste surveillance problem in the city of St. Petersburg, Russia. St. Petersburg is a city of 5 million citizens covering a total area of 1,439 square kilometers, a density of 3,391 citizens per square kilometer. On average, solid waste produced in the city is 1.7 million tunes per year. The daily amount of municipal solid waste generated is 0.93 kilograms per citizen. On a daily basis, the municipality of St. Petersburg uses 476 waste collection trucks with a capacity of 5 tons per truck. The fuel consumed in one year is, on average, 1.8 million

liters. The average costs spent for fuel in one year for waste collection is more than 1 million US dollars. Finally, the traffic congestion activated by the fleet of waste collection lorries at rush hour is significant as an outcome of the slim highways and little backyards, producing indirect problems in individuals' jobs. Plainly, it is essential to efficiently look after the waste done away with in every location of a SC not simply focusing on the collection jobs yet also on its transport and reusing.

We model the waste management as a set of services on top of an IoT infrastructure in a SC. These services cover the following parts of a waste management scheme:

(i) Waste collection planning and implementation (e.g., routing solutions for collection trucks, dynamic adaptation of routes).

(ii) Transport of waste to specific locations (e.g., routing according to the type of waste).

(iii) Recycling and preparation for re-use. In this paper, we focus on the first type of services i.e., efficient planning of waste collection activities. We also focus on dynamic models on contemporary waste collection with the proliferation of Radio Frequency Identification (RFID), sensors and actuators [4].

Several devices have been adopted for enabling the efficient implementation of the dynamic waste collection e.g., RFID tags, sensors and actuators. With the term dynamic, we denote the ability of a system to change, in real time, the parameters and the techniques that affect the collection of waste throughout the collection job. Such functionalities could be incorporated into an intelligent transportation framework that results in real time directions provided to the collection trucks. Intelligent transportation contributes to dynamic waste collection since it uses smart vehicle infrastructure, which is incorporated in this research [5]. Specifically, we present a comprehensive survey on the adoption of Information and Communication Technologies (ICT) in waste management models focusing on the modern ICT tools and technologies. We survey a substantial body of knowledge, thirty-two case studies. Among them, only six models involve an IoT-enabled technology. We argue that waste management solutions should be adopted as the back-end middleware to support further inference and reasoning on top of the data coming from sensors. We also discuss a taxonomy of the studied models and, thus, we are able to compare the strengths and weaknesses of each one. A SC could incorporate various models to enable new services or efficient redesign of the existing services [8]. For instance, in the waste collection process, static models could be transformed to Waste Collection as a Service (WCaaS) which enables online dynamic scheduling and routing of the collection trucks [9].The dynamic waste collection could be described as an online decision process for defining: (i) when to collect waste from bins (i.e., scheduling), and (ii) which routes the collection trucks should follow (i.e., routing). Many technologies and hardware are already used in waste management adopting different approaches in the management of the physical infrastructure as well as the data collected in the field. For instance, the IoT hardware and technology could identify real objects and transforms them to 'smart things' [10].

The rest of the paper is structured as follows. Section 2 discusses the intelligent waste management and proposes a taxonomy adopted to compare waste management models. Section 3 reports on the survey of relevant models and the comparative assessment. Section 4 concludes the paper and discusses future work.

II. EXISTING SYSTEM

Generally the population in the urban areas is increasing day by day. These leads to the more needs of the citizen in the urban areas. as the population is increasing the amount of the waste produced is also high. then the surroundings get dirty casually. this leads to severe attack on environment if it is not reused and there by effects on citizen's health.

III.PROPOSED SYSTEM

This survey's focus is on more energy-efficient IoT as an enabler of various applications including waste management. Specifically, it aims to present a large set of models dealing with the efficient waste management. Special attention is paid on the waste collection. It present efforts for the intelligent transportation within the context of IoT and Smart Cities for waste collection.

They propose an inductive taxonomy to perform comparative assessment of the surveyed models. It focus only on efforts that incorporate ICT models for waste collection They report on the strengths and weaknesses of various models to reveal their characteristics. This survey sets up the basis for delivering new models in the domain as it reveals the needs for defining novel frame works for waste management.

A. Block Diagram

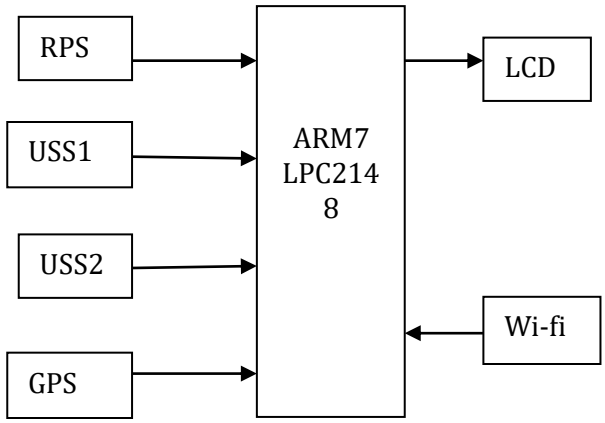

Fig2;Block diagram

MODULES DISCRIPTION:

(i). ARM LPC2148 Micro Controller:

ARM LPC2148 is a 64 pin Micro Controller which comes under ARM 7 version of ARM processors. It comes under the processor core architecture ARM7TDMI-S.It is a 32 bit Micro Controller .This is intended for high end applications involving complex computations. It follows the enhanced RISC architecture. It has high performance and very low power consumption. It has serial communications interfaces ranging from a USB 2.0 Full Speed device, multiple UARTS, SPI, and I2Cs. Various 32-bit timers, dual 10-bit ADC(s), single 10-bit DAC,PWM channels and 45 fast GPIO lines with 9 interrupt pins.

(ii).Regulated power supply:

Power supply is a supply of electrical power. A device or system that supplies electrical or other types of energy to an output load or group of loads is called a power supply unit or PSU. The term is most commonly applied to electrical energy supplies, less often to mechanical ones, and rarely to others.

A power supply may include a power distribution system as well as primary or secondary sources of energy such as Conversion of one form of electrical power to another desired form and voltage, typically involving converting AC line voltage to a well-regulated lower-voltage DC for electronic devices. Low voltage, low power DC power supply units are commonly integrated with the devices they supply, such as computers and household electronics.

(iii).Ultrasonic sensor:

Ultrasonic sensors emit short, high-frequency sound pulses at regular intervals. These propagate in the air at the velocity of sound. If they strike an object, then they are reflected back as echo signals to the sensor, which itself computes the distance to the target based on the time-span between emitting the signal and receiving the echo. As the distance to an object is determined by measuring the time of flight and not by the intensity of the sound, ultrasonic sensors are excellent at suppressing background interference. Virtually all materials which reflect sound can be detected, regardless of their color. Even transparent materials or thin foils represent no problem for an ultrasonic sensor. Micro sonic ultrasonic sensors are suitable for target distances from 30 mm to 10 m and as they measure the time of flight they can ascertain a measurement with pinpoint accuracy. Some of our sensors can even resolve the signal to an accuracy of less than 0.18 mm. Ultrasonic sensors can see through dust-laden air and ink mists. Even thin deposits on the sensor membrane do not impair its function. Sensors with a blind zone of just 30 mm and an extremely narrow beam spread are finding totally new applications these days: measuring levels in yoghurt pots and test tubes as well as scanning small bottles in the packaging sector - no trouble for our sensors. Even thin wires are reliably detected.

- And also it offers excellent non contact range detection with high accuracy and stable readings in an easy way to use package from 2cm to 400cm or 1'' to 13'' feet.

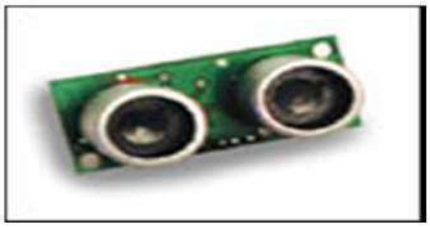

Fig3.Ultrasonic Sensor Module

(iv).GPS: (Global Positioning System):

The Global Positioning System (GPS) is a burgeoning technology, which provides unequalled accuracy and flexibility of positioning for navigation, surveying and GIS data capture. The GPS NAVSTAR (Navigation Satellite timing and Ranging Global Positioning System) is a satellite-based navigation, timing and positioning system.

The GPS provides continuous three-dimensional positioning 24 hrs a day throughout the world. The technology seems to be beneficiary to the GPS user community in terms of obtaining accurate data up to about100 meters for navigation, meter-level for mapping, and down to millimeter level for geodetic positioning.

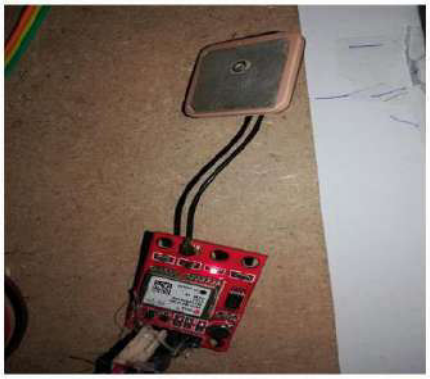

Fig4; GPS module on condition

LCD DISPLAY:

One of the most common devices attached to a micro controller is an LCD display. Some of the most common LCD's connected to the many microcontrollers are 16x2 and 20x2 displays. This means 16 characters per line by 2 lines and 20 characters per line by 2 lines, respectively.

(v).Software tools:

Keil: Keil Software launches amongst the ideal entire improvement tool collections for ARM7 software program application, that's utilized throughout endeavor. For development of C code, their Developer's Kit product has their C51 compiler, in addition to a contained ARM7 simulator for debugging. A discussion layout of this thing is conveniently offered on their website, yet it consists of numerous challenges.

The C program language produced computer systems, although, along with say goodbye to embedded structures. It does presently not maintain straight acquire admission to register, neither does it make it possible for the checking out in addition to developing of singular bits, exceptionally essential needs for ARM7 software program application. In addition, a great deal of software program application designers are acquainted with producing packages that will done by utilizing a working gadget, which makes use of system calls the program can additionally use to access the tools.

However, a bargain code for the ARM7 is produced for straight use at the cpu, without an running manufacturer. To maintain this, the Keil compiler has in fact provided countless developments to the C language to transform simply exactly what would certainly probably have in fact typically been implemented in a device phone conversation, along with the connecting of interrupt instructors. The intent of this manual comparable method supply a summary for the restrictions of the Keil compiler, the alterations it has really made to the C language, as well as the ways to earn up those in producing software application for the ARM7 microcontroller.

Flash magic: Squint Magic is an application progressed through Embedded Systems academy to empower you to quickly gain admittance to the qualities of a microcontroller gadget. With this program you could remove private squares or the total Flash memory of the microcontroller. This item program is to an awesome degree huge for people that paints inside the electronic devices subject. A champion among the most crucial home window of the program contains 5 zones where you may locate the perfect ordinary limits in a movement to programming a microcontroller gadget. Making use of the "Exchanges" area you can pick the techniques, a particular instrument associates in your PC system. Select the COM port to be utilized and furthermore the baud cost. It is suggested that you select a diminished baud cost starting and moreover change it later on.

This shape you'll choose the particular best rate with which your gadget limits. Remembering the ultimate objective to pick which parts of the memory to oust, pick from the things inside the "Erase" area. The third stage is non-compulsory. It supplies you the chance to set a HEX data. In the succeeding section you can discover striking shows decisions, that consolidate "insist after ventures", "gen square checksums", "perform" and also others. When you're performed, tap the Start switch that might be orchestrated in the "Start" territory. The item application will irrefutably begin the device, and you'll with the limit of see the development of the procedures toward the complete of thought home window.

V. RESULTS

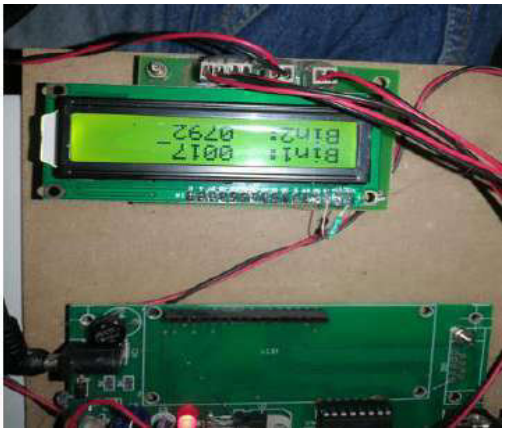

Fig5. Dust bins status.

The output results are shown in figuret7. Results can be seen from telnet application, which can be downloaded from playstore and install it. IP address can be tracked from this application. All sensor values and ouput results can be monitored in telnet application. Otherwise Ip address can be tracked by browsing IP from google. The results are shown only when thresholds are high.

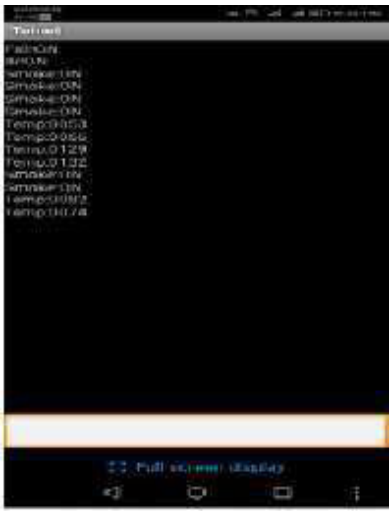

Fig6:Output results with location

VI. CONCLUSION

This survey's focus is on more energy-efficient IOT as an enabler of various applications including waste management. Specifically, it aims to present a large set of models dealing with the efficient waste management. Special attention is paid on the waste collection. We present efforts for the intelligent transportation within the context of IOT and Smart Cities for waste collection.

We propose an inductive taxonomy to perform comparative assessment of the surveyed models. We focus only on efforts that incorporate ICT models for waste collection in SC. We deliver the strengths and weaknesses of the surveyed models. Finally, our future work is focused on the definition of an effective IOT-enabled model for waste collection, which will touch on the incorporation of high capacity waste trucks as mobile depots. In addition, waste bins are placed to optimize comfort of residents. However, as part of the future work we will be looking at bin connectivity constraints that may affect their placement, for example, the output power of a communicating sensor would need to be set too high which may drain the battery faster. In this case, the bin may be placed somewhere where energy consumption is more efficient.

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OBSERVING OPERATING ACTIVITIES OF WORK VEHICLES BY USING ZIGBEE NETWORK SYSTEM

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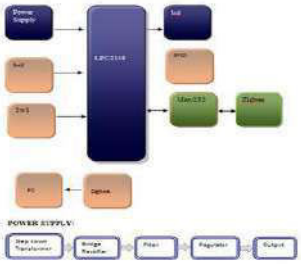
Abstract—: **Observing activities of working vehicles on a work site, such as a factory, is important in regard to managing the lifetime of vehicles and achieving high operational availability. However, it is a problem that an administrator cannot completely grasp the activities of a working vehicle. Existing systems cannot cover a large area, particularly in an indoor environment. A system is proposed for monitoring operating activities of working vehicles, regardless of whether they are operating indoors or outdoors. The system calculates the activity rate of a vehicle by analyzing the topology of a network configured by the wireless technology ZigBee. In addition, it was experimentally verified that network topology and RSSI can be used to estimate activities of working vehicles.**

Keywords— ZigBee; Sensor Network; Activity; Status;

1.INTRODUCTION

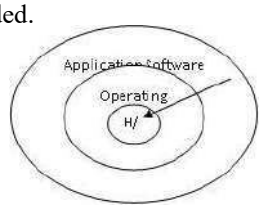
EMBEDDED SYSTEMS: Each day, our lives become more dependent on 'embedded systems', digital information technology that is embedded in our environment. More than 98% of processors applied today are in embedded systems, and are no longer visible to the customer as 'computers' in the ordinary sense. An Embedded System is a special-purpose system in which the computer is completely encapsulated by or dedicated to the device or system it controls. Unlike a general-purpose computer, such as a personal computer, an embedded system performs one or a few pre-defined tasks, usually with very specific requirements. Since the system is dedicated to specific tasks, design engineers can optimize it, reducing the size and cost of the product. Embedded systems are often mass-produced, benefiting from economies of scale. The increasing use of PC hardware is one of the most important developments in high-end embedded systems in recent years. Hardware costs of high-end systems have dropped dramatically as a result of this trend, making feasible some projects which previously would not have been done because of the high cost of non-PC-based embedded hardware. But software choices for the embedded PC platform are not nearly as attractive as the hardware.

Typically, an embedded system is housed on a single microprocessor board with the programs stored in ROM. Virtually all appliances that have a digital interface -- watches, microwaves, VCRs, cars -- utilize embedded systems. Some embedded systems include an operating system, but many are so specialized that the entire logic can be implemented as a single program



1.Overview of an Embedded System Architecture

Every Embedded system consists of a custom-built hardware built around a central processing unit. This hardware also contains memory chips onto which the software is loaded.



The operating system runs above the hardware and the application software runs above the operating system. The same architecture is applicable to any computer including desktop computer. However these are significant differences. It is not compulsory to have an operating system in every embedded system. For small applications such as remote control units, air conditioners, toys etc.

2. ARM LPC2148: The LPC2141/42/44/46/48 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combine microcontroller with embedded high speed flash memory ranging from 32kB to 512 kB. . For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty. Due to their tiny size and low power consumption, LPC2141/42/44/46/48 are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. Serial communications interfaces ranging from a USB 2.00 Full-speed device, multiple UARTs, SPI, SSP to I2C-bus and on-chip SRAM of 8 kB up to 40 kB, make these devices very well suited for communication gateways and protocol converters, soft modems, voice

recognition and low end imaging, providing both large buffer size and high processing power.
Various 32-bit timers, single or dual 10-bit ADC(s),10-bit DAC,PWM channels and 45 fast GPIO lines with upto nine

for the board to setup, once the signal is gone, the CPU starts immediately. However, if the reset signal latches these microcontrollers suitable for industrial control and medical systems nine edge or level sensitive external interrupt pins make

2.LITERATURE SURVEY

2.1.EXISTING SYSTEM

GPS is a typical way for achieving such positioning; however, it cannot be used in indoor environments because GPS signals are blocked by wallsceilings The Global Positioning System (GPS),originally Navstar GPS,[1] is a satellite-based radionavigation system owned by the United StatesUnited States government and operated by the United States Air Force.[2] It is a global navigation satellite system that provides geolocationand time information to a GPS receiver anywhere on or near the Earth where there is an unobstructed line of sight to four or more GPS satellites.[3]

Disadvantage:

It requires vehicle to be in outdoor for correct positioning.

2.2.PROPOSED SYSTEM

This system utilizes a ZigBee device attached to a working vehicle to observe the activities of the vehicle. The system collects topology and RSSI data from the network built by the ZigBee. These data are used for estimating relative positions of the working vehicles. The activity rate of each working vehicle is calculated by analysing the position information in a time-series manner. Finally, the calculated activity rate of each working vehicle is displayed.

Advantages:

1.No need of external microcomputer since ZigBee has inbuilt one in it.
2.The links between the nodes are established with probability of 95%.

3.PIPELINING

An instruction cycle has 3 stages:

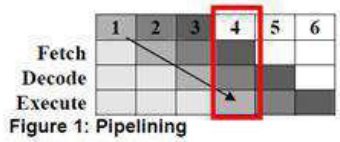


Figure 1: Pipelining

During the execution of the 1st instruction, the 2nd instruction being decode and the 3rd instruction is being fetch. See the Figure 1 below

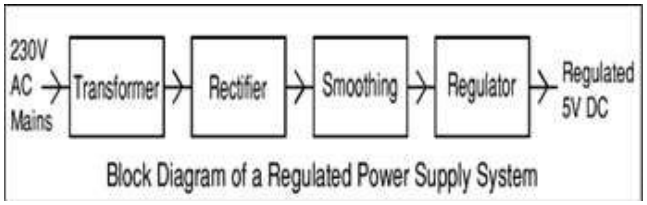
RESET AND WAKEUP TIMER:

LPC2148 can be reset in 2 ways; from the RESET button or Watch Dog Timer. taken for the board to setup, once The signal is gone, , the CPU starts immediately

wake up timer starts. During this time, the board setup itself. If the reset signal latches longer than the time However, if the reset signal latches shorter than the time taken for the board to setup, once the signal is gone, the board waits for the wake up time to finish its first loop before starting the CPU (See Figure 3).

Reset and wakeup timing diagram

4.HARD WRE REQURIED



For example a 5v regulated supply:

Each of the blocks is described in more detail below:

Transformer - steps down high voltage AC mains to low voltage AC.

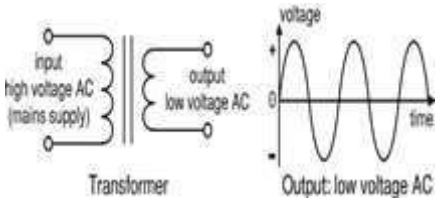
Rectifier - converts AC to DC, but the DC output is varying.

Smoothing - smoothes the DC from varying greatly to a small ripple.

Regulator - eliminates ripple by setting DC output to a fixed voltage.

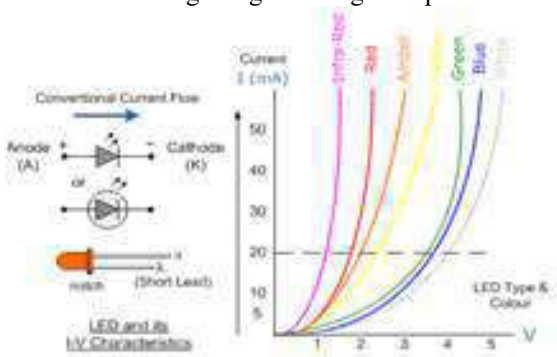
Power supplies made from these blocks are described below with a circuit diagram and a graph of their output:

4.1 TRANSFORMER ONLY



4.2 LIGHT EMITTING DIODES I-V CHARACTERISTICS

Before a light emitting diode can "emit" any form of light it needs a current to flow through it, as it is a current dependant device. As the LED is to be connected in a forward bias condition across a power supply it should be Current Limited using a series resistor to protect it from excessive current flow. From the table above we can see that each LED has its own forward voltage drop across the PN-junction and this parameter which is determined by the semiconductor material used is the forward voltage drop for a given amount of forward conduction current, typically for a forward current of 20mA. In most cases LEDs are operated from a low voltage DC supply, with a series resistor to limit the forward current to a suitable value from say 5mA for a simple LED indicator to 30mA or more where a high brightness light output is needed.

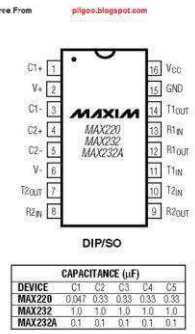


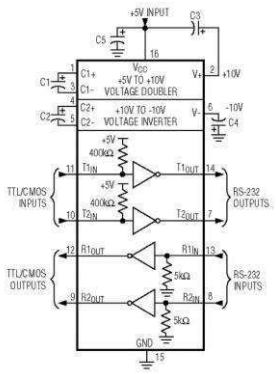
RS232 Line Type & Logic Level	RS232 Voltage	TTL Voltage to/from MAX232
Data Transmission (Rx/Tx) Logic 0	+3V to +15V	0V
Data Transmission (Rx/Tx) Logic 1	-3V to -15V	5V
Control Signals (RTS/CTS/DTR/DSR) Logic 0	-3V to -15V	5V
Control Signals (RTS/CTS/DTR/DSR) Logic 1	+3V to +15V	0V

Communication can happen right after the association. *Direct addressing* uses both radio address and endpoint identifier, whereas indirect addressing uses every relevant field (address, endpoint, cluster and attribute) and requires that they be sent to the network coordinator, which maintains associations and translates requests for communication. *Indirect addressing* is particularly useful to keep some devices very simple and minimize their need for storage. Besides these two methods, *broadcast* to all endpoints in a device is available, and *group addressing* is used to communicate with groups of endpoints belonging to a set of devices The receivers reduce RS-232 inputs (which may be as high as ± 25 V), to standard 5 V TTL levels. These receivers have a typical threshold of 1.3 V, and a typical hysteresis of 0.5 V. The later MAX232A is backwards compatible with the original MAX232 but may operate at higher baud rates and can use smaller external capacitors – 0.1µF in place of the 1.0µF capacitors used with the original device. The newer MAX3232 is also backwards compatible, but operates at a broader voltage range, from 3 to 5.5V..

PIN DIAGRAM OF MAX232

Max232 is designed by Maxim Integrated Products. This IC is widely used in RS232 **Communication** systems in which the conversion of voltage level is required to make TTL devices to be compatible with PC serial port and vice versa. This chip contains charge pumps which pumps the voltage to the Desired Level





4.3 TYPICAL APPLICATIONS

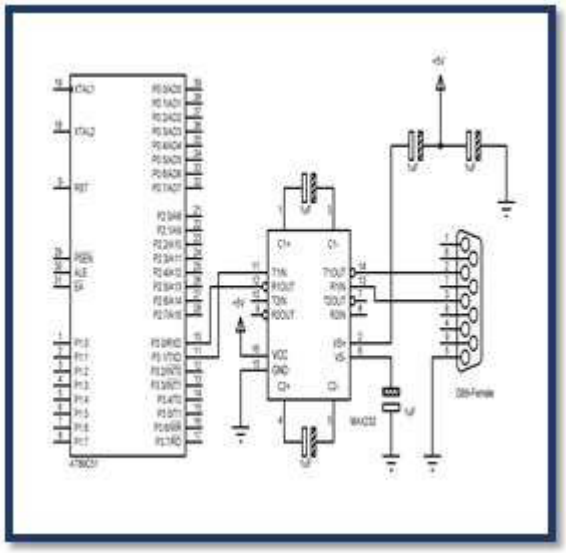
he MAX232(A) has two receivers that convert from RS-232 to TTL voltage levels, and two drivers that convert from TTL logic to RS-232 voltage levels. As a result, only two out of all RS-232 signals can be converted in each direction. Typically, the first driver/receiver pair of the MAX232 is used for TX and RX signals, and the second one for CTS and RTS signals.

4.4 VOLTAGE LEVELS

TIA-232 line type and logic level	TIA-232 voltage	TTL voltage to/from MAX232
Data transmission (Rx/Tx) logic 0	+3 V to +15 V	0 V
Data transmission (Rx/Tx) logic 1	−3 V to −15 V	5 V

Control signals (RTS/CTS/DTR/DSR) logic 0	−3 V to −15 V	5 V
Control signals (RTS/CTS/DTR/DSR) logic 1	+3 V to +15 V	0 V

It is helpful to understand what occurs to the voltage levels. When a MAX232 IC receives a TTL level to convert, it changes a TTL Logic 0 to between +3 and +15V, and changes TTL Logic 1 to between -3 to -15V, and vice versa for converting from RS232 to TTL. This can be confusing when you realize that the RS232 Data Transmission voltages at a certain logic state are opposite from the RS232 Control Line voltages at the same logic state. To clarify the matter, see the table below.

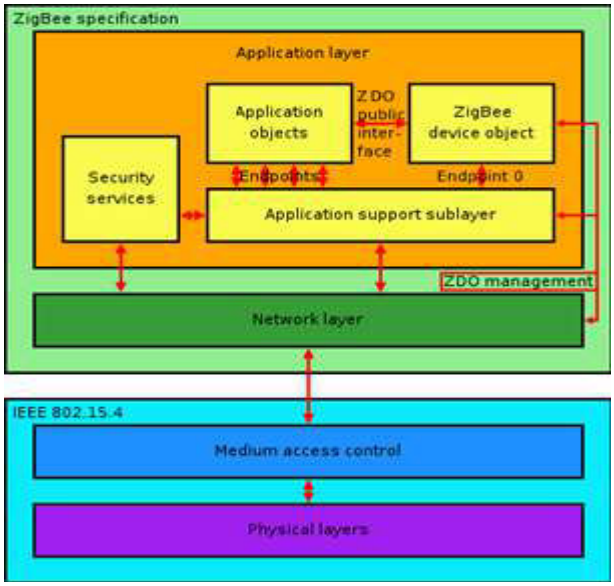


5.TECHNICAL OVERVIEW

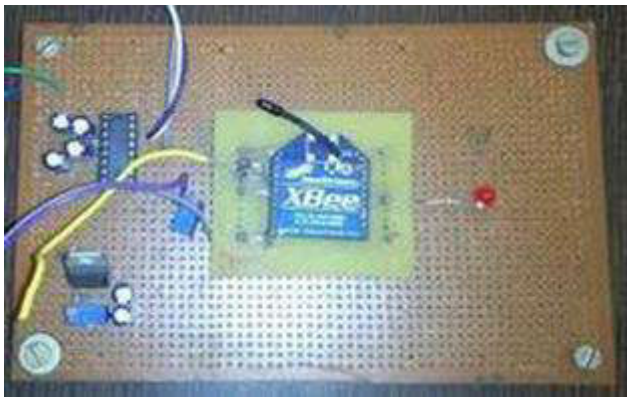
ZigBee is a low-cost, low-power, wireless mesh network standard. The low cost allows the technology to be widely deployed in wireless control and monitoring applications. Low power-usage allows longer life with smaller batteries. Mesh networking provides high reliability and more extensive range. ZigBee chip vendors typically sell integrated radios and microcontrollers with between 60 KB and 256 KB flash memory

Zigbee is a wireless technology developed as an open global standard to address the unique needs of low-cost, low-power wireless IoT networks. ... The Zigbeestandard operates on the IEEE 802.15.4 physical radio specification and operates in unlicensed bands including 2.4 GHz, 900 MHz and 868 MHz..

Zigbee is not a product, rather it is a protocol developed by the Zigbee alliance, that allows for the universal compatability of devices created by different manufacturers all over the world for use in a wireless home management system (Zigbee 2011). Zigbee's relatively low priced wireless home synchronization specification is carried over the IEEE 802.15.4 architecture (Radmand, unk)



6.ZIGBEE IN OUR PROJECT



Typical applications without special security needs will use a network key provided by the trust center (through the initially insecure channel) to communicate.Thus, the trust center maintains both the network key and provides point-to-point security. Devices will only accept communications originating from a key provided by the trust center, except for the initial master key. The security architecture is distributed among the network layers as follows:

1.The MAC sub layer is capable of single-hop reliable communications. As a rule, the security level it is to use is specified by the upper layers.

2.The network layer manages routing, processing received messages and being capable of broadcasting requests. Outgoing frames will use the adequate link key according to the routing, if it is available; otherwise, the network key will be used to protect the payload from external devices.

3.The application layer offers key establishment and transport services to both ZDO and applications.

4.It is also responsible for the propagation across the network of changes in devices within it, which may originate in the devices themselves (for instance, a simple status change) or in the trust manager (which may inform the network that a certain device is to be eliminated from it). It also routes requests from devices to the trust center and network key renewals from the trust center to all devices. Besides this, the ZDO maintains the security policies of the device.

The security levels infrastructure is based on CCM*, which adds encryption- and integrity-only features to CCM.

Chip vendors/devices include

To become ZigBee certified as a semiconductor company, vendors must ensure their applications are interoperable. Periodic interoperability events verify that devices work with other certified devices.

Atmel ATmega128RFA1, AT86RF230/231

- Digi International XBee XB24CZ7PIS-004
- Ember EM250, EM351, EM357
- Free scale MC13224, MC13226
- Green Peak GP520-GP530-GP540

KEIL SOFTWARE

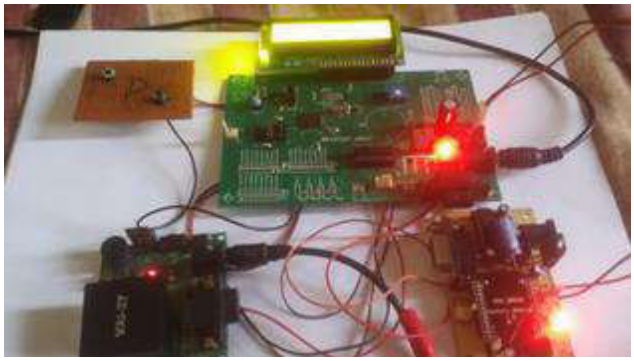
The **Keil** 8051 Development Tools are designed to solve the complex problems facing embedded **software** developers. When starting a new project, simply select the microcontroller you **use** from the Device Database and the µVision **IDE** sets all compiler, assembler, linker, and memory options for you.

KEIL SOFTWARE WORKING

KIT

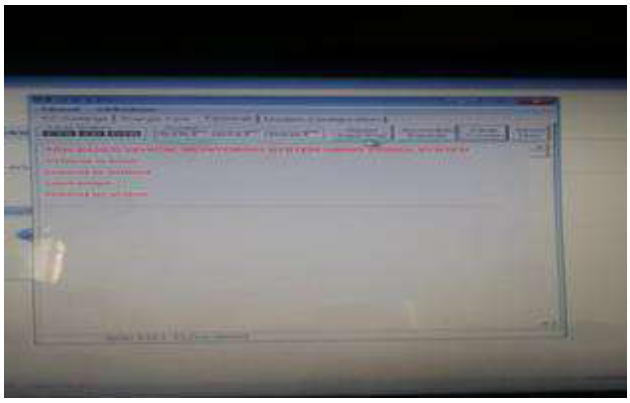
Zigbee is an IEEE 802.15.4-based specification for a suite of high-level communication protocols used to create personal area networks with small, low-power digital radios, such as for home automation, medical device data collection, and other low-power low-bandwidth needs, designed for small scale projects which need wireless connection.

TRANSMITTER



RECEIVER

OUTPUT



ADVANTAGES

By this system we can monitor the vehicle working from far distance.
Reduce the man power for machinery.
Saving the time and money.

APPLICATIONS

We can use this system in mining area.

In chemical industries.
In dangerous area, prohibited area
And used in industries like glasses making, steel mining etc..

ACKNOWLEDGMENT

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4. The author wishes to thank Key Laboratory of Shanghai On-line measurementand control technology and all colleagues who provided technical support. This work was supported by the National Science & Technology PillarProgram (Grant No. 2014BAK02B04), the Project of General Administration ofQuality Supervision, Inspection and Quarantine of the People's Republic of China(Grant No.2014QK138).

CONCLUSION

A system is proposed for monitoring the operating activities of working vehicles, regardless of whether they are operating indoor or outdoor. The proposed system determines the relative positional relationship between the working vehicle from a change in the ZigBee topology and RSSI. The topology is estimated by a combination of response-time estimation and node search (a standard function of ZigBee). It was found that the response time between adjacent devices is 30 ms or less. Based on these experimental results, an algorithm for estimating the patterns of activities of working vehicles was proposed. This algorithm was used for in an experiment on collecting topology data from AGVs. The results of the experiment indicate that the operating activities of each AGV differ according to working hours.
In the future, to grasp the activity of a working vehicle by creating an activity pattern, the proposed system will be evaluated experimentally. In addition, a function for visualizing the activity of working vehicles on a tablet will be implemented. This study was partly supported by SCAT.

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RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing

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ABSTRACT

We propose a correct multiplier that is quick yet essentialness viable. The methodology is to round the operands to the nearest case of two. Thusly the computational concentrated bit of the duplication is disposed of improving pace and essentialness usage at the expense of a little mix-up. The proposed approach is material to both stamped and unsigned increments. We propose three hardware utilization of the exact multiplier that joins one for the unsigned and two for the checked errands. The capability of the proposed multiplier is surveyed by differentiating its execution and those of some exact and correct multipliers using assorted diagram parameters. Besides, the sufficiency of the proposed exact multiplier is considered in two picture getting ready applications.

Keywords — Accuracy, approximate computing, energy efficient, error analysis, high speed, multiplier**.**

I. INTRODUCTION

Imperativeness minimization is one of the standard arrangement necessities in any electronic structures, especially the adaptable ones, for instance, propelled cells, tablets, and particular contraptions. It is exceedingly needed to achieve this minimization with irrelevant execution (speed) discipline. Propelled hail dealing with (DSP) squares are key portions of these minimized devices for recognizing diverse blended media applications. The computational focus of these squares is the math basis unit where duplications have the best offer among each calculating movement performed in these DSP systems. Thusly, improving the speed and power/imperativeness capability characteristics of multipliers expect a key part in upgrading the adequacy of processors.

A. Conversion from RBR

This table exhibits the logical estimation of each possible match of bits. As in conventional parallel depiction, the entire number estimation of a given depiction is a weighted whole of the estimations of the digits. The weight starts at 1 for the furthest right position and goes up by a factor of 2 for each next position. Generally, a RBR grants negative characteristics. There is no single sign piece that advises if a RBR addressed number is sure or negative. Most numbers have a couple of possible depictions in a RBR.

Propelled multipliers are for the most part used in number juggling units of chip, intuitive media, and electronic banner processors. Various counts and structures have been proposed to design quick and low power multipliers. A first methodology uses 4-2 blowers, while a second system uses overabundance combined (RB) numbers [1,

2]. The two systems allow the deficient thing diminish tree to be lessened at a rate of 2:1. The dreary combined number depiction has been familiar by Avizienis with perform stamped digit calculating; the RB number can be addressed in different ways. Snappy multipliers can be arranged using dull combined development trees. The abundance combined depiction has in like manner been associated with a floating point processor and realized in VLSI. Better RB multipliers have turned out than be noticeable as a result of the beneficial features, for instance, high estimated quality and pass on free extension. : NRBPPAS = [log (N/4 + 1)], = n − 1, if N = 2^n (1).

II. LITERATURE

Here, a segment of the past works in the field of correct multipliers are immediately reviewed. I an exact multiplier and a correct snake in light of a strategy named broken-display multiplier (BAM) were proposed. By applying the BAM figure strategy for to the conventional changed Booth multiplier, a correct checked Booth multiplier was presented .The exact multiplier gave control usage save finances shape 28% to 58.6% and zone diminishes from 19.7% to 41.8% for different word lengths in connection with a general Booth multiplier. Kulkarni et al. [6] proposed an exact multiplier containing different 2 × 2 misguided building deters that saved the power by 31.8%– 45.4% over a correct multiplier. An exact checked 32-bit multiplier for hypothesis purposes in pipelined processors was laid out. It was 20% faster than a full-snake based tree multiplier while having a probability of mix-up of around 14%. A goof tolerant multiplier, which enlisted the exact result by dividing the expansion into one correct and one exact part, was exhibited, in which the correctnesses for different piece widths were represented.

By virtue of a 12-bit multiplier, a power saving of over half was represented. In [3, 4], two exact 4:2 blowers for utilizing in a standard Dadda multiplier were delineated and explored.

Multipliers

Multipliers expect a fundamental part in the present propelled signal getting ready and distinctive applications. With advances in development, various researchers have endeavored and are attempting to diagram multipliers which offer both of the going with plan targets

1. High speed,
2. Low power usage,
3. Regularity of outline and hereafter less district or even blend of them in one multiplier in this way making them proper for various quick,
4. Low power and littler VLSI execution.

A. History of Multipliers

The early PC structures had what are known as increase and Accumulate units to perform enlargement between two parallel unsigned numbers. The duplicate and Accumulate unit was the most direct utilization of a multiplier. The fundamental square diagram of such a structure is given underneath.

B. Implementation

The MAC unit requires a 4-bit multiplicand select, 4-bit multiplier enroll, a 4-bit full snake and a 8-bit gatherer to hold the thing. In the figure over the thing enlist holds the 8-bit result. In a normal parallel increment, in perspective of the multiplier bit being dealt with, either zero or the multiplicand is moved and after that extra

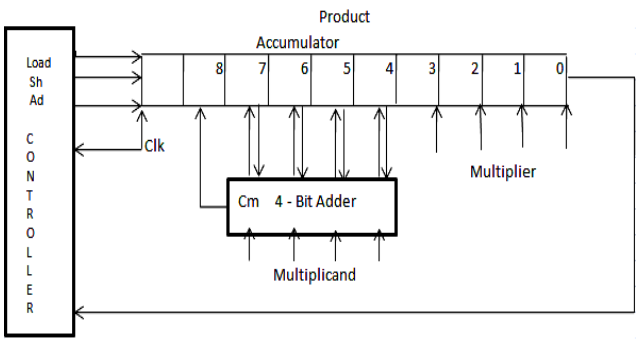

Fig. 1 Multiplier Block Diagram

III. PROPOSED ACCURATE MULTIPLIER

A. Multiplication Algorithm of RoBA Multiplier

The guideline thought behind the proposed exact multiplier is to make use of the straightforwardness of errand when the numbers are two to the power n (2n). To develop the errand of the exact multiplier, first, let us mean the balanced amounts of the commitment of An and B by Ar and Br, independently.

The growth of A by B may be altered as

$$A \times B = (Ar - A) \times (Br - B) + Ar \times B + Br \times A - Ar \times Br. \quad (1)$$

The key discernment is that the growthes of Ar × Br, Ar ×B, and Br ×A may be executed just by the move undertaking. The hardware execution of (Ar − A) × (Br − B), regardless, is to some degree stunning. The greatness of this term in the last result, which tons of the right numbers from their balanced ones, is close to nothing. Therefore, we propose to prohibit this part from (1), enhancing the expansion undertaking. Thusly, to play out the enlargement strategy, the going with enunciation is used:

$$A \times B \sim= Ar \times B + Br \times A - Ar \times Br. \quad (2)$$

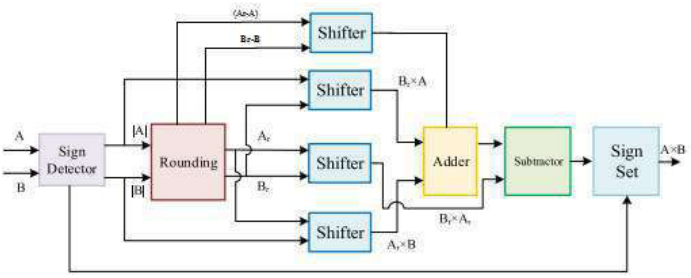

Fig. 2. Block diagram for the hardware implementation of the proposed multiplier

Therefore, one can play out the duplication action using three move and two development/subtraction errands. In this methodology, the nearest characteristics for An and B as 2n should be settled. Right when the estimation of An (or B) is identical to the 3 × 2p−2 (where p is an emotional positive entire number greater than one), it has two nearest characteristics as 2n with measure up to add up to contrasts that are 2p and 2p−1.

While the two characteristics incite a comparative effect on the exactness of the proposed multiplier, picking the greater one (except for the occurrence of p = 2) prompts a humbler gear utilization for choosing the nearest balanced regard, and from now on, it is considered in this paper. It begins from the way that the numbers as 3 × 2p−2 are considered as couldn't mind less in both assembling and down streamlining the strategy, and smaller method of reasoning enunciations may be refined in case they are used in the assembling. The principle unique case is for three, which for this circumstance, two is considered as its nearest motivating force in the proposed exact multiplier.

IV. FPGA

A. General

Consolidated circuit (IC) advancement is the enabling development for a whole host of imaginative contraptions and structures that have changed the way in which we live. Jack Kilby and Robert Noyce got the 2000 Nobel Prize in Physics for their advancement of the consolidated circuit; without the planned circuit, neither transistors nor PCs would be as fundamental as they are today.

VLSI structures are fundamentally smaller and eat up less power than the discrete parts used to make electronic systems beforehand the 1960s. Coordination empowers us to manufacture systems with various more transistors, empowering fundamentally all the more figuring ability to be associated with dealing with an issue. Consolidated circuits are moreover fundamentally less requesting to plan and make and are more tried and true than discrete structures; that makes it possible to make remarkable reason systems that are more powerful than all around helpful PCs for the activity waiting be finished.

B. Usages of VLSI

Electronic systems by and by play out a wide arrangement of errands in consistently life. Electronic systems in some cases have supplanted instruments that worked mechanically, utilizing pressurized water, or by various means; devices are for the most part tinier, more versatile, and less requesting to profit. In various cases, electronic structures have made completely new applications. Electronic systems play out a variety of endeavors, some of them recognizable, some more concealed:

- Personal beguilement structures, for instance, helpful MP3 players and DVD players perform propelled figuring's with astoundingly little essentialness.
- Electronic systems in cars work stereo structures and introductions; they also control fuel mixture structures, change suspensions to fluctuating scene, and play out the control limits required for antilock braking (ABS) structures.
- Digital equipment pack and decompress video, even at unrivaled quality data rates, on-the-fly in client contraptions.
- Low-cost terminals for Web examining still require complex equipment, notwithstanding their gave limit.
- Personal PCs and workstations give word-planning, cash related examination, and beguilements. PCs join both central dealing with units (CPUs) and excellent reason gear for hover get to, speedier screen appear, et cetera.

C. Proposed Method

We focus on proposing a high-speed low power/energy yet approximate multiplier appropriate for error resilient DSP applications. The proposed approximate multiplier, which is also area efficient, is constructed by modifying the conventional multiplication approach at the algorithm Level assuming rounded input values. We call this rounding-based approximate (RoBA) multiplier.

The proposed multiplication approach is applicable to both signed and unsigned multiplications for which three optimized architectures are presented. The efficiencies of these structures are assessed by comparing the delays, power and energy consumptions, energy-delay products (EDPs), and areas with those of some approximate and accurate (exact) multipliers.

Applications:

1. Multimedia

2. Digital signal processing

Advantages:

Area and power reduced.

CONCLUSION

In this paper, we proposed a quick yet imperativeness capable correct multiplier called RoBA multiplier. The proposed multiplier, which had high precision, relied upon altering of the commitments to the kind of 2n. Thusly, the computational concentrated bit of the expansion was ignored upgrading pace and essentialness usage at the expense of a little error. The proposed approach was proper to both stamped and unsigned increments.

Three gear use of the correct multiplier including one for the unsigned and two for the checked errands were discussed. The efficiencies of the proposed multipliers were evaluated by differentiating them and those of some exact and correct multipliers using particular arrangement parameters. The results revealed that, in most (all) cases, the RoBA multiplier models beat the relating exact (remedy) multipliers. Similarly, the ampleness of the proposed correct increase approach was analyzed in two pictures taking care of uses of sharpening and smoothing. The relationship revealed a comparable picture qualities as those of right growth estimations.

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Video Watermarking Techniques-Classifications and Applications

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Abstract— Digital watermarking is a scheme that involves in concealing the information within the signal which is translucent to the user. Video Watermarking is one among the inspiring fields to ensure the improvement of the system by facilitating the authentication of data, advertisement surveillance, safety, tracing of piracy and copyright protection procedures for digital media, concealed within dynamic video codec. Digital watermarking technology is being adopted to ensure and facilitate data authentication, safety and copyright protection of digital media. It is contemplated as the most significant technology in the modernized world, to avert illegal replication of data. Digital watermarking can be practiced on multimedia data. In this work, we emphasized particularly on the overview of different domains in video watermarking schemes, along with its definitions, properties, applications and evaluation constraints utilized to expand the security of data.

Keywords— Imperceptibility, Payload, Robustness, Compressed domain, Frequency domain.

1. Introduction

The evolution of the Internet and the augmentation of the digital multimedia technology have not only permitted the people to practice, dispense and accumulate digital content effortlessly, but also have endowed the ability of replicating it swiftly and absolutely without loss of quality, with no restriction on the number of copies, avoiding and hacking without authorization. Service providers are unwilling to extend services in digital form, even though digital data comprise various advantages in contrast to analog data, as they panic unimpeded replication and spreading of copyrighted material. The intellectual property ought to be guarded [1]-[2]. The consequences of illegal replication on a huge scale made the content creators and owners more anxious. This issue is not just theoretical. The financial damage due to illicit replication of copyrighted materials [3] runs into billions of dollars. Hence, there is an enormous requirement for the methods which can safeguard the financial value of digital video, image as well as medical image [4] ,and preserve the rights of content owners.

Illicit duplication, circulation and amendment of digitized works are infringe upon intellectual property rights. Hence authenticity and integrity with regard to digital video has become an important research area nowadays. Thus digital watermarking has come into existence for copyright protection, ownership and authentication to avert illegal copying. In addition, other methods that can ensure security to the digital content are cryptography and Steganography. Steganography and watermarking mutually appear under data-hiding techniques, i.e., they are used to hide covert information within the cover. Yet, there is a difference between Steganography and watermarking. Steganography masks the existence of covert information. Steganography arrests the continued existence of covert information while in watermarking the use of covert information can be identified. Thus watermarking makes the covert information unfeasible. Digital watermark is normally used to spot the ownership or verify the authenticity of any digital data or multimedia. As the digital copy of data is identical to the original, the digital watermarking is a security means and marks the data, but does not control the right to use it.

Earlier digital video watermarking procedures utilizing frequency domain approaches were explored, but nowadays the focus is laid on concealing the watermark in compressed format along with hybrid domain through certain amendments. The compressed and hybrid video watermarking were drawing much concentration from the period when video signals were stored and conveyed in format of packed. As the digital video carries a large quantity of details, in real period it is tough to hide the watermark into raw video.

The rest of the paper is set in the following manner. Section 2 describes the fundamentals of video and video formats. Section 3 illustrates the overview of video watermarking. Section 4 specifies different video watermarking approaches. Eventually Section 5 determines evaluation constraints and requisites of watermarking methods. Section 6 describes dissimilar applications of video watermarking. Section 7 concludes this proposal.

2. Fundamentals of Video

2.1 Digital Images and Video

An image I (x, y) is a signal which corresponds to the amount of light emanated to a spectator at the entire spatial coordinates (x, y). An analog image is a signal with continuous values, obtaining a real value at each coordinate. A digital image maintains values simply at discrete coordinates, recognized as pixels. A digital image is attained in two steps from an analog image: initially the analog image is sampled to appear as a discrete-signal; next, consequent to sampling, each and every sampled value is quantized to a particular value amongst countable group of values. All pixel values of

several images are indicated by 8 bits which allocate up to 256 discrete intensity levels. Digital video [5]-[6] is viewed as a prearranged series of digital images to facilitate the display in sequence, in addition to the subsequent audio and synchronization signals. All images of the video are recognized as a frame. Frame rate is the number of displayed frames for each unit time. Each frame is signified as two detached fields in several videos that are put on show in an interlaced or interleaved manner. Analog television makes use of the fields more intently, analogous to the interlaced scanning. In the course of presentation of the video, the synchronization signal is utilized to persist reliability, assuring that the visual and audio signals are put on view simultaneously at the accurate time.

2.2 Analog Video

A video signal can be delineated as a series of two-dimensional (2-D) images, projected from a three dimensional (3-D) object against the image surface of a video camera. The signal of analog video with continuous space and amplitude. Usually video is captured frame-by-frame by an analog camera. It also attains a frame by scanning successive lines through assured line spacing. These scanned lines in all frames are renewed into an electrical signal corresponding to the analog video signal.

2.3 Digital Video

Through sampling and quantization, or by employing a digital video camera directly, a digital video can be attained from an analog video signal. The imaged scene is sampled by a digital video camera as discrete frames. Every frame is composed of a few lines and every line is sampled to build a numeral of pixels (samples) for each line. A pixel is provided as a rectangular region through constant color. The intensity of each pixel is indicated by 8 bits (monochrome video) or 24 bits (color video). The data rate and the resolution of a digital video are determined as follows:

Data rate = (number of frames/second) × (number of lines/frame) × (number of pixels/line) × (number of bits/pixel).

Resolution = (number of pixels/line) × (number of lines/frame)

2.4 Color Spaces

The emitted or reflected light at a specific 3-D point is recorded by the color value at every part of a video frame in the observed scene. The intensity or luminance of all pixels of a monochrome video frame is specified by just a single number; but, color video frames need atleast three numbers to indicate a color value at all pixels correctly. The coordinate system that corresponds to color is signified as color space. The color value at all pixels in the RGB color space, is denoted by three foremost colors of light, Red (R), Green (G) and Blue (B)). The unlikely colors can be formed by integrating red, green and blue in proper proportions. The RGB color space is a familiar method in favor of monitor displays. The HVS does not recognize certain pictures exclusively. Consequently, a color is expressed in terms of its luminance and chrominance autonomously to make feasible more competent processing along with broadcasting of color signals. A variety of 3-component color spaces are presently available. Of these, one component corresponds to the luminance and the other two, jointly stand for hue and saturation. Y: Cr: Cb color space is admired amongst them. It is usually brought into play to specify a digital video. The YCrCb color space is the scaled and altered version of the analog YUV color space. The luminance component 'Y' is designed as a weighted average of the 3 color components R, G and B. The chrominance or color difference (Cr and Cb) components indicate the variation among the color intensity and the luminance component. Cr point to red chrominance component (Cr = R - Y) as well as Cb point to blue chrominance component (Cb = B - Y).

2.5 YCrCb Sampling Formats

When compared to RGB an imperative benefit of the YCrCb color space is that the Cr and Cb components possibly will be denoted through an inferior resolution than that of Y component since the Human Visual System (HVS) is not as much of sensitive to color than luminance. This lessens the quantity of data essential to signify the chrominance components lacking a foremost outcome on visual quality. There are a mixture of YCrCb formats, wherein the chrominance components are sub-sampled with unusual sub-sampling factors. Fig.1 illustrates three YCrCb formats that are sustained by H.264/AVC.

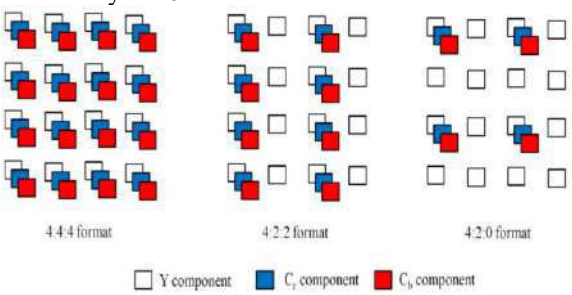

Fig.1. Sub-sampling patterns for chrominance components.

The video applications to facilitate extremely high resolutions employ 4:4:4 format. In this format, the chrominance components are sampled in precisely the equivalent resolution as the luminance components. Explicitly, every pixel location has mutually chrominance and luminance samples at full resolution. To lessen the essential data rate, BT.601 delineated 4:2:2 format, wherein the chrominance components are sub-sampled beside every line by a factor of 2, implying that there are 2 Cb samples and 2 Cr samples for every 4 Y samples. To further lessen the essential data rate, BT.601 also identifies an additional format, which subsamples the Cr and Cb components by half mutually in the vertical and horizontal directions. This is recognized as the 4:2:0 format and is exercised in video circulation, such as, movies on Digital Versatile Disc (DVD) and Video-OnDemand (VOD). The 4:2:0 format, encloses 1 Cb sample and 1 Cr sample for every 4 Y samples. 2.6 Video Formats The Common Intermediate

Format (CIF), given by the International Telecommunications Union Telecommunications sector (ITU-T), has the luminance resolution of 352 × 288. This design was extended in favor of video conferencing applications. The quarter CIF (QCIF), with half the resolution of CIF in mutually vertical as well as horizontal dimensions, is employed for mobile multimedia applications. The Source Intermediate Format (SIF) is extended for video applications entailing standard quality, such as, CD movies and video games. This format is regarded the same as CIF i.e. (352 × 288/240). There are two SIF formats: one, with the luminance resolution of 352 × 288 plus a frame rate of 25Hz, and the other, with a luminance resolution of 352 × 240 plus a frame rate of 30Hz. The Society of Motion Pictures and Television Engineers (SMPTE) has identified quite a few High Definition (HD) formats which entail huge uncompressed data. 720p HD video format has the luminance resolution of 1280 × 720. Further, 1080p HD has the luminance resolution of 1920 × 1080. Hardly any standard (pixel) dimensions on behalf of digital video frames are described in Table 1.

Table 1. General dimensions of digital video frames

Name	Luminance Pixels per Line	Luminance Number of Lines
Sub-QCIF	128	96
QCIF	176	144
CIF*	352	288
4CIF	704	576
16CIF	1408	1152
CCIR601 [145]	720	480
SMPTE 274M [146]	1920	1080
SMPTE 296M [147]	1280	720

*Common Intermediate Format

Data rate of the video is a challenge for storing or processing a digital video. An uncompressed 4:2:2 YCBCR CCIR601 video delineated by means of 8 bits/pixel and 30 frames/s, has a data rate of: [(720 Y pixels/line) × (480 Y lines/frame) +(360 CB pixels/line) × (480 CB lines/frame) +(360 CR pixels/line) × (480 CR lines/frame)]× (30 frames/s) × (8 bits/pixel) = (691 200 pixels/frame) × (30 frames/s) × (8 bits/pixel) = 165 888 000 bits/s = 20 736 000 bytes/s ≈ 70 Gbytes/hour An eminent compact disc (with more or less 650 Mbytes of storage) probably will accumulate very soon in 30 seconds of this video regardless of the detail that a DVD (with almost 17 Gbytes capacity) can save in about 15 minutes. The data rate of nearly 160 Mbits per second goes beyond the capacity in support of a range of low cost, local-area networks, such as, 10 Mbits/s or 100 Mbits/s Ethernet. Evidently dealing with uncompressed video is either expensive or unrealistic. The inspiration of digital video compression is on account of the prerequisite for meting out uncompressed video at high data rates.

3 Watermarking Overview

3.1 Phases in Digital Watermarking

Digital watermarking has been presented as a key to the problem of copyright protection of multimedia data in the next generation networks [7]. Essentially, nowadays with a broad range of video applications, Multimedia transmissions over wireless channels and the Internet requires that multimedia resources must be protected. Thus, video coding integrated with digital watermarking techniques can be efficiently employed to achieve this goal. However, digital video watermarking has many aspects that must be considered during the design of any digital video watermark schemes such as imperceptibility, robustness, capacity, complexity, synchronization, bit-rate control and error drift [8] [9] [10] [11]. A watermarking system consists of two main components: a watermark embedding unit and a watermark extracting unit as shown in Figure 2 The embedding unit adds the watermark component to the host data. The output of the embedding unit is the watermarked data. Attackers intend to do one of the following illegal actions such as modifying, copying, destroying or removing the watermark from the host data.

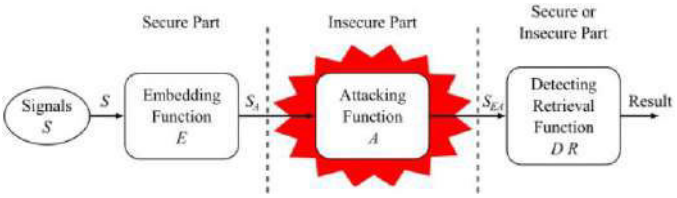

Fig.2 Digital watermarking life cycle phases

After embedding watermark, the watermarked media are sent over Internet or some other transmission channels. Whenever the copyright of the digital media is under question, the embedded information is decoded to identify copyright owner. The decoding process can extract the watermark from the watermarked media (watermark extraction) or can detect the existence of watermark in it (watermark detection). The embedding or encoding process can be viewed as a function or mapping that maps the input X (original media), W (watermark) and/or K (key) to output X ″ (watermarked media). Mathematically it can be expressed as

$$X' = E(X,W,[K]) \quad (1)$$

where E(·) denotes the embedding process and [·] represents optional argument. Similarly the decoding or extraction process D(·) can be expressed formally as

$$W' = D(X'',[X],[K]) \quad (2)$$

and the detection process d(·) can be expressed as

$$\{\text{Yes or No}\} = d(X'',[X],W,[K]) \quad (3)$$

3.2 Watermark Theory

The watermark contains information of the origin, ownership, destination, copy control and transaction. A watermark is inserted into a cover content like a digital code into a video sequence. A watermark can hold any information but the quantity of information is restricted. The information gets affected if the watermark holds more information. Moreover, the capacity of watermark is limited by the size of a particular video sequence. There are primarily three assessment constraints in video watermarking and at the same time there is an intricate trade-off among these constraints which are imperceptibility, robustness and payload. Simultaneously,

security (authoritative persons only can spot the watermark) and complexity (number of computations incorporated while embedding and extracting the watermark) are the two requirements for the efficient and robust watermarking techniques.

Besides the essential obligations, a watermarking technique to succeed as a real-time method, ought to gather the following additional requisites for compressed image and video data valid to recording device:

Oblivious: Even after lacking the original unwatermarked data, it must be viable to extort the watermark information, as a recorder and a set-top box at their disposal lack the original data.

Low complexity: The watermarking techniques cannot be too intricate since they are to be practiced in real time and also utilized in customer products, so they have to be economical. This means that entirely decompressing the data, inserting a watermark and compressing the data, do not constitute a choice for inserting a watermark.

Preserve host data size: The dimension of the compressed host data must not be augmented with the watermark. Sending the data over a preset bit-rate channel can create problems like the one in hardware decoders where the buffers rush out of space; otherwise there will be a problem in the synchronization of audio and video incase the dimension of a compressed MPEG-video stream enhances. Security systems that exploit watermarking methods have in common a sequence of cryptographic methods. Primarily the watermark information has to be encrypted. Consequently, the processed watermark information is appended to the host data in the course of inserting methods. The encryption and inserting methods exercise keys; these keys may differ in time. Cryptography protocols have to look after the key-management intricacy. The center of attention is on extending, analyzing and verifying the inserting methods for watermarks.

3.3 Oblivious vs. non-oblivious watermarking

In non-oblivious watermarking (private, non-blind), watermark extraction algorithms can utilize the original unwatermarked data to place the watermark in a few applications like copyright protection and data monitoring, whereas the blind techniques can extort a watermark without any reference to the original content. The detection is in general made complicated and the data capacity is also limited by the blind watermarking scheme. A huge database of original content is required by the non-blind watermark extraction though it is more robust, representing the technique which is impracticable for several applications. In the majority of applications like copy protection and indexing, the watermark extraction algorithms have no contact with the original unwatermarked data, which make the watermark extraction more intricate. Watermarking algorithms of this kind are known as public, blind or oblivious. By making amendments for every bit of the watermark to the host data, a robust watermark can be accomplished. In spite of large scale amendments in the host data and a lot of variations for each watermark bit, a maximum quantity of watermark bits can be stored in a data object. Consequently, a trade-off is supposed to be established concerning the diverse requirements, with the intention that a pre-eminent watermark can be developed for each application. The mutual dependence among the essential prerequisites is revealed in Fig.3. The security of a watermark ensures its robustness, but the watermark cannot be robust if it is not protected.

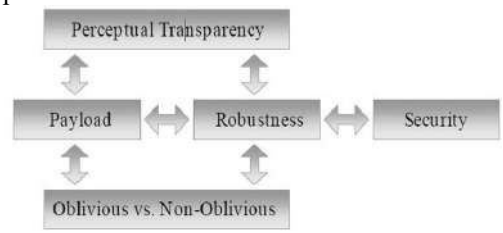

Fig. 3. Mutual dependence among the basic necessities.

3.4 Watermark Attacks

This section offers a study of possible attacks on watermarks. Watermark attacks can be organized into four major groups [12]:

Simple attacks are theoretically simple. They endeavor to destroy the inserted watermark by amendments to the entire image without any attempt to identify and segregate the watermark. Examples comprise frequency reliant compression, noise addition, cropping and adjustment.

Detection-disabling attacks strive to shatter correlation and to make identification of the watermark unattainable. Typically, they make a few geometric alterations akin to zooming, transfer in spatial or temporal direction, rotation, cropping or pixel transformation, deletion or inclusion. The watermark in the cover content can be retrieved with enhanced intelligence by the watermark detector.

Ambiguity attacks try to confound the detector by generating forged watermarked data to lessen the influence of the watermark by inserting numerous extra watermarks so that it becomes obscure.

Removal attacks assess or guess the watermark from a number of unusual watermarked copies, detach it and dispose of the watermark. Collusion attack, denoising and utilizing theoretical cryptographic fault of the watermark method are a few examples. A few attacks do not obviously fit into a solitary group.

4 Classifications of Watermarking Techniques

In the process of embedding the watermark, video watermarking schemes are segregated into three major groups such as spatial domain, frequency domain and compressed domain. Dissimilar methods are applied in each domain. In this sector, a concise analysis is elucidated with the present video watermarking schemes based on the domain in which watermarking is carried out.

4.1 Spatial domain watermarking

The schemes employed while inserting the watermark in the spatial domain involves in amending the pixel locations or pixel values of the original video or the watermark bits to be inserted are normally added to the luminance part or to the color components without exploiting the mathematical transforms on the original content. The watermarks are generally encoded as a noise-like progression and

then appended to the original content, whereas with a correlation based receiver the extraction is typically achieved. As mathematical transforms are not entailed, these schemes are reasonably efficient in terms of computations entailed. In real-time applications this is benefited where accessible of resources is narrow for inserting the watermark. Thus the chief benefits achieved with this scheme are the low time complexity in addition to simplicity of execution. Conversely, these schemes provide several difficulties in meeting robustness and imperceptibility constraints [13]. Countless methods have been anticipated for extending watermark schemes in the spatial domain, some of them are the Least Significant Bit (LSB) and Spread Spectrum Signal Correlation (SSSC) schemes, etc. In the LSB method, the original frame is utilized to insert the watermark. The places of the pixels are customized based on a secret key by engendering a pseudo-random number. Another scheme termed as SSSC involves in adding a pattern of noise which is pseudo-random towards the luminance value frames in the spatial domain, besides the likeness amongst the pattern of noise and probably watermarked video for each frame is also calculated. When the likeness surpasses a particular threshold then, the watermark is noticed [14].

4.2 Frequency domain watermarking

To surmount the major drawbacks in the spatial domain most of the video watermarking schemes have been utilized in the domain of frequency transform. Moreover, to augment watermark robustness and imperceptibility in the frequency domain, analysis of the bands is a prerequisite. Conversely, these schemes have a few shortcomings in terms of complexity. While switching from the spatial to a frequency domain numerous of transforms are entailed. For instance, some transforms such as the discrete Fourier transform, discrete cosine transform, discrete wavelet transform, and hybrid transforms are discussed in this section. In addition, a review is given of some proposed methods that have been applied to developing watermark techniques in the frequency domain. The spatial-domain watermarking methods are on average uncomplicated but not much robust. When weighed against methods sustained on frequency domain, for instance, the discrete Fourier transform (DFT) [15],[16], discrete cosine transform (DCT) [17]-[18], discrete wavelet transform (DWT) [19],[20], along with singular value decomposition (SVD) [21],[22], slant transform [23] permit the deployment of signal characteristics and human visualization properties to conquer enhanced robustness and invisibility. In the earlier period, quite a few watermarking algorithms have been built-up based on assorted incorporation of the above mentioned transforms [24],[25]. Due to multiresolution capability of DWT in time and frequency, it turns into an eminent transform for image processing . For extremely allied image data, the DCT grasps outstanding energy compaction. Watermarking by means of DWT and DCT typically reveal high-quality recital in terms of robustness and invisibility. Besides these two transforms, SVD is a dominant numeric tool cooperative for applications akin to data hiding and image compression. A matrix is factorized into three component matrices in the SVD, which correspondingly enclose left singular vectors, singular values in diagonal, and right singular vectors. Either by modifying the singular values [25] or the singular vectors associated with the largest singular value, a watermark bit can be inserted into an image block. Indeed, quite a lot of endeavors [25]-[26] have been made on the escalation of robust watermarking techniques in an amalgam domain relating the DCT, DWT and SVD. Quite a few existing watermarking techniques are identified by the typical compression process and matrix decomposition. These encompass unsighted SVD techniques that are placed in the bits of the mark within the singular values matrix. Schur transform also decomposes the image, video or mark into unitary transform U and upper triangle matrix T. The diagonal access are eigen values of all blocks in which the most of the energy is potted. A blend of DCT and SVD [28], DWT and SCHUR [29], DCT-DWT-SVD [27] methods seeks to erect watermarking techniques robust in conflict with the majority of attacks. The refined properties of SVD technique are utilized in image watermarking, [30]. This technique is endowed with a proficient means to extort algebraic features like a 2-D matrix. The foremost properties of the matrix of the SVs can be extended in video watermarking. A Little deviation arises in the matrix of the SVs, when a slight amendment is made to the original video. This makes the scheme robust against attacks [30]. By means of this property, the watermark can be inserted into this matrix without discrepancy in the acquired video.

4.3 Compressed and Bit-Stream domain watermarking

In this domain of watermarking the watermark is inserted into the bit stream of compressed video. The benefit of this scheme is that the computational cost is low compared to the earlier domains. As the digital video carries a large quantity of data, it is complicated, and so it is realistic to insert watermarks merely in raw video in real time. Usually, before watermarking compression has to be performed on a raw video prior to transmission through the network. Thus the chief concern is how to design a practical compressed video watermarking scheme such that the concealed watermarks probably will be perceived in real time. Consequently the watermark can be inserted in a video in three ways: raw-video, bit-stream and encoding process. The raw video watermarking algorithm inserts the watermark in the frames of video sequences and it is not strong to video compression. Bit-Stream watermarking technique inserts a watermark into the compressed video stream which requires fewer calculations. The third way of inserting the watermark in the encoding process is tough against MPEG compression and there is no bit rate rise of the video stream. Now a days embedding is done in compressed domain since video signals are always stored and transmitted in the compressed format and also as compression is one type of attack, there will be no need to assess it separately against the compression attack. Chiefly there are two approaches for inserting the watermark in compressed video. In this approach, the watermarking process and compression are mutually performed; the error induced by watermark does not extend as the watermarked data are used for subsequent predictions. But there is a rise in bit-rate which must be restricted in this category. In the subsequent approach the compressed video need not be entirely decoded, which reduces the critical computations during assessment

progression and recompression. As the inaccuracy persists, maintaining excellence is the chief trouble in this approach and also cannot be approved in real-time encoder system. As most of the digital video is transmitted in the compressed form, many compressed methods [35-37] have been proposed. M. Kutter et. al [31] proposes an algorithm to place in the watermark by varying the motion vectors. J. Zhang et. al [32] alters kutters algorithm by inserting the watermark into the motion vector of macro blocks that have large amplitude and little phase change. Zina Liu et. al [33] proposes an algorithm to embed a watermark in the motion vectors. Initially the Y component of P frame is separated into high and low texture areas. The motion vectors are modified based on the texture of the area. Then the prediction errors of the matched blocks are calculated at another time according to the distorted motion vectors. At last the new motion vectors collectively with new prediction errors, are encoded into compressed bit streams and thus reducing the flaws and block effects of watermarked video. I. Setyalwan et. al [34] have urbanized an algorithm called extended differential energy watermarking (XDEW) in which the watermark was inserted together into I frames and P frames. Although DEW and XDEW have little difficulty they are not strong enough against attacks which involve frame operators.

5 Evaluation Constraints and requisites of Watermarking

The performance criteria while watermarking at any rate must include perceptual transparency, robustness, capacity as well as security. The complete simulation outcomes are assessed by analyzing the Imperceptibility, Robustness along with Data payload. Imperceptibility:- Imperceptibility is a feature of the watermarked video which facilitates in maintaining the quality of the video. The watermark should be perceptually unobvious and must not amend even after inserting the watermark into the image, video or text. The visual feature of the watermarked video is approximated by the PSNR (peak signal-to-noise ratio). PSNR is a regularly exercised objective perceptual quality assessment. The divergence of the watermarked and attacked frames on or after the original video frames, is verified by analyzing the PSNR and is given in Eq(4).

$$PSNR = 10\log_{10}\frac{255^2}{MSE} \qquad (4)$$

To assess the PSNR, the Mean Square Error (MSE) linking the original and watermarked frame is worked out, since MSE is the mean square error relating the original video and the watermarked video which is specified in Eq (5).

$$MSE = \frac{1}{R \times C}\sum_{i}^{R}\sum_{j}^{C}[V(\mathrm{i},\mathrm{j}) - \mathrm{V}'(\mathrm{i},\mathrm{j})]^2 \qquad (5)$$

At this moment, the notations R and C correspond to the width and height of a frame, V(i, j) is the pixel value of coordinate (i, j) in original video, and V'(i, j) is the pixel value of the watermarked video. Thus the invisibility is measured by calculating the average mean square error (MSE) and the average PSNR. The higher the PSNR, the better is the quality of the video. In general, for digital images, noise with PSNR is higher than 30 dB which is hardly noticeable. Robustness:- It is the capability of a detector to extort the unseen watermark from some distorted watermarked data. It is frequently assessed through the endurance of a watermark after attacks, such as, compression, re-sampling, cropping, geometric distortions, frame swapping, frame dropping, frame averaging and scaling. Robustness is the resistivity of the watermark in opposition to common signal processing and malicious attacks. It is supposed to be skilled in extorting the watermark from the watermarked video. Even if the algorithmic principle of the watermarking method is public, the watermark should not be viable to be taken away. In particular, the watermark must be robust to the following: Common signal processing: The watermark should be retrievable although common signal processing operations (such as, analog-to-digital conversion and digital-to-analog, re-sampling, re-compression and common signal enhancements to image contrast and color) are affected on the video sequence. Common geometric distortions: The watermark should be resistant to geometric image operations, such as, cropping, rotation and scaling. Subterfuge attacks: Collusion and Forgery: The watermark should be robust to collusion by several individuals even though all hold a differently watermarked copy of the identical content merging their copies to demolish the watermark. Likewise, it should be unfeasible to merge the copies to generate a latest valid watermark. For comparing the similarities between the original and extracted watermarks, the two-dimensional normalized correlation (NC) value was employed. The NC value can be between '0' and '1'. In principle, if the NC value is closer to '1', the extracted watermark is getting more similar to the embedded one. In order to evaluate the performance of watermarking algorithm objectively, NC (normalized correlation) function is evaluated and computed by using Eq. (6)

$$NC(V,V') = \frac{\sum_{i=1}^{R}\sum_{j=1}^{C}[V(\mathrm{i},\mathrm{j}),V'(i,j)]}{\sum_{i=1}^{R}\sum_{j=1}^{C}[V(\mathrm{i},\mathrm{j})]^2} \qquad (6)$$

Where, V' is the extracted watermark and V is the original watermark. V(i,j) represents original watermark image and V'(i,j) represents the extracted watermark image. Payload:- It is the quantity of information which is interleaved into original video (i.e. mark size). We delineate the watermark cost 'δ' as the augment in number of bits utilized to encode the watermarked video for every watermark bit and is given by Eq (7).

$$\delta = \frac{TB_{watermarked} - TB_{original}}{\sum_{f=1}^{L_f} N_w(f)} \qquad (7)$$

Where TBoriginal is the number of bits utilized to code the original video sequence, TBwatermarked is the number of bits exploited to code the watermarked video sequence and Nw(f)

is the overall number of watermarked coefficients in that video sequence.

6 Watermarking Applications

Content protection along with content tracking has frequently been proclaimed as the inspiration for digital watermarking. Watermarking can be exploited in other applications and potential applications which encompass the following.

• **Content Tracking:** Through inserting a watermark into all copies of the content the proprietor personalizes. The inserted watermark recognizes the customer who has supervision of that copy. If an incredulous copy of the content is revealed, identifying the watermark relates the origin of the expected copy. These watermarks are seldom termed as fingerprints. Content tracking is not in actual fact intended for individual customers. For instance, assume that the video owner deals with the services of disparate mastering and allocation companies to build and issue the video on media. Conversely, the owner is anxious that several companies possibly will have deficient protection actions to conserve the video. Deceitful corporations or employees possibly will conspire to provide illegitimate copies to pirates. To map out protection contravenes, the owner inserts an unrelated watermark into the copies he offers to the mastering corporation. The video owner recognizes the watermark, if prohibited copies are generated prior to the authorized emancipation of the video to spot the company, whose protection is required. Then the content owner might prefer disagreement with that corporation. A related application arises where the movie owner is anxious regarding collusion, connecting various theater owners and pirates in digital cinema.

• **Property owner or Copyright recognition:** In copyright watermarking, the implanted watermark encompasses the information regarding ownership, such as, the uniqueness of the proprietor and the copyright date. Identifying the watermark gives the content owner a reason to argue for ownership. The inserted information possibly will also be supportive in identifying plagiarism. The watermark is noticed in the original content.

• **Copy Protection:** The watermarked content is categorized as a copy protected with the existence of the watermark. An appliance that complies with the copy protection procedure discerns the watermark and subsequently rejects the making of copies. A few copy protection systems restrict the customer from making supplementary copies from a copy, but permit the customer to build a solitary generational copy. In such methods, the inserted watermark encloses information, such as, "forever allocate supplementary copies", "merely single extra copy acceptable" and "refusal of further copies permitted". Exploiting watermarks in this style entail assistance from recording devices to identify the watermark and evade illicit repetition. The inserted watermark will not avert the video from being hackneyed if the recording device overlooks the watermark. Consequently a compromise amongst the inconsistent requirements of the service providers along with the customers would be the inserting of a Serial Copy Management System (SCMS), like copy protection system in all digital recorders. By the SCMS, customers can create replica of several digital sources. But they cannot create copies of copies. This copy protection system verifies the video streams on behalf of a predefined copy forbid watermark. If such a watermark is identified, the arriving video should have been copied earlier and is then rejected by the recorder. The watermark is inserted, if the copy-forbid watermark is not identified, and the watermarked video is preserved. Thus the video data preserved on this recorder forever includes a watermark and cannot be replaced if a recorder is outfitted with such a copy protection system.

• **Broadcast Monitoring :** An inserted watermark might be utilized to discern or spot a signal of curiosity, chiefly after the signal has been merged with supplementary signals. Identification arises the instant the watermark is noticed. For instance, an advertiser desires to confirm that a precise advertisement is being relayed as contracted. Validation and inspection are vital concerns as the making and allocation of telecast video content, accompanied by advertisements, amusement content, and news, comprises vast economic value.

• **Authentication:** The aptitude to discern distorted or fake video is crucial in applications, such as, video surveillance. To validate the reliability of the watermarked signal, inserted watermark should encode information which is essential. If amendments are perceived, the watermark permits the recognition of the imprecise regions. Authentication furthermore incorporate anti-forgery, where a watermark is inserted to boost the intricacy in generating illicit content. For instance, watermarks are projected to look after documents, such as, passports and identification cards.

• **Robust data hiding:** The inserted watermark may be utilized as a concealed channel to communicate messages from one customer to another. For instance, the dispatcher inserts the watermark within a video, encoding the covert message inside the watermark. The watermarked video is afterwards offered to the beneficiary, probably by means of an unconfident channel or by making the video openly accessible. As the watermarked video and original video are perceptually alike, the communication of the covert message is concealed by means of the original video signal as an inoffensive envelop. The anticipated beneficiary discerns and deciphers the watermark to attain the covert information. These watermarking techniques can further be exploited in fingerprinting and many other applications, some of which are explained below.

Fingerprinting: A customer can accept digital services, similar to pay TV or video on order, through cable or satellite dish by means of a set-top box along with a smart card, which he has to purchase and can as a result be allied to his uniqueness. To prevent other non-paying customers to take advantage of the equivalent services, the service contributor encrypts the data, in support of which he utilizes single or additional keys. This defends the services all through the broadcast. The set-top box in the residence of the customer decrypts the data if a legitimate smart card is utilized, and appends a watermark, in lieu of the uniqueness of the

customer, to the data compressed obviously. The fingerprinted data can currently be contributed to the in-house video decoder to inspect the data or the data can be preserved in compressed form. The service contributor can presently recognize customers who convey the data to third parties, flouting their license deal.

Indexing: Guiding of video mail, where annotations can be inserted within the video content; indexing of motion pictures and news items, where markers and annotations can be interleaved, can be utilized by search engines. Medical security: placing the date and the patient's name in medical images may possibly be a supportive protection measure.

7 Conclusion

In this paper fundamentals of video and various video formats are specified. Further, dissimilar classifications of video watermarking schemes were illustrated along with the theory of watermark and various watermark attacks. Additionally the evaluation constraints and requisites of various watermarking methods were mentioned. Finally various disparate applications of video watermarking are enlightened.

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Robust optimized DWT-SVD based Watermarking

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Abstract— A video watermarking technique is projected in this work by exploiting discrete wavelet transform (DWT) in addition to Singular Value Decomposition (SVD) transform. In this paper, DWT is applied on every luminance frame which is divided into 8x8 blocks of the video 'V' thus producing dissimilar frequency sub-bands, later SVD transform is implemented on the selected dwt blocks of HH bands of all frames. The selected dwt blocks were acquired through exploiting the Artificial Bee colony Optimization algorithm (ABC). At the receiving part, retrieval of watermark contents is achieved by a similar evaluation scheme practiced during the embedding procedure. This scheme recommends better visibility of watermarked video along with the retrieval of watermark content due to DWT-SVD- ABC combination. Simulation results show that the imperceptibility of watermarked video is better as PSNR is above 53 dB for all set of videos. Besides, robustness of the scheme is better than the existing scheme for similar set of videos in terms of normalized correlation (NC).

Keywords—SVD transform, DWT, ABC, Imperceptibility, Robustness.

1.INTRODUCTION

With the progress of transaction of data on the Internet and the widespread practice of digital media which is economical, there have been of enormous curiosity to digital data owners in multimedia safety and multimedia copyright security. The digital commodity Proprietors are worried regarding illicit doubling of their artifacts. Safety and copyright fortification are becoming imperative issues in multimedia applications. Watermarking digital image/video is a procedure utilized for copyright security of digital media. Watermark is a data related to owner concealed into the digital media without disturbing its perceptual quality. In the event of any disagreement, the watermark content can be identified or extorted, moreover utilized as an evidence of ownership. The techniques in watermarking that do not entail the original image for extraction of the watermark are called "blind" watermarking. The main efficacies of the digital watermarking technology can be characterized into four broad categories [1] such as Copyright fortification, continuous checking, Validation, Security and Indiscernible Communications. Digital watermarking persists to survive even after acquiring the data at the receiver side. If subtle data is disclosed to illicit personal, the digital watermark enclosed in them can be utilized to trace back to the intended receiver [2]. Digital watermarking exercised for concealed communication augments an additional level of protection contrast to cryptography. Though, the assailant is conscious of the endurance of the secret key, can be confident that within adequate interval he can decode the information, whereas while inserting the watermark digitally, the assailant can in no way be assured that hidden content is being conveyed. The foremost benefit of digital watermarks is that it lasts to persist though the receiver acquires the material. In applications related to medical [3] , watermarks are accomplished for credentials and retrieval of distinct patient archives. This specific application may avert human faults such as record discrepancy consequently precluding mortal faults [2].

The watermark in the projected method is entrenched in the video clip frames. Methodologies in video watermarking can be ordered into two leading classes based on the process of concealing watermark data in the original video. The two classes are: Spatial domain watermarking as well as transform-domain watermarking [4-16]. In spatial-watermarking procedures, entrenching and recognition are accomplished based on values of spatial pixels of the entire video frame. Spatial-domain schemes are simple to execute; on the contrary they are not resilient in conflict to accustomed digital signal processing functions such as video coding. Watermarking in the transform domain is more protected and strong. Transform-domain schemes, in contrast, amend spatial pixel values of the host video in relation to encoded transform. Recurrently exercised transforms are the Discrete Cosine Transform (DCT) [7, 8], the Fast Fourier Transform (FFT), the Discrete Wavelet Transform (DWT) and the Singular Value Decomposition (SVD) [9-11]. Transform-domain schemes of watermarking are established to be more strong besides unnoticeable when assessed in contradiction to spatial domain methods, subsequently dispersing the watermark in the spatial domain of video frame, makes it very tough to eliminate the inserted watermark. Every transform has its specific characteristics and indicates the image in diverse ways. SVD and Schur decompositions [12] are two mathematical tools used to analyze matrices. When some perturbation occurs in the watermarked image, the extraction of the watermark is not affected much. SVD is computationally expensive. Watermarking by means of Schur decomposition is faster when weighed against to SVD decomposition. With the aim of developing the achievement of image processing schemes at present many nature

influenced optimization methods [13-15] have appeared as powerful tools. In the proposed work also we are exploiting the ABC method which is optimization scheme to obtain improved results concerned to Imperceptibility and robustness.

Herein a resilient unsighted digital video watermarking algorithm is projected. The anticipated scheme merged the SVD transform by the DWT transform besides exploiting the ABC method to yield a competent technique with more robustness besides imperceptibility. This paper is systematized as follows. Different methodologies such as DWT and SVD transform along with ABC algorithm is deliberated in section 2. Projected algorithm is presented in section 3. Simulation outcomes are presented and compared with the existing methods in section 4. Conclusions are specified in section 5.

2. METHODOLOGIES

The disparate theories and practices exploited in this work are deliberated in this section so as to acquaint the reader with the elementary concepts.

2.1. Singular value decomposition (SVD)

A symmetric matrix is fragmented by SVD into three sub-matrices in which singular values are alienated into diagonal matrix [16]. This progression is also recognized as diagonalization of matrix. The three matrices that have undergone decomposition are termed as left singular matrix (L), singular matrix (W) and right singular matrix (R). Assuming C as a symmetric matrix SVD can be calculated with Eq. 1.

$$C = LWR^T \qquad (1)$$

In Eq (1), Matrix W appear as a diagonal matrix which is rectangular. The magnitude of diagonal values of matrix W are organized in a descendant order. Such diagonal values are identified as singular values of matrix C. For matrix C with m×m order, Singular matrix (W) can comprise of utmost m diagonal values. Layer wise involvement of L and R matrices in the matrix C is represented through singular values; over which the fragmentation is accomplished. The matrix quality becomes worse when the order of regeneration of matrix decreases . In contrast, there is no much disturbance in the quality of matrix with a minor disparity in the singular values. Eq. 2 shows one of the most important properties of singular values of diagonal matrix W.

$$f_1 \geq f_2 \geq f_3 \geq \ldots\ldots\ldots > f_{k+1} > d_{k+2} = d_m \qquad (2)$$

Where 'k' , ($k \leq m$) indicates the rank concerned to singular matrix W, $f_1, f_2, f_3, \ldots\ldots f_m$ symbolizes the diagonal values and m denotes the order of matrix. The matrices L and R likewise follow: $LL^T = I_m$ and $RR^T = I_m$.

2.2. Discrete wavelet transform (DWT)

The knowledge of wavelets is exploited by DWT to depict the images in an energy compact manner [17]. Wavelets are delineated as the small waves with frequencies which are always changing. DWT offers a great energy packaging capacity and explicitly it is the reason to apply in numerous image processing needs such as compression of the image, watermarking of the image, etc. In DWT, the novel image is changed into wavelet domain, consisting of four bands. Among the four sub-bands, three (HL, LH and HH) are identified as sub-images which encompass high frequencies with fringe data. The other sub-band (LL) comprises of low frequency, termed as approximate sub-image since it holds an estimated data of original image. It is attained by low-pass filtering together in the row as well as column directions. Additionally decomposition of sub-bands is feasible to reach higher level of decomposition. This progression can be passed to numerous levels as required in the application. When related to HL, LH and HH sub-bands, LL sub-band proves to be more stable in nature and it is extremely tough to get transformed by attacks as this band holds principal portion of energy of original image. This feature makes the approximate sub-band more apt for concealing the watermark with robustness. The exceptional spatio-frequency localization property pertained to DWT is exploited by disparate image watermarking methods in recent to contribute a raised value with regard to imperceptibility besides robustness. Figure 1 depicts disparate levels concerned to discrete wavelet transform.

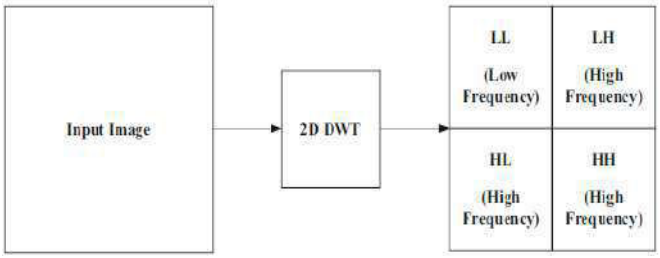


Fig. 1 First level decomposition of wavelet for an image

2.3. Artificial bee colony (ABC)

Among several evolutionary procedures [18] identified Artificial Bee Colony (ABC) as one such simple, rapid population based method and performance wise also it is too robust. ABC is practiced effectively on disparate domains to offer relatively raise in results [19-22]. Analogous to other Evolutionary procedures, variable values which are optimal are to be inspected by exploiting the ABC method with the aim of maximizing/ minimizing the specified cost function. Simulation outcomes demonstrates that ABC attains identical results comparable to several dissimilar metaheuristics practices along with this it also presents an extra benefit of adopting fewer control constraints. ABC is familiar for its capability to explore the search related to multidimensional which is the main focus of the projected work also. The basic steps intended for implementation of ABC algorithm can be realized from [23].

ABC method functions according to the sharp foraging behavior of the honey bee swarms. The feasible solutions for any specified issue is categorized by the food source in ABC scheme, further the fitness of any outcome is measured by the quantity of nectar in a food source. Three forms of bees arise in ABC, termed as working bees, spectator bees and detective bees. Working bees directs the number of explanations in the

specified population dimensions. ABC is originated with an initial population of results of dimension L (places where food is available) with each having a dimension X. i.e., early solution can be symbolized as P_k={p(k,1), p(k,2)……p(k,X)}; Where k=1,2…..L.

The searching process is a repetitive procedure subsequent to the initial circulation, while selecting optimum solution until the ending state is obtained. The spectator bees opt for the sources of food which are finest, depending on the value of fitness function in addition to the information provided by working bees, while the detective bees kept their recent sources of food with the purpose of exploring improved sources of food. In ABC procedure, working bees and spectator bees are answerable for the process of exploitation, while detective bees take attention of appropriate inspection.

The ABC algorithm encompass the following stages:

1. The sources of food with L number are preferred arbitrarily among the acceptable lower P_{min} = ($p_{(min,1),\ldots\ldots}$ $p_{(min,X)}$) as well as upper limit P_{max} = ($p_{(min,1),\ldots\ldots}$ $p_{(min,X)}$) of distribution with each including dimension of X through Eq.(3)

$$p_{(k,l)} = p_{(min,l)} + rand(0,1) \times (p_{(max,l)} - p_{(min,l)}) \quad (3)$$

2. All working bees produces a novel result with the local information accessible to it and relates the fitness of engendered result with the parent result. The improved result between these two is utilized for succeeding iteration. The novel result Q_k is engendered from existing result by making use of Eq.(4)

$$q_{(k,l)} = q_{(k,l)} + \phi_{(k,l)} \times (q_{(k,l)} - p_{(m,l)}) \quad (4)$$

Here $\phi_{(k,l)}$ is an arbitrarily acquired numeral between [-1,1] and indices m € (1,2,….L) and l € (1,2,……X) are arbitrarily acquired in such a form that m and l persist to be unlike.

3. The working bee distributes the fitness details with the spectator bee. The spectator bee produces a probability (Pi) of nectar (fitness) quantity by means of Eqs. (5) and (6).

$$F_K = \frac{fit_K}{\sum_{k=1}^{L} fit_K} \quad (5)$$

$$fit_k = \begin{cases} \dfrac{1}{f(Y_k)+1}, iff(Y_k) \geq 0 \\ 1 + abs[f(Y_k)], otherwise \end{cases} \quad (6)$$

At this point f(Y_k) denotes the value of objective function at the position of food Y_k.

4. An arbitrary numeral is engendered for all spectator bees within zero and one; if Fk , the position of food possess larger value than the arbitrary numeral then step 2 is tracked by the spectator bee as well.
5. If prearranged number of repetitions cannot alter the positions of food, at that time such positions are supposed to be eliminated. The value of prearranged numeral of repetitions is considered as significant constraint and identified as boundary. In such circumstances, detective bees regulates the novel places arbitrarily with the aim of exchanging the places that are eliminated.

   Stages 1 to 5 are reproduced up to the prearranged ending condition (maximum repetition, least variation) encounter.

3. PROPOSED ABC BASED DWT-SVD VIDEO WATERMARKING TECHNIQUE

3.1. Watermark Embedding

The planned watermarking method comprises primarily of two phases; watermark concealing and watermark extortion. For embedding watermark into video, we prefer YUV QCIF videos and partition the video clips into video scenes. The frames of video scene are evaluated. The frames of YUV video are in RGB color model and they are transformed to YCbCr color model. The luminance part is not far delicate to amendments when analogized with chrominance elements (Cb & Cr). For that reason while implanting watermark, take away luminance element. The procedure of embedding and extracting the watermark is shown in Figures 2 &3 respectively. Sequentially to entrench the watermark into all frames the consequent steps are taken.

Step1. The original video 'V' is segregated as set of M number of frames, the watermark 'W_m' is entrenched inside the video 'V'.

Step2. In the group each frame is transformed into YC_bC_r color model from RGB, further the luminance values Y of the frames are later accomplished.

Step3. In the video 'V' only luminance frames are alienated into 8x8 non-overlapping blocks.

Step4. Apply 2D DWT on entire 8x8 luminance frame blocks of the video ‘V’ as shown in Eq(7).

$$V_{DWT} = DWT(V) \quad (7)$$

Step5. ABC method is employed primarily to elect particular 8x8 blocks signified as Sel_dwtblock to embed watermark in every frame for attaining perceptibility.

Step6. SVD transform is implemented on the Sel_dwtblock of V_{DWT} of all frames to obtain left singular matrix L and singular matrix W as well as right singular matrix R. The eigen values are at diagonal location of each block. Majority

of the strength is preserved in the eigen values of the video, besides we attain Lv in addition to Wv, as depicted in Eq(8).

$$Cv = Lvb \times Wvb \times Rvb^T \quad (8)$$

Where b represents the number of the blocks selected for concealing the watermark.

Step7. SVD transform is applied to the watermark and we obtain L_{wat} and R_{wat}, as shown in Eq(9)

$$Wat = L_{bwat} \times W_{bwat} \times R_{bwat}^T \quad (9)$$

Step8. We add Wbwat to the Wvb matrix to obtain W_{vbnew} as given in Eq(10)

$$W_{vbnew} = Wvb + \beta\, Wbwat \quad (10)$$

The selection of the 'β 'coefficient depends on the compromise strength or imperceptibility preferred by the user.

Step 9. Inverse SVD is applied to obtain modified selected blocks as given in Eq(11).

$$C_{vnew}=L_{vb}\, W_{vbnew}\, R_{bv}^T \quad (11)$$

Step 10. Reposition the modified blocks in the frame of video to obtain V_{DWTnew}

S*tep11.* Apply Inverse DWT which is defined in the following Eq. 12

$$R_{wat} = DWT^{-1}\,(V_{DWTnew}) \quad (12)$$

3.2. Watermark Extortion

The gradual progression for the extortion of watermark in detail is delineated as follows:

Step1. The attained watermarked video is separated into clusters of k frames.

Step2. Every frame of the cluster is reformed from the RGB into the YCbCr color model.

Step3. Each luminance frame is transformed into 2D DWT.

Step4. Segment all luminance frames of the video 'V' as non-overlapping 8x8 blocks.

Step5. Spread on 2D DWT on entire 8x8 blocks of the luminance frame of the video, 'V' and the dwt block with outsized texture value is extorted which is signified as Sel_dwtblock by exploiting ABC method where watermark is entrenched.

Step6. Simulate SVD transform on all the Sel_dwtblock of V_{DWT} of each frame and obtain L, W and matrix R as follows:

$$C_v' = L_{bwat}' \times W_{bwat}' \times R_{bwat}^T \quad (13)$$

Step7. The diagonal entries are Eigen values of every block and are obtained by the following Eq (14)

$$Wbext = \frac{W_{vbnew} - Wvb}{\beta} \quad (14)$$

*Step 8.*The watermark is rebuild using the following Eq (15)

$$WE_{EXT} = L_{wat}\, W_{wat}\, R_{wat}' \quad (15)$$

Where WE_{EXT} is the extracted watermark

4. SIMULATION RESULTS AND ANALYSIS

The entire simulation results are assessed by finding the imperceptibility and robustness. The simulation results with proposed algorithm are contrasted with those of [23] and [24] for testing primarily two criteria's: imperceptibility test as well as robustness test. The superiority is shown in two evaluations; they are: Peak Signal to Noise Ratio (PSNR) on top of Normalized Correlation (NC) for mutually before and after attacks.

4.1 For Testing Imperceptibility

The simulated value of NC is 1 i.e. the extorted watermark is alike to the original and precise extortion is accomplished. While relating the planned scheme with [23] and [24] the projected scheme recorded a PSNR up to 59.93db for Suzie video which is superior to the PSNR stated by [23] and [24]. Table.1 demonstrates the PSNR assessment of the projected video watermarking procedure with earlier hybrid optimized video watermarking methods. The performance evaluations of the planned method with former hybrid optimized video watermarking schemes are shown in Table.2 for the Suzie video sequence in terms of the NC.

Table.1. Relative PSNR assessments with [23] and [24] after dissimilar sorts of attacks on the video of Suzie

Different types of Attacks	PSNR		
	Proposed method	[23]	[24]
(a) No attack	59.93	48.12	58.45
(b) Resizing	54.22	48.98	52.34
(c) Rotation	57.63	49.54	54.67
(d) Cropping	53.58	39.99	50.78
(e)Frame swapping	54.44	47.34	51.16
(f) Sharpening	56.32	38.67	50.72
(g)Frame Averaging	54.45	44.54	53.69
(h)Salt &Pepper noise	54.89	47.86	49.25
(i)Gaussian noise	54.12	43.97	52.02
(j)Histogram Equalization	53.04	39.35	50.30

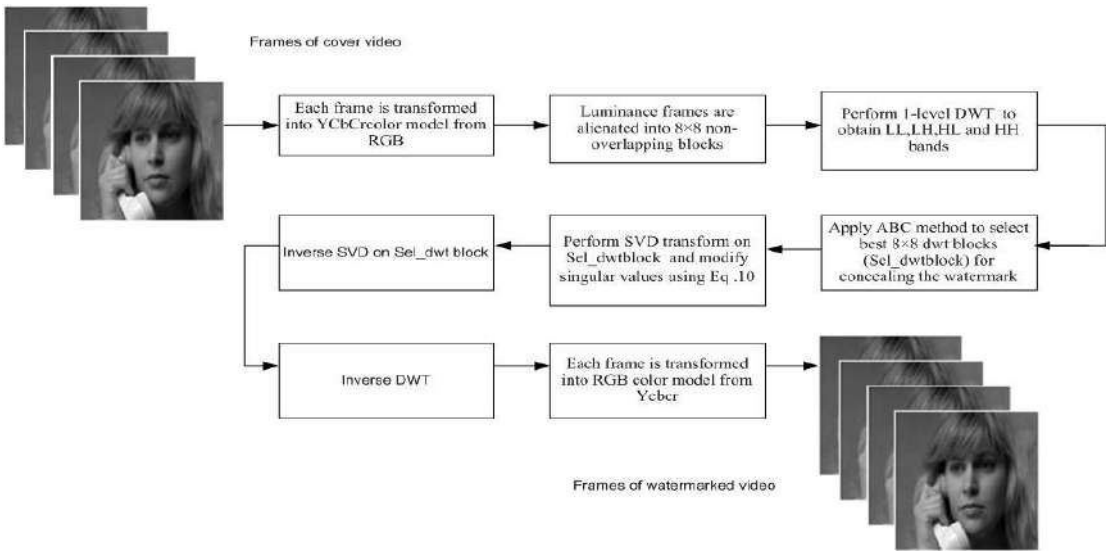


Fig.2.Procedure of Embedding the watermark

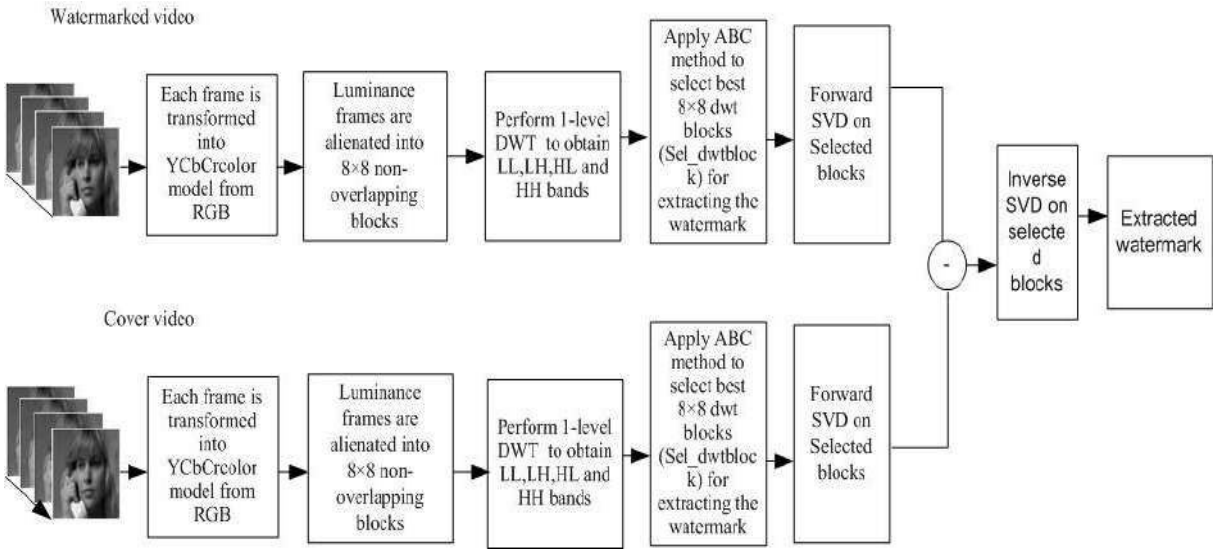


Fig.3.Procedure of Extracting the watermark

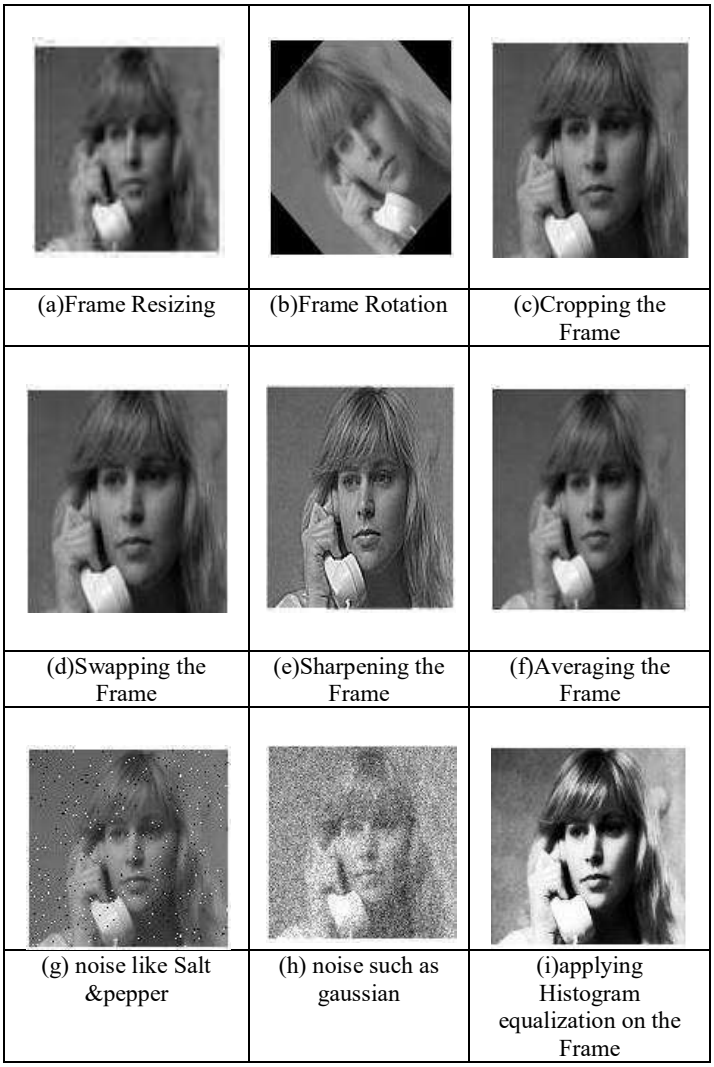
Table.2. Relative NC values with [23] and [24] after dissimilar sorts of attacks on the video of Suzie

Different types of Attacks	**Proposed scheme**	**[23]**	**[24]**
(a) No attack	1	0.9	1
(b) Resizing	0.99	0.84	0.93
(c) Rotation	0.95	0.89	0.9
(d) Cropping	0.98	0.89	0.91
(e)Frame swapping	0.88	0.7	0.8
(f) Sharpening	0.93	0.76	0.87
(g)Frame Averaging	0.91	0.79	0.91
(h)Salt &Pepper noise	0.99	0.87	0.92
(i)Gaussian noise	0.9	0.85	0.86
(j)Histogram Equalization	0.89	0.6	0.82

4.2. For Testing Robustness

Robustness is the capability of detector to extort the masked watermark even after altering the watermarked data. Owing to enormous volumes of data and intrinsic redundancy between frames, the video used for embedding the watermark is extremely susceptible to plagiarize assaults which include

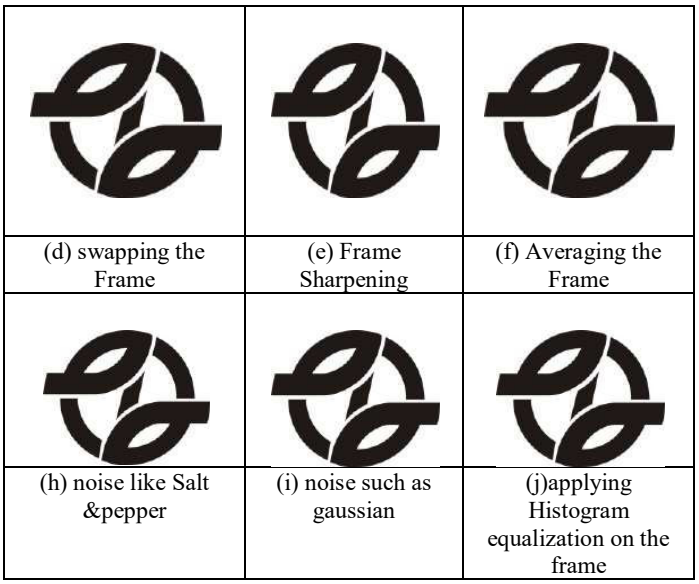
averaging of frames, rotation, tumbling of frames, sharpening etc. Frequently robustness is assessed by the endurance of watermark after disparate varieties of attacks, such as Resizing of frames, Rotation of frames, Cropping the frame, swapping the frame, Sharpening the frame, averaging the frame, effect of noise like Salt & pepper besides Gaussian and applying Histogram equalization on the frames, etc. The retrieved watermark after applying different types of attacks as shown in Fig.4. on Suzie video is depicted in Fig.5.



(a)Frame Resizing	(b)Frame Rotation	(c)Cropping the Frame
(d)Swapping the Frame	(e)Sharpening the Frame	(f)Averaging the Frame
(g) noise like Salt &pepper	(h) noise such as gaussian	(i)applying Histogram equalization on the Frame

Fig.4. Disparate varieties of attacks on the video of Suzie

(a)Frame Resizing	(b) Frame Rotation	(c) Frame Cropping



(d) swapping the Frame	(e) Frame Sharpening	(f) Averaging the Frame
(h) noise like Salt &pepper	(i) noise such as gaussian	(j)applying Histogram equalization on the frame

Fig.5. Extracted watermark after applying dissimilar types of attacks on the video of Suzie.

In the proposed scheme the NC values are always above 0.85, revealing the developed quality of the extorted watermark. Thus the recommended algorithm illustrates upright robustness though the attack is resilient. The object next to the greater concert of the planned algorithm beneath numerous kinds of attacks is as a result of: relating superior categories of transforms in union to optimization procedure, therefore limited numerals of coefficients interrupt on the excellence of the restored watermark; also gradually it authorizes us to exploit highest entrenching feature with enhancement in robustness.

5. CONCLUSION

In this work, an optimized DWT–SVD block-based video watermarking scheme is presented. Primarily, the video is segregated into blocks. Subsequently, DWT is applied on all of these blocks then only selected blocks were preferred by ABC method to attain high-level rating for the watermarking constraints and sustain the trade-off among them, finally the SVD characteristics were exploited to choose the best embedding regions to include the watermark, to attain more robustness. The embedding strength applied at the period of inserting watermark is so principal that only the appropriate owner can recover the watermark, identifying the legitimate constraints. The projected scheme outperformed all related earlier schemes and accomplished the highest imperceptibility. In terms of robustness, good resiliency was examined in opposition to all types of video processing attacks and numerous types of geometrical attacks.

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Custom Queueing method for enhancing security of a Packet Scheduling Process in Real time Networks

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***Abstract* — The wireless technologies became a part of our day to day life, for sending and sharing data very rapidly so that everyone today uses wireless networks for their business or personal. The traditional wireless communication technology is unable to satisfy real-time transmission requirements in mobile electronic commerce application such as access of books from digital libraries, access of stock exchange information etc. Recent real-time wireless networks require high level security to guarantee the information passed through wireless channels. So, designing flexible security mechanisms for real time applications and transmitting packets through wireless networks is highly desirable. The present work introduces a new packet scheduling algorithm to enhance security which mainly aims to dynamically determine security levels of packets based on security requirements of an application and also guaranteeing deadlines for packets. By incorporating Custom Queuing method with this packet scheduling algorithm, the overall performance of real time networks is increased.**

Keywords— Wireless Networks, Packet Scheduling, Custom Queuing

I. INTRODUCTION

Wireless technology today has become one of the most affordable and easy to use in the field of information technology and academics because of its fastest growth of various applications in recent are using wireless networks. Almost every common man today can access to the Internet at their homes, libraries, universities, restaurants, railway stations, airports, and even while driving in vehicles to conduct their business, accessing and learning e-books, transfer money, paying electricity bills, booking movie tickets, sharing stock exchange information etc.

As Internet users become increasingly mobile and online business applications become very much interactive and traditional wireless communication technology methods are unable to satisfy the real-time transmission requirements in mobile electronic commerce applications such as access of books from digital libraries, access of stock exchange information etc. The remedy to this problem is real-time wireless communication techniques allowing users to collect and transmit data in a timely manner increases interest in many academicians, scholars and researchers. Supporting efficient and reliable data transmission, especially real time data transmission, through wireless networks is extremely difficult and challenging task because wireless networks must be facing more complicated environments compared with conventional wired networks such as computer viruses, intruders, worms, spy wares, and similar threats.

Many security policies related to authenticity and confidentiality strategies and wireless communication protocol-based security schemes [1] have been proposed and applied in real-time wireless networks. However, most of them considered only security issues in a static mode, in which security levels are all configured when wireless network systems are built. In some real-time systems like stock quote updating and trading system, users may need flexible quality of security, measured as security levels. Suppose in an industry the data may be more secured when compared to the past twenty years data in that company. i.e security levels are higher at present for that company. Thus designing flexible security mechanisms for real time applications transmitting packets through wireless networks is highly desirable.

The Custom Queuing method for improvement of Security Aware Packet Scheduling Algorithm aims to dynamically determine security levels of packets according to applications, security requirements while guaranteeing deadlines for packet and also increases the speed i.e overall performance. Apart from achieving high quality of security, it can significantly improve guarantee ratio, which is a fraction of total transmitted packets that are found to be delivered before their deadlines.

II. RELATED WORK

There is a rapid growth of applications in the domain of wireless networks in the real world, i.e. usage of Internet at all places in homes as well as business for sales, purchases, finding remote locations, making payments and playing games and many more. Because enormous development of Wireless technologies makes a person day to day life more comfortable. Many devices with wireless technology developed and used for an individual and for business point of view which leads an increase of users every day. Security risks automatically raised and it is a challenging task for secured transmission of data. National Telecommunications Cooperative Association (NTCA) reported in the year of 2005 nearly 61% of survey

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defendants provided wireless services to their regular customers and nearly 55% of real time services are for voice like services. In the coming years Wireless technologies will offer further many new features and functions for protecting data and safe transmission.

Wireless technologies, makes easy for communication due to no cables required for connection. i.e. two or more devices are enabling communication without connecting physically each other with transmission cables. Instead they use micro and radio waves [2] with specific range of frequencies for providing communications among larger distances. Depending on speed, coverage area and size there are many categories of wireless networks available. Wireless personal area networks which covers very smaller distances within a room (Bluetooth), Wireless Local Area Networks that covers few kilometers by connecting laptops with the device having wi-fi access point, wireless metropolitan area networks range hundreds of kilometers with multiple nodes and wireless wide area networks covers the distance across worldwide through various cellular technologies (WiMAX, CDMA, GSM etc) [3]. Best example for Wireless Wide Area Network is an Internet. Wireless technologies range from complex systems to simple hand held devices [4]. Different packet scheduling algorithms surveyed from exited work [5, 6].

A. Security Issues

Security plays an important role in the design and development of wireless mobile educational and business applications, international wireless organizations, wireless equipment providers and thus academic researchers made extreme efforts in increasing the features of existing security mechanisms [7, 8] and finding attractive and creative security policies of wireless networks. IEEE introduced many standards for improving security by defining various security related functions. Cisco provides the solutions for wireless applications by using strong encryption technology and providing unified WLAN. Papers addressing the security problems also provide valuable solutions for wireless business applications.

In recent years, wireless networking has become more popular and users are accessing wireless technology while moving also for their daily activities. Thus, protecting data from unauthorized access or the attacks like active and passive attacks etc is a challenging issue apart from efficient and reliable transfer of data. There are many existing algorithms to improve performance of wireless networks. This paper highlights those security threats, and explains what we need to know to use wireless safely, both in the home and in public.

B. Packet Scheduling

Packet Scheduling methods are generally used when multiple packets exist in a buffer and they share a common outgoing link. Packet scheduling algorithm determines the service policy of a node and it plays important role for providing quality of service. Many packet-scheduling algorithms exist in the literature for increasing the quality of service within a node while delivering packets from source node to destination node. Chang and Yu presented packet-scheduling algorithms [9] to guarantee the quality of service in wireless applications of ATM and video traffic. Different packet scheduling algorithms developed for achieving quality of service in the nodes such as FIFO, Priority Queue, Weighted fair queue and low latency queue etc. In FIFO method the packets are served based on their arrival order. Priority Queues gives preference for important traffic to be cleared during transmission. Weighted fair queue works based on weighted bandwidth allocation. It divides bandwidth across multiple queues. However most of these packet scheduling algorithms works well for better delivery packets and achieve quality of service, but not concentrating on security constraints. This paper mainly integrates the proposed packet-scheduling algorithm [10,11] with dynamic security adjustment strategy. In doing so, we build a new secure packet scheduling scheme along with custom queueing policy for real-time wireless networks.

III. PACKET SCHEDULING ALGORITHM WITH SECURITY CONSTRAINTS

The packet scheduling Algorithm with security has been introduced with the aim to increase the performance and reliable delivery of packets by using various security levels [14]. This Security based Packet scheduling algorithm improves the performance by raising security levels where a security level controller is used.

Initially packets are sent into the accepted queue and security levels are increased for every packet at accepted queue by determining the guarantee and deadline of packets. When packet has considerable deadline, it is admitted into accepted queue otherwise it will be sent into the rejected queue. The below given constraint verifies whether packet has considerable deadline.

$$CTi - STi <= di$$

where,

STi is the start time of transmission of the ith packet,

CTi is the transmission completion time, di is the deadline of packet.

Based on the deadlines of the packets, they are processed. i.e. the packet which is arrived first is scheduled first. This algorithm is initiated with very low-level security levels. Further, the security is increased based on below constraints.

(i) when Pi is transmitted earlier than given deadline.

(ii) Pi packets are guaranteed even the deadlines have been inititaed later.

The above constraint (ii) is important and reasonable if the packet is arrived in real time link, then its timing constraint has to guaranty the arrival. Simply this security algorithm confirms that an admitted packet is not harmfully affected by simultaneous admitted packets.

A. The Custom Queuing for Efficiency

This strategy works for fixed-length packets scheduling [10,11]. FIFO within priority queues. It is based on interface or protocol. Time is divided into frames. Each session is

assigned a weight in terms of number of packets that could be served during a frame. For every session a separate counter is kept in order to register the number of packets served in that specific frame. It guarantees bandwidth per queue. It is not used for voice. It increases speed and performance during transmission of packets.

B. Algorithm

//calculate no. of packets to be served each round//
min = find smallest weight
For each flow f
f.packets_to_be_served=f.weight/min
//main loop
Loop
For each non_empty flow queue f
min(f.packets_to_be_served,f.packets_waiting).times
do
serve packet f.get packet

IV. SYSTEM MODEL

The system model includes a wireless channel as an NN switch [2] shown in Fig.1. A transceiver is used for transmission of packets even though a separate transmitter and receiver is equipped by each wireless node in the system. As such, a node cannot transmit and receive packages simultaneously. A packet scheduler matching transmitter is equipped to the corresponding receivers in this model.

In the above-mentioned model, a centralized scheduler collects, via a control channel, global network information. The scheduler uses a slotted system and a matching algorithm 2 to match transmitters to their intended receivers. Clearly, there is no need for a transmitter to transmit to the receiver on the same mobile node. Therefore, the possibility of a transmitter sending to the receiver on the same mobile node is disallowed. The resulting system of N transmitters and N receivers, with exactly one transceiver on each mobile node, can be modeled as a special case of an NN switch. The N transmitters can be thought of as the N input ports of a switch and the N receivers as the N output ports. The centralized scheduler node is modeled as the arbiter or scheduler of the switch. This PAN model assumes that each node's transmission can reach any of the other N_i nodes and the central node3.

A matching in a bipartite graph G = (V,U,E) is a subset of edges G (i.e., of E) such that no node in V or in U has more than one edge of this subset incident on it. A maximal matching in a bipartite graph is any matching such that given this matching, no other edge can be added to it without violating the definition of the matching. A maximum matching in a bipartite graph G is a matching consisting of the maximum possible number of edges in G. The central node or the scheduler could be either one of the N nodes or a separate entity.

This also includes a PAN, based on this model a Wireless Switched PAN or simply a Switched PAN. With these assumptions, the model can be represented by a special bipartite graph.

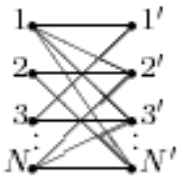

Fig 1: N-Node Bipartite Graph (NNBG)

There are three more components in the system apart from switch model, including Security Controller (SC), an Admission Queue Controller (AQC), and Deadline Controller (DC) as depicted in Fig. 2.

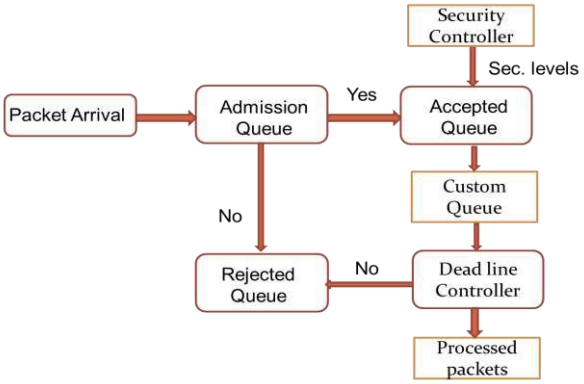

Fig.2. System architecture

This model represents a connection between two nodes in specified wireless network. And the packets are submitted independently to the wireless link with arrival rates abided by Poisson distribution. The Admission Queue Controller mainly decides given packet is accepted or not. If it is accepted then sent into accepted queue otherwise into rejected queue. The security levels for packets in the accepted queue will be assigned by the Security Controller. The Deadline Controller scheduler uses deadline policy for all admitted packets in which security levels have been increased by the Security Controller.

A. The Packet Model

The packets transmitted in this model have deadlines to reach destination node and every packet to be transmitted individually. All the packets have arrival times based on the classical Poisson distribution. Packet Pi is represented as a tuple (ATi, PTi, DLi, SLi), where ATi and PTi represents the arrival time and the processing time of packet i. DLi depicts deadline and SLi specifies the security level of packet *i*. Besides, without loss of generality we assume that each packet is assigned a quality of security measured as a security level *SLi* that in the range [1, 2, ..., 10], where 1 and 10 are the smallest and largest security levels. The security level 1 means that smallest security level of the packet and level 10 is largest. To calculate the security overhead without loss of generality, the below given formula (1) is used to model the security overhead envisioned as the extra processing time experienced by packet *i*.

$$SOi = ETi * (SLi / R) \quad - (1)$$

where SOi and SLi depicts security overhead and security level of packet i, ETi is the transmission time of the packet and R is set to 10. Thus, the total processing time WLi of packet i can be expressed as:

$$WLi = ETi + SOi = ETi * (1 + SLi / R)$$

Where, SOi-security overhead of packet
SLi - security level
ETi- transmission time of packet
R value set to 10

V. SIMULATION AND RESULT ANALYSIS

The transmission of packets with in a node while delivering from source node to destination node using custom queuing method is shown in the given table 1.

The simulation parameters considered for SPSCQ algorithm are 60 source nodes, 40 destination nodes and 5 intermediate nodes. The packets are transmitted from source node to destination node through intermediate nodes by changing security levels ranging 1-10. The arrival rate is 5 packets/sec. bandwidth taken as 1mbps.

(i) Guarantee % = (no.of accepted packets/no.of arrived packets) *100
(ii) Agg. security % = (security level used for accepted packets/ no. of arrived) *100

Table 1. Packet schedule process with CQ

P.No.	Generation of packets				Acc/rej	Incr. sec	With Custom Queuing (CQ) Method (packets)
	St (s)	End (s)	dead line	Secu. level			
1	1	3	15	2	acc	7	[4,4,9,10,7]
2	2	5	14	6	acc	6	Parallely sending [5,5,11,10,9]
3	3	7	17	8	acc	8	[2,2,5,14,6]
4	4	9	10	7	acc	7	Parallely sending [10,10,20,14,7]
5	5	11	10	4	acc	9	[1,1,3,15,7]
6	6	13	4	1	rej		---
7	7	15	18	3	acc	8	[3,3,7,17,8]

The guarantee percentage (GP) and aggregate security level percentage (ASP) of SPACQ is calculated and compared with other algorithms SPSS [12,13], ISAPS[15], RSAPS[16] as shown in above fig2 and fig3.

The experimental results shown that the new SPSCQ approach provides an improvement in terms of guarantee ratio, security level, and speed. Thus, the overall performance for real time wireless networks has been improved using Custom Queuing approach and the security levels organized dynamically based on the network traffic.

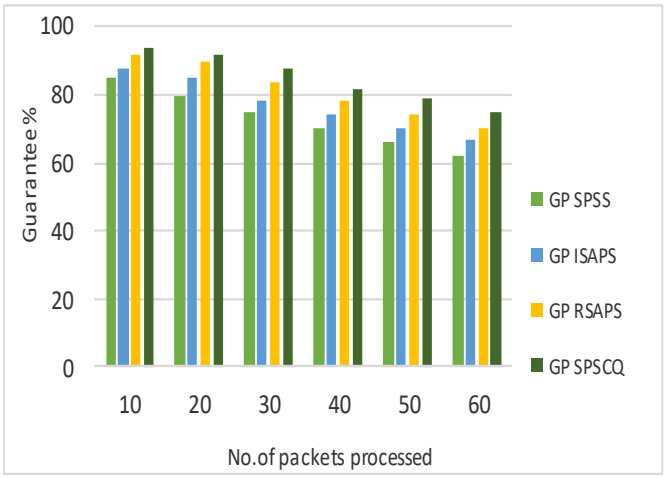

Fig2. Guarantee % (GP) of various Algorithms

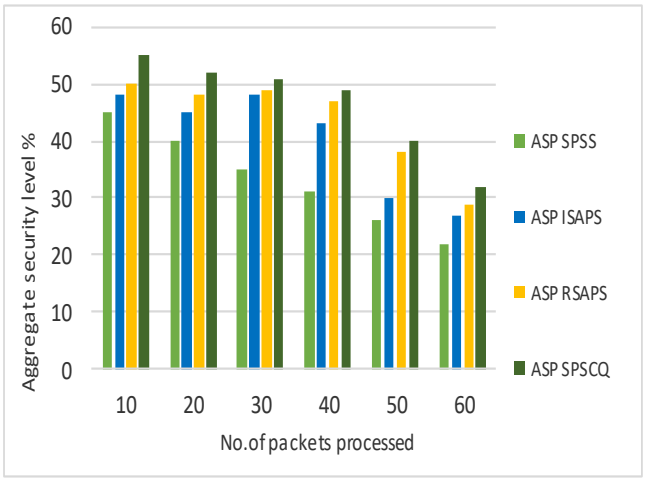

Fig3. Security % (ASP) of various Algorithms

VI. CONCLUSION

In modern wireless networks high quality of security is essential apart from guarantee ratio of packets, in order to protect data which is stored in the packets to be transmitted. The proposed work suggested a novel dynamic Security based Packet Scheduling algorithm with Custom Queuing approach (SPSCQ), which is capable of achieving high quality of security service for real-time packets and reliable while delivering packets. The algorithm is also designed in a way that makes it possible to achieve a reasonably high guarantee ratio and optimized security level. In particular, the proposed SPSCQ algorithm leverages an intelligent Security Level Controller to adaptively assign security levels to incoming real-time packets transmitted through a wireless network links. The performance of the present approach can be further improved by using combinations of various other packet scheduling algorithms.

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Design and Implementation of High Speed, Area, Power, Time Delay Optimization of 32 bit Vedic Multiplier

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ABSTRACT

Multipliers are the key block in high speed Arithmetic logic unit, Multipliers and Accumulate unit and Digital signal processing application. Many researchers have come up with various multipliers such as Booth multiplier, Carry Save Adder, Wallace tree etc. In this paper, We proposed 32 bit Ripple Carry Adder based Vedic-multiplier with partial product concatenation (RCA-PPC) architecture. This techniques exhibit their excellence in speed, area, power and time delay optimization. In this paper which shows the comparison for the speed, Area, Power and Time delay between existing Vedic Multiplier with Proposed Ripple Carry Adder based Vedic-multiplier with partial product concatenation (RCA-PPC). Simulation results specify these proposed architectures as increase in Speed and decrease in Area, Power and Time delay.

Keywords

Vedic multiplier, Ripple carry array, power-delay product, carry-select adder

1. INTRODUCTION

Multipliers are the key block in high speed Arithmetic logic unit (ALU), Multipliers and Accumulate unit (MAC) and Digital signal processing (DSP) application. Many researchers have come up with various multipliers such as Booth multiplier, Carry Save Adder, Wallace tree etc. An Array-to-Array multiplier use arrays of Full Adders connected to each other in order to perform multiplication of two binary numbers. Similarly, a Booth Multiplier involves shift operations and addition operations to perform multiplication. Booth multiplier reduce number of partial products to be added. The Booth multiplier is the highest speed multiplier when compared to the Dadda, Wallace and Vedic multipliers. The Vedic multiplier consists of low power and low area when compared to other multipliers. Wallace Tree is used to reduce the number of sequential adding stage. This paper explains Vedic multiplier which uses a technique of grouping the bits of two input binary numbers involved, concatenating the partial products obtained from sub -multipliers in intermediate of the multiplication process. Vedic multipliers are widely utilized as part of commercial and budgetary purpose. The need for efficient, high speed multipliers with less area and power consumption drives researchers to build new Vedic multiplier architectures. We proposed 32 bit Ripple Carry Adder based Vedic-multiplier with partial product concatenation (RCA-PPC) architecture. This techniques exhibit their excellence in speed, area, power and time delay optimization. In this paper which shows the comparison for the speed, Area, Power and Time delay between existing Vedic Multiplier with Proposed Ripple Carry Adder based Vedic-multiplier with partial product concatenation (RCA-PPC). Simulation results specify these proposed architectures as increase in Speed and decrease in Area, Power and Time delay.

II. VEDIC MATHEMATICS-URDHVA TIRYAKBHYAM SUTRA

Vedic Mathematics is an ancient and eminent approach which is mainly based on 16 Sutras dealing with various branches of mathematics like arithmetic, algebra, trigonometry, analytical geometry etc. In order to perform multiplication, one of the most preferred algorithms among these 16 Sutras is the Urdhva Tiryakbhyam Sutra. The words Urdhva and Tiryakbhyam are derived from Sanskrit which mean verticality and crosswise respectively. The main advantage of utilizing this algorithm in comparison with the existing multiplication techniques is that, the partial products required for multiplication are generated in parallel. These partial products are added in such a way that saves a lot of processing time. This algorithm is applicable for the multiplication of binary numbers, so we have chosen this Sutra for implementation of Vedic multiplier.

Let us consider for a 4 × 4 multiplication that gives output product as $P_7P_6P_5P_4P_3P_2P_1P_0$. The multiplicand and multiplier are decomposed equally as $X_H = A_3A_2$ and $X_L = A_1A_0$ for X and $Y_H = B_3B_2$ and $Y_L = B_1B_0$ for Y, where H and L represents higher and lower order bits of X and Y. According to Vedic mathematics, initially vertical multiplication of X_L & Y_L is carried out, which gives partial product outputs P_0 [3 : 0]. Then, the middle one shows crosswise multiplication of two, 2 × 2 multiplier with inputs X_H & Y_L and X_L & Y_H, generates P_1[3 : 0] and P_2[3 : 0] partial product outputs respectively. Finally, the last block inputs X_H Y_H multiplies vertically and generates the partial product outputs as P_3[3 : 0]. The first two final product outputs P_0 and P_1 are same as that of the partial products P_0[0] and P_0[1]. The remaining product terms are obtained by using three conventional adders as shown in Fig. 1. The inputs for adder1 are $\{p_3[3:0], 00\}$ and $\{00, p_2[3:0]\}$ and for adder2 are p_1[3 : 0] and $\{00, p_0[3:2]\}$. The outputs of adder1 and adder2 are given inputs to the adder3, that generates the final product terms P [7 : 2]. Thus, the final product terms are obtained by parallel multiplication using sub multiplier blocks and addition as $P_7P_6P_5P_4P_3P_2P_1P_0$, that can reduces the delay of the multiplier.

Vedic multiplication implementation equations as

$P_0 = A_0 B_0$

$P_1 = A_1 B_0 + A_0 B_1 + P_0$(1)

$P_2 = A_2 B_0 + A_1 B_1 + A_0 B_2 + P_1$ (1)

$P_3 = A_3 B_0 + A_2 B_1 + A_1 B_2 + A_0 B_3 + P_2$ (2to1)

$P_4 = A_3 B_1 + A_2 B_2 + A_1 B_3 + P_3$(2to1)

$P_5 = A_3 B_2 + A_2 B_3 + P_4$ (2to1)

$P_6 = A_3 B_3 + P_5$ (2to1)

$P_7 = A_3B_3$

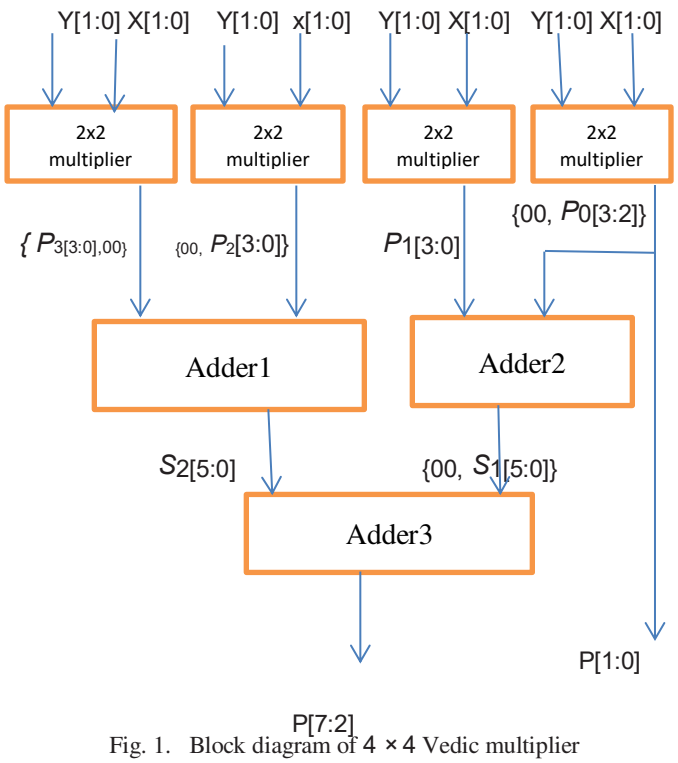

Fig. 1. Block diagram of 4 × 4 Vedic multiplier

III. PROPOSED DESIGNS

The proposed Vedic Multiplier architectures utilize a technique of concatenating partial products obtained from sub-modules. For example, a 4x4 bit multiplier uses four sub-modules of 2x2 bit multipliers. The partial products obtained from the sub-modules are then concatenated and added using addition blocks to obtain the desired output of the NxN bit multiplier (where N is a power of 2). The concatenation of the partial products for a 4x4 bit multiplier is explained in Table I. For a 4x4 bit multiplier, the grouping of input bits is done such a way that Group I has 2 least significant bits of first input (A), Group II has 2 most significant bits of first input (A), Group III has 2 least significant bits of second input (B), and Group IV has 2 most significant bits of second input (B). These groups are given as inputs to four 2x2 sub-multipliers to perform I x III, II x III, I x IV and II x IV multiplication in parallel. The products obtained from each sub-multiplier are named as P3- 0, P7-4, P11-8 and P15-12 respectively. Instead of waiting to incorporate the partial products obtained from II x IV until the final stage, both proposed architectures instead concatenate these into the same line as I x III, due to the lack of overlap in place value. This allows for the removal of previously stated unneeded successive calculation stages. Through a proper addition technique, the product of A and B named as P7-0 can be obtained.

III.1 Ripple Carry Adder based Vedic multiplier with Partial Product Concatenation (RCA_PPC)

The Ripple Carry Adder based Vedic multiplier with Partial Product Concatenation (RCA_PPC) architecture of a 4x4 bit multiplier passes PP_0 and PP_1 straight to the solution, adds II x II and I x IV using 4-bit RCA, and then adds P_2, P_3, P_{12}, P_{13}, P_{14}, and P15 (P15-12P3-2) to the sum of II x III and I x IV using 6-bit RCA. This makes up the final 6 bits of the solution.

We explained the grouping of the input binary bits to the multiplier sub-modules (sub-multipliers). The sub-NxN bit multipliers use same technique as of multiplier to obtain product of its two inputs. NxN bit multiplier uses four N/2 x N/2 bit sub-multipliers. N-bit adder and $\frac{3N}{2}$ bit adder.

Table I. Concatenation of Partial Products Methodology

Design	**Pair**					A_3	A_2	A_1	A_0
						Group II		Group I	
						B_3	B_2	B_1	B_0
						Group IV		Group III	
PREVIOUS Design	**I x III**					P_3	P_2	P_1	P_0
	II x III			P_7	P_6	P_5	P_4		
	I x IV			P_{11}	P_{10}	P_9	P_8		
	II x IV	P_{15}	P_{14}	P_{13}	P_{12}				
	Concatenating Partial Products								
Design proposed		P_{15}	P_{14}	P_{13}	P_{12}	P_3	P_2	P_1	P_0
				P_7	P_6	P_5	P_4		
				P_{11}	P_{10}	P_9	P_8		
Sum		P7	P6	P5	P4	P3	P2	P1	P0

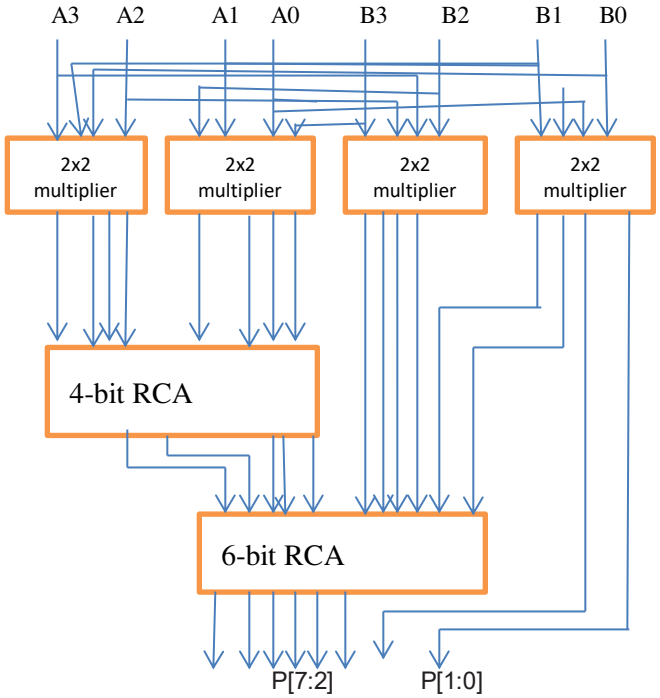

Figure 2. 4x4 Bit RCA_PPC Multiplier

III.2 4-bit Ripple Carry Adder

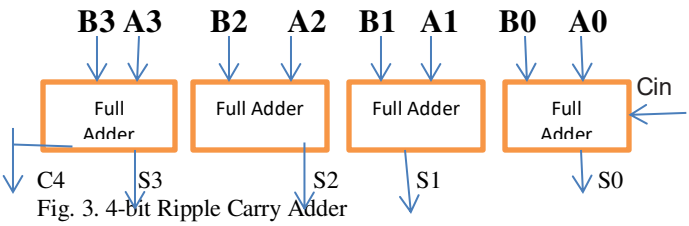

Fig. 3. 4-bit Ripple Carry Adder

This architecture proved highly successful in reference to time delay and stayed within appropriate bounds in power and area to yield a competitive APDP for 7nm, 14nm, 16nm, 45nm, 90nm, and 180nm technologies. All of these values can be seen in the results section.

We proposed 16x16 bit multiplier and 32x32 bit multiplier uses Ripple Carry Adder with partial product Concatenation (RCA-PPC) as shown in fig.4 and fig.5. For 16×16 bit multiplier, 32x32bit multiplier uses four 8x8bit sub-multipliers, 16-bit RCA and 24-bit RCA . Similarly for, 32x32bit multiplier uses four 16x16bit sub-multipliers, 32-bit RCA and 48-bit RCA.

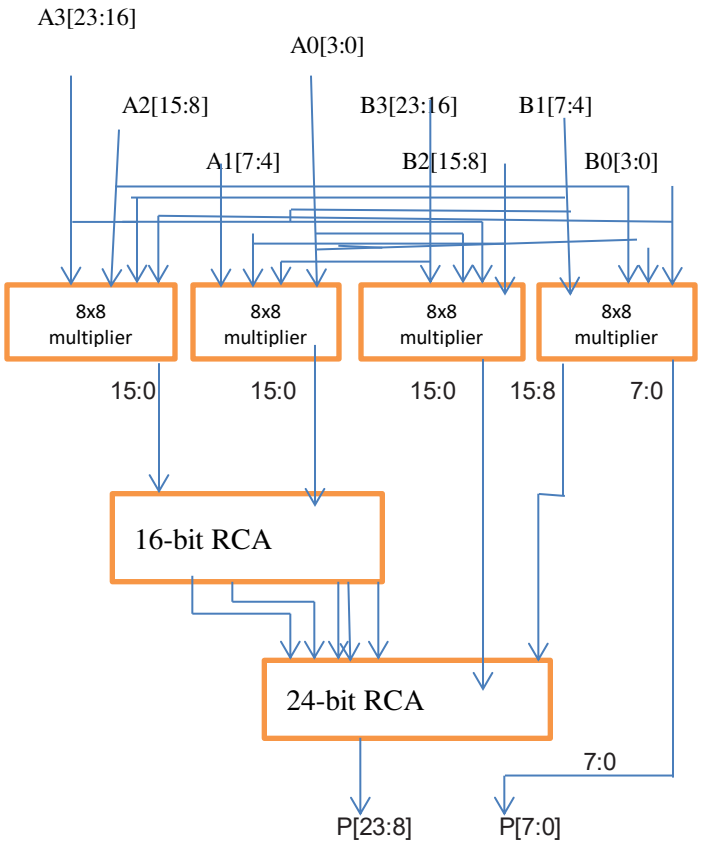

Figure 4. 16x16Bit RCA_PPC Multiplier

From the results we can observe that when compared to the existing architecture. RCA_PPC is 14.11%-46.33% faster, occupies 10.59%-15.38% less area and utilized 12.04%-22.13% less power. The Area Power Delay Product (APDP) of RCA_PPC has greater efficiency when compared to the existing architectures. The efficiency is also shown in PDP. The APDP of RCA_PPC is half the APDP of existing architectures.

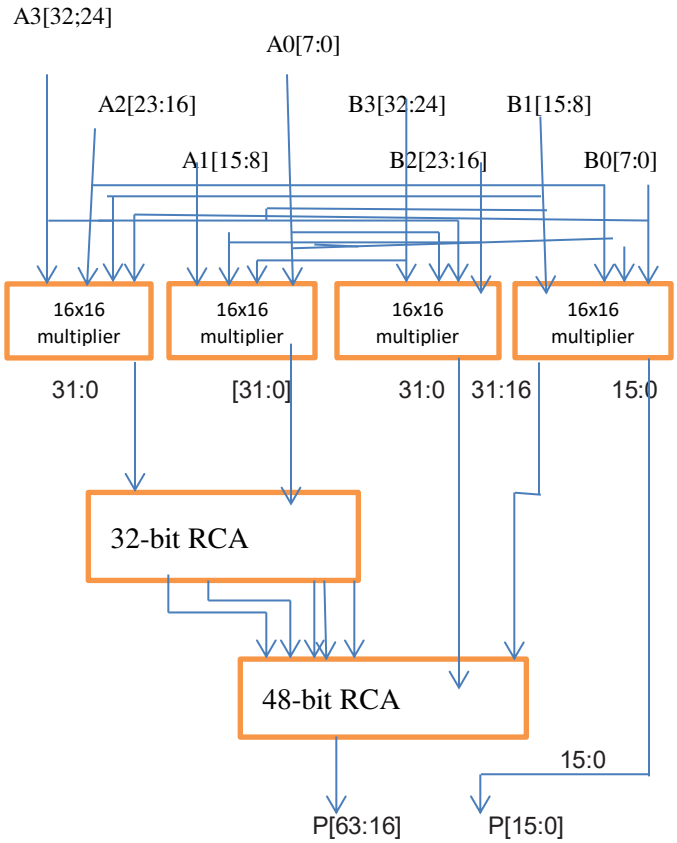

Figure 5. 32x32Bit RCA_PPC Multiplier

IV. Experimental Results

Table II: Performance Comparisons of Various Architecture

Technology	**45nm**				
Parameters Architecture	**Area (μm^2)**	**Power (mW)**	**Delay (ns)**	**APDP (aJs)**	**PDP (pJ)**
Vedic Math Technique [4]	23636.2	15.227	8.66	3116819.1	131.865
RCA_PPC	21304.3	14.352	5.03	1538047.3	72.194
Technology	**90nm**				
Parameters Architecture	**Area (μm^2)**	**Power (mW)**	**Delay (ns)**	**APDP (aJs)**	**PDP (pJ)**
Vedic Math Technique [4]	55089.5	29.792	10.01	16438542	298.396
RCA_PPC	50359.9	27.716	6.04	8430482.6	167.404
Technology	**180nm**				
Parameters Architecture	**Area (μm^2)**	**Power (mW)**	**Delay (ns)**	**APDP (aJs)**	**PDP (pJ)**
Vedic Math Technique [4]	203921	181.57	21.85	8.09E+08	3967.47
RCA_PPC	197744	171.88	12.55	4.27E+08	2157.13

V. CONCLUSION

The circuit implementation of both the proposed architecture for Vedic multipliers has been demonstrated which help us to obtain efficiency in area, power and speed. With a glance at the simulation results, it is clear that both of the Proposed Vedic multiplier architectures have a decrease of 11%-59% on Area- Power-Delay product (APDP) when compared to the previous Vedic multiplier designs. Simulation results prove that the first proposed architecture is highly efficient, particularly in terms of speed. When compared to the previous architectures, RCA_PPC is 14.11%-46.33% faster, occupies 10.59%-15.38% less area and 12.04%-22.13% less power.

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PAPR Reducing in FBMC Systems Using a SGPA Constellation Extension Method

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***Abstract*—The filter bank multicarrier (FBMC) modulation scheme has recently seen renewed interest and is being considered as a viable alternative to orthogonal frequency division multiplexing (OFDM). FBMC, however suffers from the same high peak-to-average power ratio (PAPR) drawback as OFDM systems. Conventional OFDM PAPR reduction techniques cannot be directly applied to FBMC due to the overlapping nature of FBMC symbols. A novel technique is proposed based on an evolution of the smart-gradient project active constellation extension (SGP-ACE) PAPR reduction method used for OFDM systems, namely the FBMC SGP-ACE method. The proposed method is applied to a set of contiguous FBMC symbols, thereby compensating for the overlapping nature of FBMC modulation. The proposed method requires less iterations than a projection-onto-convex-sets (POCS) ACE approach to converge to a lower PAPR and significant reduction in complexity can be achieved as opposed to current FBMC PAPR reduction techniques which tend to require the addition of advanced signal processing. The proposed FBMC SGP-ACE method outperforms a conventional FBMC POCS-ACE method by 2.6dB in PAPR reduction at a clip probability of 10^{-4} on the 1st iteration.**

I. Introduction

Filter bank multicarrier (FBMC) schemes have attracted increasing attention recently as a viable replacement to orthogonal frequency division multiplexing (OFDM) as well as a suitable candidate for cognitive radio applications. This is due to the increased frequency efficiency, improved spectral shaping and low out-of-band (OOB) interference inherent in FBMC techniques [1], [2], [3]. Tight spectral shaping is achieved through a bank of filters with longer impulse responses thereby increasing frequency domain resolution. The higher resolution increases the computational complexity when compared to an OFDM system, although the complexity can be reduced using an efficient polyphase implementation [2], [4], [5], [6].

FBMC suffers from a high peak-to-average power ratio (PAPR) that plagues all multicarrier systems. A high PAPR severely degrades the efficiency of the high power amplifier (PA) resulting in signal clipping if the PA is driven into saturation. This results in OOB interference as well as in-band interference, which negatively impacts the bit error rate (BER) of the system. OFDM PAPR reduction techniques are well established and can offer large PAPR reduction capabilities at mostly negligible BER degradation [7]. These techniques cannot however be directly applied to FBMC systems due to the symbol overlap inherent of FBMC systems. Current techniques for FBMC PAPR reduction require additional processing and often the added complexity of solving an optimization problem [8], [9], [10]. Iterative based FBMC PAPR clipping techniques [11] are often not feasible as the modulation process is considerably more complex than the OFDM counterpart, resulting in an unaffordable implementation.

The smart-gradient project active constellation (SGP-ACE) method for FBMC proposed in this paper, henceforth referred to as FBMC SGP-ACE, does not require the use of an optimization method or any significantly advanced signal processing. The FBMC SGP-ACE method applies simplistic signal processing in order to adapt the SGP-ACE method proposed for OFDM systems to an FBMC system [12]. ACE based methods have the added benefits of not requiring transmission of any side information, BER is not significantly degraded and all processing is performed on the transmitter side. No alterations are necessary on the receiver side. The main drawback of ACE based methods is an increase in average transmit power, albeit almost negligible [12]. It will be shown that the proposed method obtains significant PAPR reduction in a single iteration, by employing a relatively simple amount of signal processing. It therefore has significant complexity advantages over current FBMC techniques which either require a large number of iterations or advanced signal processing in order to obtain a significant PAPR reduction.

II. FBMC Modulation

FBMC modulated systems consist of a bank of well defined filters with tight spectral characteristics. These filters are effectively frequency and phase shifted versions of an original prototype filter with impulse response that complies with Nyquist constraints. The prototype filter response is designed to be K times longer than the maximum number of subcarriers N, giving a length of $L = KN$. This allows for increased

resolution in the frequency domain and better pulse shaping. K is also referred to as the overlapping factor and determines the number of overlapping complex symbols in the FBMC modulation technique. The symbol overlap is required to maintain the same theoretical throughput as that of an OFDM system.

A. FBMC-OQAM

FBMC requires purely real input symbols. Orthogonal quadrature amplitude modulation (OQAM) is a staggering technique used to transform complex input data symbols into real symbols at twice the sampling rate. OQAM is used in FBMC to ensure that only real symbols are fed into the filter bank. This is analogous to elements of a pulse amplitude modulation (PAM) system that are transmitted with a time offset of half a symbol duration $T_0/2$ [1]. The discrete signal at the output of the FBMC-OQAM modulator at sampling point n can be written as [11]

$$s[n] = \sum_{m=-\infty}^{\infty} \sum_{k=0}^{N-1} \theta_k \mathrm{R}\{X_m[k]\} p\left[n - mN\right] + \theta_{k+1} \mathrm{s}\{X_m[k]\} p\left[n - mN - \frac{N}{2}\right] e^{jk(n-mN)\frac{2\pi}{N}}, \tag{1}$$

with

$$\theta_k = \begin{cases} 1, & \text{if } k \text{ is even} \\ j, & \text{if } k \text{ is odd,} \end{cases} \tag{2}$$

where $X_m[k]$ is the complex input symbol at subcarrier k at time m, and R and s represent the real and imaginary components respectively and $p[n]$ is the prototype filter.

B. Polyphase implementation

A direct form implementation of (1) can be achieved using the transmultiplexer (TMUX) realisation. This is implemented using N upsamplers and a filter bank of N branches. However, filtering has to be applied to each upsampled subcarrier branch, greatly increasing system complexity [13]. A reduction in the complexity is obtained with the polyphase implementation, that employs the efficient inverse fast Fourier transform (IFFT) [4], [5], [6].

The output of the polyphase filtering process $Y(z)$ can be written in matrix notation as [6]

$$Y(z) = \boldsymbol{G}^T(z)\tilde{\boldsymbol{X}}(z^{N/2}), \tag{3}$$

where

$$\boldsymbol{G}^T = [tt_0(z)\ tt_1(z) \ldots tt_{N-1}(z)] \tag{4}$$

$$tt_k(z) = \sum_{m=0}^{L-1} p[m] e^{j\frac{2\pi k}{N}\left(m - \frac{L-1}{2}\right)} z^{-m}, \tag{5}$$

and m is the sampling index of the prototype filter. The matrix $\tilde{\boldsymbol{X}}(z^{N/2})$ represents the upsampled, OQAM processed, input symbols such that,

$$\tilde{\boldsymbol{X}}(z^{N/2}) = [\tilde{X}_0(z^{N/2})\ \tilde{X}_1(z^{N/2}) \ldots \tilde{X}_{N-1}(z^{N/2})]^T. \tag{6}$$

Making use of the low-rate polyphase filters [6]

$$A_k(z^2) = \sum_{t=0}^{K-1} p[k + tN] z^{-t}, \tag{7}$$

(3) can be implemented as illustrated in Fig. 1, where all upsampling is moved through the filters and IFFT processes by using the multirate identity [4], [5]. This allows the filtering to be applied at a lower sampling rate, greatly reducing the number of computations required [6].

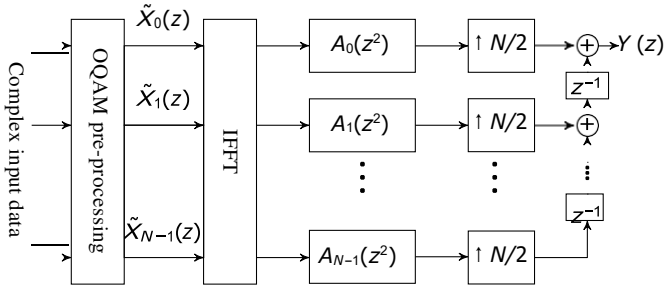

Fig. 1: Polyphase implementation of FBMC modulator

The delay line in Fig. 1 is of length N whereas the upsampling is only of length $N/2$ resulting in an effective delay line overlap. This implies that k-th and $k+N$-th subchannel could effectively share a delay line. This effectively compensates for the data rate loss due to OQAM modulation as the symbol rate is $T_0/2$. Once the system has reached steady state and taking into account the symbol overlap, the efficiency of the system can be seen as one complex symbol per sampling point for a critically sampled implementation. The effective throughput is therefore the same as an OFDM system without cyclic prefix (CP).

III. PAPR IN MULTICARRIER SYSTEMS

The PAPR is an important metric in multicarrier transmission schemes with a non-constant envelope. It is defined, with $x[n]$ the baseband modulated signal, as [14]

$$\mathrm{PAPR}(x[n])_{dB} = 10\log \frac{\max |x[n]|^2}{E\{|x[n]|^2\}}. \tag{8}$$

The cumulative complementary distribution function (CCDF) is an established method of measure for PAPR in multicarrier systems [12]. CCDF is defined as the probability that the PAPR of the m-th modulated symbol $\boldsymbol{x}_m$ exceeds a given threshold γ and is defined by [12]

$$\mathrm{CCDF}[\mathrm{PAPR}(\boldsymbol{x}_m)] = \Pr(\mathrm{PAPR}(\boldsymbol{x}_m) > \gamma). \tag{9}$$

A. OFDM case

The PAPR for the m-th symbol in an OFDM system is defined by [15]

$$\mathrm{PAPR}_m = \frac{\max |x_m[n]|^2}{E|[x_m[n]|^2} \quad n \in \{0 \le n \le N-1\}. \tag{10}$$

However, it is well established in literature that in order to accurately estimate the true analogue signal, oversampling of some form needs to be performed [12], [15]. In a critically sampled system, (10) is therefore a very optimistic approach to the true PAPR of the symbol.

B. FBMC case

Fig. 2. illustrates the overlapping nature of FBMC with an overlap factor of $K = 4$ [9]. It is clear that after the filtering process is applied, the symbols are extended in length by K. To compensate for OQAM modulation as well as the extended symbol length, the symbols are effectively overlapped with a factor of $2K$ as shown in Fig. 2. Due to the transient state present in an FBMC system, the PAPR cannot be accurately measured at the start and end of an FBMC data block. For accurate PAPR measure in an FBMC system, it is necessary to consider at least $2K+1$ symbols as shown in Fig. 2. The PAPR can then be measured in the steady state portion of the data block. The discrete baseband FBMC modulated signal $s[n]$ is then broken up into discrete symbols of length T_0 and the PAPR is measured over each symbol for accurate comparisons to an OFDM system.

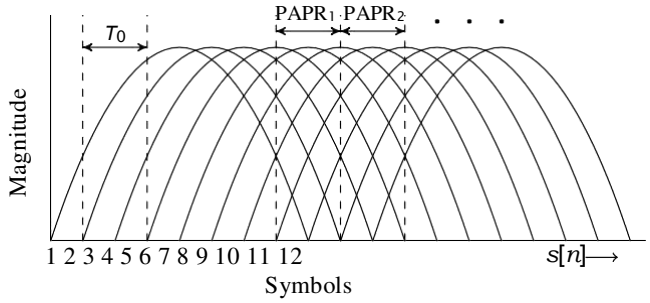

Fig. 2: Overlapping nature of FBMC modulation

If M FBMC symbols are transmitted, due to the nature of convolution applied in filtering, the output is of length $(M - 1) \times N/2 + L$. The discretely sampled data block $s[n]$ can therefore be defined, over a large number of transmit symbols M, with the following bounds

$$n \in \{0 \leq n \leq (M-1) \times N/2 + L\}. \tag{11}$$

The PAPR for the m-th symbol, as shown in Fig. 2, is defined as

$$\text{PAPR}_m = \frac{\max|s[m \times N + n + L]|^2}{E|[s[m \times N + n + L]|^2}$$
$$n \in \{0 \leq n \leq N-1\}, m \in \{0 \leq m \leq (M - 2K - 1)/2\}. \tag{12}$$

Equation (12) defines new symbols over which the PAPR can be calculated. If the sampling indexing n begins at zero at the start of each new period T_0, as shown in Fig. 2, the PAPR for FBMC in (12) reduces to the OFDM PAPR expression in (10). One can then obtain PAPR_1, PAPR_2 etc. such as in Fig. 2. It should be clear from (12) that as $M \to \infty$,

$$\text{PAPR}_m = \frac{\max|s[m \times N + n]|^2}{E|[s[m \times N + n]|^2} \tag{13}$$
$$n \in \{0 \leq n \leq N-1\}, m \in \{0 \leq m \leq M/2\}$$

where the transient response of the system can be neglected.

IV. PAPR REDUCTION USING ACE FOR OFDM

The ACE algorithm is well documented in the literature [7], [12]. It is an efficient method for reducing high PAPR in OFDM without requiring the transmission of side information. Projection-onto-convex-sets (POCS) ACE involves clipping the time domain signal after modulation, demodulating the clipped signal, and correcting the new constellation points. The constellation points that still satisfy the minimum Euclidian distance constraint are maintained whilst those that reduce the minimum Euclidian distance are corrected. All OOB distortion is also corrected. The new modulated signal therefore results in a reduced PAPR at the expense of a slight increase in average transmit power [12]. The smart-gradient project (SGP) method as applied in OFDM [12], is used to greatly reduce convergence time to a lower PAPR. The SGP method applies a scaling factor to the clipped portion of the modulated signal. The scaling factor is optimized by obtaining a maximum scaling value μ, per OFDM symbol, that can be applied without resulting in peak regrowth. For each OFDM transmit symbol, μ is calculated and applied to that symbol in order to reduce its PAPR.

V. PROPOSED PAPR REDUCTION METHOD FOR FBMC

PAPR reduction methods for FBMC have a higher order of complexity due to the overlapping nature of FBMC. It is also more difficult to define isolated discrete symbols of length L in an FBMC system when employing a polyphase implementation due to the overlap. Techniques that modify discrete symbols in order to reduce the PAPR, require additional signal processing. This added complexity may not always be practically viable.

The proposed method is performed on a multi-block level, thereby maintaining the continuous nature of the FBMC system and exploiting the polyphase implementation for reduced complexity. ACE based methods require modulation and demodulation in order to corret the constellations prior to transmission. Since these processes in FBMC involve a high complexity, it is of great importance to reduce the number of ACE iterations required for an achievable PAPR.

POCS based ACE methods require a large number of iterations to obtain significant PAPR reduction. An SGP method is defined based on an adaptation from the SGP implementation for OFDM systems defined in [12] in order to decrease convergence time and therefore reduce overall system complexity.

A. FBMC POCS-ACE

The multi-block approach requires PAPR reduction to be performed on a large data block i.e. a large number of

overlapping symbols. When applying POCS-ACE to FBMC a larger number of overlapping symbols must be accounted for, whereas in OFDM, POCS is performed on a symbol-by-symbol basis. In FBMC, after demodulation, multiple symbols are obtained due to the overlapping nature, if a multi-block approach is followed. The POCS approach is easily realisable by simply clipping the time domain signal above a certain threshold δ. This clipped signal is then demodulated and the constellation points corrected as in POCS-ACE for OFDM systems, but for multiple symbols.

The adaptation of POCS-ACE from OFDM to FBMC is relatively straight forward and respectable PAPR reduction can be obtained after a number of iterations. By defining $\varphi[n]$ as the phase angle of the n-th FBMC modulated sampling point taken from the M overlapping symbols, we can summarize the FBMC PAPR reduction algorithm by the following steps [12]:

1) Clip the discrete FBMC modulated baseband signal $s[n]$ to an amplitude of δ

$$s'[n] = \begin{cases} \delta e^{j\varphi[n]} & s[n] > \delta \\ s[n] & s[n] \le \delta \end{cases} \quad (14)$$

2) Compute the negative of the clipped portion of the signal $c[n]$

$$c[n] = \begin{cases} \delta e^{j\varphi[n]} - s[n] & s[n] > \delta \\ 0 & s[n] \le \delta \end{cases} \quad (15)$$

3) Demodulate $c[n]$ to obtain the extension regions $C_m[k]$ where m and k represent the frequency domain symbol and subcarrier respectively
4) Maintain only those real or imaginary components of $C_m[k]$ which fall within the allowable extension regions and set the rest to zero
5) For oversampling or digital frequency domain filtering, set OOB (out-of-band) components to zero, i.e. null all points greater than N [16]
6) Modulate $C_m[k]$ to obtain the time domain portion of the corrected clipped signal $\hat{c}[n]$
7) Scale $\hat{c}[n]$ by some constant μ and add it to the original time domain signal $s[n]$ to obtain $\hat{s}[n]$

$$\hat{s}[n] = s[n] + \mu\hat{c}[n] \quad (16)$$

8) Transmit $\hat{s}[n]$ if it meets PAPR requirements, otherwise repeat from step (1) replacing $s[n]$ with $\hat{s}[n]$

B. FBMC SGP-ACE

The SGP method is used to optimize μ in order to minimize peak regrowth. In order to apply the method for calculation of μ for OFDM, proposed in [12], to an FBMC system; we derive an expression to obtain an optimal μ across a large number M of overlapping data symbols. For OFDM, a μ value is calculated for each symbol. In the proposed FBMC implementation, a single μ is calculated for the entire block of M overlapping symbols, hence the term multi-block. This involves generating a large number of symbols and applying a standard POCS approach to obtain the clipped portion of the signal $\hat{c}[n]$ as described previously. Projections of $\hat{c}[n]$ onto the original signal $s[n]$ are then calculated. All positive projections result in possible peak regrowth, whilst negative projections imply amplitude reduction and therefore are not considered. An optimal ratio based on each sampling point and their relative projections versus the peak and its projections can then be calculated as in [12].

It is important to consider only projections once the system has reached steady state, i.e. between a full filter length L into the transmit signal and refrain a full filter length prior to the end of the block. This is illustrated in Fig. 3. As in Fig. 2, the transmit signal $s[n]$ is a function of the overlapping symbols. The transient response occurs up till symbol 8 for an overlap of $K = 4$. Any sampling point after symbol 8 is effectively a function of 8 overlapping symbols and therefore the system is considered to be in steady state. The optimal scaling point can only be calculated, as shown in Fig. 3 with $M = 11$, between symbol 8 and where symbol 12 would start. The dashed signal spanning the full length of the effective multi-block represents the corrected clipped portion of the transmit signal $\hat{c}[n]$ and is superimposed over the original transmit signal in Fig. 3. The solid section of $\hat{c}[n]$ illustrates the viable region over which μ should be calculated.

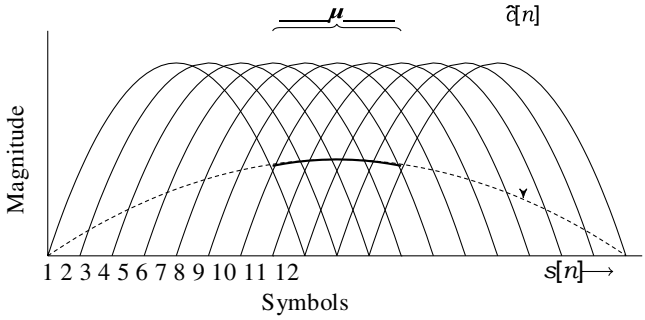

Fig. 3: Clipped signals superimposed over original FBMC modulated signal for $M = 11$

The SGP process for FBMC can be summarized as follows

1) Find the peak of the transmit data block, P, inside the viable or steady state region (the peak should always exist in the steady state region of the transmit data block) as well as the peak position n_{max}
2) Calculate the projections of the clipped signal $\hat{c}[n]$ only along the viable interval by performing the dot product:

$$c_{proj}[n] = \hat{c}[n] \cdot s[n] \quad n \in \{L+1 \le n \le (M-1) \times N/2 - L\} \quad (17)$$

3) Consider only the values of $c_{proj}[n]$ that are positive and therefore result in magnitude growth
4) Compute the scaling factor for each of these projections:

$$\mu[n] = \frac{P - s[n]}{c_{proj}[n] - c_{proj}[n_{\max}]} \quad (18)$$

5) Use the minimum value of $\mu[n]$ as the scaling factor for the whole data block, namely

$$\mu = min(\mu[n]) \quad (19)$$

6) Scale the clipped signal $\hat{c}[n]$ and add it to the original signal to obtain the new transmit signal

$$\hat{s}[n] = s[n] + \mu\hat{c}[n] \quad (20)$$

7) If μ is negative, stop the iterative ACE algorithm as any further PAPR reduction attempts will result in peak regrowth

VI. Results

All simulations were performed using the polyphase implementation for FBMC modulation and the PHYDYAS [6] prototype filter with $K = 4$. A critically sampled (digital) system was employed with 64 subcarriers employing QPSK modulation per complex symbol for accurate comparison to current FBMC PAPR literature. A clipping ratio δ of 5dB was chosen and 3 FBMC SGP-ACE iterations were performed per transmit data block of length $M = 25$ with 10^6 iterations.

A. Baseband performance evaluation of the proposed method

The CCDF performance of the proposed technique is shown in Fig. 4. The proposed technique offers significant PAPR reduction in a single iteration. A POCS method requires more than 4 iterations to achieve similar performance to a single FBMC SGP-ACE iteration. The proposed method compares favourably to OFDM based PAPR reduction methods which is also illustrated in Fig. 4. This illustrates that ACE methods can be effectively extended to FBMC implementations, with some additional signal processing, and still maintain good performance.

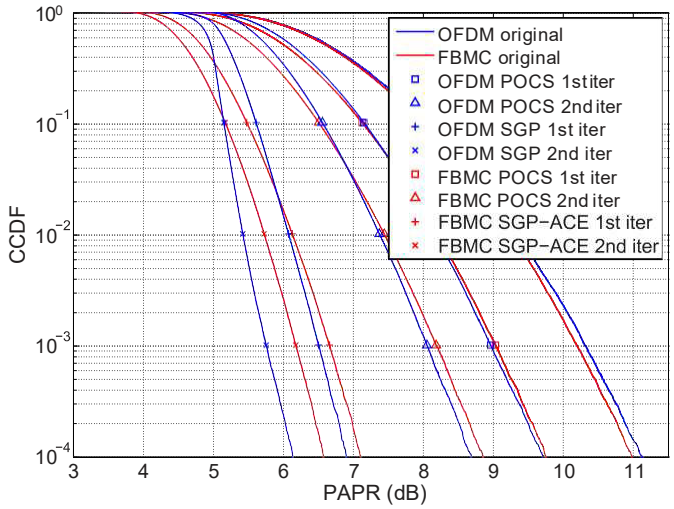

Fig. 4: PAPR performance comparison between proposed FBMC SGP-ACE and POCS-ACE algorithm with $N = 64$

The ACE algorithm has a minor affect on sidelobe amplitudes [12]. This stems from the increase in average transmit power of the system after the ACE algorithm is employed. This can be averted by not performing ACE on the edge frequency subcarriers [12]. The FBMC SGP-ACE method resulted in an increase in average transmit power of 0.256, 0.302 and 0.335dB for the 1st, 2nd and 3rd iteration respectively, as opposed to an increase of 0.049, 0.091 and 0.126dB for the 1st, 2nd and 3rd iteration in the POCS method.

A matter of critical importance is the spectral leakage of the proposed methods. FBMC offers very low spectral leakage, however, when a high power amplifier (HPA) clips, severe spectral leakage occurs. This is one of the fundamentally important features of PAPR reduction techniques, they prevent HPA clipping and therefore reduce unwanted OOB radiation. In order to accurately simulate and observe the results of the proposed PAPR reduction techniques in terms of power spectral density (PSD), the system was simulated using 64 active subcarriers with twice oversampling prior to 8 times oversampling for estimation to analogue. An ideal class A HPA was simulated with a clipping level of 5dB and the results of the OOB distortion can be seen in Fig. 5.

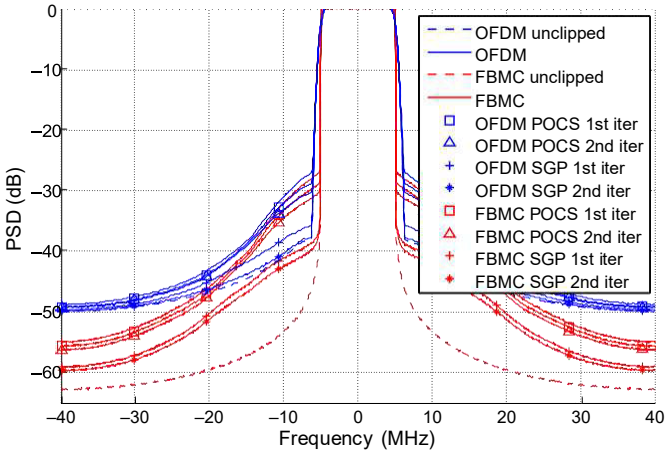

Fig. 5: Power spectral density effects of the proposed FBMC SGP-ACE method

A topic that is often averted in PAPR reduction methods is the bit error rate (BER) degradation associated with the relevant techniques. An increase in average transmit power, inherent of all PAPR reduction techniques, results in BER degradation, albeit mostly a non-significant amount. This stems from an increase in energy required per bit if extra information is added in the form of extra tones, constellation distortion or side information. The BER degradation associated with this increase in average transmit power using the proposed technique for $A = 5$dB, $M = 25$ and employing 64 subcarriers is illustrated in Fig. 6. It should be noted that, even though the ACE algorithm increases the minimum Euclidian distance of constellation points, this does not necessarily equate to increased BER performance. This issue is not mentioned by many authors. For a fair comparison, all systems need to be normalized to unity energy and therefore the ACE algorithm effectively adds variance to the constellation points. This

variance results in BER performance degradation. The POCS method also results in an increase in BER degradation, but because of the smaller increase in average transmit power for the 1st and 2nd iteration, it is not as noticeable as the proposed technique and is therefore not included in Fig. 6.

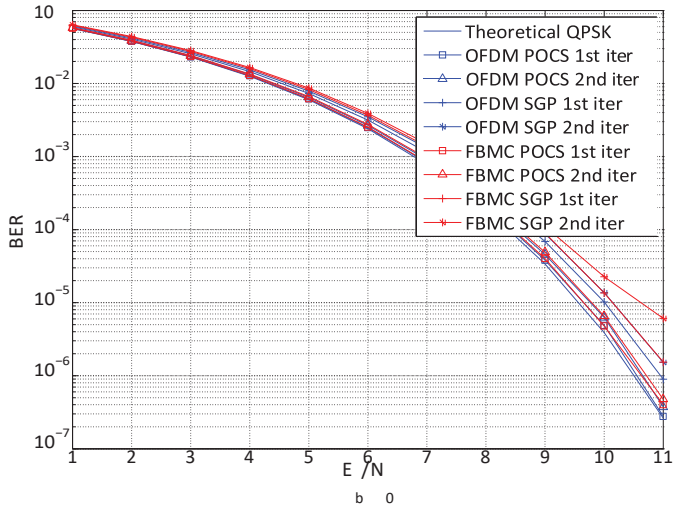

Fig. 6: BER effects of the proposed FBMC SGP-ACE method

B. Power amplifier efficiency

The PA operation point needs to be adjusted to the average input power of the multicarrier signal in order to avoid clipping. To accomodate the input signal in the PA dynamic range, we apply an input back-off (IBO) to the signal prior to amplification. The required amount of the IBO is closely related to the PAPR. Considering a linear class A amplifier, modelled as an ideal limiter, the PA efficiency η and the PAPR are related by $\eta = \frac{\eta^{max}}{PAPR}$ where $\eta_{max} = 50\%$ for an ideal class A amplifier.

Table I summarizes the PA efficiency obtained with the proposed techniques considering a clipping probability of 10^{-4}. Original FBMC and OFDM are also included for comparison purposes.

	OFDM	FBMC	POCS 1	POCS 2	SGP 1	SGP 2
PAPR [dB]	11.1	11	9.7	8.8	7.1	6.5
η %	3.88	3.97	5.35	6.59	9.75	11.2

TABLE I: PA amplifier efficiency for FBMC POCS and SGP-ACE PAPR reduction methods

VII. Conclusion

The proposed SGP-ACE algorithm adapted for FBMC modulation systems can significantly reduce the PAPR of the baseband signal. Just under 4dB PAPR reduction at a CCDF of 10^{-4} was achieved in a single iteration in a critically sampled system equating to an improvement of 2.6dB on the POCS approach. The PAPR reduction capabilities of the proposed implementation method for FBMC allows for similar performance gains when compared to an SGP method for OFDM. The increase in average transmit power is slightly larger for FBMC methods than OFDM methods which results in a slight decrease in BER performance. This is however an acceptable trade-off when considering the large decrease in OOB leakage that is achieved using the proposed FBMC method. The proposed method provides a low complexity implementation for PAPR reduction in FBMC systems by maintaining a polyphase based FBMC implementation, and the favourable results presented, provide further justification for consideration of FBMC as an alternate to OFDM.

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Literature Survey on UPQC based M3C and Flexible AC Transmission System.

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ABSTRACT

In this article, we discuss and learn about one of the most flexible alternate currents transmissions System (FACTS), which is a Unified Power flow controller (UPQC). Using an integrated power flow controller can control all power system parameters individually or simultaneously. The purpose of this article is to provide an overview of the load flow analysis integrated UPQC controllers for optimal power flow control. We also discuss the various control mechanisms of the UPQC dynamic models and various optimization techniques for optimal positioning. In order to improve the power quality in medium / high voltage distribution networks, this article presents a single-phase integrated power quality (UPQC) based on a modular multilevel matrix converter. (M3C). M3C-UPQC consists of four identical multilevel converter arms and filter inductors. According to the specified equivalent circuit M3C-UPQC, the operating principle and the power budget of each arm are theoretically analyzed, and the design parameters are examined for the inductance of the arm and the module capacity. Thus, an integrated control method for M3C-UPQC, in which the DC circuit current is used to instantaneously balance the active power in each branch, is provided to prevent the capacitor voltage from the divergence between and within the arm, thus obtaining the balance of M3C -UPQC Voltage. Finally, the effectiveness of the proposed control method is verified by an 8 kV prototype.

Keywords: UPQC, FACTS, PSO

1. INTRODUCTION:

In recent years, problems with energy quality have attracted more and more attention as more and more types of precision instruments are used. However, with large non-linear load applications and ground access of renewable energy associated with distribution systems, such as non-linear, switching, and reactive units, some low power quality (PF), undulation and sagging voltage, current harmonics [1], [2]. These common problems challenge the stability of the voltage and frequency associated with reactive and reactive power. In addition, distributed generators such as wind, solar and electric vehicles will play an important role in reducing the environmental impact of future distribution systems figure 1.

FACTS are widely used in energy systems around the world. This device is used to improve the operating options and to increase the power transmission capacity of the electricity grid. Semiconductor devices such as diodes, transistors, thyristors and GTOs are used to develop different types of FACTS. These devices have the ability to control many parameters of the transmission system, such as series impedance, shunt impedance, current, voltage amplitude, and phase angle. The FACTS controller is a system based on power electronics and other static devices that are capable of controlling various electrical parameters in a transmission network that can be adjusted to provide the right conditions for the transmission network. FACTS controllers have been shown to be able to be used to improve the control system, thereby minimizing higher transmission capacity and power losses in the transmission network [3].

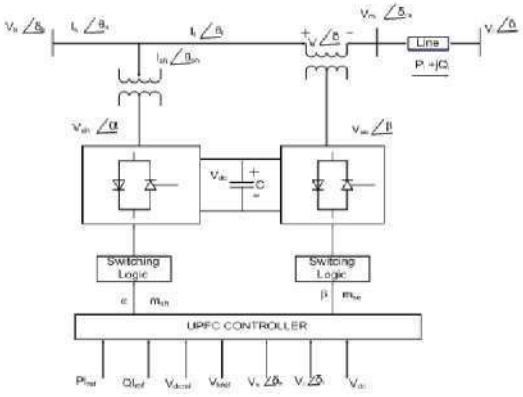

Fig 1: UPQC Block Diagram

Maximum performance with the FACTS controller to increase the TTC and minimize losses must be achieved by selecting the optimum number, parameters, and position in the transmission system.

Modern heuristic optimization techniques are successfully used to effectively solve complex optimization problems [4]. United current flow controller (UPQC) is the most versatile and most complex power electronic devices used to control and optimize the energy flow in a power transfer system. It offers the most important potential benefits for the operation of static and dynamic transmission lines. The UPQC combines the functions of different FACTS devices simultaneously with voltage adjustments to series compensation and phase angle, generating separate control commands for actual power and reactive power that are simultaneously transmitted via channel application. The UPQC is thus an effective means of managing the flow of energy and improving the temporary stability of the electricity grid. [5] The Unified Power Flow Controller (UPQC), the most efficient flexible AC transmission system (FACTS), maximizes the power transfer capabilities of the connected power supply systems. [6] With the UPQC the power supply of the voltage and bus channels can be regulated separately or simultaneously. Now the installation of FACTS devices in the flowchart of the algorithm is considered as a requirement for planning, implementation, and control. In general, the existing charging program must be changed to combine this device. Add assigned next to the reference bus the number of FACTS the network, FACTS are present, the force must be supplied by the fact impedance input in the original recording matrix and in the vector skew: necessary for various reasons, such as changes power. Excellent research has been done to reduce the complexity of load flow programs with UPQC devices [7]. UPQC is the most powerful and versatile FACTS device for controlling the energy flow and stability of the fuel system. The UPQC uses semiconductor devices that offer functional flexibility that is not normally achieved by conventional thyristor systems [8]. The UPQC is a combination of a static synchronous compensator (STATCOM) and a static synchronous serial compiler (SSSC) combined via a common DC voltage connection. The DC connection of the two converters is connected to the DC capacitors. Standard inverters control the voltage injection and phase angle in series with the lines to control the active and reactive power flow in the transmission line. That is why the serial converter exchanges the active and reactive forces with the line. UPQC can also work under static and dynamic conditions. Static analysis is a stable state and dynamics is an analysis of transition states as errors in the transmission system. It offers the possibility to simultaneously control all system transmission parameters, ie voltage, impedance, and phase angle [9]. There is a growing interest in more modular transducers plane (MMC) for years the effective reduce not only the switching devices but also greatly improve the quality of the waveform of the improvement of the output voltage [10] - [14]. In addition to the initial target applications associated with high-voltage DC transmission systems [15], MMC has been identified as an excellent solution for many other needs. To improve the quality of energy [16] the heavy systems using high voltage transformer point / neutral UPQC hybrid or multiple inverter-based studies [17]-[21], use a solution, lose and low cost

2. LITERATURE SURVEY

In this section, we summarize the short research activities on the integration of an integrated flow controller (UPQC) for energy flow control. Fuzzy regulator for power flow control based integrated dynamic power transmission ability "to improve conversion and management 79652 Energy: E" In 2014, Shameem Ahmad, M.albatsh Fadi Saad Mekhilf, Hazlie Mokhlis [1] a reading described as follows "-665. This article is a UPQC model (Dynamic Unified Power Flow Controller) designed to increase the Power Transmission Capacity (PTC) via the transmission line. The new UVP controllers were developed on the basis of FL controllers. The basis of the FL controller compared to the UPQC controller based on IP, where the FL-based controller manages the controllers based on IP.

Kamela 2014 F. Juradoa, J.A. Pecas [2] Lopes has published an article on "wishes UPQC models for the control of energy flow" published research into electrical energy systems. This article presents a comparative study of various Unified Power Flow Controllers (UPFC) implementation techniques in load flow algorithms. In addition to these techniques, this document introduces the UPQC model, which has been developed solely on the basis of the current injection approach. This model has been implemented in the current Newton-Raphson injection method (NR-CIM). This model examines the main weaknesses of earlier techniques.

In 2010 Suppakarn Chansareewittaya and Peerapol Jirapong [3] presented "Use Types improving the Multi-Controller FACTS transmission capacity Particle Swarm Optimization" a paper entitled in the IEEE conference publications. In this article Particle Swarm Optimization (PSO) is proposed to determine the optimal allocation of multi-type FACTS controllers to increase the transmission capacity power operations between the

sources and settle System domains shown in fig 2. Power Test system test results show that optimal OPF positioning with FACTS controllers over PSO can effectively improve the possibilities for energy transfer via PE. The advantage of PSO is that it offers greater benefits to accelerate costs and convergence percentages.

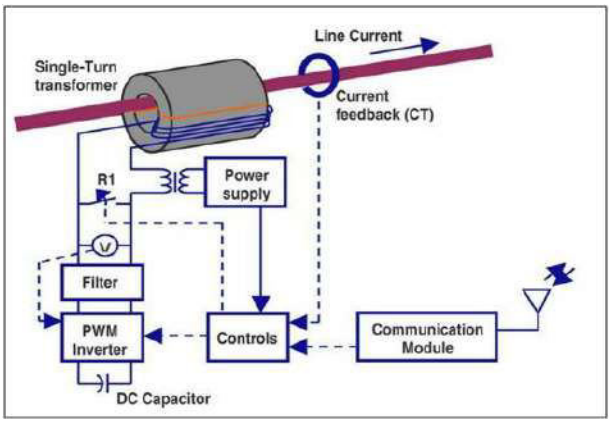

Fig 2: FACTS block diagram

In 2015, Kunal Gupta, Naseem Khan and Samina E. Mubeen [4] published an article on "Available transfer options via integrated power control" in the IEEE conference publication. On the liberalization markets, the available transfer capacities are of great importance. In this article, the authors associate the UPQC with a feeding system and increase the overall flow of the system by using it. The power source model of the FACTS device is built in due to its advantages due to the injection model. The bus system example 5 serves to display the results.

In 2012, Suppakarn Chansareewittaya and Peerapol Jirapong [5] conducted a study on "Improving total transmission capacity through the best use of hybrid numbers TSSA by UPQC" in the IEEE conference publications. This article proposes a method for Tabular Search in Hybrid Space research and simulated annealing (TSSA) to increase the optimal amount and distribution of power flow controllers (UPQCs) to determine the ability to transmit force transactions. Power between generator and load. System. Test results on the IEEE 118 bus system show that the optimal number of room management criteria and methods provided by the UPSC Hybrid TSSA UPQC survey yields a better return on the undivided search space method.

In 2016 Sandeep Sharma and Shelly Vadhera [6] published a paper on "Improving the transfer capacity of systems with use (UPQC)" in IEEE Vol. 3. This document suggests the use of UPQC façade models to maximize the power transfer capabilities of interconnected energy systems. Modeling is done in the Mat Lab / Simulink with a test system consisting of 20 bus systems that combine the UPQC. The results of this simulation give us a clear picture of the use of UPQC to connect two different power supply systems to maximize the actual current strength between them.

In 2012, Prof. Udaya Shankar, Nimmi Sreedharan, Dr. Rani Thottungal [7] a paper entitled "Improving the stability of the electricity network with optimal positioning of UPQC" in the international journal Advanced Engineering Research and Studies. To improve the stability of the feeding system, the authors introduce two optimization methods, such as conventional algorithms and genetic algorithms, to determine the optimal UPQC position. The simulation is performed with the 5-bus IEEE test system. Based on these results, both techniques were better used to optimize FACT devices and genetic algorithms that performed well compared to conventional algorithms.

In 1997 C.R. Fuerte-Esquivel E.Acha [8] a document entitled "Unified Power Flow Controller: Uncritical Comparison or UPQC Algorithm in Newton Raphson's Power Flow Studies" Titles in IEE Proc. Gener. Gearbox. Distrib. Bd 144, n. 5. This work presents a general model of UPQC energy flow. The UPQC model is included in the existing Newton Raphson FACTS Flow Charging Algorithm. Critical comparisons are made with the existing UPQC model, which shows that the new model is much more flexible and efficient. The algorithm maintains Newton's quadratic convergence and its efficiency is illustrated by a numerical example. The results obtained indicate that the SVS model should only be used if the UPQC branch converter is connected to an unrestricted busbar.

In 2015 MR Qader [9] presented an article on "Design and simulation of multiple controllers based on Integrated Power Flow Regulators (UPQC) to improve energy quality". This article provides a complete overview of the UPQC model under practical circumstances; The document also discusses control strategies and temporary models of the UPQC. The control system on the card can regulate the voltage/ flicker; eliminate harmonics at the same time. In addition, the MATLAB / Simulink model is prepared for the paper after analyzing the principles for UPQC in the Simulink environment. The results of tests with different modeling feeding systems are presented throughout the work to

illustrate the efficiency of an integrated energy flow controller.

In 2014, Jayanti Sarker published S.K. Goswami [10] an article about "Solutions for various UPQC positioning problems using the gravity search algorithm" in international journals on electrical and energy systems. This article presents a heuristic method based on the severity of the search algorithm (GSA) to find the optimal number and best location of the UPQC devices, considering the generation costs and losses of the electricity grid. The performance of the GSA is compared with the accuracy and convergence properties of heuristic research techniques. The proposed UPQC positioning algorithm has been tested on many real-world performance tests and systems and some results are generated in this document to determine the computational possibilities and robustness of the method.

After analyzing the research paper mentioned above, we investigate the following problems and solutions: Complications in large, interconnected systems have led to instability and reduced dependency on power, system flows and energy flows, and security problems have caused many disruptions in different parts of the system. World These problems and concerns are mainly due to systematic errors in planning and operation, network congestion, system connections with low power or maintenance errors.

The advantages of positioning the UPQC on system performance have been explored by various authors. Due to the high cost of UPQC equipment, their optimal position gives rise to serious concerns. The position of the device on the transmission line is responsible for the analysis of the parameters of the power system. This means that if we place the device in the wrong position of the transmission line, it will not work and after optimization will not give the best results for the parameters of the power system. For the best results, therefore, you must know the exact location of the UPQC before installation. Changes that are required for various reasons, such as: in addition to the reference bus that is linked to the number of FACTS to be added to the network, the FACTS impedance must be included in the initial admission matrix provided by the FACTS Performance. wrong alignment of power. The developed UPQC model can easily be inserted into the NR load current algorithm without changing the original Jacobi matrix.

3. CONCLUSION

After reviewing this report, we conclude that the integrated flow controller UPQC is one of the flexible AC transmission devices used to control the parameters of the flow system. Another thing is that there is another UPQC control mechanism among the fuzzy logic controllers, the best control mechanism for a dynamically integrated power control model. By finally entering the UPQC, we can control and improve the energy system in the transmission line.

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Energy-Efficient Hybrid TDMA/CDMA Protocol for Wireless Sensor Networks

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Abstract—**Smart city is a great promise to boost the living standards through effective management and utilization of scarce resources such as power, bandwidth, energy etc, in this paper, we review existing research endeavours and develop a smart energy efficient tool for the smart city. We also conduct some simulations and evaluations in smart energy, which will be an important application in smart cities. An energy Efficient and Effective Protocol for Wireless Networks which provide a novel low power guaranteed delay for wireless sensor networks (WSNs) is presented in this paper. The protocol used in this method is a Hybrid MAC protocol. It is a combination of TDMA and CDMA. This technique permits the network to work in a collision-free manner thereby boosting the smart city communications**.

Keywords— **CDMA, TDMA, MAC, WSN.**

1. INTRODUCTION

A wireless sensor network are of paramount interest for a smart city is a spatially distributed large network of sensor nodes [1].The constraint with the sensors network in smart city is that the wireless sensors and devices have limited resources.

Since WSNs are deployed in unmanned and hazardous environment, replacement or recharging of the batteries is difficult when it is depleted. A major problem with WSN is to determining a most efficient protocol for conserving energy in order to have a smart city.

Therefore, to make a city smart and big city, smart and strong communication infrastructure is required for connecting sensors with the smart objects or people. For performance enhancement and decision-making, the Smart cities also have to deal with a Big Data.

A Medium Access Control (MAC) protocol enables the sensor nodes access to the shared medium [3]. MAC protocol plays a major role in energy conservation.

Two important problems in MAC layer are message collision and idle listening [5]. The MAC protocols for WSN can be broadly classified into two categories [6], they are contention based and schedule based protocol. To deal with the problems aroused in MAC protocol, many MAC protocols have been proposed [7]. Few typical protocols are SMAC, DMAC, BMAC, ZMAC and HMAC.

The idea behind the Sensor- MAC [8] (S-MAC) protocol is: based on synchronizations. A drawback of the S-MAC algorithm is of two different schedules results in more energy consumption due to idle listening and overhearing.

The aim of DMAC [9] is to achieve low latency, but still to be energy efficient. Collision avoidance methods are not utilized is the major drawback.

The B-MAC utilizes an adaptive preamble to reduce idle listening. The disadvantage is that the performance creates large overhead.

ZMAC [10] uses CSMA basically but follows TDMA and it depends on the contention level.

HMAC [13] is based on the IEEE 802.11 Power Saving Mechanism (PSM) and slotted aloha. When nodes are in back off procedure and in idle mode, the energy consumption using CSMA/CA is high.

Hybrid TDMA/CDMA MAC protocols for WSN [14] merge the strengths of TDMA and CDMA while nullifying their weaknesses.

Based on the above hybrid MAC protocols, this presents a hybrid TDMA/CDMA MAC protocol for WSN that merge the strengths of TDMA and CDMA while alleviating their weaknesses and also allowing the network to operate in a collision-free manner. By merging the strengths of both the protocol, it helps to improve the network lifetime more efficiently, thereby a key success for a smart city

2. PROPOSED SYSTEM

In this section, TDMA and CDMA protocols are first briefly described and then the hybrid TDMA/CDMA MAC protocol is described.

2.1 TDMA

In TDMA protocol each node of a wireless network is assigned with a different time slot. Only for finite period of time, the entire bandwidth is available to the user. But TDMA requires time synchronization since users share the bandwidth in the frequency domain.

Data transmission in TDMA occurs randomly but occurs in bursts. This results in low battery consumption since when not in use, the subscriber transmitter can be turned OFF. Due to the intermitted transmission in TDMA the handoff process is much simpler for a subscriber unit, since during idle time slots it is able to listen to other base stations.

2.2 CDMA

CDMA is a multiplexing technique in which the data channel can be accessed by the user periodically [14].

The problem in CDMA is assigning of code to each terminal within a network. This problem is minor in small networks, but disquiet in large networks

2.3 *HYBRID TDMA/CDMA MAC PROTOCOL*

The Hybrid MAC protocol uses TDMA as the primary method and uses CDMA as the secondary method. Initially, a time slot assignment is performed, the interference with any of its previously-visited one-hop and two-hop neighbours are checked.

A new slot is assigned to one of the nodes if the conflict nodes have the same next-hop node,. But when conflict nodes have different next-hop node, they use the same slot but the spreading codes are different in order to minimze the interference. Every time the topology changed, the time slot assignment is not being used as in the case of TDMA, also Unlike CDMA, assigning a unique spreading code to every node is not required.

The hybrid TDMA/CDMA can tremendously increase the throughput and reduce the latency. So by combining the strengths of both TDMA and CDMA, the system becomes more efficient.

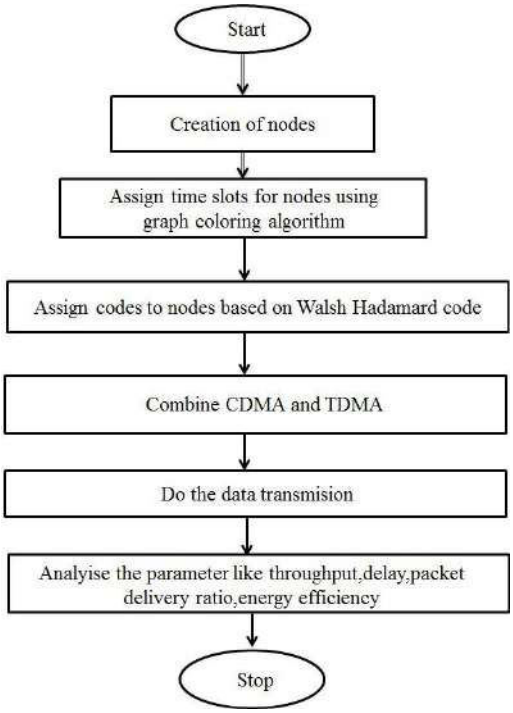

Figure 1 Flow Diagram of Proposed System

Figure 1 describes the proposed system. The nodes are first created in a network. The node initially senses the data and processes it. The time slot has been assigned for TDMA using graph coloring algorithm. Then, assign codes to nodes based on Walsh Hadamard codes. After assigning TDMA time slots and CDMA codes, combine both TDMA and CDMA and then perform the data transmission. Analyse the parameter like throughput, delay, and packet delivery ratio and energy efficiency.

For transferring the data without any interference , algorithm performs Graph coloring as scheduling algorithm. Graph coloring [15] is coloring the nodes of a graph with the least number of colors avoiding same color for any two adjacent nodes. Figure 2 shows the example of graph coloring algorithm.

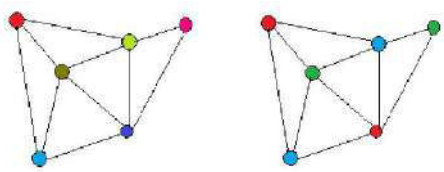

Figure 2 Example for graph coloring algorithm

The Graph Coloring is an assignment of colors (or any distinct marks) to the vertices of a graph.

$$G = (V, E) \longrightarrow (1)$$

where V indicates vertices and E indicated edge. [16].

Figure 3 shows the allotment of TDMA time slots to the nodes using Graph coloring algorithm are as follows:

- Calculate the maximum /minimum packet size of the frame.
- Calculate the maximum number of possible time slots can be divided within the packet size.
- Using Graph coloring algorithm, assign time slot to the nodes.
- Then, Check for conflicts between two hop neighbours and the adjacent neighbour, if there is any conflicts then again assign the time slot to the nodes
- If there is no conflict, then transmit the data.

The Time slot calculation for 802.15.4 is as follows: The maximum packet size that can be transmitted in 802.15.4 is 127 bytes. The time duration for 1 bit is 4µs.

The time duration for 1 packet transmission = max packet size*1 bit duration $\longrightarrow (2)$

$=127*8*4*10^{-6}$

$=4.06$ ms

The total time taken for packet transmission=12.288 sec

The guard time between two packets are taken as 0.5 ms.

Therefore, the total time duration for 1 packet transmission is given as, 4.56ms.

No. of users = Total time/ time duration for 1 packet transmission $\longrightarrow (3)$

$=12.288/4.06$ms

$=3026$

Since, 3026 users are not available; this can be divided into two slots. Therefore, the number of users will be 1513. Therefore, 2 packets can be transmitted in 1 slot.

1slot= 2* time duration for packet $\longrightarrow (4)$

$=2*4.56$ms

$=9.12$ms

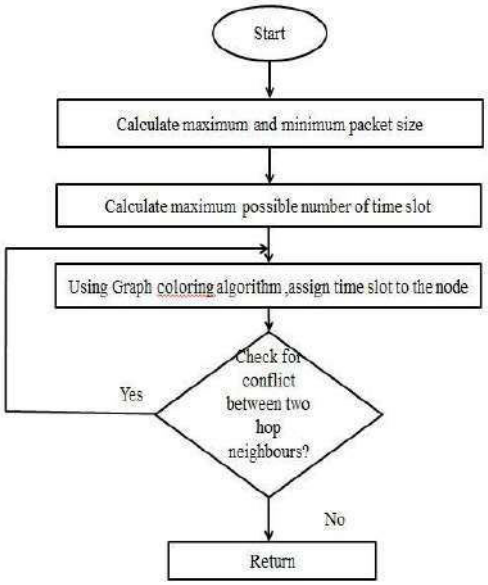

Figure 3 Flow Diagram of TDMA Time Slot Allocation

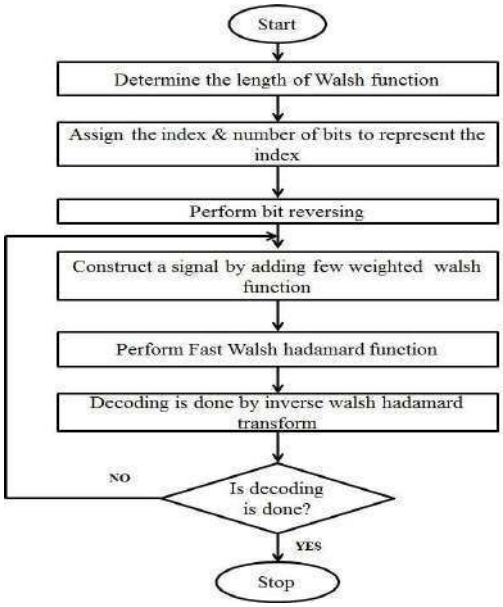

Figure 4 Flow Diagram of CDMA Code Assignment

Figure 4 describes the steps for CDMA code assignment:

- Determine the length of the Walsh function.
- Assign the index and the number of bits to represent the index.
- Then, perform bit reversing.
- Construct a signal by adding few weighted Walsh function.
- Perform Fast Walsh Transform
- Then by using inverse Walsh Hadamard Transform, decode the signal. Thus the reconstructed signal will be created.
- Compare the original signal and the reconstructed signal.

3. RESULTS

The simulation of the Hybrid TDMA/CDMA MAC protocol conducted using MATLAB.

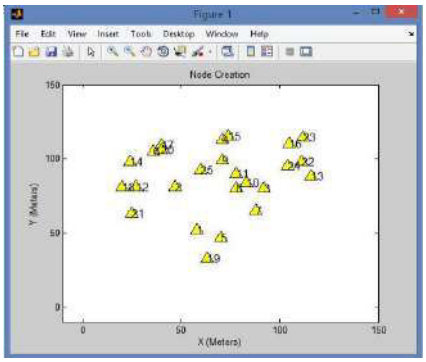

Figure 5 Topology of Network

The Figure 5 shows the creation of nodes.

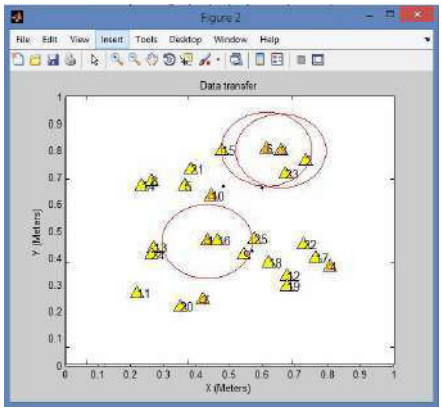

Figure 6 Data Transmission in a network

The Figure 6 shows the transmission of data between nodes.

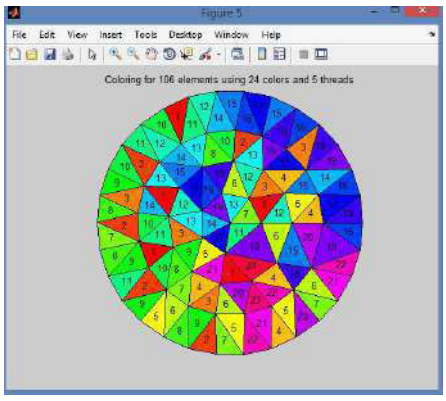

Figure 7 Data transmission within networks using 24 colors

The Figure 7 shows the transmission of data using graph coloring algorithm

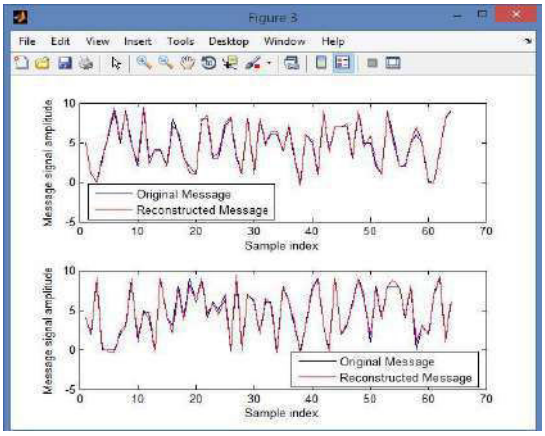

Figure 9 Decoded message of CDMA code using Walsh code

The Figure 9 shows the original message and reconstructed message of CDMA code by using Walsh Hadamard code.

4. CONCLUSION

In this paper, an energy efficient hybrid of TDMA/CDMA MAC protocol is proposed. Hybrid TDMA and CDMA is used in order to improve the network life time of the sensor nodes. By using TDMA and CDMA channel accessing, the delay of the data transmission is subsided and the energy efficiency of the network is increased, thus the life time of the sensor nodes are revamped. From the obtained results and performance analysis, it renders that the proposed system is satisfactory than the existing system. In a nutshell, the integration of new wireless technology protocol can bring stupendous improvement in future smart cities.

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Review on Flexible AC Transmission System Components in the Deregulated Power System

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***Abstract*—In deregulated power system, the flexible alternating current transmission system (FACTS) devices plays an important role for improving transmission system reliability, management, dynamic control of real and reactive power at significant buses and quality of power supply for sensitive industry. Many researchers have been developing innovative practices and procedures for effective implementation of FACTS components, but still plethora of nations are unable to use all FACTS devices such as static synchronous series compensator (SSSC), unified power flow controller (UPFC), static compensator (STATCOM, Static VAR Compensator (SVC), thyristor controlled Series Reactor (TCSR) and thyristor-controlled series capacitor(TCSC) due to their economical constrains and control issues in the online environment. This paper thoroughly reviews the impacts of different FACTS components on different issues of power system issues like stability, quality, control, load flow, power oscillation damping, avoidance of outage, reliability indices and so on. In particular this paper also includes the overview of FACT devices and its classification in different ways, different observations and identified the research gap to investigate further for effective utilization of FACTS devices in the modern power systems across the world.**

Keywords—FACTS, TCSC, SSSC, SVC , STATCOM, UPFC etc.,

I. INTRODUCTION

The FACTS controllers offer a great opportunity to regulate the transmission of alternating current (AC), increasing or diminishing the power flow in specific lines and responding almost instantaneously to the stability problems. Many researchers have been work with different FACT devices to improve stability on transmission line, for the last many years. *L'Abbate .et al*[1] has been presented the technical, economic and environmental Features of FACTS and HVDC on transmission expansion plan.A.K.Mohanty.et al [2] also presented Performance comparison of different FACTS controllers the likely future direction of FACTS technology. And FACTS applications to optimal power flow and deregulated electricity market.

M. M. Farsangi.et al [3] was also presented the importance of identifying effective stabilizing signals for the FACTS devices in a power system. Naresh Acharya .et al. [4] was presents the benefit gained from fact devices, issue related to fact controller, cost associated to these device and practical. L.Yao.et al [5] showed modified IEEE 30 bus system with/without the SSSC demonstrate the feasibility as well as the effectiveness of the SSSC for congestion management with high penetration of wind power in the netwok. O. L. Bekr.et al [6] was done on control model for a FACTS device (TCSC, SVC,UPFC) with concept of current injection method. Robson F .et al [7] proposed FACTS to drain, or inject, energy from the line without changing its electrical characteristic. Adamczyk. et al [8] was evaluated the performance of different FACT devices services and compares challenges of WPPs against FACTS solutions in the cause of wind generation.

Y. Han.et al [9] discussed technology used for application of smart grid such as un-interruptible power supply (UPS), adaptive VAR compensator (AVC), static synchronous compensator (STATCOM), active power filter (APF), unified power quality conditioner (UPQC), micro-grid, solar and wind generation, and high voltage direct current (HVDC) transmission technology.A.. Ch.Rambabu. et al [10] was done optimal locations of the multi-type FACTS devices to have a better voltage profile and power loss. P.Rames.et al [11] eliminated the common dc link between the shunt and series converter transmits power through the transmission line at the third-harmonic frequency with lower cost of the DPFC than the UPFC. P. Gopi Krishna et al. [12] presented the usage of UPFC in the computations of available transfer capability (ATC) in the deregulated environment, optimal location of UPFC, its effect on ATC on IEEE- 9 bus test system.

M.Eslami et al [13] was done on the necessary features of FACTS controllers and their potential to increase system stability and the location and feedback signals used for design of FACTS-based damping controllers were also discussed. A.K.M. Rezwanur Rahma.et al [14] A genetic algorithm has been presented with larger parameters than previous methods to optimally locate FACTS devices in the power system by simulated IEEE 30 bus and IEEE 118 bus. A.R. Krishna.et al [15] has been presented the right technology for improvement of power quality problem by using FACT device controller. Chonika .et al [16] presented various types of FACTS devices such as: load tap changers, phase-angle regulators, static VAR compensators, thyristors controlled series compensators, interphase power controllers, static compensators, and unified power flow controllers and there classification based on steady sate and transient state stability and Power electronic and control technology. Bhagyashri G. et al [17] increased the capacity of transmission line by super imposing dc in to ac transmission.

K. S. Mani.et al [18] FACTS SSFC scheme based on a tri-loop dynamic error driven intercoupled input to VSC controller for power quality improvement, voltage stabilization, power losses reduction and power factor enhancement and is interfaced with Smart Grid-Distribution Network has been presented. Jena R. et al and Liao H.et al [19][20] New FACTS topologies are emerging to ensure decoupled ac-dc interface, improved voltage security,

reactive compensation, voltage and power factor improvement, and loss reduction. Akanksha Singh.et al [21] was done on comparison on with and without STATCOM and TSC to control the power flow by testing five bus system using MATLAB.

The essential features of FACTS controllers and their potential to improve system stability is the prime concern for effective & economic operation of the power system. The motivation behind this review is an increasing steady state power system control problems and the need of controlling the active and reactive power flows in a transmission line by controlling its series and shunt parameters. This increases the requirement of comparison of different FACTS controllers in the power system for stability enhancement and selecting appropriate method for the problem after getting the gap on reviewed paper. The general objective of a review is to summarize and review different fact controller used in transmission system and finding the gap on the area.

II. Overview of FACTS devices

Most of FACTS devices were developed using power electronic components to improve the performance of weak AC Systems and to make long distance AC transmission feasible. Moreover, FACTS can help to solve various technical problems in the interconnected power systems. Different types of fact devices described in shown below. The FACTS devices are used in the different circuits by the symbols as shown in Fig.1.

A. Static compensator (STATCOM)

The STATCOM is a solid-state synchronous condenser connected in shunt with the AC system. Nodal voltage magnitude or the reactive power injected at the bus controlled by adjusting the output current [16].

B. Static synchronous series compensator (SSSC)

The SSSC is a series device of flexible AC transmission systems family using power electronic to control power flow and improve transient stability on power grids.in place of using capacitor and reactor banks [22-24].

C. Unified power flow controller (UPFC)

The UPFC consists of a static synchronous series compensator (SSSC) and a STATCOM, connected in such a way that they share a common DC capacitor. The UPFC, by means of an angularly unconstrained, series voltage injection, is able to control, concurrently or selectively, the transmission line impedance, the nodal voltage magnitude, and the active and reactive power flow through it. It may also provide independently controllable shunt reactive compensation [16][25][26][35-48].

D. Static VAR Compensator (SVC):

An electrical device used for providing fast-acting reactive power compensation on high voltage electricity transmission networks and SVCs are part of the FACTS device family, regulating voltage and stabilizing the system. It is known that the SVCs with an auxiliary injection of a suitable signal can considerably improve the dynamic stability performance of a power system [28-34].

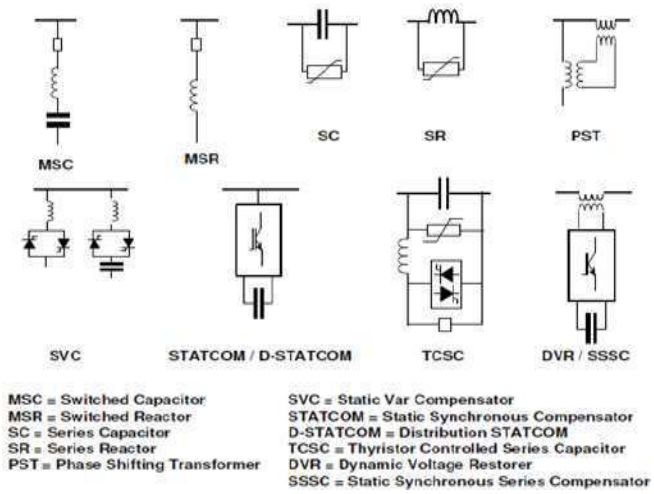

Fig. 1: General symbol of some FACT devices

E. Thyristor controlled Series Reactor (TCSR)

A TCSR consists of a series reactor in parallel with TCR so as to provide smooth variable series reactance control [58].

F. Thyristor-controlled series capacitor(TCSC)

Oscillations constitute a hazard to power system stability .The task of TCSC is to damp low frequency inter-area power oscillations between the power systems on either side of the inter-connection [60-66].

III. Classification of FACTS

After FACTS devices can be classified according to the power electronics technology used for the converters and as a voltage source controllers.

A. Thyristor-based controllers[95]

This category includes the FACTS devices based on thyristors, namely the SVC, the TCSC, the TCPST and the DFC;

B. Voltage source-based controllers

These devices are based on more advanced technology like Gate Turn-Off (GTO) Tyristors, Insulated Gate Commutated Thyristors (IGCT) and Insulated Gate Bipolar Transistors (IGBT). This group includes the STATCOM, the SSSC, the IPFC and the UPFC.

C. Traditional Classification

In the modern technology FACTs are classified in to two generations for realization of power electronics-based FACTS controllers: the first generation employs conventional Thyristor-switched capacitors and reactors, quadrature tap-changing transformers, that second generation employs gate turn-off (GTO) Thyristor-switched converters as voltage source converters (VSCs). The first generation has resulted in the Static Var Compensators (SVC), the Thyristor- Controlled Series Capacitor (TCSC), and the Thyristor-Controlled Phase Shifter (TCPS). The second generation has produced the Static Synchronous Compensators (STATCOM), the Static Synchronous Series Compensators (SSSC), Static switch filter compensator (SSFC), the Unified Power Flow Controller (UPFC) [73][74][75] and the Interline Power Flow Controller (IPFC).the system, large dynamic swings between different parts of the system and bottlenecks [76]. FACTS devices can be also traditionally classified according to their connection, as shown in Fig. 2.

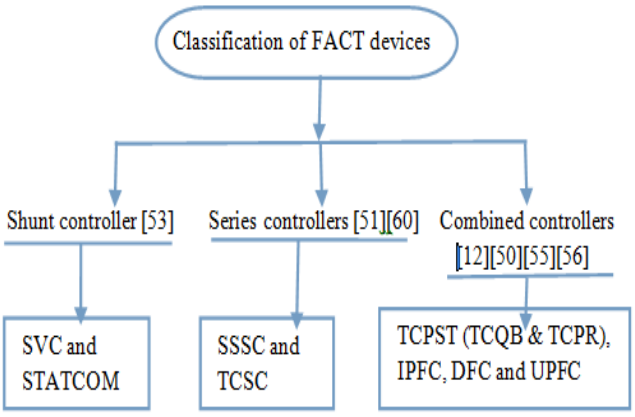

Fig. 2: Traditional classification of FACTS

D. Modern Classification

In the modern technology FACTs are classified in to two generations for realization of power electronics-based FACTS controllers: the first generation employs conventional Thyristor-switched capacitors and reactors, quadrature tap-changing transformers, that second generation employs gate turn-off (GTO) Thyristor-switched converters as voltage source converters (VSCs). The first generation has resulted in the Static Var Compensators (SVC), the Thyristor- Controlled Series Capacitor (TCSC), and the Thyristor-Controlled Phase Shifter (TCPS). The second generation has produced the Static Synchronous Compensators (STATCOM), the Static Synchronous Series Compensators (SSSC), Static switch filter compensator (SSFC), the Unified Power Flow Controller (UPFC) [73][74][75] and the Interline Power Flow Controller (IPFC).the system, large dynamic swings between different parts of the system and bottlenecks [76].

There is also new generation in addition to first and second generations which is called as a last generation or DFACT devices. They are smaller and less expensive than traditional FACTS. DFACT devices are used in distribution systems, while FACT devices are used in transmission systems. The most examples of DFACT devices are D-STATCOM and DSSC. In this paper, the another classification of FACTS devices based on principle and impacts on system performance is described in the section-E.

E. Classification based on pricipe

Flexible AC transmission system devices are classified in three different categories depend on its principle as shown Fig. 3 [82 - 87].

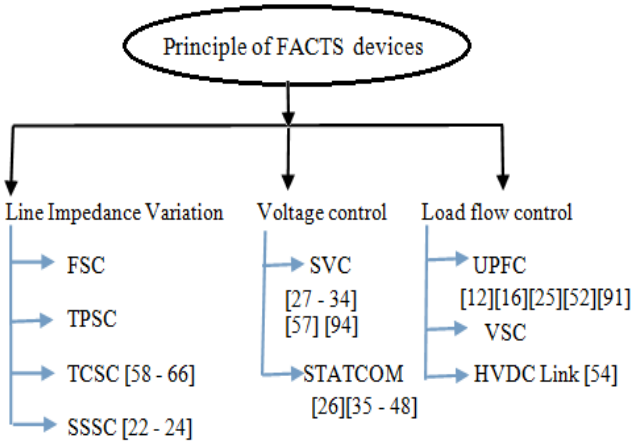

Fig. 3: Classification based on principle

The FACT devices has several impacts on the transmission system performance described in Table I.

TABLE I. Impacts of FACTS devices on system performance

Impacts on system performance	FSC	TPSC	TCSC	SVC	STATCOM	UPFC	VSC
Load Flow	Small	Small	Medium			Medium	Strong
Stability	Strong	Strong	Strong	Medium	Medium	Strong	Strong
Voltage Quality	Small	Small	Small	Strong	Strong	Strong	Strong
Voltage control	Medium		Strong	Strong	Strong	Strong	
Reactive Power Control	Strong			Strong	Strong	Strong	Strong
Avoidance of outage			Strong	Strong	Medium	Strong	
Unbalance Control (Option)			Medium	Strong		Strong	Strong
Power Oscillation Damping (POD)				Strong			Strong
Thermal Limit Action	Medium	Medium	Strong	Strong	Strong	Strong	

F. Comparison of different Research works

The researchers work on FACTS as per this paper references is shown in Fig. 4 by rising order using pyramid and the cost of different FACTS devices are shown in Fig. 5.

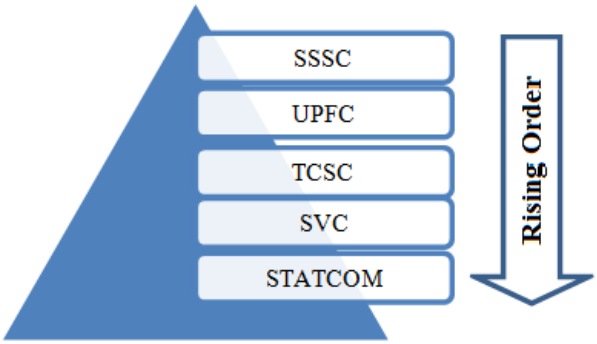

Fig. 4: Amount different works done by researchers

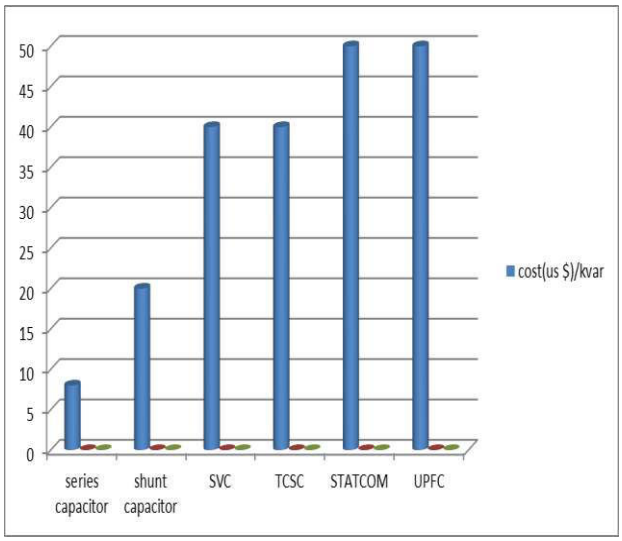

Fig. 5: Costs of different FACT devices

G. Benefits and challenges of FACTS [77]

- FACTS devices stabilize transmission systems with increased transfer capability and reduced risk of line trips.
- The improved stability in a power system substantially reduces the risk for forced outages, thus reducing risks of lost revenue and penalties from power contracts.
- FACTS devices can help to provide the required quality including constant voltage and frequency, and no supply interruptions. Voltage dips, frequency variations or the loss of supply .
- FACTS installation has the flexibility for future upgrades and requires small land area.
- The construction of new transmission line has negative impact on the environment.
- Utilizing the transmission systems optimally with the use of FACTS, the total number of line fault is minimized, thus reducing the maintenance costs.
- FACTS devices comes from the additional sales due to increased transmission capability, additional wheeling charges due to increase transmission capability and due to delay in investment of high voltage transmission lines or even new power generation facilities.
- As compared to conventional devices, FACTS controllers are very expensive.
- It makes system complexity than the conventional method.

IV. Observations and Key References of the Review

This section includes the overall observations and the key references of different research works on FACTS devices.

- The UPFC is the most powerful and versatile FACTS device. The line impedance, terminal voltages, and the voltage angle can be controlled by it as well [6].
- All thyristors based technology is has slower response times than modern fully controllable semiconductor devices [9].
- The multi-type FACTS devices located at their own optimal locations is observed to have a better voltage profile and power loss [10].
- Typical delivery time and size of CSC is higher than other device.[16]
- VSC-based FACTS devices including IPFC and SSSC, shunt devices like STATCOM, and combined devices like UPFC, are more complex and usually modeled as controllable sources. [78, 79].
- A new hybrid model for OPF incorporating FACTS devices was investigated to overcome the classical optimal power flow algorithm where load demands, generation outputs, and cost of generation are treated as fuzzy variables. An improved GA was presented to solve OPF problems in power system with FACTS where TCPS and TCSC are used to control power flow [80, 81].
- It is observed that the damping introduced by the SVC and STATCOM controllers with only voltage control was lower than that provided by the PSSs and the STATCOM provides better damping than the SVC as this controller is able to transiently exchange active power with the system [82].
- Some researchers concerned with enhancing the steady state and dynamic performance of the Flexible AC Transmission System (FACTS) using Computational Intelligence methods, like Genetic Algorithms (GA), Fuzzy Logic (FL), Neural Networks, (NN), and Adaptive Neuro-Fuzzy Inference Systems (ANFIS)

V. Conclusions and Recommendations

A. Conclusions

Most researchers are doing with STATCOM and UPFC but still there is a gap in this area especially in the developing countries. UPFC works best for control of power flow, DVR as a series compensator is used for voltage sag compensation and STATCOM as a shunt compensator is employed for compensation of both reactive power and voltage sag. As STATCOM, DVR, UPS etc., are useful for compensating a specific kind of power quality problems, it has become significant to develop a new type of Unified Series-Shunt Compensator (USSC) which can reduce a wider range of power quality problems. FACTS based Static Switched Filter Compensator (SSFC) scheme for effective

power quality enhancement, voltage stabilization, power factor improvement and losses reduction in distribution grid networks with the distributed wind energy interface. Generally this paper shows which FACT devices are used to improve power quality, voltage profile, stability (either dynamic or static) and soon, with high controlling capability.

B. Recommendations

The recommendation only based on the references including in this paper.

- VSC based devices like STATCOM, SSSC, or UPFC are more attractive, because their operation in not so strongly dependent on the grid conditions for stability of wind generation.
- Combining STATCOM with TSC to extend operational range in addition to more sophisticated control systems will improve the operation facts devices
- Improvement in semiconductor technology with higher current carrying capability and higher locking voltages could reduce the cost of facts devices and extend their operation range.
- It is recommended that Future applications of FACTS devices include renewable energy resources, residential and commercial smart building, residential use of hybrid DC-AC grid, increased use of vehicles-to-grid and vehicles-to house, battery charging system, and street, buildings and airports light emitting diode (LED) lighting technology.
- For better reduction of ripple and total harmonic distortion at the AC side recommended that working with multi-stage voltage source inverters with switching strategies based on double carrier, inverse sine carrier and optimized switching techniques.

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Implementation of XOR and Edge Identification Method in Steganography

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Abstract:

In this paper, a novel image steganography algorithm that combines the strengths of edge detection and XOR coding, to conceal a secret message either in the spatial domain or an Integer Wavelet Transform (IWT) based transform domain of the cover image is presented. Edge detection and XOR coding are used in to conceal the secret message. Edge detection enables the identification of sharp edges in the cover image and this when embedding results in good image quality. Edge detection method presented here is capable of estimating the exact edge intensities for both the cover and stegno images (before and after embedding the message), which is essential when extracting the message. The XOR coding, on the other hand, is a simple, yet effective, process that helps in reducing differences between the cover and stegno images. Experimental results are observed using XILINX ISE and demonstrated that the proposed method has achieved better imperceptibility results than other popular steganography methods.

Keywords- Image Steganography, Human Visual System (HVS), EDGE detection and XOR Coding.

I. INTRODUCTION

Steganography is an art of hiding information in a way that prevents the detection of hidden messages and this is achieved by hiding one piece of information within another piece of innocent-looking information. Spatial and time domain methods, Transform domain methods and fractal coding methods are the several methods of embedding data. These methods hide / embed information in different types of media such as video, audio, image, text, etc. Varieties of different file formats, digital images are considered the most popular type of carriers because of their size and frequency of distribution. Image steganography is the steganography subdivision where digital images are used as information carrier file formats. The joint image format (JPEG), the graphics exchange format (GIF), the bitmap (BMP) image format and the Portable Network Graphics (PNG) format are the most popular image file formats Share on the Internet. Steganography is the art of hiding messages in a medium called a cover object in such a way that

the existence of the message is undetectable. Imperceptibility is clearly the most important requirement. The cover object can be a digital image, an audio file or a video archive. The secret message called payload could be plain text, an image, a video file or an audio. Steganography methods are classified in the domain spatial domain and domain incorporation Embedding In the frequency domain, images are transformed into frequency components DCT, FFT or DWT and then the messages are embedded in the bit level or in the block level. In Space domain LSB replacement is the most widely used data hiding method. However, most of the LSB techniques are prone to seizures. Due to the low computational complexity and high This work is mainly concerned with the LSB steganography method.

Imperceptibility is an essential requirement for steganography techniques, which reflects the ability of these techniques in maintaining the visual quality of the produced stegano images. It is well known that the HVS is less sensitive to changes in sharp areas of images compared to smooth areas. The first steganography method designed based on this fact was the Pixel-value differencing (PVD), which attempts to embed into sharp areas. The original PVD algorithm introduced by Wu and Tsai (2003) converts the 2D image into a 1D vector. The number of bits that can be used for embedding in each pixel is calculated based on the difference between that pixel and its neighbour. Thus, more bits are to be embedded in a pixel if its grey level is noticeably different from that of its neighbouring pixel. This method, however, only considers differences in one dimension (either horizontal or vertical), which does not guarantee that all edges are identified.

II. LITERATURE SURVEY

Since the early stages of the human civilization, there has been an increased interest in information security, particularly the protection and privacy of communications (Pal & Pramanik, 2013). In modern societies, the excessive use of electronic data has made protection from malicious users more difficult (Grover & Mohapatra, 2013). Information hiding has emerged as an effective solution to this problem (Wu & Tsai, 2003; Wu, Lee, Tsai, Chu, & Chen, 2009).

Steganography is a kind of information hiding, in which a secret message is concealed within digital media (image, audio, video or text data) (Bassil, 2012; Cheddad, Condell, Curran, & Mc Kevitt, 2010). This property distinguishes steganography from other information security techniques (Modi, Islam, & Gupta, 2013). For instance, in cryptography, the message that needs to be transferred is encrypted to prevent intruders from understanding it. Hence, people can recognize the existence of the message, however it cannot be understood without decryption (Bassil, 2012; Cheddad et al., 2010; Verma, 2011).

As opposed to data concealing, steganalysis was initially designed to distinguish whether a given digital media has a secret message embedded in it.

Moreover, some steganalysis methods may determine the type of steganography technique or estimate the length of the secret message (Li, He, Huang, & Shi, 2011). In term of security measurement, steganalysis has been utilized to evaluate the efficiency of steganography techniques from a security point of view (Geetha, Ishwarya, & Kamaraj, 2010). Steganalysis methods can be performed either by using image processing operation or by implementing methods that analyze the statistical features of the stegno image structure, such as first order statistics (histogram) or second order statistics (correlations between pixels) (Cheddad et al., 2010). Ziou and Jafari suggested five requirements for steganalysis methods: (1) detection of the existence or absence of an embedded message in a given image, (2) identification of the stegano graphic method that have been used to hide the secret message, (3) approximation of the hidden message length or location and (4) extraction of the secret message (Ziou & Jafari, 2014).

Table 1
Differentiation between image steganography schemes in spatial and transform domains.

Domain	Advantages	Disadvantages
Spatial Domain	High embedding capacity Shorter computational time High controllable imperceptibility	Vulnerable to geometric attacks.
Transform Domain	Robustness against attacks such as Geometric attacks and compression	High computational time Limited embedding capacity Lower controllable imperceptibility

In order to enhance the embedding efficiency, coding methods (mainly matrix encoding) have been introduced with the aim of minimizing the modifications created by embedding the message (Crandall, 1998; Hou, Lu, Tsai, & Tzeng, 2011).

In this paper, we propose a useful and basic picture steganography technique that depends on recognizing edge areas on the cover picture and joins a XOR coding capacity. The XOR work, which has a lower calculation multifaceted nature contrasted with other grid encoding techniques, includes some security and lessens the bending caused by installing the message. Implanting in both spatial and wavelet changed spaces has been executed.

III. RELATED WORK

Wavelet transform

Change space implanting techniques give a larger amount of strength, especially while applying some picture handling activities, contrasted with spatial area strategies. A standout amongst the most mainstream changes is the Discrete Wavelet Transform (DWT) (Baby, Thomas, Augustine, George, and Michael, 2015; Thanikaiselvan et al., 2014). The Wavelet change requires less computational expense contrasted with DCT and FFT (Fourier Transform) and offers sub-portrayals of the picture that can be viewed as identified with how the human visual framework (HVS) sees pictures. By and large, the wavelet change permits inserting information in high recurrence districts where the HVS can't recognize alterations contrasted with uniform areas with low recurrence (Sharma and Swami,2013). At the point when DWT is performed to a picture it is separated into 4 sub-groups: Low– Low (LL), Low– High (LH), High– Low (HL) and High– High (HH) recurrence sub-groups, as appeared in Fig. 1. The low recurrence sub-band speaks to coarse data of pixels, while the high recurrence sub-groups speak to the edge data (Sharma and Swami, 2013). Concealing Information in the high recurrence sub-groups (LH, HL, and HH) builds the vigor and guarantees the visual quality, where the HVS is less delicate to alterations in these sub-groups. The Integer Wavelet Transform (IWT) maps whole numbers to whole numbers and enables the development of lossless pressure to precisely recover the first information (Thanikaiselvan et al., 2014).

EDGE detection in steganography

The usage of edge identification in picture steganography has been considered by various scientists. Because of affectability of the human eye to changes in smooth regions of the picture contrasted with sharp difference zones, it is sensible to concentrate on sharp edges while implanting the mystery message. In any case, the primary snag to applying conventional edge discovery techniques in picture steganography is the right ID of edge pixels in the stegno picture S that need to precisely coordinate the first edge pixels in the cover picture C. This issue emerges from the way that the implanting procedure acquaints minor changes with the stegno picture, which may make the created stegno picture not indistinguishable with the cover picture, and this can influence the message extraction process. A portion of the current edge-based steganography techniques proposed certain answers for conquer this issue. An edge picture is made by performing Canny and fluffy edge recognition strategies. The cover is then conveyed into squares of n pixels. The principal pixel of each square is changed to speak to the status of (n − 1) pixels on the off chance that it is considered as edge pixel. LSB strategy is utilized to insert x bits into non-edge pixels and y bits into edge pixels. The principle downside of this strategy is the undesirable adjustment that are made in the stegno picture in light of the fact that the technique replaces (n − 1) bits from the main pixel of each square.

Coding theory

Upgrading the implanting productivity has been the focal point of numerous steganography calculations, as limiting the measure of changes in the picture while inserting (installing rate) will empower the installing of greater messages. Crandall's technique uses the XOR capacity to cover 2 bits of message into a square of 3 pixels. The F5 steganography calculation, proposed by Westfeld (2001), is the principal execution of grid encoding to build the limit of installing information and in addition to limit the difference in DCT coefficients. This strategy has turned out to be outstanding on the grounds that it incorporated the Hamming code with the change area execution, which can install k bits of the mystery information in 2k − 1 cover bits by changing at most one piece as it were. Accordingly, this technique has a constrained inserting limit, for instance when k = 3, the strategy just implants 3 bits in each 7 bits of the cover picture.

IV. PROPOSED SYSTEM

The spatial domain algorithm Identification of edges:

The edge picture created by conventional edge identification techniques is normally delicate to changes in the first dark picture, regardless of whether the progressions are minor or not huge. This property restrains the use of edge location in steganography, as covering the message would acquaint a few changes with the first picture. Along these lines, implanting in pixels distinguished by one of the current edge discovery strategies, for example, Canny, can't ensure the ID of the correct edge powers for the cover and stegno pictures. Here a basic better approach to find the edge (sharp) locales of the cover picture, to such an extent that the two edge pictures created utilizing the first cover picture and the stegno picture are indistinguishable is proposed. This will empower the right extraction of the disguised message from the stegno picture. The calculation begins by partitioning the picture into non-covering hinders that would be separately assessed for incorporation of edges. The key thought behind protecting a similar edge picture isn't to insert in the pixels that are utilized to figure the edge quality, which are the external pixels of the square.Below are the detailed implementation steps.Sources of info: Cover picture (C), square size (n × n, which is required here to be 3 × 3), limit (Th runs somewhere in the range of 4 and 96)

Yield: edge picture with edge greatness (E) Step 1: Divide the picture C into non-covering squares of the size n × n.

Step 2: Compute without a doubt the mean distinction between the left and right segments of the square (greatness of vertical edge). Rehash for even, first slanting and second corner to corner edges. Fig. 3(a) demonstrates the explicit pixels used to compute the edges for the 3 × 3 square.

Stage 3: Find the most extreme of the four qualities and allot it to e. On the off chance that e > Th, the square is viewed as an edge square, else it's anything but an edge square. Build E that contains the determined estimation of every one of the edge squares, and 0 for non-edge squares. A paired edge picture can likewise be built, which contains 1 for edge squares and 0 for non-edge squares.

Stage 4 : For the edge squares, install in the shaded 5 pixels.

Message installing:

The stream graph of our proposed strategy is shown in Fig. 1. The information installing process starts with perusing the cover picture and the mystery message. A high edge (96) is at first considered, which is then balanced dependent on the quantity of pixels required for installing (distinguished by the produced double edge picture) and the message length, as per the accompanying condition:

Step 5 : For the edge blocks, embed in the shaded 5pixels.

Message embedding:

The flow diagram of our proposed method is illustrated in Fig. 1. The data embedding process begins with reading the cover image and the secret message. A high threshold (96) is initially considered, which is then adjusted based on the number of pixels needed for embedding (identified by the generated binary edge image) and the message length, according to the following condition:

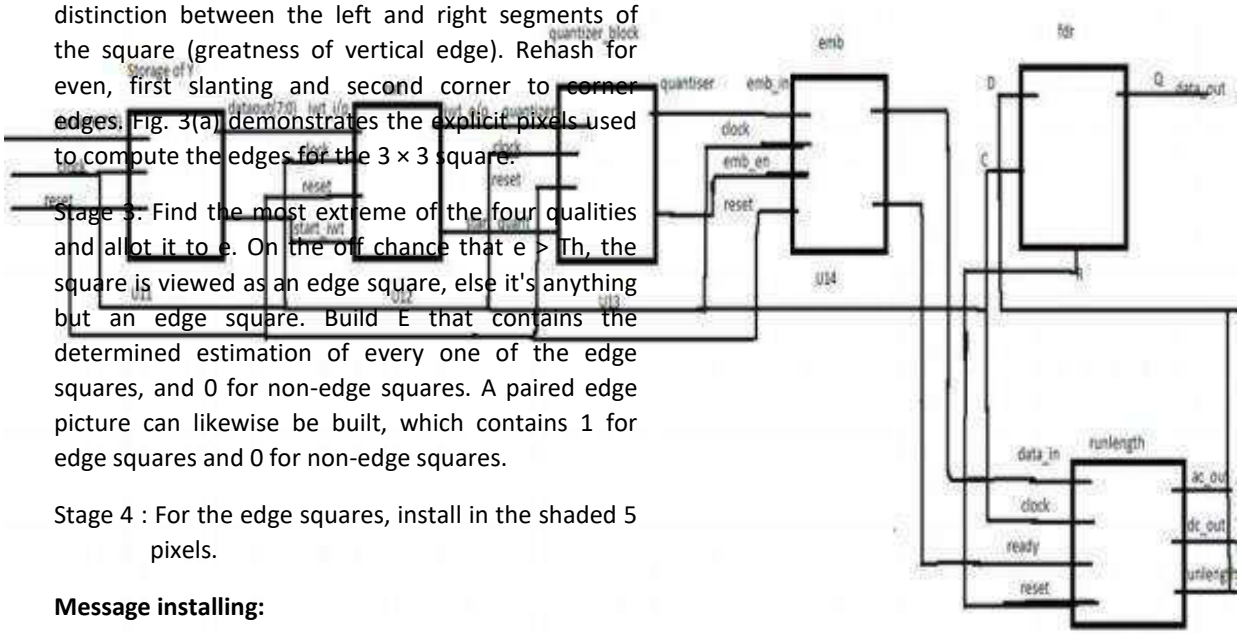


Fig. 1. Block Diagram of message Embedding For the given threshold value, if (no. of edge pixels=(4 ∗ Message Length)/3)) then the discovered area is enough to embed the secret message.

The embedding system is performed on the perceived edge regions using the proposed XOR coding. This procedure sections the document table into social events of four pixels and encodes three message bits into the pixels of each get-together. The XOR action ensures that the riddle message is masked into the cover with slightest number of pixel changes. In this way, the three puzzle bits m1, m2, and m3 are embedded in the four LSBs p1, p2, p3, and p4 (one piece for each edge pixel) as demonstrated by the going with methodology.

1. Play out the accompanying three XOR

activities k1 = p1 ⊕ p2

k2 = p3 ⊕ p4

k3 = p1 ⊕ p3

2. To embed the three puzzle bits m1, m2, and m3, the three decided bits k1, k2 and k3 are differentiated and the secret message bits m1, m2, and m3. The delayed consequence of this examination, which can take one of eight possible results, makes sense of which of the four bits p1, p2, p3, and p4 must be modified. We will imply the new four bits of the stegno picture as q1, q2, q3, and q4. The table demonstrates that implanting 3 message bits1. Play out the going with three XOR activities k1 = p1 ⊕ p2

k2 = p3 ⊕ p4

k3 = p1 ⊕ p3.

To embed the three riddle bits m1, m2, and m3, the three decided bits k1, k2 and k3 are differentiated and the puzzle message bits m1, m2, and m3. The result of this relationship, which can take one of eight possible results, makes sense of which of the four bits p1, p2, p3, and p4 must be modified. We will insinuate the new four bits of the stegno picture as q1, q2, q3, and q4. The table exhibits that introducing 3 message bits into 4 cover bits will cause a normal alteration of 1.25 bits.

3. The limit esteem ought to likewise be implanted, as it is required by the extraction procedure. In this calculation, the edge esteem is installed into the last pixel of the cover picture.

Message extraction:

The extraction procedure is simpler and quicker than the inserting procedure. Fig. 6 speaks to the stream graph of the extraction procedure. It begins by recovering the limit esteem. The edge squares of the stegno picture are then recognized utilizing the recovered edge, which will restore a similar edge picture as the one got utilizing the cover picture. This will be trailed by isolating the LSBs of the edge pixels into gatherings of four. At last, for every one of the four stegno edge bits q1, q2, q3, and q4 the XOR activities recorded beneath are utilized to recover three message bits m1, m2, and m3

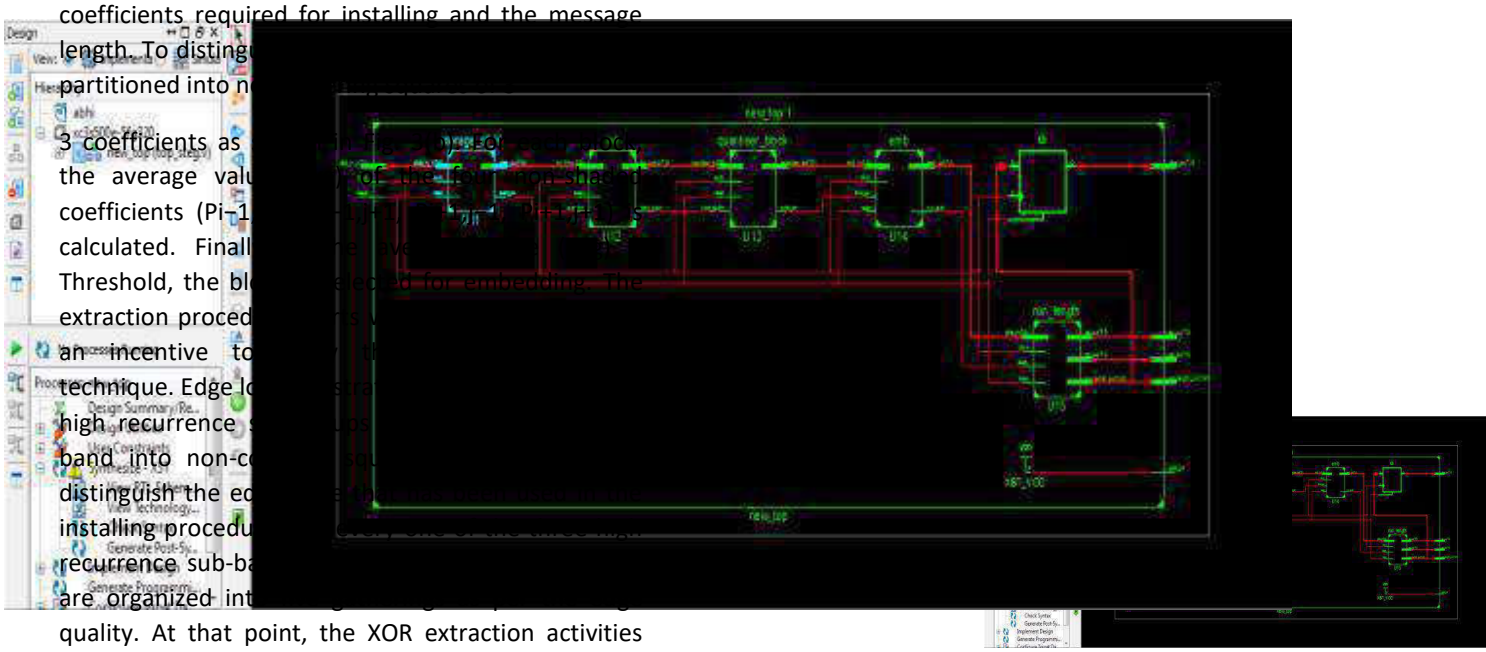
m1 = q1 ⊕ q2

m2 = q3 ⊕ q4

m3 = q1 ⊕ q3

While thinking about any mix of m1, m2, m3, p1, p2, p3, and p4 to confirm the inserting and extraction forms, one can find that the extraction procedure really re-establishes the first message. Inserting and extraction of n bits per coefficient of the Integer Wavelet Transform Domain. The proposed Integer Wavelet Transform (IWT) based inserting process begins by changing over the cover picture to the recurrence area utilizing IWT. Since the HVS is delicate to little alteration into the lower recurrence band contrasted with the higher recurrence, the mystery information is inserted just in the high recurrence sub-groups of the IWT area to accomplish a high power and intangibility results. At the end of the day, information stowing away is completed in the three sub-groups HH, LH and HL (the LL sub-band is avoided). Like the spatial space implanting, the XOR task is likewise used here.The installing procedure starts with HH sub-band and distinguish the edge coefficients to begin implanting with the most grounded edges to the weakest edges. In the event that the HH sub-band isn't sufficient to implant the mystery message, at that point the procedure moves to the LH sub-band, and after that to the HL sub-band. The usage of the installing procedure is clarified in the accompanying advances.

Read the cover image and the secret message and applied the First-Level of IWT on the cover image to decompose the cover image into four sub-bands (LL, HL, LH and HH).Identified edge areas in the high recurrence sub-groups (LL, HL, LH and HH). To build the installing payload of the wavelet change strategy, n LSB from each edge coefficients are used in inserting. A higher limit esteem (Th) is instated, which is then diminished dependent on the quantity of coefficients required for installing and the message length. To distingu



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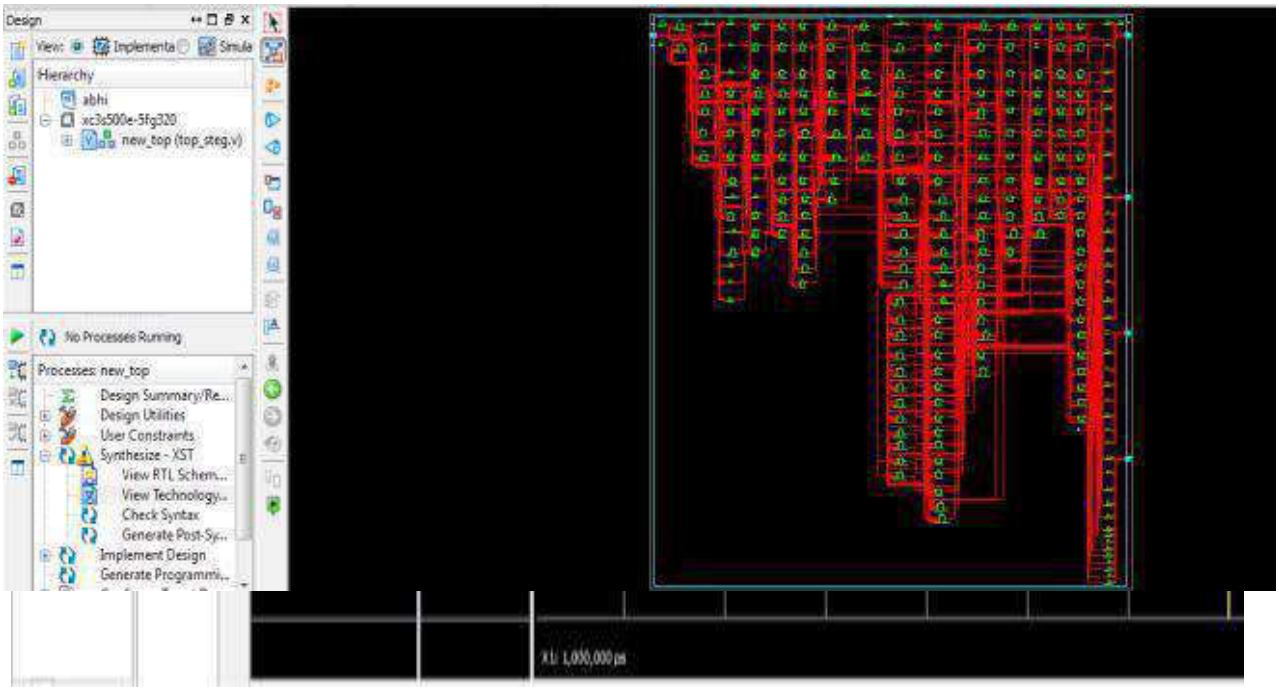
IV. EXPERIMENTAL RESULTS:

The Design is written in Verilog HDL Modules and has been successfully simulated and verified using modelsim and synthesized using Xilinx ISE 13.2.



Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	79	4656	1%
Number of Slice Flip Flops	114	9312	1%
Number of 4 input LUTs	80	9312	0%
Number of bonded IOBs	49	232	21%
Number of GCLKs	1	24	4%

```
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clock'
  Total number of paths / destination ports: 38 / 38
-------------------------------------------------------------------------
Offset:              4.063ns (Levels of Logic = 1)
  Source:            U15/run_length_out_7 (FF)
  Destination:       run_length_out<7> (PAD)
  Source Clock:      Clock rising

  Data Path: U15/run_length_out_7 to run_length_out<7>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             2    0.514   0.380  U15/run_length_out_7 (U15/run_length_out_7)
     OBUF:I->O                 3.169          run_length_out_7_OBUF (run_length_out<7>)
    ----------------------------------------
    Total                      4.063ns (3.683ns logic, 0.380ns route)
                               (90.6% logic, 9.4% route)

=========================================================================
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CONCLUSION:

XOR installing process conceals two data signals (sound and ECG) into cover picture. The proposed picture steganography points in building up a stegno procedure, indistinct and with high payload limit. At first the scaled tested are convolved utilizing XOR coding to decrease size of data and to build security of the procedure. The primary commitment of the proposed strategy is presenting new and effective edge recognition calculation utilizing non-covering obstructs that assesses a similar edge forces for the cover and stegno pictures is resolved in this venture and has accomplished preferred intangibility results over other prominent steganography strategies.

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SELF-DRIVING CARS:THE NEXT GENERATION

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Abstract—**In the present scenario, the vehicles are focused to be automated to give human driver relaxed driving. In the field of automobile various aspects have been considered which makes a vehicle automated. Google, the biggest network has started working on the self-driving cars since 2010 and still developing new changes to give a whole new level to the automated vehicles. Google driverless cars are designed to operate safely and autonomously without requiring human intervention. In this paper we have focused on an automated car, they won't have a steering wheel, accelerator or a brake pedal because they don't need them, software and sensors do all the work. It takes you where you want to go at the push of a button. It exists automated driving during the heavy traffic jam, hence relaxing driver from continuously pushing brake, accelerator or clutch. The idea described in this paper has been taken from the Google car, defining the one aspect here under consideration is making the destination dynamic. This paper explores the impact that has been working towards the goal of vehicles that can shoulder the entire burden of driving. This Technology step towards improving road safety and transforming mobility for millions of people.**

Keywords: Autonomous, Self Driving, Sensors.

I. INTRODUCTION

Consumers all around the whole world are enthusiastic about the advent of autonomous cars for public. An autonomous car can operate without human control and does not require any human intervention. Campbell et al. stated that modern autonomous vehicles can sense their local environment, classify different kinds of objects that they detect, can interpret sensory information to identify appropriate navigation paths whilst obeying transportation rules. Considerable advancements have been made in giving an appropriate response to unanticipated circumstances where either a backlash can occur in the vehicular systems or some medium in the external environment may not behave as predicted by internal prototypes. To carry out successful autonomous navigation in such situations, combining a variety of technologies from different disciplines that span computer science, mechanical engineering, electronics engineering, electrical engineering, and control engineering, etc.

AUTONOMOUS vehicles usually refer to self-driving vehicles that can fulfill main transportation capabilities of a traditional vehicle. Such vehicles are viewed as a promising answer to traffic congestion, accident and pollution problems that disturb people around the world; because the movements of vehicles could be controlled in a smoother, safer and economical manner, if the vehicles are built "intelligent" enough.

To reach this goal, some prototypes of autonomous vehicles had been designed and tested during the last few decades. For example, Google and Tesla had demonstrated their autonomous cars can run on road recently. More companies claimed that they will have their own autonomous vehicles running on road within the next 5 years. An important question naturally arises as: "*how could we prove an autonomous vehicle is capable to drive in live traffic?*" The accidents that were made by not fully tested Honda cars had demonstrated the disastrous consequences of improper testing. So, unless their reliability and safety can be

thoroughly tested and ensured, autonomous vehicles cannot be put into market.

To find an answer, the Defense Advanced Research Projects Agency (DARPA) had sponsored a series of competitions for autonomous vehicles. The first two "Grand Challenges" had been held in 2004 and 2005 to check whether autonomous vehicles could travel long distances in off-road terrain. The third "Grand Challenges" had been held in 2007 to foster innovation in autonomous driving in busy urban environments . These tests fired researchers with keenness for autonomous driving. Similar autonomous vehicle competitions had also been held in Europe and China. National Science Foundation of China had spent over 30 million dollars to support seven "Intelligent Vehicle Future Challenges" that had been held in different cities of China, through 2009 to 2015. Several prototype vehicles had successfully passed these competition tests. Notice that competition tests cannot replace real road tests, several countries allowed autonomous vehicles to be tested on ordinary roads since 2010s. This had triggered a debate on whether it is safe to allow under-testing autonomous vehicles runs into live traffic.

It wasn't that long ago when road maps may become extremely valuable as Antiques. A couple of months ago a Google CEO Larry Page drives in a car around to pick up a friend of his. This car has one special feature; there is no driver at all. The car drove Larry's friend twenty miles to Google without a driver. We will dream this about decades. Already we have seen a host of advancements to make safer drive like Lane assists, parking assists or even collision prevention assistance. With more advance technologies that finds greater emergence, future roadways and become a mesh network along autonomous vehicles. They share information with each other and large network speed, breaking and other variables and move in a coordinated formation. Here we are talking about Google driverless car. A world with increasingly connected climate, cars take over, where humans are out of equation.

II. LITERATURE

After the development of the autopilot airplanes, selfdriven sailboats and ships; the deceptively modest dream that has rarely ventured beyond the pages of science fiction since our grandparent's youth is the self-driving car. By the passage of time, much work has been carried out in the area to make cars self-driven but due to technological advancement in the roads and the increasing population has made difficult for this dream to becoming true. In the pre-computer days of the 1930s, the driverless cars were only the science fiction things. But the development of the digital computer made possible to dream of self-driven vehicles outside the fiction. By the 1960s the self-driven cars have been dreamed to navigate on ordinary streets on their own. German pioneer Ernst Dickmanns, in the 1980s, got a Mercedes van to drive hundreds of miles autonomously on highways, a tremendous feat especially with the computing power of the time. In the mid-2000s, the Defense Advanced Research Projects Agency (DARPA) sorted out the Grand Challenges where groups assembled to contend with selfdriving vehicles. In 2009, Google began the self-driving car venture, including colleagues who had effectively devoted years to the innovation. By 2012 the Google car hits the road for testing. By the passing years, the car is developed and equipped with multiple sensors, radars, lasers, Global Positioning System (GPS), it uses heavily detailed maps, and many other things to safely drive and navigate itself with no human interaction. The car can not only drive itself but it can be parked on its own, it can go on freeways, Cameras are used to find and detect objects that are then processed by the computer within the car. In May 2014, Google presented a new concept for their driverless car that had neither a steering wheel nor

pedals and unveiled a fully functioning prototype in December of that year that they planned to test in 2015. In summer 2015, Google launched and tested some different features where each prototypes speed is capped at a neighborhood-friendly 25mph, and during this phase safety drivers aboard with a removable steering wheel, accelerator pedal, and brake pedal that allow them to take over driving if needed. After many successful roads testing of Google car has made to believe in some years roads will be safely occupied with self-driven cars. The authors in have developed unmanned vehicle prototypes in which they have worked on the obstacle avoidance and path planning. This paper presents a concept of Google car is focused, the Google car has to reach the static destination automatically we have made the destination dynamic here was to tackle heavy traffic congestion and allow the vehicle to move automatically during that traffic congestion.

II. AUTONOMOUS VEHIVCLE

An Autonomous vehicle (sometimes referred as automated car or self driving car) is a robotic vehicle that is designed to fulfilling the transportation capabilities without a human operator. Qualifying to it as fully autonomous, vehicle must be able to navigate without human input to the destination that is predetermined over un adapted roads and is capable to sense the environment. Audi, BMW, Google, Ford are some of the companies developing and testing these vehicles. Technologies making a system fully autonomous are Anti Lock Brakes (ABS), Electronic Stability Control (ESC), Cruise control, Lane Departure Warning System, Self Parking, Sensors, and Automated Guided Vehicle Systems.

GOOGLE DRIVERLESS CAR EXPLAINED

Only with occasional human intervention, Google's fleet of robotic Toyota Cruises has logged more than 190,000 miles (approx. about 300,000 Km), driving in busy highways, in city traffic and mountainous roads. In a near future their driverless car technology could change the transportation. Director of The Stanford Artificial Intelligence Laboratory, Sebastian Thrun guides the project of Google Driverless Car's with elucidations:

- Steering can be done by itself, while looking out for obstacles.
- For corrections of speed limit, it can accelerate by itself.
- On any traffic condition it can GO or STOP by itself.

Figure 1: Google Car

UNDER THE BONET

It integrates three constituents:
Google Maps
Hardware Sensors
Artificial Intelligence

GOOGLE MAPS

A self - driving computerized car has unveiled by Google; which has no wheel for steering, brake or accelerator, just has buttons to start, stop, pullover and a computer screen to show the route. Through GPS and Google maps to navigate. A Google map provides the car with information of road and interacts with GPS to act like a database.

HARDWARE SENSORS

Real time and dynamic Environmental conditions (properties) attained by the car. To need real time results, sensors are attempted to create fully

observable environment. These hardware sensors are LIDAR, VEDIO CAMERA, POSITION ESTIMATOR, DISTANCE SENSOR, AERIAL and COMPUTER

LIDAR

(Light Detection And Ranging also LIDAR) is an optical remote sensing technology which is used to measure the distance of target with illumination to light in the form of pulsed laser. It is a laser range finder also known as "heart of system", mounted on the top of the spoiler. A detailed #D map of the environment is generated by the device VELODYNE 64 beam Laser (for autonomous ground vehicles and marine vessels, a sensor named HDL 64E LIDAR is designed for obstacle detection and navigation. Its scanning distance is of 60 meters (~ 197 feet). For 3D mobile data collection and mapping application this sensor becomes ideal for most demanding perceptions due to its durability, very high data rates and 360 degree field of view. One piece design patented the HDL 64E's uses 64 mounted lasers that are fixed and each of it is mounted to a specific vertical angle mechanically with the entire spinning unit, to measure the environment surroundings. **Reliability, field of view and point cloud** density is dramatically increased by using this approach.) High resolution maps of the world are combined by the car laser measurement to produce different types of data models that allows it to drive itself, avoiding obstacles and respecting traffic laws. A LIDAR instrument consists of a Laser, Scanner and a specialized GPS receiver, principally.

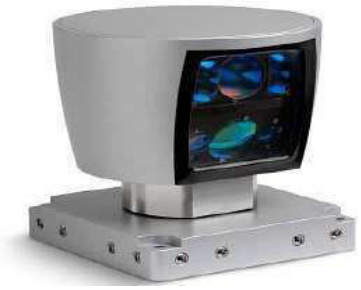

Figure 2: HDL-64E Lidar

HOW IS LIDAR DATA COLLECTED?

A beam of light is reflected by the surface when it encounter with the Laser that is pointed at the target area. To measure the range, this reflected light is recorded by a sensor. An orientation data that is generated from integrated GPS and Inertial Measurement Unit System scan angles and calibration with position. The result obtained is a dense, and "point cloud" (A detail rich group of elevation points consists of 3D spatial coordinates i.e. Latitude, Longitude and Height).

VIDEO CAMERA

A sensor that is positioned near to the Rear-view mirror that detects the upcoming traffic light. It performs the same function as the mildly interested human motorist performs. It reads the read signs and keeps an eye out for cyclists, other motorists and for pedestrians.

POSITION ESTIMATOR

An ultrasonic sensor also known as(Wheel Encoder) mounted on the rear wheels of vehicle, determines the location and keep track of its movements .By using this information it automatically update the position of vehicle on Google Map.

DISTANCE SENSOR (RADAR)

Other sensors which include: four radars, mounted on both front and rear bumpers are also carried by this autonomous vehicle that allows the car to "see" far enough to detect nearly or upcoming cars or obstacles and deal with fast traffic on freeways.

AERIAL

A highly accurate positioning data is demanded by a self – navigating car. Readings from the car's onboard instruments (i.e. Altimeters, Tachometers and Gyroscopes) are combined with information

received from GPS satellites to make sure the car knows exactly where it is.

COMPUTER

Car's central computer holds all the information that is fed from various sensors so to analyze the data, steering and acceleration and brakes are adjusted accordingly. Not only traffic laws, but also the unspoken assumption of road users is needed to understand by the computer.

ARTIFICIAL INTELLIGENCE

Artificial Intelligence provides the autonomous car with real time decisions. Data obtained from the Hardware Sensors and Google Maps are sent to A.I for determining the acceleration i.e. how fast it is; when to slow down/stop and to steer the wheel. The main goal of A.I is to drive the passenger safely and legally to his destination.

WORKING OF GOOGLE CAR

 Destination is set by "The Driver" and software of car calculates a route and starts on its way.
 LIDAR, a rotating, roof mounted sensor monitors and scans a range of 60 - meters around the surroundings of car and creates rudimentary detailed 3-D map of immediate area
 An ultrasonic sensor mounted on left rear wheel monitors movements to detect position of the car relative to 3-D map.
 DISTANCE SENSORS mounted on front and rear bumpers calculate distances to obstacles.
 All the sensors are connected to Artificial intelligence software in the car and has input from Google VIDEO CAMERAS and street view.
 Artificial Intelligence stimulates the real time decisions and human perceptions o control actions such as acceleration, steering and brakes.
 The surface installed in the car consults with Google Maps for advance notification of things like landmarks, traffic signals and lights.
 To take control of the vehicle by human is also allowed by override function.

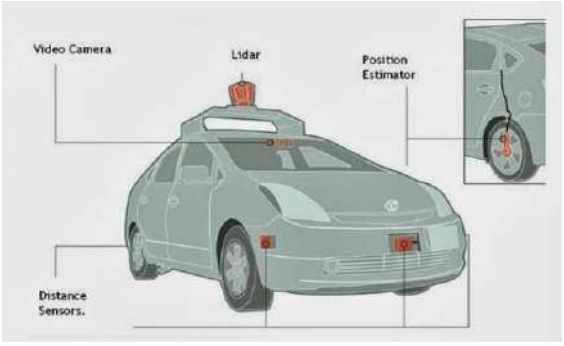

Figure 3: How it Works

AN END TO TRAFFIC JAMS FOREVER

Autonomous cars will be able to "talk" to each other and navigate safely by knowing where they are, by using RADAR, CAMERAS, GPS, SENSORS and Wireless Technology in relation to other vehicles and by means with connectivity they can communicate with obstacle like traffic signals. As a result traffic flow becomes smoother; an end to traffic jams and greater safety would be achieved by illuminating the frustration and dangerous driving that's often triggered by sitting in heavy congestion for ages. When it comes to sustainability, the self-driving car also holds great promise by figuring out the most – direct, least traffic jammed route by driving without quickly accelerating or breaking too hard, all which leads to saving on fuel consumption.

Figure 4: Going Driverless on road

TRIALS AND TRIBULATIONS

We seldom think about , what needs to be happen behind the scenes to bring this potentially life- changing technology to the market , while it's easy to get lost into it. Ahead of the Law is the major problem to this technology, as Lawmakers have a huge impact on innovation. In the US most federal and state automobile Laws assume a human operator. Before the technology can be commercialized these need to be repealed. To legalize the operation of autonomous cars on the roads, Nevada became the first state in 2012. An attempt to gain state support for similar changes in Law, Lobbyists from Google have been travelling around other states and targeting Insurance companies as well. The technology also poses serious puzzle to Insurance in terms of Regulatory issues and Liability.

CONCLUSION

This paper explained about the Google Driverless car revolution which aims at the development of autonomous vehicles for easy transportation without a driver. For the economy, society and individual business this autonomous technology has brought many broad implications. Cars that drive themselves will improve read safety, fuel efficiency, increase productivity and accessibility; the driverless car technology helps to minimize loss of control by improving vehicle's stability as these are designed to minimize accidents by addressing one of the main causes of collisions: Driving error, distraction and drowsiness. But still these cars have a lot of hurdles to go through before they became everyday technology.

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Wireless Health Monitoring System using ZIGBEE

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Abstract— Remote health care monitoring system (RHCMS) has drawn considerable attentions for the last decade. As the aging population is increasing and at the same time the health care cost is skyrocketing there has been a need to monitor a patient from a remote location. Moreover, many people of the World are out of the reach of existing health- care systems. To solve these problems many research and commercial versions of RHCMS have been proposed and implemented till now. In these systems the performance was the main issue in order to accurately measure, record, and analyze patients' data. With the ascent of wireless network RHCMS can be widely deployed to monitor the health condition of a patient inside and outside of the hospitals. In this work we present a ZigBee based wireless healthcare monitoring system that can provide real time online information about the health condition of a patient. The proposed system is able to send alarming messages to the healthcare professional about the patient's critical condition. In addition the proposed system can send re- ports to a patient monitoring system, which can be used by the healthcare professionals to make necessary medical advices from anywhere of the World at any time.

Keywords**:** *ARM processor, ZIGBEE module, heartbeat sensor, temperature sensor, LED's, and LCD.*

Introduction

Over the recent years remote health care monitoring systems for the elderly people have drawn considerable attentions. According to UNFPA, the global population is no longer young for the first time in the history [1]. Population ageing is affecting the entire world and is happening in all regions. But, it is progressing at a faster rate in the developing countries. Seven out of the fifteen countries in the developing world have more than 10 million old people. By the year 2050 another fifteen developing countries are expected to have 10 million old people.

It is worthwhile to mention here that the average life expectancy in the United States was 47.3 years in 1900. But, it has increased to 68.2 years and 77.3 years in 1950 and

2002 respectively [2, 3]. People are living longer because of better nutrition, sanitation, medical advances, education, economic well-being, and health care. Population ageing poses challenges to individuals, families, and societies.

By adopting proper policies societies should be prepared for an ageing world. Overall, the older people should not be considered as a burden for the society. Their wisdom, energy, and experience are added advantages for us to take care of the challenges of the 21st century. In order to keep the ageing population healthy we have to deal with some challenges. The major challenge for us is to keep them healthy with our limited resources.

II. RELATED WORK:

2.1.ARM PROCESSOR:

The ARM7TDMI-S is a general purpose 32-bit micro- processor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related

2.2.BLOCK DIAGRUM:

decode mechanism are much simpler than those of micro programmed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core. Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously.

Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory. The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue. The key idea behind Thumb is that of a super reduced instruction set.

2.3.ZIGBEE MODULE:

Zig Bee is a low-cost, low-power, wireless mesh networking proprietary standard. The low cost allows the technology to be widely deployed in wireless control and monitoring applications, the low power-usage allows longer life with smaller batteries, and the

Transmitter Section:

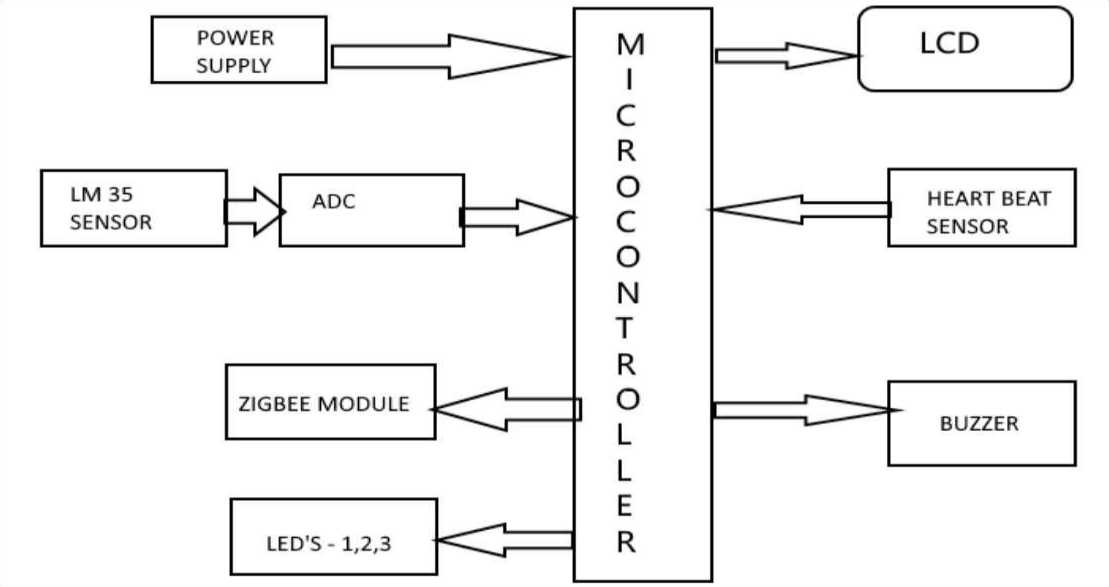

Figure-1: Block diagram of Patient Section

Receiver Section:

Figure-2: Block diagram of Doctor Section

mesh networking provides high reliability and larger range. The ZigBee Alliance, the standards body that defines ZigBee, also publishes application profiles that allow multiple OEM vendors to create interoperable products.

The protocols build on recent algorithmic research (Ad- hoc On-demand Distance Vector, neuron) to automatically construct a low-speed ad-hoc network of nodes. In most large network instances, the network will be a cluster of clusters. It can also form a mesh or a single cluster. The current profiles derived from the ZigBee protocols support beacon and non-beacon enabled networks.

III. SENSORS:

3.1 TEMPERATURE SENSOR (LM35)

LM35 is a precision IC temperature sensor with its output proportional to the temperature (in oC). The sensor circuitry is sealed and therefore it is not subjected to oxidation and other processes. With LM35, temperature can be measured more accurately than with a thermistor. It also possess low self heating and does not cause more than 0.1 oC temperature rise in still air. The operating temperature range is from -55°C to 150°C. The output voltage varies by 10mV in response to every oC rise/fall in ambient temperature, i.e., its scale factor is 0.01V/ oC.

Figure-3: temperature sensor

3.2 HEARTBEAT SENSOR:

Modern heart rate monitors usually comprise two elements: a chest strap transmitter and a wrist receiver (which usually doubles as a watch) or mobile phone. In early plastic straps, water or liquid was required to get good performance. Later units have used conductive smart fabric with built-in microprocessors that analyze the EKG signal to determine heart rate. Strapless heart rate monitors now allow the user to just touch two sensors on a wristwatch display for a few seconds to view heart rate data. These are popular for comfort and ease of use, though they don't give as much detail as monitors that use a chest strap. More advanced models offer measurements of heart rate variability, activity, and breathing rate to assess parameters relating to a subject's fitness. Sensor fusion algorithms allow these monitors to detect core temperature and dehydration. Another style of heart rate monitor replaces the plastic around-the-chest strap with fabric sensors - the most common of these is a sports bra for women that include sensors in the fabric.

IV. RESULTS:

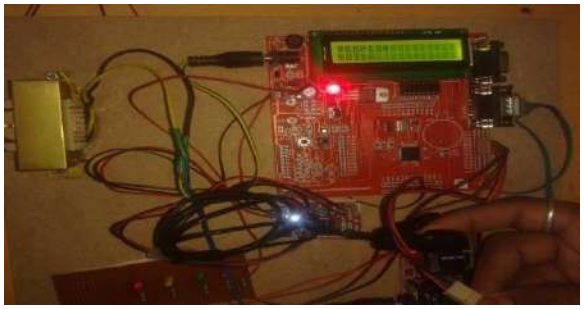

Figure-5: Sensors output values on PC

V. CONCLUSION:

With the fast development of the industrialization and urbanization process in the world and hence with the in- crease of busyness of people it has become difficult to monitor the health conditions of a patient continuously. Also with the increase in the number senior citizens and chronic diseases, the number of elderly patients who need constant assistance has increased. One key point of all critical care for elderly patient is the continuous monitoring of their vital signs. To avoid unexpected health problems and obtain higher accuracy in diagnosis of the health conditions of a patient, efficient and comprehensive data collecting, monitoring and control play an important role to improve the health care system more reliable and effective.

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Communication Technologies for Industrial Systems

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***Abstract*— In case of industrial sites located in isolated geographical areas, access to wired internet connection can be a challenge. This paper presents an evaluation of possible configurations for a remote monitoring and control of a wastewater plant. The plant does not have a public IP and the internet is acquired using a mobile connection on a router directly connected to the plant PLC. Two possible solutions are presented, using a VPN router and through an OPC tunnel.**

Keywords— data transmission, GSM communication, SCADA, remote control, VPN tunnel.

I. INTRODUCTION

In today's economic environment, every major producer of goods, like national utility companies from the water or energy sector, oil extraction and processing companies, renewable energy etc., has their production and supply chain geographically situated all over the country, continent or world. This situation shows a necessity for the companies and brings a new problem for the system integrators to solve, the communication between geographically scattered sites.

What started as a simple human to human communication between sites, using telephone lines and later, using the internet for communication between plant managers, evolved in accordance with the new technologies and standard communication protocols, to machine to machine, plant to plant communication and data and information transfer using industrial internet protocols, GSM, GPRS, satellite communication, telecontrol, radio or Wi-Fi.

The new means of communication increase the availability of plant data and allow the implementation of new applications that can reduce the involvement of the human operator, allow direct data integration in ERP or asset management applications, and, by use of mobile application or alarming modules, can raise the speed in which the plants or the dispatcher is informed regarding process operation [1].

Another usage for remote data acquisition is maintenance and data analysis of the plant. This allows remote supervisor applications to analyze information that is acquired from the target plants. The information is analyzed and decisions can be made if human intervention or predictive maintenance is needed. The remote data acquisition is a key requirement for unmanned remote plants, like distributed wind farms, water supply pumps, wastewater pumps, gas supply installations etc. In case of industrial sites located in isolated geographical areas, access to wired internet connection can be a challenge. While satellite connections are highly expensive, the most accessible solution is represented by GSM/GPRS networks. At the same time, to ensure there are no security breaches, only certain areas of a plant can be accessed remotely. The correlation between requirements from the process control engineer points of view, plant network security, service provider and implementation cost must be taken into consideration in identifying a best solution.

This paper presents a typical case of a plant that must be connected to a remote Decision Support System and evaluates possible interconnection solutions considering there is no current internet connection available. Our objectives are to research potential methods of implementing the communication component of a wastewater plant, and to present and analyze the method applied in our situation that was implemented within the project.

The rest of the paper is structured as follows: section II presents existing technologies and architectures for remote plant connection. Section III describes the plant used as case-study, existing limitations and data connection requirements. Section IV presents two possible connection solutions for accessing remote plant data without the need of a fix IP address. Section V concludes this paper.

II. AVAILABLE COMMUNICATION TECHNOLOGIES

A. Previous Related Work

Remote control is the kind most facility technology up to date, as it allows us to do things from a distance, in a short period, and with minimal effort. Combined with the acquisition of production-related information and process state, remote control can help implement the digital enterprise concept at the plant level [2]. This topic has been addressed previously in several research papers.

In [3] the authors present the remote control of a pumping station in the water supply system by using monitoring systems installed in the entire building and assisted by alarm

sensors which quickly help identifying faults. This leads to an increase in the overall efficiency of the management system.

The link between the station and the operation and maintenance center is established using radio frequency data transmission leveraged by the mobile operators. It is a web-based system, which uses a long-range GSM link and conventional internet transmission to collect data, also in real time of the pumping station systems.

In [4], by using a system made of three microcontrollers, the authors could monitor the waterwheel of a small hydroelectric power station, which is autonomous and located in isolated remote area. For automatic control, a "peak power tracking" algorithm is implemented and its output is sent every 10 seconds via GPRS/ Internet to the monitoring terminal.

Three communication modules are implemented: control, surveillance and communication by using the following protocols: TCP/IP, GPRS, SMS and ZigBee.

A remote monitoring system of a conventional wastewater treatment plant, which was previously manually operated for an energy-saving project is presented in [5]. The focus on the energy savings can be spotted in the section which controls the dissolved oxygen in the context of nitrogen removal. By using automatic controllers, the oxidation process is adjusted through controlling the air flow to the time varying treatment requirements.

A RTU (Remote Terminal Unit) is used for each plant to collect and transmit data via low-speed dedicated modem lines, radio modems in the UHF band, GPRS and/or Ethernet lines. The paper describes the first step in the project development, the setup of the plant monitoring from a management center, and, using a VPN connection, from an authorized client.

With regards to the fuel management spending, there are a lot of published technical documents, which describe experiences on remote technology [6]. At the reactor sites, interim storage facilities, reprocessing or disposal facilities, due to the heavy weight and large size of spent fuel casks, heavy duty handling facilities capable of accommodating at least a truck access are required.

To minimize human interaction remote automation is used for devices, bolt/stud tensioners, robotic manipulators, even though the cask surface is supposed to be within acceptable dose limits to the workers.

Major concerns for remote technology applications are raised especially where human operation and intervention is extremely dangerous or impossible, for example, inside radioactive enclosures [6]. To avoid dangerous situations, like human exposure, the best solution is to implement tele-operations and tele-robotics. However, due to lack of experiences or reliability, this has limited use.

These researches enable the faster adoption of cloud, wireless sensor networks or context-aware approaches at the industrial level. An example of how these technologies have been integrated into industrial applications was presented in [7].

B. Available Technologies

There are several solutions available, adapted to the particularities of each site location. Current routing devices integrate Ethernet, GSM and WiFi connections, and their performance depends mainly on the service provider, so from the applications' point of view the network type is not important. Depending on the allocated budget, the beneficiary can choose between a public or private, static or dynamic IP address. Difference between these determine the technologies that can be used.

A list of available remote connection solutions based on OPC protocol over an Ethernet transmission, according to the IP connection type is presented in Table 1. A public IP or external IP is considered a user's IP that can be directly accessed from the Internet. The opposite of this is a private IP which determines how a device can be accessed inside a network. Because the number of available public IPs is lower than the number of users, some ISPs can provide customers a private IP. Moreover, some ISPs can provide a static IP, meaning an IP that never changes, or dynamic IP, one that may change. Under these considerations, a static or dynamic IP can be either under a public network, thus being reachable, or over a private one, where they can only initiate connections to reach remote locations.

TABLE 1: REMOTE CONNECTION SOLUTIONS

IP type	***Solutions***	***Min. requirements***
Static IP over a public network (Public IP)	Direct OPC server connection	DCOM and firewall settings
	OPC tunnel	OPC server for the PLC protocol
	Remote access application	PC on site, large network bandwidth
Dynamic IP over a public network	VPN connection	Router with VPN client, remote VPN server with public IP
		Router with VPN server and dynDNS
	OPC tunnel	Router with dynDNS OPC server for the PLC protocol
	Remote access application	PC on site, large network bandwidth
Dynamic or Static IP over a private network	VPN connection	Router acting as a VPN client, VPN server with public IP
	OPC tunnel	Cloud application for OPC tunnel connection
	Commercial remote access application	PC on site large network bandwidth

III. PLANT DESCRIPTION

A. Wastewater treatment plant

The production process from the food and drinks domain result in a big quantity of wastewater generated from tanks cleaning, vegetables washing or processing. To control the

impact of these residues on the environment, strict regulations must be followed to ensure proper organic levels.

The remote plant referred in this article is an experimental 100L wastewater treatment plant. The plant is a two-phase acid/gas wastewater treatment plant designed following the principle of anaerobic digestion.

The plant has for major components, where the chemical and biological processes occur: the feed area, the acidogenic area, the methanogenic area and the gas handling area. The installation's objective is to process wastewater and pulp waste that results following normal operations in small and medium food and drinks production companies, into biogas that can be captured and used as fuel for heating or electricity generation.

The project developed a small scale cost-effective solution of a wastewater treatment plant to be used by SMEs in the food and drink sector. The technology uses a two-stage anaerobic reactor that combines wastewater with nutrients, under strict pH and temperature control, to ensure proper levels of COD (chemical oxygen demand), Natrium, Phosphor and TSS (total suspended solids) or the production residues. This process results in biogas production that can be reused in the plant energy consumption.

B. Data transmission

The wastewater plant was designed independently of a food processing facility and tests were performed at different locations, in two types of plants (juices and wine) for evaluating its efficiency. Because of this, its control system was completely independent of the local network and of the control system from the installation facility.

The control application allows the monitoring of main process parameters (temperature, pH, tank level, input and output flow) and different levels of control from individual actuator action (pumps or heaters), to starting or stopping individual processes and even fully automatic control.

With the main purpose of minimizing operation costs, the implemented control logic was designed for continuous operation under automatic control based on fuzzy rules. Because of this, wastewater plant monitoring and control can only be done through a local HMI, without continuous operator supervision. The connection to a remote decision support system enables proper evaluation of plant state and performance. Fig. 1 shows the plant's data transmission diagram. Process parameters are collected by a PLC and are sent to a remote SCADA application through a GSM mobile connection.

C. Decision Support System

We designed the DSS as a modular and scalable system that can connect simultaneously to several plants for both concurrent data acquisition (in case of SCADA monitoring, alarm management and FLC trend analysis applications) and individual analysis and optimization.

The focus of the system is on increasing efficiency in data collecting, but the chosen solution also provides the possibility of remote commissioning for fast engineering technical support.

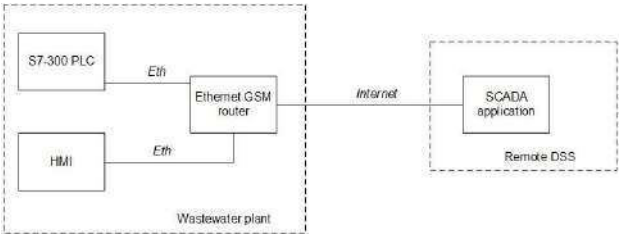

Fig. 1. Data transmission between site components

IV. Remote Communication Setup

We identified two possible solutions for the remote connection: using an OpenVPN configuration, or through an OPC tunnel integrated in a cloud application.

A. Communication using OpenVPN

We evaluated the integration of the local Siemens S7-300 PLC to the DSS through a secure VPN connection. The interconnection diagram is illustrated in Fig. 2.

To set up the VPN connection we installed a Spectre v3 router from B+B SmartWorks and configured it as a VPN client. A VPN server was installed on SIS's remote site using OpenVPN. By installing specific certificates generated for this application, we can connect many VPN clients to the server using a standard internet connection, and not necessary a fixed external IP. This increases the flexibility and minimizes the installation requirements for a possible beneficiary.

OpenVPN allows to create a secure connection over the Internet using client-server model of communication. OpenVPN tunnel configuration was created between the following equipment:

- ASUS RT-AC56U router – the server. WAN connection is residential type subscription (public and dynamic IP – a DDNS free service provided by ASUS is used to return the IP address to client at any given time).
- B+B SmartWorx powered by Advantech Spectre V3 LTE router – the client. WAN connection is postpaid mobile type subscription (IP address is not public).

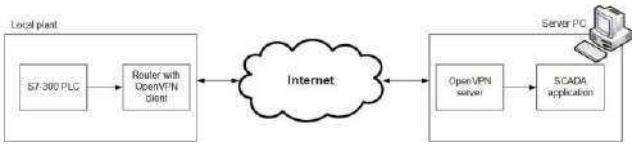

Fig. 2. Remote data acquisition and control using OpenVPN

The connection of a new plant to the DSS system implies only the reconfiguration of the devices IP, the configuration of

the router to be a new VPN client, and the configuration of the mobile network according to existing operators in the plant area. Each PLC, HMI and router for all interconnected plants will be accessible as network resources of the VPN server from any of the supervisory stations in the DSS.

B. OPC Tunneling

The remote data acquisition can also be accomplished using specialized software tools from Skkynet and Cogent. These tools allow the data acquisition form the plant under strict security regulations and don't require any changes in the local network of the plant. Another benefit of this approach is that the network traffic is limited only to process data, increasing data collection efficiency at the DSS level and reducing communication costs for the beneficiary.

For the remote data acquisition using this configuration, the following are needed:

- Data is sent from the PLC using TCP or Modbus TCP protocol (PLC acts as Modbus slave);
- Data is received by an ETK-enabled router. We configured a Spectre router with the ETK driver;
- Data is sent through Skkyhub to a Cogent DataHub application that acts as a Modbus TCP master;
- Cogent Data Hub makes the data available through OPC to be included in the remote SCADA application.

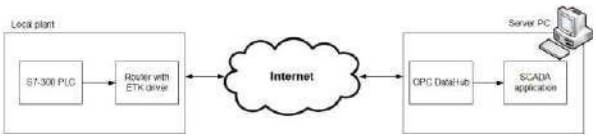

Fig. 3. Remote data acquisition and control using OPC tunneling

The solution identified for the data acquisition can be easily applied to our control system, as it does not require any installation of software products on a PC, but some minor additional configuration will be needed in the control strategy to make the data available through Modbus TCP.

C. Implementation

Testing of the VPN option was done using an ASUS router. The router was configured as a VPN server and the connection certificates were generated. This router's information was then entered in the plant router configuration (Fig. 4).

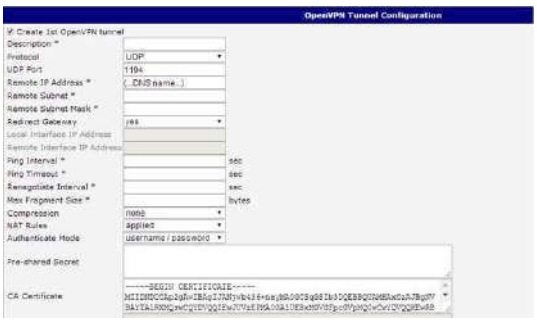

Fig. 4. VPN client router configuration example

For the implementation of the OPC tunnel we used Cogent DataHub [8]. It can connect to another Datahub, installed in another network, by using his domain name or his IP address and port. The connection information was configured in the client application (Fig. 5).

The server part of the tunnel must have the correct port available for listening and opened for connections. The Datahub is using OPC DA for data transmission between ends of the tunnel. The results for an initial set of data acquisition in an OPC client application is illustrated in Fig. 6.

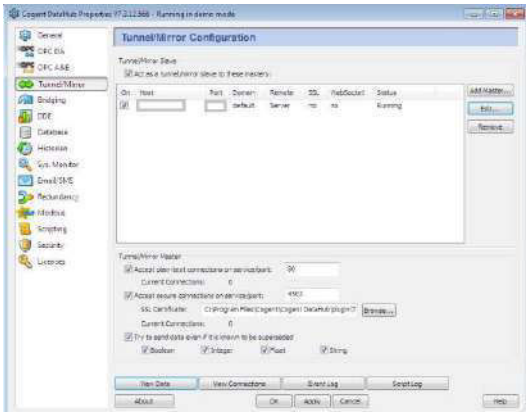

Fig. 5. OPC tunnel configuration example

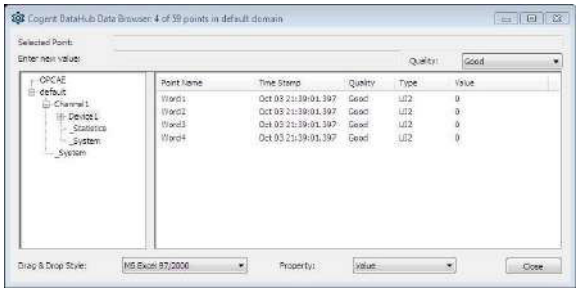

Fig. 6. Data aquisition

V. CONCLUSIONS

Remote plant monitoring and control becomes more accessible with the latest technologies that provide reduced latency even for mobile communications. To benefit most from these advances, reduced cost and secure solutions can be implemented without the acquisition of a public IP from the services providers. This paper presented and tested two such configurations for a typical PLC to a remote decision support system connection. Results showed that such architectures enable greater accessibility and improved plant operations.

Future work will include performance evaluation between these two options and the implementation of algorithms for wastewater plant operation optimization.

ACKNOWLEDGMENT

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DESIGN OF BUS TRACKING AND FUEL MONITORING SYSTEM

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ABSTRACT

In today's world, actual record of fuel filled and fuel consumption in vehicles is not maintained. It results in a financial loss. To avoid this we are implementing a microcontroller based fuel monitoring and vehicle tracking system. In this paper, the implementation of embedded control system based on the microcontroller is presented. The embedded control system can achieve many tasks of the effective fleet management, such as fuel monitoring, vehicle tracking. Using GPS vehicle tracking technology Fuel monitoring have been the major problem that most of bus companies looking to solve. This paper developed a bus tracking and monitoring the fuel and speed system to provide a facility for the management requirements by the administrator using GPS and GSM Technology.

Keywords: microcontroller, GPS, GSM, fuel level indicator.

II. INTRODUCTION

The challenges of successful fuel monitoring involve efficient and specific design, and a commitment to implementation of the monitoring project, from data collection to reporting and using results. Tracking is the use of GPS technology to identify, locate and maintain contact reports with one or more fleet vehicles. Implementing real-time vehicle tracking as part of a commercial company's mobile resource management policy is essential for comprehensive operational control driver security and fuel savings. Rising fuel costs constantly challenge fleet operators to maintain movement of vehicles and monitor driver behavior to avoid delaying traffic conditions by either, combining deliveries, reconfiguring routes or rescheduling timetables. This aims to maximize the number of deliveries while minimizing time and distance Fuel monitoring system help the administrator to know the exact amount of fuel content of the bus, so fuel theft could be avoided and administrator could maintain the fuel more efficiently. In addition to that alcohol breath of the driver to sense whether he has drunken or not.

Vehicle tracking system

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The design and development of a vehicle tracking and fuel monitoring system especially useful for mining in real-time has been reported in this paper. The system principally monitors vehicle moving and tracking such as position, and speed and subsequently identifies alcohol detection. A lot of vehicle theft occur and accident due to over speed, alcohol drunken by driver .GPS is increasingly being used in vehicle tracking and monitoring services. To resolve the problems like avoid speed and collision, traffic jams ARM processor based vehicle monitoring is implemented as well providing information for the vehicle owner. The system has been designed for ARM processor vehicle tracking and monitoring will provide effective and real time vehicle location using GPS and GSM. A GPS based vehicle tracking will inform where you vehicle is and where it has been and how long it has been. The system uses geographic positions and time information from the global Positioning Satellites. The system has on board which resides in the vehicle to be tracked and a Base Station that monitor data from the various vehicles.

BLOCK DIAGRAM

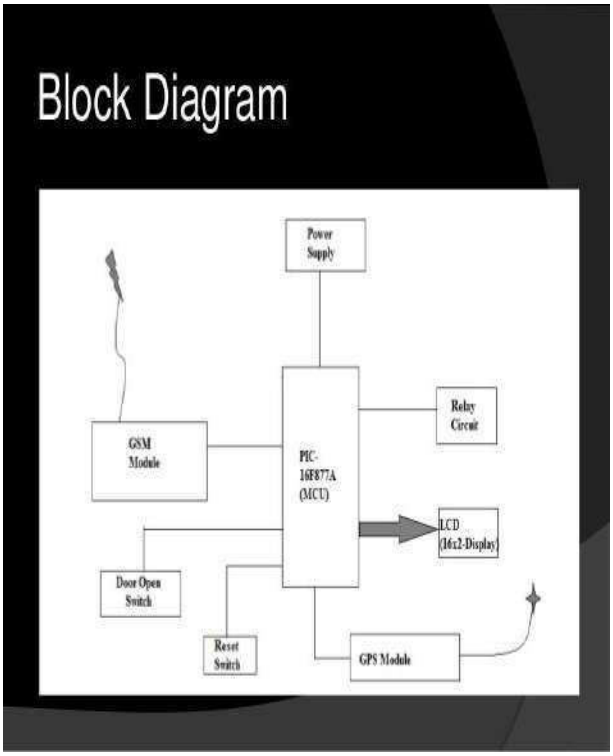


Fig . System block diagram System Overview

Power Supply:

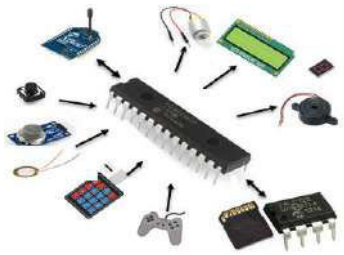
This section is meant for supplying Power to all the sections mentioned above. It basically consists of a Transformer to step down the 230V ac to 9V ac followed by diodes. Here diodes are used to rectify the ac to dc. After rectification the surface level of nearly any fluid, including water, saltwater, and oils.

IV. CONCLUSION

This paper offers a smart design of tracking and monitoring and fuel monitoring system which helps the bus companies to provide high quality of service. This design can provide the location of the busses etc. of the service with an error less than 10m in the case of slow speed and clear environment and the system give the accurate arrival time of the bus and provide the location of the bus in Google map for both user and administrator. This system reduces the waiting time of remote users for bus and provides bus tracking at any location, management and fuel monitoring obtained rippled dc is filtered using a capacitor Filter. A positive voltage regulator is used to regulate the obtained dc voltage.

Microcontroller:

This section forms the control unit of the whole project. This section basically consists of a Microcontroller with its associated circuitry like Crystal with capacitors, Reset circuitry, Pull up resistors (if needed) and so on. The Microcontroller forms the heart of the project because it controls the devices being interfaced and communicates with the devices according to the program being written.



LCD Display:

This section is basically meant to show up the status of the project. This project makes use of Liquid Crystal Display to display / prompt for necessary information.

GPS modem:

A GPS modem is used to get the signals and receive the signals from the satellites. In this project, GPS modem get the signals from the satellites and those are given to the microcontroller. The signals may be in the form of the coordinates; these are represented in form of the latitudes, longitudes and altitudes.

GSM modem Section:

This section consists of a GSM modem. The modem will communicate with microcontroller using serial communication. The modem is interfaced to microcontroller using MAX 232, a serial driver. The Global System for Mobile Communications is a TDMA based digital wireless network technology that is used for communication between the cellular devices. GSM phones make use of a SIM card to identify the user's account.

Fuel level indicator:

The sensor used for measurement of fluid levels is called a level sensor. The sensing probe element consists of a special wire cable which is capable of accurately sensing.

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An Energy-Efficient Cooperative Spectrum Sensing for Cognitive Radio: A Review

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Abstract - Cognitive radio (CR) is a promising solution for improving spectral utilization. Those bands of frequencies which are allocated to primary users (PU) or licensed users, can be used by secondary users (SU) or cognitive users, when PU are not present. Hence, spectrum sensing is necessary to identify the available spectrum and to prevent harmful interference with licensed users. Cooperative spectrum sensing (CSS) is used commonly because spectrum sensing of individual nodes cannot achieve high detection accuracy. The drawback of CSS scheme is that there exists a tradeoff between energy consumption and sensing performance. A more accurate sensing procedure requires minimizing energy consumption without degrading detection performance. In this paper, a survey of various works which aims to maximize the energy efficiency without degrading sensing performance is done.

Keywords – primary users; secondary users; cooperative spectrum sensing; energy efficiency; detection performance.

INTRODUCTION

Spectrum resources are required for the purpose of communication. The frequency spectrum has been divided into different parts and each part is assigned for specific use. The electromagnetic radio spectrum is a natural resource, the use of which by transmitters and receivers is licensed by governments [1]. The following observations can be made about the spectrum:-

- Some frequency bands in the spectrum are sparsely occupied.
- Some other frequency bands are partially used
- The remaining frequency bands are heavily occupied.

This underutilization of the electromagnetic spectrum leads to spectrum holes or white spaces. A spectrum hole is a band of frequencies assigned to PU, but the band is not being utilized by that user. CR has been proposed to promote the efficient use of spectrum by exploiting the existence of spectrum holes. CR is an intelligent wireless communication system that senses its operational electromagnetic environment and adjusts its radio operating parameters like modulation type, power output, frequency etc to modify system operations such as maximizing throughput, mitigating interference, etc. SUs are the CR entities that uses spectrum hole. These SUs should not cause any interference to the PU. Hence, it is important to detect the PU correctly.

Spectrum sensing is the key function of CR. It is the process of monitoring the spectrum to detect the presence of PU on a specific channel. If the PU is absent (not utilizing spectrum) then, SU can utilize spectrum. Otherwise, SU cannot use the spectrum. Spectrum sensing techniques include energy detection, matched filter detection, cyclostationary feature detection, waveform detection etc [2]. A matched filter is a linear filter designed to maximize the output signal to noise ratio (SNR) for a given input signal. In matched filter detection technique, an unknown signal is correlated with a time shifted version of impulse response of the matched filter. Cyclostationary feature detection technique is the best method for detecting modulated signal with high levels of noise. PU signal is periodic in nature and hence they will exhibit

periodic statistical properties which will not be present in noise and interference. In energy detection technique, sum of square of received signals amplitude is taken. The energy detection method is also called as blind detector because it ignores the structure of the signal. Energy detection is commonly used because it is easy to implement and is less complex. Moreover, prior information about PU is not required as in case of matched filters.

Spectrum sensing by individual nodes suffers from the problem of hidden terminals, multipath fading, noise, shadowing, etc. This will reduce detection performance [3]. Therefore, CSS is used. Here, a parallel fusion sensing architecture is employed. CSS is the process of making final decision (regarding the presence or absence of PU) based on the sensing data collected by SU. In CSS, large number of SUs are employed to detect the channel. This information is passed on to a central entity, called as fusion center (FC). After collecting the sensing result, fusion is performed by FC and a decision is made.

In order to avoid interference and for efficient utilization of spectrum, correct decision should be made. Detection performance can be improved by –

- Increasing the sensing time
- Increasing the number of nodes
- Reducing the transmission distance
- Increasing the number of data samples transmitted to FC

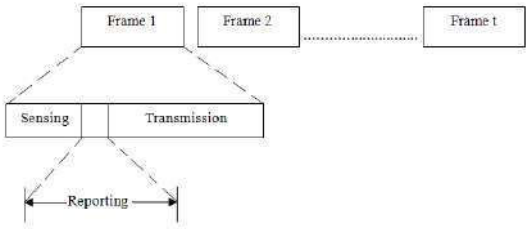

Fig. 1. Time frame architecture

Along with the increase in detection performance, more number of processes will be involved. Hence, more energy will be consumed. As the sensing performance increases, the energy consumption will also increase [4]. In this paper, possible ways of energy saving without compromising sensing performance is discussed.

The rest of this paper is organized as follows. System model is presented in section II. In section III, some of the works which helps in achieving energy efficiency is discussed. Finally, the work is concluded in section IV.

II. SYSTEM MODEL

Assume that the time is divided into frames and each frame follows a CSS scheme and data transmission. This is illustrated in Fig. 1.
Processes involved in each frame [4] are as follows:-

- Single node spectrum sensing and processing
- Delivery of data to the FC
- After collecting data from all the SU, processing and decision making is done by the FC
- Decision circulation among the nodes
- Data transmission by the allowed SU

Only first three processes are involved in spectrum sensing phase. A block level description of this is shown in Fig. 2. Consider a CR network with M SUs, one control channel (channel between SU and FC), one licensed channel (channel between PU and SU) and one FC. Here, each of the SU will be sensing the PU signal. Spectrum sensing can be formulated as a binary hypothesis problem, given by (1) and (2).

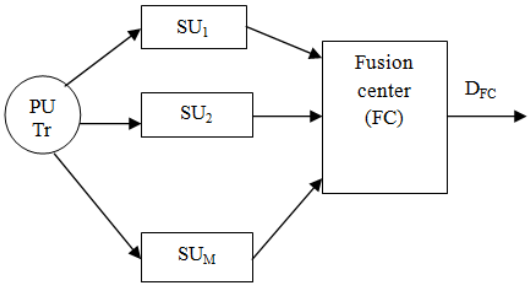

Fig. 2. Cooperative spectrum sensing

H_0: $y(n) = u(n)$ (1)
H_1: $y(n) = h(n)s(n) + u(n)$ (2)

where H_0 and H_1 denote the absence or presence of PU on the licensed channel respectively. y(n) represent received signal at each SU. u(n) represent noise. S(n) is the PU signal. h(n) is the channel gain. PU is said to be present if it belongs to the hypothesis H_1 and is said to be absent if it belongs to the hypothesis H_0.

First of all, the signal from PU is sampled. Each SU perform spectrum sensing by energy detection echnique [3]. In this technique, average of energy content in received sample is taken. Let E_i denote local statistics of SU i and is given by (3).

$$E_i = \frac{1}{N_i} \sum_{i=1}^{N} |y_i(n)|^2$$

Where Ni denotes number of samples, yi(n) received signal at the ith SU and n = 1, 2, 3,..... Ni. This sensed information is transmitted by the SU to the FC. FC is responsible for making the final decision. SU can transmit either the data or the decision to the FC.

According to the type of information that SUs transmits to the FC, CSS schemes can be generally categorized into two kinds: soft combination schemes and hard combination schemes [5]. In soft combination scheme, SUs directly send their local statistics which are energy values of the received signals from the SU to the FC. It includes equal gain combining (EGC) or square law combining (SLC) and maximum ratio combining (MRC). In EGC, estimated energy is sent to FC where they will be added together. This is given in (4).

$$E_{EGC} = \frac{1}{M} \sum_{i=1}^{M} E_i$$

where Ei is the energy of the ith node. Decision is made by comparing EEGC with the threshold value. In MRC, Weighted estimated energy is sent to FC where they will be added together. This is given by (5).

$$E_{MRC} = \frac{1}{M} \sum_{i=1}^{M} W_i \, E_i$$

where Wi is the weight of the ith node and Ei is the energy of the ith node. Decision is taken by comparing EMRC with threshold value. On reaching the FC, this estimated energy is compared with a threshold value. PU is said to be present if the estimated energy is greater than the threshold value. In hard combination scheme, SU converts local statistics into one-bit decision, i.e., 0 or 1 implies that a PU is absent or present, respectively. Then, they send these one-bit decisions to the FC. Hard decision fusion rule, includes OR, AND, half voting (HV), majority, and, in general, the K-out-of-N (KN) rule. As per OR rule, the PU is considered to be present, if at least one of the nodes detects the event. For PU detection using AND rule, all the nodes should detect it. In case of HV and majority rules, at least half and more than half of the nodes, respectively, should detect the PU. As per KN rule, the PU is considered to be present if at least K out of N nodes detects it. The cooperative detection probability and false alarm probability for AND, OR and the general KN rules are given by (6), (7) and (8) respectively, where `x' denotes `detection' or `false-alarm' and Pxi denotes the detection or false-alarm probability of the ith node.

$$Q_{x,AND} = \prod_{i=1}^{M} P_{xi} \quad (6)$$

$$Q_{x,OR} = 1 - \prod_{i=1}^{M} (1 - P_{xi}) \quad (7)$$

$$Q_{x,KN} = \sum_{i=k}^{M} \binom{M}{i} P_x^i (1 - P_x)^{M-i} \quad (8)$$

Two metrics which determine spectrum sensing performance is probability of detection and probability of false alarm. Probability of detection is the probability that the PU is active, and SU detect it successfully. Probability of false alarm is the probability that the PU is not active but the SU detects it to be active. Therefore, detection probability should be maximized to avoid interference, and false alarm probability should be minimized for efficient utilization of spectrum.

III. ENERGY SAVING METHODS

The authors in [6] proved that there exist an optimal sensing time which gives maximum throughput for the SUs provided the PU is protected. Here, the optimal sensing time is found by solving a concave optimization problem or by exhaustive search algorithm. The throughput is maximized in such a way that probability of false is less than the targeted probability of false alarm. The number of samples collected by the SUs from the PU reduces along with the reduction in sensing time. This helps in reducing the number of processes involved in spectrum sensing. Moreover, the ON time of spectrum sensing sensor reduces and hence battery life of the sensor increases. Optimization of sensing time helps in increasing the data transmission time. Hence, spectrum utilization can be improved. However, sensing period energy consumption is less compared to the energy consumed during transmission of data to the FC. Here, transmission time energy consumption is not considered. As a result, much of the energy cannot be saved using this method.

As the number of nodes increases, sensing performance will also increase. Once the number of cooperative nodes has reached a certain number, detection performance is only marginally increased upon addition of nodes. The number of active nodes should be chosen in such a way that the sensing performance is only marginally improved if an additional sensor is added and is decremented if a sensor is removed. In [7], relay is selected based on residual battery capacity and interference condition. The device is considered to be active only if residual battery capacity is greater than set energy threshold

level and interference with the PU is less than the interference threshold level. By using this method battery life of sensors can be saved. Also, the sensors need not be replaced frequently. However, this method will not help in improving spectrum utilization because channel conditions are not considered.

Correct decision can be obtained only if the channel between SU and FC is perfect. But in practice, reporting channel may experience fading which will degrade the performance of CSS. In [8], the authors proposed a cluster based spectrum sensing technique. Here, those SUs which are close to each other are grouped into clusters, so that the channel between any two nodes in the same cluster is perfect. Then, in each cluster, SU with the largest channel gain is selected as the cluster head. Each SU will transmit their local statistics to cluster head. Cluster head will make a cluster decision. Finally, decision made by the cluster head is transmitted to FC, where final decision is made about presence or absence of the PU. As the transmission distance between nodes is reduced only less transmit power, is required. This method reduces the reporting error and hence sensing performance can be improved. On the other hand, computational complexity increases with the increase in number of SUs and an extra energy is consumed due to the exchange of information.

Edward Peh and Ying-Chang Liang in [9] shows that cooperating a certain number of SU with highest PUs signal to noise ratio (SNR) has better performance than cooperating all the SU. Either a targeted probability of detection or probability of false alarm is set. After setting one of the probabilities, the other one is optimised. In order to give PU their desired level of protection, probability of detection is set at a fixed value while false alarm probability is reduced. To have high capacity, probability of false alarm is fixed at a constant value and detection probability is maximized as much as possible. It is shown that by reducing number of nodes probability of false alarm decreases significantly with constant detection probability (under the OR fusion scheme) and probability of detection increases with constant false alarm probability (under the AND fusion scheme). The advantage is that the communication overhead in terms of exchanged messages and processing is reduced. Hence, energy consumption reduces. But variable channel conditions will induce SNR variations. Moreover, each SU instantaneous SNR is needed and it has to be delivered to the FC. Practically, it is difficult to obtain the instantaneous SNR of each node.

In fading channels, the link between the SUs and the FC may not be good. A reporting link selection algorithm between the cooperative node and the FC is done in [10]. Here, nodes are arranged based on decreasing order of their SNR value and the links corresponding to higher SNR value is chosen as the reporting links. Number of links that has to be chosen depends on the total error rate (sum of miss detection and false alarm probability). Total error rate should be less than the targeted error bound for a given detection threshold. The number of links transmitting its data to the FC reduces and hence, less number of processes is involved in decision making. This reduces the energy consumed by FC. But channel conditions will cause variations in SNR. This may lead to selection of non-reliable links.

In [11], Yngve Sel´en, Hugo Tullberg, and Jonas Kronander has proposed algorithms to chose nodes which are spatially separated because closely spaced sensor will experience same shadow fading. Here, sensors are selected based on location of sensors and associated uncertainty. In correlation measure based node selection algorithm, it is assumed that all nodes are active and a sensor with largest summed correlation measure (e.g. - Euclidian distance) relative to the other sensors is removed. In iterative partitioning algorithm, sensors that are separated by more than decorrelation distance (minimum distance between sensors that experience uncorrelated shadow fading) from all the present sensors in the active set are chosen. As the number of sensors participating in spectrum sensing reduces battery life time can be improved. A large number of processes are involved in computation of correlation measure. This may increase the complexity. The proposed sensor selection method is good compared to the random sensor selection method.

As the number of SUs increases, larger bandwidth is required for reporting the result to the FC. Therefore the authors in [12] proposed a censoring technique, where only those SUs with enough information are allowed to transmit their data to FC. This is done by setting two thresholds $\lfloor 1$ and $\lfloor 2$. If the energy collected by the SU lies between $\lfloor 1$ and $\lfloor 2$, then no decision is made and there will not be any data transmission to FC. If the collected energy is greater than $\lfloor 2$ then decision H1 is transmitted and if it is less than $\lfloor 1$ decision H0 is transmitted to the FC. After censoring, average number of bits transmitted from the SU to the FC is quantized. By reducing the number of bits, number of computations involved in FC reduces. In this method, irrelevant information is not transmitted to the FC. It is showed that a large amount of reduction in sensing bits is possible with a very little performance degradation. If all the SU makes no decision, then the FC will not be able to make any final decision regarding presence or absence of the PU.

Sleeping and censoring scheme is presented in [13]. In sleep mode, each of the radio will switch

OFF its spectrum sensing transceiver. In censoring process, only awake nodes, which lie in a particular information region, are allowed to transmit data to FC. Moreover, optimal sleeping and censoring parameters are obtained which minimizes the energy consumption. Also, it provides detection probability greater than the minimum targeted probability of detection and false alarm probability less than maximum permissible probability of false alarm. When prior information about PU is not available, Neymen Pearson setup is followed and when prior information is available Bayesian setup is followed. It was shown that sleeping rate is higher when the sensing and transmission energies are equal and censoring rate is higher when transmission energy is greater than sensing energy. The proposed method helps in reducing the energy consumption significantly. However, in this work it is assumed that all nodes receive same SNR. This is possible only when all users have same distance to the PU.

Another algorithm for node selection is presented in [14]. Here, three methods are proposed for choosing nodes with best detection performance. The three methods are simple counting (SC), partial agreement counting (PAC) and collision detection (CD). In SC algorithm, number of ones (PU present) of each radio during the training period is counted and those CR with the highest count is allowed to cooperate. SC algorithm assumes that all nodes have same targeted false alarm rate. In PAC algorithm, SUs which have highest agreement with the FC is chosen to cooperate in spectrum sensing. The PAC method assumes that the FC has highest performance. This is not possible practically. In CD scheme, it is assumed that absence of PU is the global decision. Then the FC will transmit a channel release message to the SU. On receiving this message it will reply with an acknowledgement. If the FC receives the acknowledgement, the channel is assumed to be error free. This is not possible practically because channel conditions will cause unsuccessful message transmission. The proposed node selection algorithm helps in reducing the energy consumption but performance will decrease if malicious users are present. Moreover, if majority of SUs face bad channel conditions, incorrect decision will be made.

The linear CSS scheme (proposed in [15]) outperforms likelihood ratio test (LRT). The channel between SU and FC will not be ideal. Therefore, likelihood threshold has to be provided to each of the nodes. This is not possible practically. Here, linear combination weights are provided instead of changing the threshold for each node. The objective of [15] is to maximize the probability of detection while maintaining probability of false alarm below a targeted value.

IV. CONCLUSION

CR technology has been proposed to make full use of limited spectrum resource. In CR technology, it is essential to make correct decision in order to achieve efficient spectrum utilization and to avoid interference. CSS is an efficient method for making final decision regarding presence or absence of PU. The detection performance depends on a number of parameters like number of cooperative nodes involved in CSS, sensing time, distance and number of samples involved in processing. But all these methods will lead to larger energy consumption. Thus an increase in sensing performance can be achieved only by comprising energy efficiency. A cooperative spectrum sensing algorithm should consume less energy and should ensure high sensing performance in terms of probability of detection and probability of false alarm. In this paper, works which gives high sensing performance is studied. High sensing performance can be achieved by increasing the number of nodes involved in cooperative spectrum sensing, increasing the sensing time, reducing the distance etc. But all these parameters have an optimal value beyond which there won't be much increase in sensing performance. Choosing that optimal value for all the parameters might give an energy efficient system.

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IOT BASED CHILD SAFETY WEARABLE DEVICE

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***Abstract*— This paper discusses the concept of a smart wearable device for little children. The major advantage of this wearable over other wearable is that it can be used in any cellphone and doesn't necessarily require an expensive smartphone and not a very tech savvy individual to operate. The purpose of this device is to help parents locate their children with ease. At the moment there are many wearables in the market which help track the daily activity of children and also help find the child using Wi-Fi and Bluetooth services present on the device. But Wi-Fi and Bluetooth appear to be an unreliable medium of communication between the parent and child. Therefore, the focus of this paper is to have an SMS text enabled communication medium between the child's wearable and the parent as the environment for GSM mobile communication is almost present everywhere. The parent can send a text with specific keywords such as "LOCATION" "TEMPERA TURE" "UV" "SOS" "BUZZ", etc., the wearable device will reply back with a text containing the real time accurate location of the child which upon tapping will provide directions to the child's location on google maps app and will also provide the surrounding temperature, UV radiation index so that the parents can keep track if the temperature or UV radiation is not suitable for the child. The prime motivation behind this paper is that we know how important technology is in our lives but it can sometimes can't be trusted, and we always need to have a secondary measure at hand. The secondary measure used in this project is the people present in the surrounding of the child who could instantly react for the child's safety till the parents arrive or they could contact the parents and help locate them. The secondary measure implemented was using a bright SOS Light and distress alarm buzzer present on the wearable device which when activated by the parents via SMS text should display the SOS signal brightly and sound an alarm which a bystander can easily spot as a sign of distress. Hence this paper aims at providing parents with a sense of security for their child in today's time.**

Keywords—, Children, Arduino, Safety, Wearable.

1.INTRODUCTION

The Internet of Things System (loT) [1] refers to the set of devices and systems that stay interconnected with real-world sensors and actuators to the Internet. loT includes many different systems like smart cars, wearable devices [2] and even human implanted devices, home automation systems [3] and lighting controls; smart phones which are increasingly being used to measure the world around them. Similarly, wireless sensor networks [4] that measure weather, flood defenses, tides and more. There are two key aspects to the loT: the devices themselves and the server-side architecture that supports them The motivation for this wearable comes from the increasing need for safety for little children in current times as there could be scenarios of the child getting lost in the major crowded areas. This paper focusses on the key aspect that lost child can be helped by the people around the child and can play a significant role in the child's safety until reunited with the parents. Most of the wearables available today are focused on providing the location, activity, etc. of the child to the parents via Wi-Fi [8] and Bluetooth [9]. But Wi- Fi and Bluetooth seem a very unreliable source to transfer information. Therefore it is intended to use SMS as the mode of communication between the parent and child's wearable device, as this has fewer chances of failing compared to Wi-Fi and Bluetooth. The platform on which this project will be running on is the Arduino [10] Uno microcontroller board based on the ATmega328P, and the functions of sending and receiving SMS, calls and connecting to the internet which is provided by the Arduino GSM shield using the GSM network [11]. Also, additional modules employed which will provide the current location of the child to the parents via SMS. The second measure added is SOS Light indicator that will be programmed with Arduino UNO board to display the SOS signal using Morse code. The different modules stay enclosed in a custom designed 3D printed case [12]. In the scenario, a lost child can be located by the parent could send an SMS to the wearable device which would activate the SOS light feature on the wearable. Therefore alerting the people around the child that the child is in some distress and needs assistance as the SOS signal is universally known as the signal for help needed. Additionally, the wearable comes equipped with a distress alarm buzzer which sets to active by sending the SMS keyword "BUZZ" to the wearable. Hence the buzzer is loud and can be heard by the parent from very considerable distance. Also the parents via SMS can receive accurate coordinates of the child, which can help them locate the child with pinpoint accuracy. Some of the existing work done on these similar lines are for example the low-cost, lightweight Wristband Vital [2] which senses and reports hazardous surroundings for people who need immediate assistance such as children and seniors. It is based on a multi-

sensor Arduino micro-system and a low- power Bluetooth 4.1 module. The Vital band samples data from multiple sensors and reports to a base station, such as the guardian's phone or the emergency services. It has an estimated battery life of 100 hours. The major drawback for the Vital band is that it uses Bluetooth as the mode of communication between child and the parent. Since the distance between the two in some cases could be substantial and the Bluetooth just won't be able to establish a close link between the two.

2. SYSTEM DESIGN AND ARCHITECTURE

This section discusses the architecture and the design methodologies chosen for the development of the Child Safety wearable device.

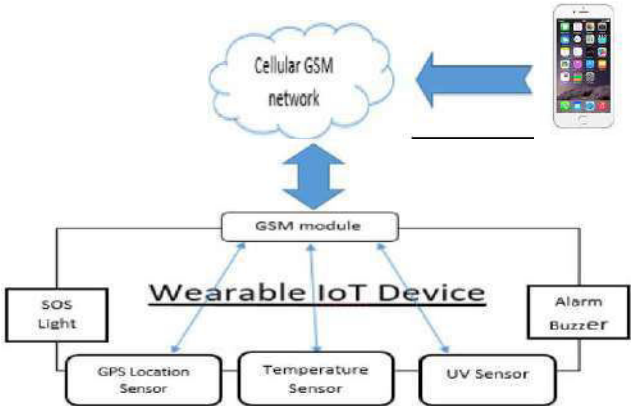


Fig 1. System overview of the wearable device.

A. System Overview

An A Tmega328p microcontroller controls the system architecture of the wearable with an Arduino Uno boot-loader. A 5 pin header allows for power (+3 V) and ground connections as well as providing access to TX, RX, and reset pins of theATMega328p. The Fig illustrates the architecture of the child safety wearable device, which depicts the various technologies and technological standards used. The system architecture of the wearable is based and controlled by an AT - mega328pmicrocontroller with an Arduino Uno boot loader. The Arduino Uno collects various types of data from the different modules interfaced to it, such as the GPS module upon being triggered by the Arduino GSM shield. The GSM shield is used as an interface to send the data received by the Arduino Uno via SMS or MMS to a smart phone over GSMl GPRS. The GSM shield functions as a trigger for the Arduino Uno to request data from its various modules. If an SMS text with distinct characters is sent to request the current location or GPS coordinates is sent to the Arduino GSM shield via the user's smartphone, then the GSM shield triggers the Arduino Uno to request the current GPS coordinates. The GSM shield uses digital pins 2 and 3 for the software serial communication with the MIO. Pin2 is connected to the MlO's TX pin and pin 3 to its RX pin. Once the Arduino Uno has received at thecoordinate information, it will process this information and transfer it over to the GSM shield, which then via SMS sends the coordinates to the user's smart phone. The user can just tap on the coordinates which will open up the default GPS application installed on the phone and will show the user the distance between the child and the user.

B. Wearable loT Device

The wearable device, for now, is not built on a SoC model, rather has been proposed using larger components and can later build on the SoC platform once put into manufacture.

The wearable loT device tasked with acquiring various data from the all the different modules connected. It comprises of Arduino Uno based on the ATmega328P microcontroller. It receives the data from its various physically connected modules, anatomizes this data and refines the data in a more user understandable format to the different available user interfaces .The user, therefore, can conveniently v i e w the information on their cell phone . The physical characteristics of the wearable device a r e proposed to be as a wrist watch which remains placed around the wrist of the child during times when the child is not being accompanied by an adult/parent. For the moment the design is not made compact, since the main focus now has been to show that this concept of smart wearable would be highly impactful for the safety of children. The wearable system runs on a battery with an output voltage of 5V. In order to maximize power consumption, the wearable device has been programmed to provide G P S and image information only upon request by SMS text via GSM shield.

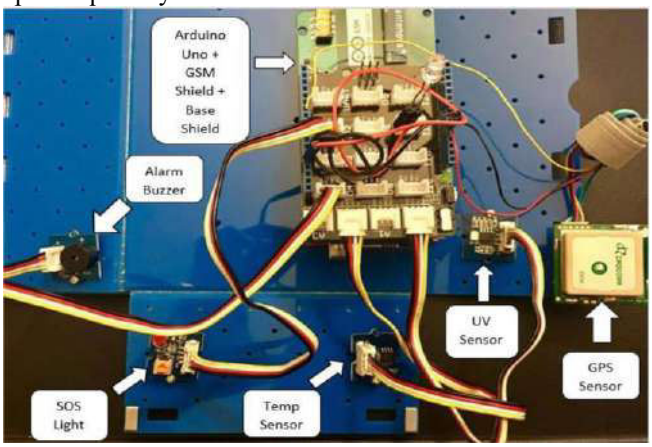
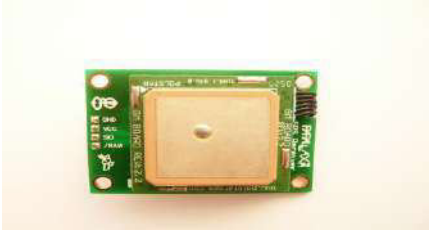


Fig 2. Proposed wearable loT Device.

1) GPS Location Sensor

For determining the real time location of the child Parallax PMB-648 GPS module has been used which communicates with the Arduino Uno through a 4800 bps TTL-level interface. The connections between the Arduino Uno and the GPS module established with three wired connections which enable the Arduino to read the GPS data.

The GPS module receives location information from the various satellites present in the NAVSTAR (American Satellites Timing and Ranging Global Positioning System)



GPS system [1]. It has a low power consunption and size of the only 32x32mm, which is very compact. 20 parallel satellite-tracking channels for fast acquisition and reacquisition. The output received from the GPS module is a standard string information which is governed by the National Marine Electronics Association (NMEA) protocol. To interface the PMB-648 GPS module with the Arduino to provide precise latitude and longitude GPS coordinates, the Tiny GPS library was added into the Arduino IDE. The Yin (red wire) on the PMB-648 GPS module is connected to the 5V pin on the Arduino Uno via jumper cables. Similarly, the GND (black wire) pin on the GPS module is connected to the GND pin on the Arduino Uno via jumper cables. The TXD (yellow wire) is connected to pin 6 of the Arduino Uno via jumper cables on the breadboard. The pin six on the Arduino Uno is a digital pin which can also be used for PWM (Pulse Width Modulation) applications. Once the SMS trigger text "LOCA nON" is sent from the cell phone of the user, this text is received by the Arduino GSM Shield which in turn triggers the Arduino Uno to execute the GPS code to fetch the current, accurate location of the GPS module. The location output received from the GPS module is in the following format:

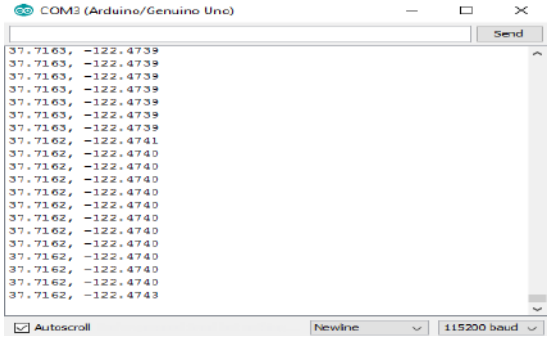
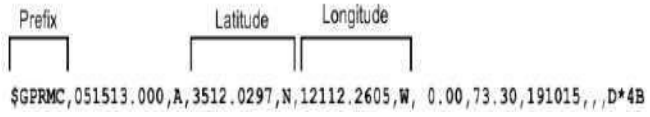


Fig 3. Output received GPS location sensor.

The latitude and longitude coordinates received are stored in variables called "flat" and "flon," which are then called upon when the SMS text received on the GSM module matches with the keyword "LOCA nON." If an SMS text is received which contains none of the pre-programmed keywords, then the Arduino GSM shield automatically deletes the text message and does not reply back the user the with any location details. Once the SMS trigger text "LOCATION" is sent from the smartphone of the user, this text is received by the Arduino GSMShield which in turn triggers the Arduino Uno to execute the GPS code to fetch the current, accurate location of the GPS module. The location output string received from the GPS module is in the following format:

1) 220516-Time Stamp 2)A-validity- A-ok, V-invalid
3) 5133.82-current Latitude 4) N-North/South
5) 00042.24-current Longitude 6) W-EastiWest
7) 173.8-Speed in knots 8) 231.8-True course
9) 130694-Date Stamp 10) 004.2-Variation
11) W-East/West 12) *70-checksum



Hence the user can just directly click on this received Google maps hyperlink which will automatically redirect the user to the Google Maps app on the smartphone and show the pinpoint location of the child. This SMS can be received directly on the default SMS app or via Android app on the user's smartphone.

2) Temperature Sensor:

In order to measure the temperature of the surround ings of the child, a seeed studio grove temperature sensor was used.

The sensor module is equipped with a thermistor for measuring the ambient temperature and the fluctuations with high accuracy. The observable temperature detectability for this sensor ranges from -40°C to -125°C and the precise accuracy for this device range from + 1.5°C to -1.5°C. The temperature is connected to the Arduino Uno and GSM shield using a Grove base shield which contains eight digital ports ranging from D 1 to D8, four analog ports ranging from AO to A3 and 4 I2C ports. Therefore, the temperature sensor is connected to the A2 analog port of the base shield. The temperature value is stored in a string getTemp(a), where "a" is the integer type. Hence the getTemp(a) is called by the GSM module upon receiving the proper SMS
keyword "TEMPERATURE" by the user's smartphone.

3) UV Sensor

In order to measure the ultraviolet radiation intensity present around the surroundings of the child, a seeed studio grove UV sensor was used. The UV sensor is built on the GUVA-SI2D sensor (spectral range of 200nm-400nm). The sensor works by outputting electrical signal which alters with UV intensity. It is a highly sensitive sensor. It is known that the absorption of UV rays in minor amounts can be progressive to the health of a person as it helps in the production of Vitamin D The purpose of a UV sensor in a child wearable device can be to protect the child from harmful radiations of the sun. The UV sensor is connected to the AO port of the base shield. In the figure belowshown is the output received from the UV sensor for thedifferent intensities of sunlight.

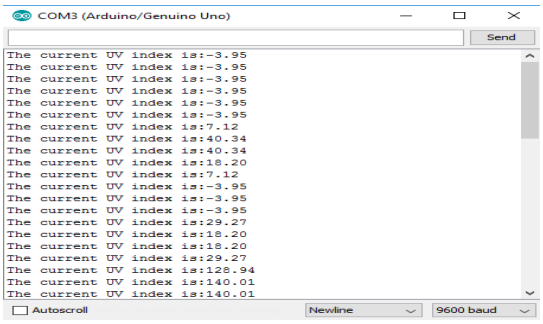
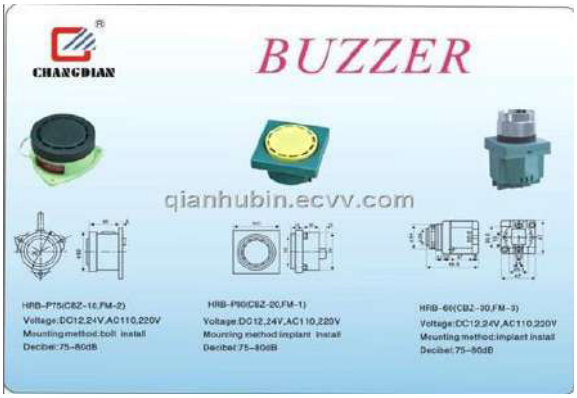


Fig 4. Output received from UV sensor

4) SOS Light

The another theory that this paper focusses on is that By standers are the fust mode of help for a missing child. The purpose of the SOS light is to be able to alert the people nearbythat the child might be in distress since the light will be flashing the universal SOS light symbol which many people nowadays know for to be a sign for help. This can be activated by the parent itself by sending an SMS text with the keyword "SOS" to the child's wearable which will activate the SOS light flashing. The SOS light works on the principal of Morse code in which "S" stands for three short dots and the "0" stands for three long dashes. Since a very long time, the SOS signal has been universally known for being the sign of distress and help. The SOS signal is referred to by all security personals, who if find the child to be missing can act and help locate the parents with surplus resources present at their disposal. The SOS Light is connected to the pin 13 of the base shield.

5) Distress Alarm Buzzer



In the scenario, if a child is separated from his/her parents. The parent can locate their child by sounding a very loud alarm on the wearable. To achieve this, grove seeed studio buzzer was used, which has a piezoelectric module which is responsible for emitting a strong tone upon the output being set to HIGH. The grove buzzer module is activated upon sending an SMS text with the keyword "BUZZ" from a cell phone. Also, this buzzer works similar to the SOS led by alerting the people nearby with the distressed tone that the child might be lost and is in need of assistance. The buzzer isconnected to the D4 digital port of the base shield.

C. Gateway:

1) Arduino GSM Shield : GSM/GPRS Modem-RS232 is built with Dual Band GSM/GPRS engine- SIM900A, works on frequencies 900/ 1800 MHz. The baud rate is configurable from 9600-115200 through AT command. The onboard Regulated Power supply allows you to connect wide range unregulated power supply . Using this modem, one can make audio calls, SMS, Read SMS, attend the incoming calls and internet ect through simple AT commands.

It transfers the information over to the user via SMS. Arduino provides GSM libraries for GSM module as well as allowing the GSM module to make/receive a call, send/receive SMS and act as a client/server. The GSM module receives 5V power supply directly from the 5V pin connection at the Arduino Uno 5V. The serial communication between the Arduino Uno and GSM module is performed between the serial pins 0,1. The Arduino has been programmed to receive SMS text messages from the parent's cellphone via GSM module. The GSM module will constantly be scanning the received text messages for the specific keywords such as "LOCATION", "TEMPERATURE", "SOS" and "BUZZ".

Its very reliable as the GSM shield is an Arduino produced device, it has the necessary GSM libraries installed into the Arduino IDE interfacing with Arduino Uno. The basic reason for using the GSM shield as the mode of communication over Wi-Fi and Bluetooth was that this wearable was aimed at being accessible to any cellphone user and not necessarily an expensive smartphone user. A user who is technologically challenged can also use it with ease as the technology is made user-friendly.

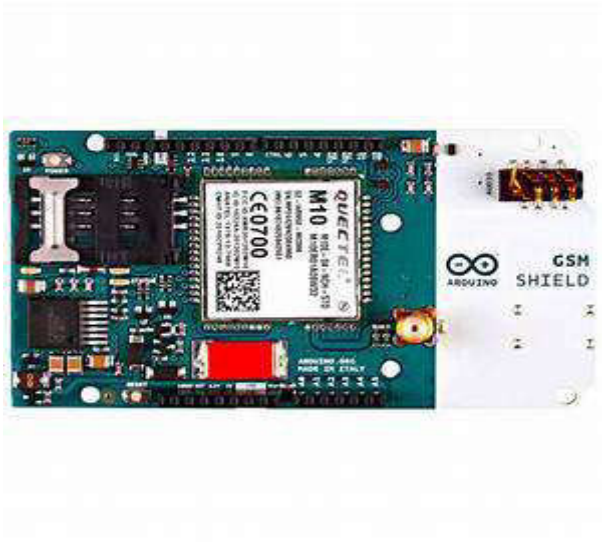


Fig 5. Gateway: Arduino GSM Shield.

2) Cellphone SMS app interface

For transfering the information over to the user via SMS by using General Packet Radio Service(GPRS) which can provide data rates around 56-114 Kbit/sec an Arduino GSM Shield is used. Arduino provides several libraries such as Ethernet, Wi-Fi for the different Arduino shields. Similarly, they provide GSM libraries for their official GSM shield as well which allows the gsm shield to make/receive a gsm shield to make/receive a call, send/receive SMS and act as a client/server.

III. RESULTS:

In this section, the experimental tests were performed to detennine the various components of the proposed wearable device.

A. GPS Location Sensor

By testing the wearable device multiple times with repeated SMS texts. The GPS location sensor will be able to respond back with precise latitude and longitude coordinates of the wearable device to the user's cellphone, which then the user would click on the received Google maps URL which would, in tum, open the gmaps app or any default browser and display location. In all cases the GPS module is tested, it responds back to the user's cellphone within a minute. The GPS turned out to be so precise with the location that it performed even better than the GPS on an expensive smartphone. As shown in the image below, the GPS module (red bubble) was able to show the current location of the wearable with pinpoint accuracy and also show exactly at which side of the building it is present. Whereas for the smartphone (blue dot) is showing the wearable to be present on the street, which is marginally off from the exact location. This marginal miss match in the pin-point location of the wearable can tum out to be fatal in a real life scenario, where the parent may be miss lead to the wrong location of the child. The only drawback that could be stated was, the GSM module could not interpret multiple valid keywords sent in a single message. For example, SMS string
sent: LOCA NON TEMPERATURE UV BUZZ SOS; it would not send a reply back to the gsm module.

B. Temperature and UV sensor:

Similar to the GPS location sensor, the Temperature, and UV sensors were tested multiple times under different temperatures and higher intensities of sunlight. Both the sensors performed exceptionally well to the test perfonned. The response time to receive a response back to the keywords "TEMPERATURE" and "UV" was under a minute. Also, the temperature sensor was subjected to higher temperatures and compared with a thermostat reading present in the room which would differ with the sensor reading by +O.2°C to -O.2°C. Also, the UV sensor was measured under different intensities of sunlight. The UV sensor was quick in responding to the changes in the intensity of sunlight. The response time to receive a response back to the keywords "UV" was under a minute as well.

Fig 7. SMS app screen for UV and Temperature sensor

c. SOS Light and Distress Alarm Buzzer:

The light and buzzer differ from the above sensors in the SMS trigger mechanism. Upon sending an SMS with either "SOS" or "BUZZ," this would trigger the light and buzzer to perform an output function instead of providing measurements back to the user's cellphone such as in the scenario of the other sensors. Upon receiving the correct keywords, the SOS light and Alarm Buzzer would first perform the particular task of flashing the SOS light and sounding a distress alarm which can take a little longer than their sensor counterparts. After completion of their respective functions, the response is sent back to the user' cell phone stating: "SOS Signal Sent" and "Playing Buzzer."

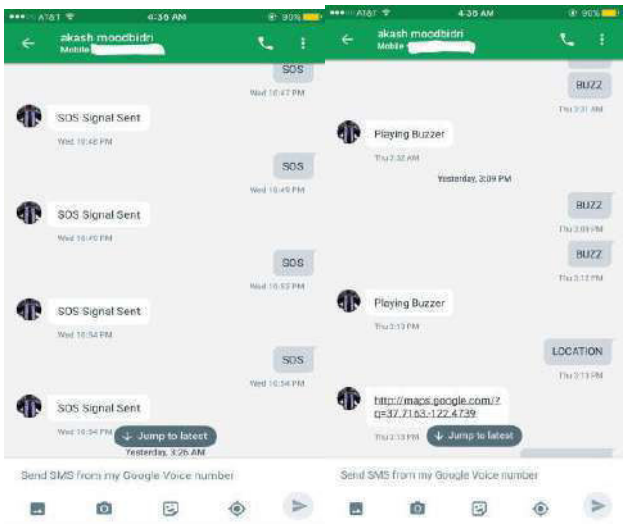


Fig 8. SMS app screen for Left: SOS Light and Right: Distress alarm buzzer.

IV. FUTURE SCOPE

1) Camera Module:

For surveillance of the child's surroundings, to get a clearer picture of the location, this wearable can also contain a camera module incorporated in it. The hardware that could be used would be a adafruit TTL serial camera. Since the major focus of this wearable project is the GSM module which is a better alternative than Bluetooth, Wi-Fi or ZigBee due to the short range and connectivity issues of these technologies. Therefore, for this project using the GSM technologies is beneficial as the cellular range is vast and since all the communication between the wearable and the user is taking place via SMS, therefore no internet connectivity is required at all. But, still, the Arduino GSM shield possess the added advantage of using GPRS which enables the board to use the internet if required. Whereas for the camera module which supports video streaming but due to the constraint of trying to use only sms, therefore only four wire connections will be taking place. The red and black wires will be connected directly to +5V and GND respectively to the Arduino uno board. Whereas for the RX pin which will be used for sending data via arduino uno and arduino gsm board and for the TX pin which will be utilized for receiving incoming data via from the modules. The lOK resistor divider, the camera's serial data pins are 3.3v logic,

and it would be a good idea to divide the 5V down so that its 2.5V. Normally the output from the digital 0 pin is 5V high, the way we connected the resistors is so the camera input (white wire) never goes above 3.3V. To talk to the camera, the Arduino uno will be using two digital pins and a software serial port to talk to the camera. Since the camera or the Arduino Uno do not have enough onboard memory to save snapshots clicked and store it temporarily, therefore an external storage source microSD breakout board will be used to save the images temporarily. The camera works on a standard baud rate of 38400 baud. The camera will be collecting information in the same manner as the GPS module. It will be on standby conserving power waiting for the particular keyword "SNAPSHOT" to be sent from the user's smartphone to the GSM shield will activate the camera to start clicking a snapshot of the surrounding and save the file temporarily on the external microSD card. After which Arduino Uno will access the saved image from the microSD storage and transfer it to the GSM module which send it to the user via SMS/MMS text.

2) Android App:

The idea behind the Android app has been derived from having an automated bot to respond to text message responses from the user. It will provide the user with predefined response options at just the click of a button. The user doesn't need to memorize the specific keywords to send. Also, the bot will be preprogrammed to present the user with a set of predefined keyword options such as "LOCATION," "SNAPSHOT," "SOS," etc. Whereas for the future aspect of this wearable device based on what type sensor is added to it, additional specific keywords could be added such as, "HUMIDITY," "ALTITUDE," etc.

V. CONCLUSIONS

The child safety wearable device is capable of acting as a smart loT device. It provides parents with the real-time location, surrounding temperature, UV radiation index and SOS light along with Distress alarm buzzer for their child's surroundings and the ability to locate their child or alert bystanders in acting to rescue or comfort the child. The smart child safety wearable can be enhanced much more in the future by using highly compact Arduino modules such as the LilyPad Arduino which can be sewed into fabrics. Also a more power efficient model will have to be created which will be capable of holding the battery for a longer time.

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DLAU: Implementation of A Scalable Deep Learning Accelerator Unit on FPGA

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Abstract—As the emerging field of machine learning, deep learning shows excellent ability in solving complex learning problems. However, the size of the networks becomes increasingly large scale due to the demands of the practical applications, which poses significant challenge to construct a high performance implementations of deep learning neural networks. In order to improve the performance as well to maintain the low power pipelined processing units to improve the throughput and utilizes tile techniques to explore locality for deep learning applications. Experimental results on the state-of-the-art Xilinx FPGA board demonstrate that the DLAU accelerator is able to achieve up to 36.1x speedup comparing to the Intel Core2 processors, with the power consumption at 234mW. cost, in this paper we design DLAU, which is a scalable accelerator architecture for large-scale deep learning networks using FPGA as the hardware prototype. The DLAU accelerator employs three

Index Terms—FPGA; Deep Learning; neural network; hardware accelerator.

I. INTRODUCTION

In the past few years, machine learning has become perva- sive in various research fields and commercial applications, and achieved satisfactory products. The emergence of deep learning speeded up the development of machine learning and artificial intelligence. Consequently, deep learning has become a research hot spot in research organizations [1]. In general, deep learning uses a multi-layer neural network model to extract high-level features which are a combination of low- level abstractions to find the distributed data features, in order to solve complex problems in machine learning. Currently the most widely used neural models of deep learning are Deep Neural Networks (DNNs) [2] and Convolution Neural Networks (CNNs) [3], which have been proved to have excellent capability in solving picture recognition, voice recognition and other complex machine learning tasks.

However, with the increasing accuracy requirements and complexity for the practical applications, the size of the neural networks becomes explosively large scale, such as the Baidu Brain with 100 Billion neuronal connections, and the Google cat-recognizing system with 1 Billion neuronal connections. The explosive volume of data makes the data centers quite power consuming. In particular, the electricity consumption of data centers in U.S. are projected to increase to roughly 140 billion kilowatt-hours annually by 2020 [4]. Therefore, it poses significant challenges to implement high performance deep learning networks with low power cost, especially for large- scale deep learning neural network models. So far, the state- of-the-art means for accelerating deep learning algorithms are Field-Programmable Gate Array (FPGA), Application Spe- cific Integrated Circuit (ASIC), and Graphic Processing Unit (GPU). Compared with GPU acceleration, hardware accel- erators like FPGA and ASIC can achieve at least moderate performance with lower power consumption. However, both FPGA and ASIC have relatively limited computing resources, memory, and I/O bandwidths, therefore it is challenging to develop complex and massive deep neural networks using hardware accelerators. For ASIC, it has a longer development cycle and the flexibility is not satisfying. Chen et al presents a ubiquitous machine-learning hardware accelerator called DianNao [6], which initiated the field of deep learning pro- cessor. It opens a new paradigm to machine learning hardware accelerators focusing on neural networks. But DianNao is not implemented using reconfigurable hardware like FPGA, therefore it cannot adapt to different application demands. Currently around FPGA acceleration researches, Ly and Chow

[5] designed FPGA based solutions to accelerate the Re- stricted Boltzmann Machine (RBM). They created dedicated hardware processing cores which are optimized for the RBM algorithm. Similarly Kim et al [7] also developed a FPGA based accelerator for the restricted Boltzmann machine. They use multiple RBM processing modules in parallel, with each module responsible for a relatively small number of nodes. Other similar works also present FPGA based neural network accelerators [9]. Qi et al. present a FPGA based accelerator [8], but it cannot accommodate changing network size and network topologies. To sum up, these studies focus

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TABLE
I
PROFILING OF HOT SPOTS OF DNN

Algorithms	Matrix Multiplication	Activation	Vector
Feedforward	98.60%	1.40%	
RBM	98.20%	1.48%	0.30%
BP	99.10%	0.42%	0.48%

application, we employ tile techniques to partition the large scale input data. The DLAU architecture can be configured to operate different sizes of tile data to leverage the trade-offs between speedup and hardware costs. Consequently the FPGA based accelerator is more scalable to accommodate different machine learning applications.

1. The DLAU accelerator is composed of three fully pipelined processing units, including TMMU, PSAU, and AFAU. Different network topologies such as CNN, DNN, or even emerging neural networks can be composed from these basic modules. Consequently the scalability of FPGA based accelerator is higher than ASIC based accelerator.

II. TILE TECHNIQUES AND HOT SPOT PROFILING

Restricted Boltzmann Machines (RBMs) have been widely used to efficiently train each layer of a deep network. Normally a deep neural network is composed of one input layer, several hidden layers and one classifier layer. The units in adja- cent layers are all-to-all weighted connected. The prediction process contains feedforward computation from given input neurons to the output neurons with the current network config- urations. Training process includes pre-training which locally tune the connection weights between the units in adjacent layers, and global training which globally tune the connection weights with Back Propagation process.

The large-scale deep neural networks include iterative computations which have few conditional branch operations, there- fore they are suitable for parallel optimization in hardware. In this paper we first explore the hot spot using the profiler. Results in Fig. I illustrates the percentage of running time including Matrix Multiplication (MM), Activation, and Vector operations. For the representative three key operations: feed forward, Restricted Boltzmann Machine (RBM), and back propagation (BP), matrix multiplication play a significant role of the overall execution. In particular, it takes 98.6%, 98.2%, and 99.1% of the feed forward, RBM, and BP operations. In comparison, the activation function only takes 1.40%, 1.48%, and 0.42% of the three operations. Experimental results on profiling demonstrate that the design and implementation of MM accelerators is able to improve the overall speedup of the system significantly.

However, considerable memory bandwidth and computing resources are needed to support the parallel processing, consequently it poses a significant challenge to FPGA implemen- tations compared with GPU and CPU optimization measures. In order to tackle the problem, in this paper we employ tile techniques to partition the massive input data set into tiled subsets. Each designed hardware accelerator is able to buffer the tiled subset of data for processing. In order to support the large-scale neural networks, the accelerator architecture are reused. Moreover, the data access for each tiled subset can run in parallel to the computation of the hardware accelerators.

Algorithm 1 Pseudocode Code of the Tiled Inputs

```
Require:
  Ni: the number of the input neurons No: the
  number of the output neurons Tile_Size: the
  tile size of the input data
  batchsize: the batch size of the input data
  for n = 0; n < batchsize; n++ do
    for k = 0; k < Ni; k+= Tile_Size do for j = 0;
      j < No; j++ do
        y[n][j] = 0;
        for i = k; i < k + Tile_Size && i < Ni; i++ do
          y[n][j] += w[i][j] x[n][i];
          if i == Ni − 1 then
            y[n][j] = f(y[n][j]);
          end if end
        for
      end for
    end for
  end for
```

In particular, for each iteration, output neurons are reused as the input neurons in next iteration. To generate the output neurons for each iteration, we need to multiply the input neurons by each column in weights matrix. As illustrated in Algorithm 1, the input data are partitioned into tiles and then multiplied by the corresponding weights. Thereafter the calculated part sum are accumulated to get the result. Besides the input/output neurons, we also divided the weight matrix into tiles corresponding to the tile size. As a consequence, the hardware cost of the accelerator only depends on the tile size, which saves significant number of hardware resources. The tiled technique is able to solve the problem by imple- menting large networks with limited hardware. Moreover, the pipelined hardware implementation is another advantage of FPGA technology compared to GPU architecture, which uses massive parallel SIMD architectures to improve the overall performance and throughput. According to the profiling results depicted in Table I, during the prediction process and the training process in deep learning algorithms, the common but important computational parts are matrix multiplication and activation functions, consequently in this paper we implement the specialized accelerator to speed up the matrix multiplica- tion and activation functions.

III. DLAU ARCHITECTURE AND EXECUTION MODEL

Fig. 1 describes the DLAU system architecture which contains an embedded processor, a DDR3 memory controller, a DMA module, and the DLAU accelerator. The embedded processor is responsible for providing programming interface to the users and communicating with DLAU via JTAG-UART. In particular it transfers the input data and the weight matrix to internal BRAM blocks, activates the DLAU accelerator, and returns the results to the user after execution. The DLAU is integrated as a standalone unit which is flexible and adaptive

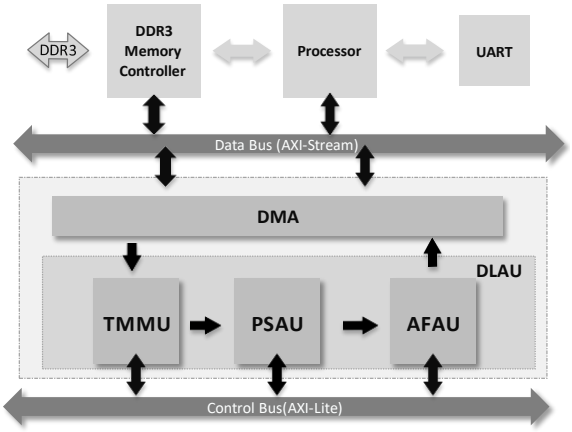

Fig. 1. DLAU Accelerator Architecture.

to accommodate different applications with configurations. The DLAU consists of 3 processing units organized in a pipeline manner: Tiled Matrix Multiplication Unit (TMMU), Part Sum Accumulation Unit (PSAU), and Activation Function Acceleration Unit (AFAU). For execution, DLAU reads the tiled data from the memory by DMA, computes with all the three processing units in turn, and then writes the results back to the memory.

In particular, the DLAU accelerator architecture has follow- ing key features:

FIFO Buffer: Each processing unit in DLAU has an input buffer and an output buffer to receive or send the data in FIFO. These buffers are employed to prevent the data loss caused by the inconsistent throughput between each processing unit.

Tiled Techniques: Different machine learning applications may require specific neural net-work sizes. The tile technique is employed to divide the large volume of data into small tiles that can be cached on chip, therefore the accelerator can be adopted to different neural network size. Consequently the FPGA based accelerator is more scalable to accommodate different machine learning applications.

Pipeline Accelerator: We use stream-like data passing mechanism (e.g. AXI-Stream for demonstration) to transfer data between the adjacent processing units, therefore TMMU, PSAU, and AFAU can compute in streaming-like manner. Of these three computational modules, TMMU is the primary computational unit, which reads the total weights and tiled nodes data through DMA, performs the calculations, and then transfers the intermediate Part Sum results to PSAU. PSAU collects Part Sums and performs accumulation. When the accumulation is completed, results will be passed to AFAU. AFAU performs the activation function using piecewise linear interpolation methods. In the rest of this section, we will detail the implementation of these three processing units respectively.

A. *TMMU architecture*

Tiled Matrix Multiplication Unit (TMMU) is in charge of multiplication and accumulation operations. TMMU is spe- cially designed to exploit the data locality of the weights and is responsible for calculating the Part Sums. TMMU employs

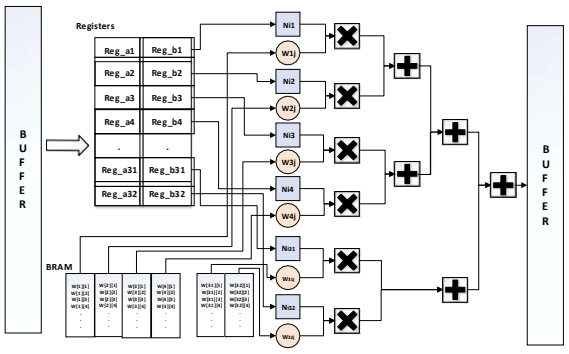

Fig. 2. TMMU Schematic Diagram.

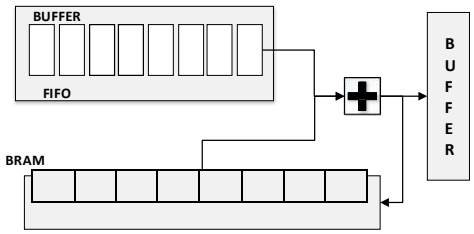

Fig. 3. PSAU Schematic Diagram

an input FIFO buffer which receives the data transferred from DMA and an output FIFO buffer to send Part Sums to PSAU. Fig. 2 illustrates the TMMU schematic diagram, in which we set tile size=32 as an example. TMMU firstly reads the weight matrix data from input buffer into different BRAMs in 32 by the row number of the weight matrix (n=i%32where n refers to the number of BRAM, and i is the row number of weight matrix). Then, TMMU begins to buffer the tiled node data. In the first time, TMMU reads the tiled 32 values to registers Reg_a and starts execution. In parallel to the computation at every cycle, TMMU reads the next node from input buffer and saves to the registers Reg_b. Consequently the registers Reg_a and Reg_b can be used alternately.

For the calculation, we use pipelined binary adder tree structure to optimize the performance. As depicted in Fig. 2, the weight data and the node data are saved in BRAMs and registers. The pipeline takes advantage of time-sharing the coarse-grained accelerators. As a consequence, this im- plementation enables the TMMU unit to produce a Part Sum result every clock cycle.

B. *PSAU architecture*

Part Sum Accumulation Unit (PSAU) is responsible for the accumulation operation. Fig. 3 presents the PSAU architecture, which accumulates the part sum produced by TMMU. If the Part Sum is the final result, PSAU will write the value to output buffer and send results to AFAU in a pipeline manner. PSAU can accumulate one Part Sum every clock cycle, therefore the throughput of PSAU accumulation matches the generation of the Part Sum in TMMU.

C. AFAU architecture

Finally, Activation Function Acceleration Unit (AFAU) implements the activation function using piecewise linear interpolation ($y=ai*x+bi$, $x \in [x_i, x_{i+1}]$). This method has been widely applied to implement activation functions with negligible accuracy loss when the interval between x_i and x_{i+1} is insignificant. Eq. (1) shows the implementation of sigmoid function. For $x>8$ and $x \leq -8$, the results are sufficiently close to the bounds of 1 and 0, respectively. For the cases in $-8<x \leq 0$ and $0<x \leq 8$, different functions are configured. In total we divide the sigmoid function into four segments.

$$f(x) = \begin{cases} 0 & \text{if } x \leq -8 \\ 1 + a[\lfloor -x \rfloor] x - b[\lfloor -x \rfloor] & \text{if } -8 < x \leq 0 \\ a[\lfloor x \rfloor] x + b[\lfloor x \rfloor] & \text{if } 0 < x \leq 8 \\ 1 & \text{if } x > 8 \end{cases} \quad (1)$$

Similar to PSAU, AFAU also has both input buffer and output buffer to maintain the throughput with other processing units. In particular, we use two separate BRAMs to store the values of a and b. The computation of AFAU is pipelined to operate sigmoid function every clock cycle. As a consequence, all the three processing units are fully pipelined to ensure the peak throughput of the DLAU accelerator architecture.

IV. EXPERIMENTS AND DATA ANALYSIS

In order to evaluate the performance and cost of the DLAU accelerator, we have implemented the hardware prototype on the Xilinx Zynq Zedboard development board, which equips ARM Cortex-A9 processors clocked at 667MHz and programmable fabrics. For benchmarks, we use the Mnist data set to train the 784 × N × 10 Deep Neural Networks in Matlab, and use M × N layers weights and nodes value for the input data of DLAU. For comparison, we use Intel Core2 processor clocked at 2.3GHz as the baseline.

In the experiment we use Tile size=32 considering the hardware resources integrated in the Zedboard development board. The DLAU computes 32 hardware neurons with 32 weights every cycle. The clock of DLAU is 200MHz (one cycle takes 5ns). Three network sizes—64×64, 128×128, and 256×256 are tested.

A. Speedup Analysis

We present the speedup of DLAU and some other similar implementations of the deep learning algorithms in Table II. Experimental results demonstrate that the DLAU is able to achieve up to 36.1x speedup at 256 × 256 network size. In comparison, Ly&Chows work [5] and Kim et.als work [7] present the work only on Restricted Boltzmann Machine algorithms, while the DLAU is much more scalable and flexible. DianNao [6] reaches up to 117.87x speedup due to its high working frequency at 0.98GHz. Moreover, as DianNao is hardwired instead of implemented on a FPGA platform, therefore it cannot efficiently adapt to different neural network sizes.

Fig. 4 illustrates the speedup of DLAU at different network sizes-64 × 64, 128 × 128, and 256 × 256 respectively. Experimental results demonstrate a reasonable ascendant speedup

TABLE II
COMPARISONS BETWEEN SIMILAR APPROACHES

Work	Network	Clock	Speedup	Baseline
Ly&Chow [5]	256×256	100MHz	32×	2.8GHz P4
Kim et.al [7]	256×256	200MHz	25×	2.4GHz Core2
DianNao [6]	General	0.98GHz	117.87×	2GHz SIMD
Zhang et.al [3]	256×256	100MHz	17.42×	2.2GHz Xeon
DLAU	256×256	200MHz	36.1×	2.3GHz Core2

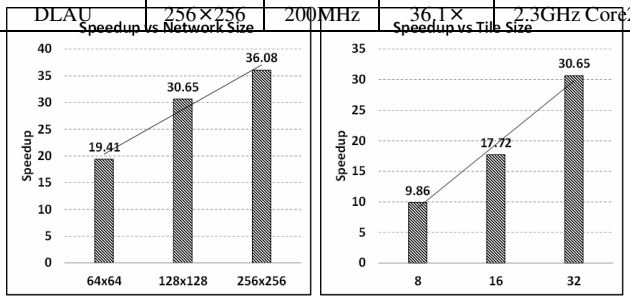

Fig. 4. Speedup at Different Network Sizes and Tile Sizes.

TABLE III
RESOURCE UTILIZATION OF DLAU AT 32×32 TILE SIZE

Component	BRAMs	DSPs	FFs	LUTs
TMMU	32	158	25356	32461
PSAU	1	2	754	632
AFAU	2	7	2216	3291
Total	35	167	28326	36384
Available	280	220	106400	53200
Utilization	12.5%	75.9%	26.6%	68.4%

with the growth of neural networks sizes. In particular, the speedup increases from 19.2x in 64 × 64 network size to 36.1x at the 256 × 256 network size. The right part of Fig. 4 illustrates how the tile size has an impact on the performance of the DLAU. It can be acknowledged that bigger tile size means more number of neurons to be computed concurrently. At the network size of 128 × 128, the speedup is 9.2x when the tile size is 8. When the tile size increases to 32, the speedup reaches 30.5x. Experimental results demonstrate that the DLAU framework is configurable and scalable with different tile sizes. The speedup can be leveraged with hardware cost to achieve satisfying trade-offs.

B. Resource utilization and Power

Table III summarizes the resource utilization of DLAU in 32 × 32 tile size including the BRAM resources, DSPs, FFs, and LUTs. TMMU is much more complex than the rest two hardware modules therefore it consumes most hardware resources. Taking the limited number of hardware logic resources provided by Xilinx XC7Z020 FPGA chip, the overall utilization is reasonable. The DLAU utilizes 167 DSP blocks due to the use of the Floating-point addition and the Floating-point multiplication operations.

Table IV compares the resource utilization of DLAU with other two FPGA based literatures. Experimental results depict

TABLE IV
RESOURCE COMPARISONS BETWEEN SIMILAR APPROACHES

Implementation	FPGA	BRAMs	DSPs	FFs	LUTs
Ly&Chow [5]	XC2VP70	257	N/A	30403	29885
Kim et.al [7]	N/A	589824	18	11790	7662
DLAU	XC7Z020	35	167	28326	36384

TABLE V
POWER CONSUMPTION OF THE UNITS

Component	Power	Component	Power
Accelerator-TMMU	189mW	Processor	1307mW
Accelerator-PSAU	5mW	DDR Controller	177mW
Accelerator-AFAU	25mW	Peripherals	26mW
Accelerator-DMA	15mW	Clocks	70mW
Accelerator-Total	234mW	System Total	1814mW

that our DLAU accelerator occupies similar number of FFs and LUTs to Ly&Chow's work [5], while it only consumes 35/257=13.6% on the BRAMs. Comparing to the Kim et.al's work [7], the BRAM utilization of DLAU is insignificant. This is due to the tile techniques so that large scale neural networks can be divided into small tiles, therefore the scalability and flexibility of the architecture is significantly improved.

In order to evaluate the power consumption of accelerator, we use Xilinx Vivado tool set to achieve power cost of each processing unit in DLAU and the DMA module. The results in Table IV-B depict that the total power of DLAU is only 234mW, which is much lower than that of DianNao (485mW). The results demonstrate that the DLAU is quite energy efficient as well as highly scalable compared to other accelerating techniques. To compare the energy and power between FPGA based accelerator and GPU based accelera- tors, we also implement a prototype using the state-of-the-art NVIDIA Tesla K40c as the baseline. K40c has 2880 stream cores working at peak frequency 875MHz, and the Max Memory Bandwidth is 288 (GB/sec). In comparison, we only employ 1 DLAU on the FPGA board working at 100MHz. In order to evaluate the speedup of the accelerators in a real deep learning applications, we use DNN to model 3 benchmarks, including Caltech101, Cifar-10, and MNIST, respectively. Fig. 5 illustrates the comparison between FPGA based GPU+cuBLAS implementations. It reveals that the power consumption of GPU based accelerator is 364 times higher than FPGA based accelerators. Regarding the total energy consumption, the FPGA based accelerator is 10x more energy efficient than GPU, and 4.2x than GPU+cuBLAS optimizations.

Finally Fig. 6 illustrates the floor plan of the FPGA chip. The left corner depicts the ARM processor which is hard- wired in the FPGA chip. Other modules, including different components of the DLAU accelerator, the DMA, and memory interconnect, are presented in different colors. Regarding the programming logic devices, TMMU takes most of the areas as it utilizes a significant number of LUTs and FFs.

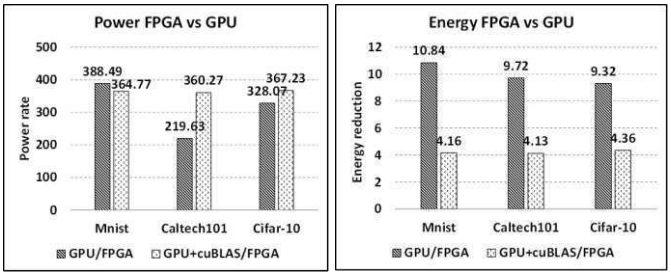

Fig. 5. Power and Energy Comparison between FPGA and GPU

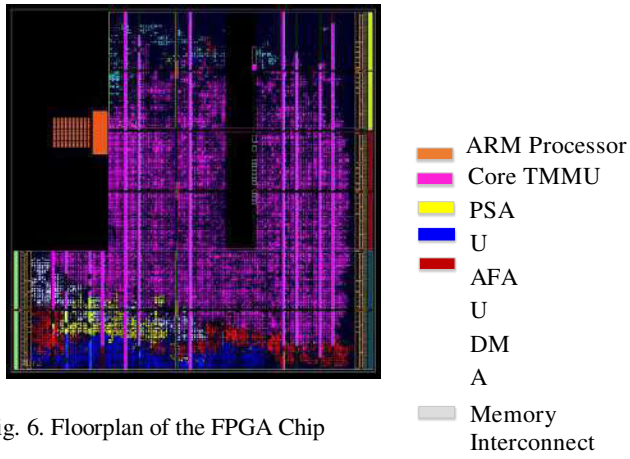

Fig. 6. Floorplan of the FPGA Chip

V. CONCLUSION AND FUTURE WORK

In this article we have presented DLAU, which is a scalable and flexible deep learning accelerator based on FPGA. The DLAU includes three pipelined processing units, which can be reused for large scale neural networks. DLAU uses tile techniques to partition the input node data into smaller sets and compute repeatedly by time-sharing the arithmetic logic. Experimental results on Xilinx FPGA prototype show that DLAU can achieve 36.1x speedup with reasonable hardware cost and low power utilization.

The results are promising but there are still some future directions, including optimization of the weight matrix and memory access. Also the trade-off analysis between FPGA and GPU accelerators is another promising direction for large scale neural networks accelerations.

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Performance analysis of Multilevel Inverter fed AC drive

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Abstract- **Multilevel Inverters are widely used in order to overcome the limitations of two level inverters such as high switching losses at high operating frequencies, ratings of the switching devices, harmonics etc. The unique structure of the multilevel inverters generates high voltages with low stress on switching devices leading to low harmonics. The output of the inverter possess low CMV and THD as it is very close to sinusoidal waveform with increased number of levels at the output. In this work, the CMV and THD are used as performance indicators. The investigation is done for various levels of output voltages such as two, three and five levels, at different operating frequencies such as 30Hz, 40Hz, 50Hz and 60 Hz. The two level, three level and five level inverter fed induction motor drive is simulated using MATLAB .The firing pulses for the switching devices are generated using space vector modulation technique and the CMV and THD are analyzed for various levels of output voltages at different operating frequencies.**

Keywords: CMV, SVM, THD, DCMLI

I. INTRODUCTION

A multilevel structure achieves multilevel of voltage or current at the output by switching its input or output nodes between the various levels of the input. By increasing the number of levels to an infinite value at the output, the harmonic distortion will reach a nearly zero value. On the other hand ,the voltage levels is limited due to problems such as imbalance in voltage, requirements for clamping the voltage, design of the circuit, complexity in control, higher number of components which leads to increased maintenance and capital costs.

The output power can be increased by increasing voltage levels and not the stress on the individual devices. Cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors are the

three basic topological models of multilevel inverters. Fig.1 depicts a basic model of various levels of multilevel inverter where the power electronic devices are replaced by ideal switches. A multilevel inverter is named with the number levels at the output voltage. For example two level inverter will have two levels with respect to the negative terminal of the capacitor at the output and three level possess three levels at the output and so on.

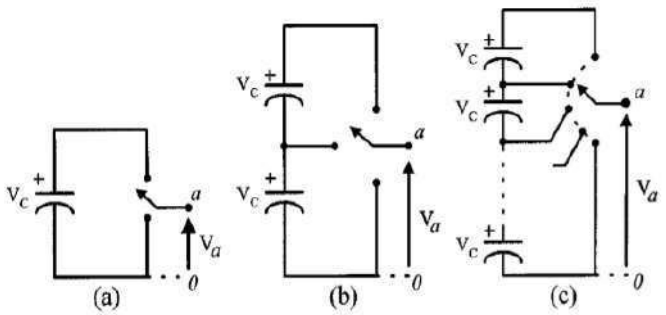

Fig.1 Multilevel Structure (a) two level (b) three level (c) n level

In this research area, the diode clamped structure of multilevel inverter topology has been used due to its benefits such as less component requirement, circuit complexity etc.

II. DIODE CLAMPED MULTILEVEL INVERTER

Among the three basic multilevel topological structures the neutral point clamped structure is preferred because the output levels at the output can be increased easily by using diodes. The clamping diodes help in generation of steps at the output by clamping the DC bus voltage. Nabae, Takahashi, and Akagi in 1981 proposed the basic three level neutral point clamped inverter [1]. In the three-level diode clamped inverter structure two pairs of switches and two diodes are used to generate the three level output. In the switch pairs, one device works in complimentary to the other. The diodes are used to access the neutral point voltage. The input is a common DC bus and the capacitors are used to divide the input for the required number of phases.

The clamping diodes Dc1 and Dc2 reduce the stress due to voltage across each switching devices to Vdc. The voltage across the capacitor is half of the DC link voltage Vdc as the midpoint is regulated at half of the DC link voltage (Vc1=Vc2=Vdc/2).

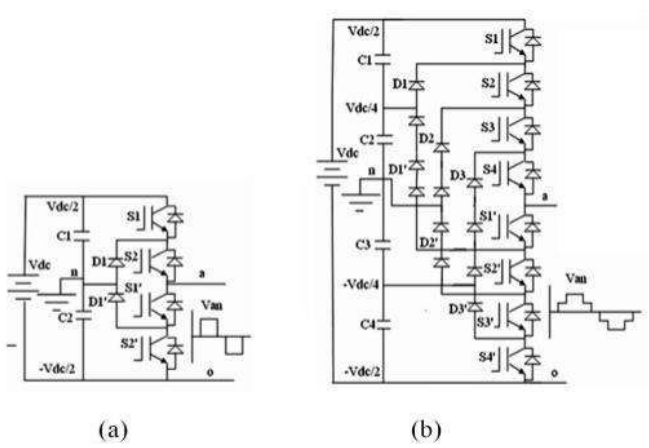

Fig.2 Diode clamped Inverter structure (a) three-level (b) five-level inverter.

For achieving a three level output there are three different possible switching states. The switching states of a three level DCMLI is given .It is obvious that a set of two switches is in ON condition at any given instant for a three level inverter and for five level inverter it is four sets of switches.

Table.1. Switch Status of a 3 level DCMLI

Switch Status	State	Pole Voltage
S_1=ON,S_2=ON S_1'=OFF,S_2'=OFF	S=+ve	V_{ao}=Vdc/2
S_1=OFF,S_2=ON S_1'=ON,S_2'=OFF	S=0	V_{ao}=0
S_1=OFF,S_2=OFF S_1'=ON,S_2'=ON	S=-ve	V_{ao}=-Vdc/2

The line voltage of three level inverter consists of total five levels at the output and five level inverter output consists of nine levels at the output. The line voltage Vab is measured between the phase A and phase B. For a N level DCMLI the output phase voltage is N level and output line voltage is (2N-1) level .The capacitor voltage is given by Vdc/ (N-1) for a N level DCMLI. The clamping diodes used for blocking the reverse voltage are of different ratings even though the voltage to be blocked by each switching device is Vdc.

The component requirements for a N level diode are 2(N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors for each leg. For output to be nearly sinusoidal, the quality of the output is increased by increasing the number of levels at the output. But increasing the number of levels to a higher value is a challenging task as it leads to various problems. There should a tradeoff between the level selection and circuit complexity. So the output of this inverter is a near sinusoidal waveform.

III. SPACE VECTOR MODULATION

The sinusoidal excitation of the motor is represented by a voltage space vector of constant amplitude moving along a circular trajectory. The total 360^0 period is divided

into six steps once in every sixty degrees .The resultant voltage space vector traces a hexagon and achieved using a six-step inverter. The six step inverter introduces low harmonic frequencies which has a great impact on the efficiency of the system. Also the dynamic performance is poor since it has control over the output voltage only at every 60^0 of a 360^0 period. So the PWM scheme provides a superior harmonic spectrum and performance.

IV.PERFORMANCE INDICATORS

A. Common Mode Voltage (CMV)

The common mode voltage is defined as the voltage between the star point of the load to the ground in a multilevel inverter. In the pure three phases balanced sinusoidal voltage the potential between star point and ground will be zero. However in the case of pulse width modulation (PWM) , the inverter is switched from a single input DC voltage source, where it is difficult to make the sum of the 3-phase output voltages equal to zero. Hence the voltage across the star point of stator winding of IM to ground will not be zero.

In case of 3-phase PWM inverter, it is not possible to get the CM voltage zero even for the balanced load. This CM voltage can also be defined as zero sequence voltage. CMV acts like a source for many unwanted Problems in Motor drives such as inducing Shaft voltage, bearing current & associated EMI problems.

B. Total Harmonic Distortion (THD)

The formula for finding THD for output voltage is given below.

$$\text{THDv} = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1}$$

Where “h” is an integer and “V_1” is the voltage at fundamental frequency. The THD is defined as the ratio of the RMS values of signals including harmonics to the signals at the fundamental frequency .The THD calculation is same for both the output current and voltage.

V. SIMULINK MODELS AND ITS RESULTS

The simulation model for two level inverter fed induction motor is shown below. The simulation is simulated using MATLAB Simulink.

A. MATLAB SCOPE AXES DETAILS

Axes 1 to 3:- Inverter block output line voltage.

Axis 4:- Inverter block output phase voltage.

Axis 5:- Inverter block output line current.

Axis 6:- Common mode voltage (CMV).

Axis 7:- Total Harmonic Distortion in line current (THD_C).

Axis 8:- Total Harmonic Distortion in line voltage (THD_V).

Axis 9:- Vector sum of 3 phase currents.

Axis 10:- Common mode current. X-axis represents time and Y-axis represents magnitude.

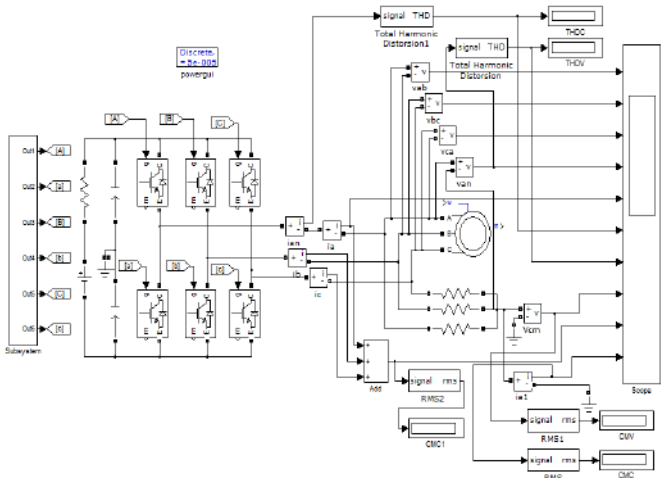

Fig.3 Simulink model of 2 level inverter

5.1 Simulation results of 2 level inverter

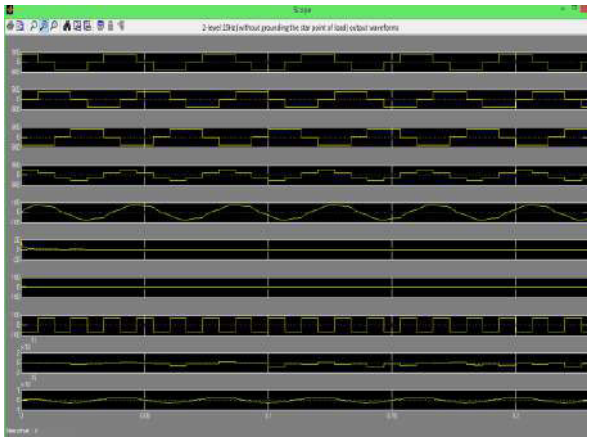

Fig.4 Output for 30 Hz frequency

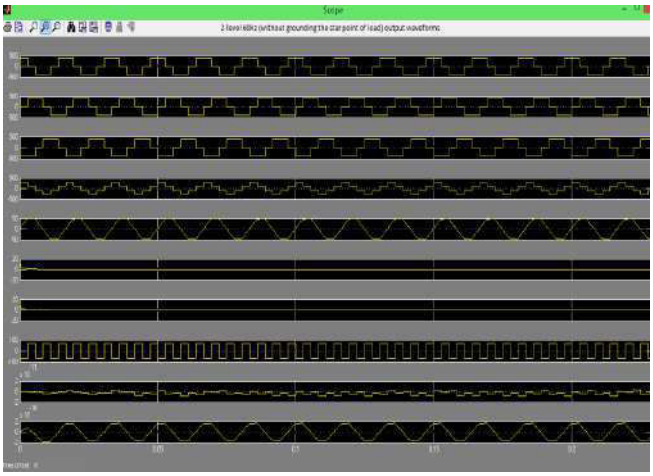

Fig.5 Output for 40 Hz frequency

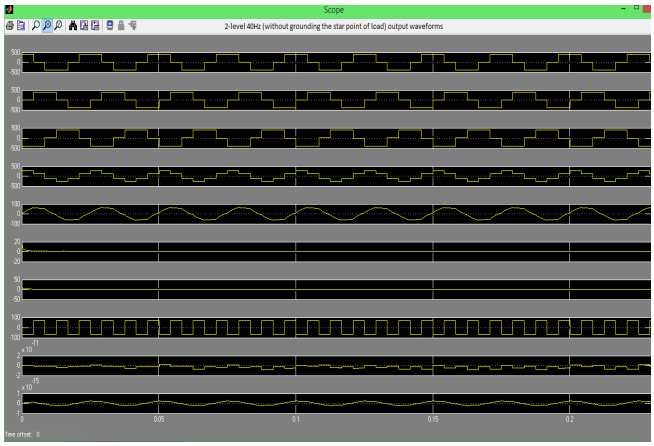

Fig.6 Output for 50 Hz frequency

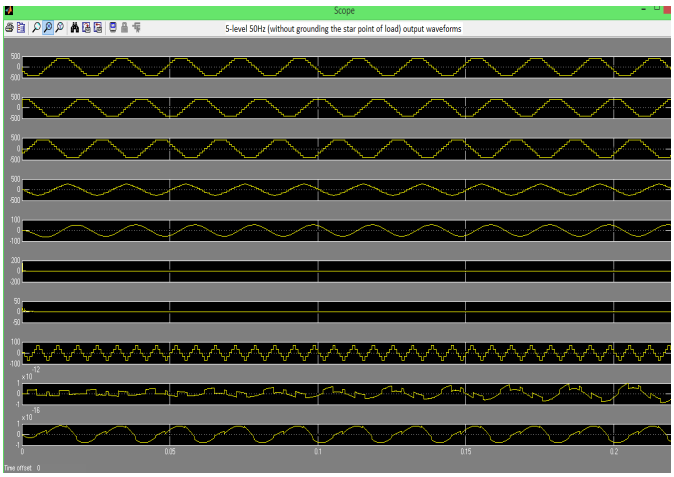

Fig.7 Output for 60 Hz frequency

5.2 Simulink model of 3-Level Inverter

The simulink model for 3-level inverter fed induction motor has been simulated. The model was shown below in the Fig. 8.

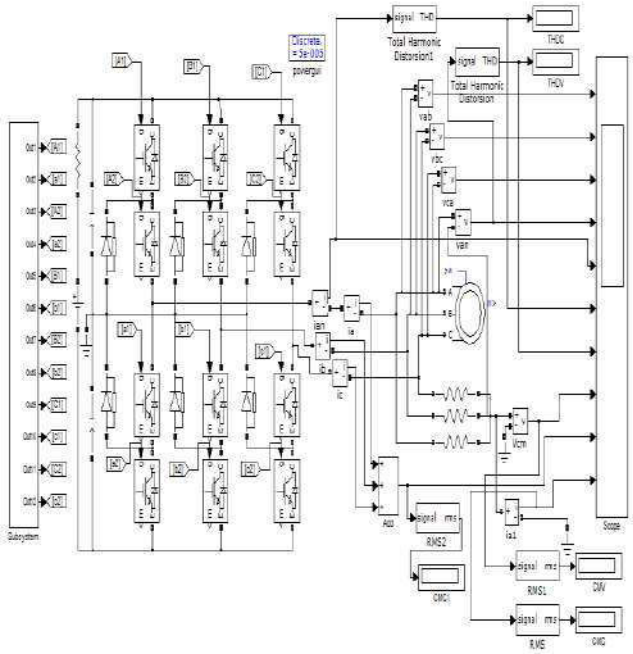

Fig.8 Simulink model of 3 level inverter

A. Simulation results of 3 level Inverter

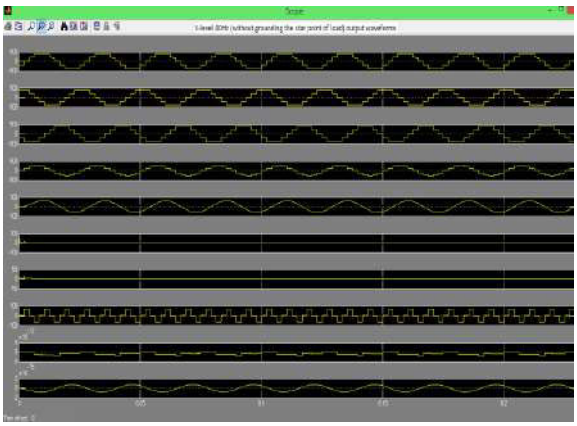

Fig.9 Output for 30 Hz frequency

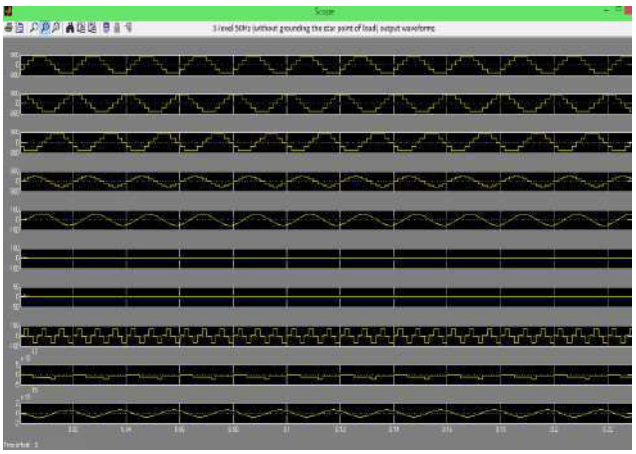

Fig.10 Output for 40 Hz frequency

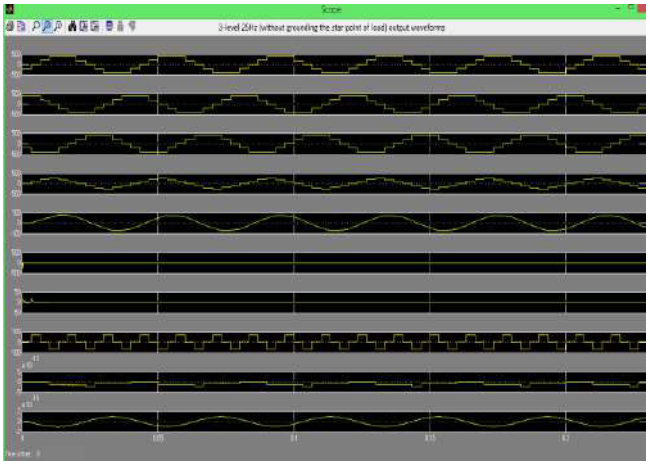

Fig. 11 Output for 50 Hz frequency

Fig. 12 Output for 60 Hz frequency

5.3 Simulation of 5 level inverter

The simulation model and results of five level inverter is given below.

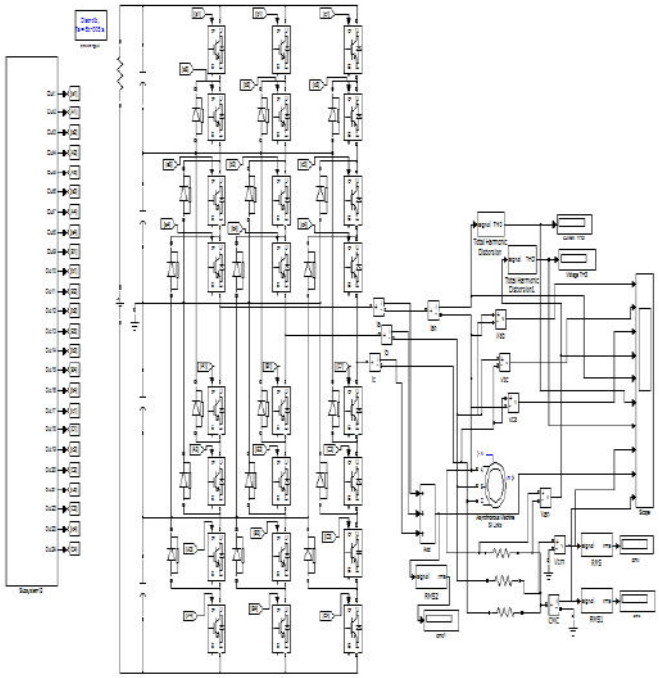

Fig.13 Simulink Model of 5-level inverter

Simulation Results of 5-Level Inverter

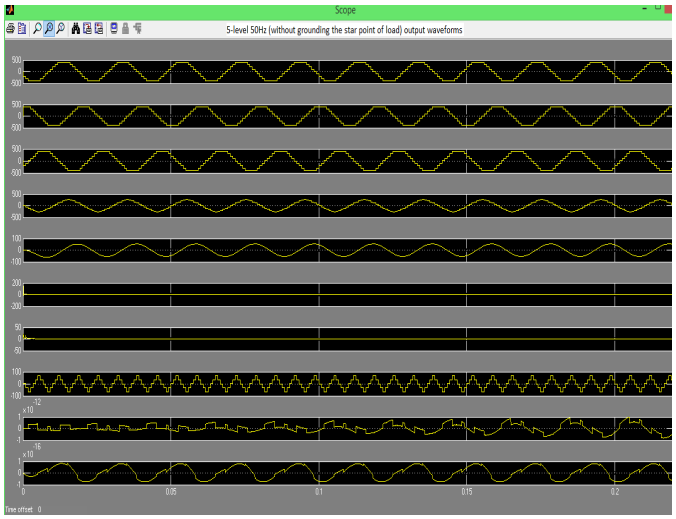

Fig.14 Output for 30 Hz frequency

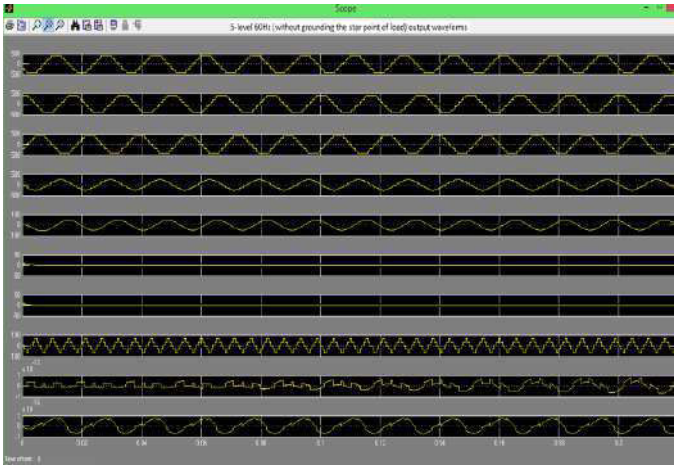

Fig.14 Output for 40 Hz frequency

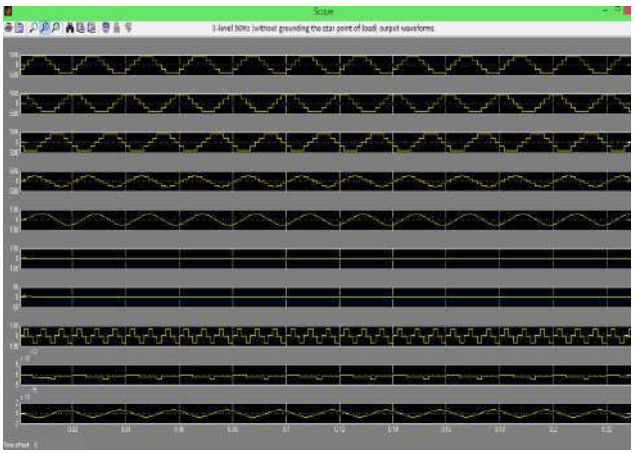

Fig.15 Output for 50 Hz frequency

VI SIMULATION RESULT ASSESSMENT

The values of THDv,THDc,CMV and CMC are listed different frequency values with the star point open .The frequency of operation taken into account was 30,40,50 and 60 Hz respectively.

The inference from the values listed is that the sum of the phase currents and the common mode currents are equal. And also the waveform shows that both the

currents are equal in phase and magnitude. The simulation results can be verified from the experimental studies.

Table: 5.2 Performance parameters (without grounding)

Level of Inverter	Frequency (Hz)	THDc	THDv	CMV (volts)	CMC (Amp)
2 level	30	0.079	0.297	64.55	6.28e-19
	40	0.057	0.312	64.98	6.29e-19
	50	0.049	0.309	65.12	6.32e-19
	60	0.041	0.310	65.32	6.33e-19
3 level	30	0.026	0.158	44.23	5.49e-16
	40	0.021	0.158	44.53	4.59e-16
	50	0.019	0.159	44.71	3.92e-16
	60	0.017	0.156	45.04	3.71e-16
5 level	30	0.012	0.094	35.73	9.55e-17
	40	0.013	0.093	38.96	7.28e-17
	50	0.0123	0.095	39.01	6.23e-17
	60	0.0128	0.094	39.13	5.54e-17

VII CONCLUSION

The Common mode voltage and the Total harmonic distortion is decreased as the levels of the inverter increased. But there is no much change in the above parameters more than three levels. Generally, the industries follow the two level only since for higher levels the complexity in circuits and the number of devices used will be more. The CMV can be reduced by different methods like cancellation methods.

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PROPOSE AND ACHIEVEMENT OF RIGGING ELUSION SCHEME USING EVM

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***Abstract*—Electronic Voting Machine (EVM) is a device that is used to count ballot and record votes instead of doing it manually using human resource to record and count votes. The many problems associated with manual counting of votes that it laborious, erroneous and time consuming. This makes the entire system very inefficient. As voting is a sensitive issue, mis-management can lead to issues as large and complicated as political unrest. The debilitating effect that political unrest can eventually lead to needs no describing. Bangladesh, being a developing nation cannot afford to be held up in its economic development due to mis-management in elections. On the other hand, for a power starved nation like Bangladesh, the gap between demand and supply of electricity remains large. A good majority of the people are deprived of this basic facility. Over-dependency on electronic devices for sensitive purposes might not seem like a viable option either. However, renewable energy based systems can be the solution to tackling such crisis. A solar powered EVM addresses all the above concerns. This paper discusses in detail the design of a solar powered EVM prototype which is efficient and allows the user a relief from the laborious act of vote collection and counting. Furthermore, it also removes the errors from the system, since it is a digital device. One of the biggest concerns of EVM is the security system which includes insider threats, network vulnerability and challenges to auditing. To limit these issues the prototype has been developed with a three stage security encryption.**

Keywords — Electronic Voting Machine, Renewable Energy, Solar Power, Microcontroller

I. INTRODUCTION

Voting is a method for a group such as a meeting or an electorate to make a decision or express an opinion, usually following discussions, debates or election campaigns. Democratic nations elect holders of high office by voting. In a democracy, a government is chosen by voting in an election: a way for an electorate to elect, i.e. choose, among several candidates for rule. In a representative democracy voting is the method by which the electorate appoints its representatives in its government. In a direct democracy, voting is the method by the electorate directly makes decisions, turn bills into laws, etc.

Like a good majority of the nations in the world, Bangladesh follows democracy, making voting an integral part of our everyday lives.

Unfortunately, unlike the developed nations following democracy, political instability is one of the diseases plaguing this country, hindering its economic development. Two years ago, Bangladesh's year started with political turmoil when the opposition party protested, demanding free and fair elections. Even though the results of the elections, through voting, gave the nations its ruling government party, controversy surrounded the election. As a result, the economy is still having to bear the brunt in many ways. Many experts, such as The World Bank, Bangladesh Bank etc. have projected the gross domestic product to be lower than 6% which is much below the target of 7.2% for FY 2014. It is evident that the political instability has contributed to this situation. This nation has suffered prolonged political crisis since its inception.

Needless to mention that election is one of the major causes of the nation's political instability, the voting mechanism being an integral part of the elections. Votes are cast by citizens by a voting system. A voting system consists of a set of rules which must be followed for a vote to be considered valid, and how votes are counted and aggregated to yield a final result.

Different voting systems have different forms for allowing the individual to express his or her vote. In ranked ballot voting system, voted order the list of options from most to least preferred. In range voting, voters rate each option separately on a scale. In plurality voting voters select only one option, while in approval voting they can select as many as they want.

The most commonly practiced system in Bangladesh is plurality voting where the voter cast their votes by marking their choice in a piece of paper and dropping the paper in a sealed box. This leaves a large window for error. Theft of vote is yet another problems that the Bangladeshi Election Committee has to face every election, no matter of whichever scale it be. Because the system is pen and paper based, there stays a big scope for felony. The vote counting is also done manually and this allows room for human error. Due to this mismanagement, the election results are often challenged. The mayhem that follows leads to a nationwide unrest.

Different forms of EVM system using different methodologies has been employed around the world based on their requirements. One of the widely used EVM systems is Diebold AccuVote-TS. In the November 2006 general election, these machines were used in 385 countries representing over 10% registered voters.The machine contains a touch screen accompanied by a card reader which the individual voter possesses after contacting the polling officers. However, although accepted widely, recent analysis shows that the

system contains numerous flaws and should not be used without further improvements. Another interesting mechanism for EVM system is Biometric EVM in which instead of requesting personal identifications or passwords, the system has the ability to detect individual fingerprints, face, retina, DNA etc. of an individual for easy and convenient verification. The objectives of biometric recognition are user convenience, better security and higher efficiency. However, the data acquired by individuals bio-identification through fingerprints and retinal scans might be used for criminal investigations or other purposed without notification which violates the civil right of a citizen.

Moreover, power supply of an EVM system is an important element that needs to be fulfilled properly during an ongoing election. This is a bigger concern mostly in developing countries where power outage is frequent due to load shedding. Without proper power supply to the EVM system, data acquired cannot be authentic and questionable. Keeping the erratic power supply position in many places in different countries, the machines have been designed to run on batteries
[9]. However, it cannot be the ultimate solution since the capacity of the battery is not unlimited which can cease to provide power supply to the EVM machine after a certain period of time. To our knowledge, no solar power based EVM system has been implemented to overcome the abovementioned problem till date.

Electronic Voting Machines (EVM) have been introduced in Bangladesh very recently. It is an electronic device used to record vote automatically. It is a device in which no times is wasted for vote counting. Due to its novice nature a majority of the population is still unaware of it. As its name suggests, the voting machines are run on electricity. Bangladesh being a power starved nation, cannot yet guarantee reliable supply of electricity in its metropolitan cities. It cannot further provide electricity facilities to rural, remote areas. This calls in for the need of such device that is electronic yet does not need to rely entirely on the grid network as its power source.

This paper proposes the design of an Electronic Voting Machine (EVM) that is run through solar power. With the fast depleting fossil fuel reserves, the world is now shifting its focus on reliable, sustainable energy generation: renewable energy based generation. Based on its geographic location, solar is the ideal choice of renewable energy source. A simple microcontroller based, solar powered EVM will allow the Election Commission some respite from the mayhem caused during and after the elections. Furthermore, it will also allow the country to keep pace with the development and achieve the government's dream of a digital Bangladesh.

The primary purpose of this paper is to develop a cost effective secured EVM system incorporated with existing solar power system to provide inexpensive continuous power supply which can be greatly beneficial for a developing country like Bangladesh where power source is infrequent. This paper has been structured as follows: Sections II introduces the concept Electronic Voting Machines (EVM). Section III gives a brief on renewable energy and solar power. Sections IV and V details the system architecture of the EVM machine. Section VI and VII discusses the findings and scope of future work respectively.

II. Electronic Voting Machine (EVM)

The electronic voting technology was introduced to people in 1960. Their first widespread use was in the USA where 7 countries switched to this method for the 1964 presidential election [4]. As the world's dependency increasingly grew on technology, the voting system evolved and adapted with the flow. These days the use of Electronic Voting Machines can be seen across the globe: United States, Canada, Brazil, Australia, United Kingdom among many others. Bangladesh have very recently joined this crowd.

EVMs have been introduced in Bangladesh to modernize the polling process. The features of EVM device includes:

- Vote casting is very easy
- Vote counting and result publishing is almost instantaneous and 100% accurate
- 0% chance of losing data, highly stable memory with 4 backups which can store data up to 100 years
- Vote records are completely safe and confidential
- Even if the device gets damaged, on most cases the device is designed such that vote record can be retrieved
- Reusable and cost effective.

In addition to the above, EVMs are usually equipped with touch screens which can display the information in servile language and has provisions for voting for audio-visual impaired voters. Thus, such features makes voting easier and comfortable for voters with disabilities.

III. Solar Power

A. *Renewable Resources*

Power crisis is one of the major problems plaguing Bangladesh. Being a power starved nation, Bangladesh cannot yet guarantee reliable supply of electricity in its metropolitan cities. It cannot further provide electricity facilities to rural, remote areas. This naturally rules out designing devices like EVMs for sensitive tasks like vote collection entirely or primarily dependent on grid power. This calls in for the need of such device that is electronic yet does not need to rely entirely on the grid network as its power source. It may be mentioned here that the power system in Bangladesh, i.e. power generation, is entirely dependent on fossil fuel based power generation. Fossil fuel reserves are being depleted world-wide and at an even faster rate in this country. The country's government is now actively vying for sustainable alternatives, namely renewable energy sources.

Renewable resources are natural resources which can be replenished with the passage of time either through biological reproduction of other naturally occurring processes. About 16% of the global final energy consumption comes from renewable resources. The share of renewable in electricity

generation is around 19% with 16% of electricity coming from hydroelectricity and 3% from new renewable (wind, solar, geothermal, biofuel and modern biomass) [5].

B. Solar Energy

Among all the renewable resources, solar is the most preferable as it is easily available in nature. In recent time the equipment associated with are accessible at a reasonable cost. However, solar is a dilute source of energy. Compared to the overall power intercepted by Earth, power received per unit area is small; maximum value is about 1000 W/m^2 [5]. Hence to acquire the required quantity of power a large collector area is required. Solar powered electricity generation uses either photovoltaics or heat engines, i.e. concentrated solar power (CSP). CSPs use lenses or mirrors and tracking systems to focus a large area of sunlight into a beam. Photovoltaics convert light into electric current using photovoltaic effect [6].

Renewable energy is a viable means of generating energy in Asia. For solar power, South Asia has the ideal combination of both high solar insolation and a high density of potential customers. Cheap solar power can bring electricity to a major chunk of the sub-continent's people who still live off-grid bypassing the need of installation of expensive grid lines.

In Bangladesh, a number of domestic solar energy systems are in use in houses around the country. The use of solar energy on this scale is highly potential and advantageous as nearly 60% of areas in the country do not have access to main grid electricity. The World Bank is backing a program of making solar energy available to wider population in Bangladesh, as part of the Rural Electrification and Renewable Energy Development Project (REREDP), which subsidizes solar energy systems. The long term average sunshine data indicates that the period of bright sunshine hours in the coastal region of Bangladesh varies from 3 to 11 hours daily. The global radiation stands at 3.8 which indicate that there are good prospects for solar thermal and photovoltaic application in Bangladesh.

C. From Energy to Power

The solar photovoltaic technology is the most commonly used technology for the conversion of solar energy to solar power. A solar cell, also called a photovoltaic cell is an electrical device that converts the energy of light directly into electricity by the photovoltaic effect. It is a form of photovoltaic cell which, when exposed to light, can generate and support an electric current without being attached to any external voltage source. The operation of a photovoltaic (PV) cell requires 3 basic attributes:

- The absorption of light, generating either electron-hole pairs or excitation
- The separation of charge carriers of opposite types.
- The separate extraction of those carriers to an external circuit.

Photovoltaic cells are made up of special materials called semiconductors such as silicon, which is currently and most commonly used. Basically, when light strikes the cell, a certain portion of it is absorbed within the semi-conductor material. This means that the energy of the absorbed light is transferred to the semi-conductor. The energy knocks the electron loose, allowing them to flow freely. A typical photovoltaic system employs solar panels, each comprising of a number of solar cells which generate electrical power.

The power output from a solar cell depends on the area of the cell and the efficiency of the solar cell. The power output of a solar PV cell is a product of cell efficiency in percentage, cell area in square meters and solar insolation.

IV. System Architecture

The circuit diagram of the solar powered Electronic Voting Machine (EVM) is provided below:

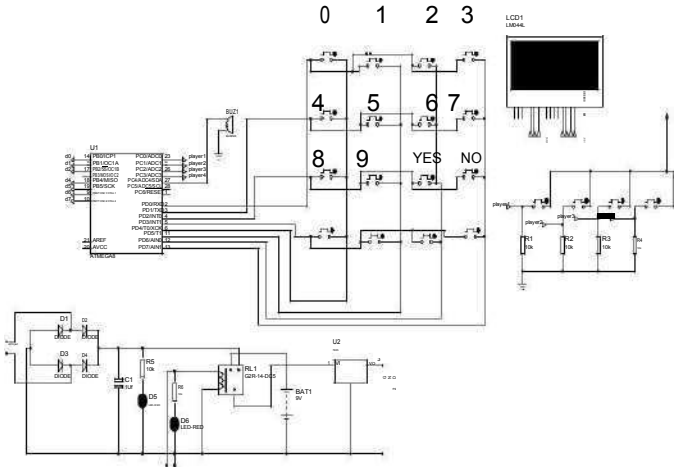

Fig. 1. Circuit design of the Electronic Voting Machine (EVM)

The major component of the EVM is the microcontroller. AVR ATMEGA8 (28 pin) microcontroller has been used in the circuit. Port B was assigned as the output and Ports C & D were the inputs. The output of the microcontroller was connected to the LCD and Buzzer. Rows of keypads were connected to PD0 to PD3 (pins 2, 3, 4 and 5) and columns of keypads were connected to PD4 to PD7 (pins 6, 11, 12 and 13). Buttons for voting were connected to PC0 to PC3 (pins 23, 24, 25 and 26). The LCD screen was connected to Port B. PB0 (pin 14), PB1 (pin 15) and PB2 (pin 16) is connected to RS pin, R/W pin and E (Enable) pin sequentially of the LCD. The reset button was connected to PC6 (pin 1) and PC4 (pin 27) was connected to the buzzer.

The circuit contains a 12V chargeable battery. A voltage regulator (IC7805) was connected to the circuit to maintain a constant 5V at the end of the power supply section. This battery is charged using solar power and to increase reliability is also connected to the grid supply. However, the grid supply is only a back-up source in case there is a failure in the solar powered system due to some technical errors. The 220V/12V step down transformer was used with the grid supply connection as the grid voltage is 220 V. A full bridge rectifier converted was kept in the circuit to convert the AC signal to DC.

The proposed EVM circuit comprises of three major portions:

- Control Section: Control section consists of 2-parts keypad and LCD. The keypads are used for setting and password input whenever password is needed. LCD is necessary for viewing the passwords and whenever author sets them to see whenever any passwords are entered, to see the votes of candidates.
- Ballot Section: Ballot section has buttons for each candidate. By pressing each of the buttons one can give vote to the corresponding candidate
- Power Supply Section: The EVM needs 5V DC to operate. The microcontroller and LCD display needs 5V to turn on.

V. System Implementation

The Electronic Voting Machine (EVM) has three stage password protection system. The 1st and 2nd password is for the operator. 3rd password is highly protected. The length of each password is maximum 10 characters. Here the maximum number of candidates is four. But the number can be increased. Once the system starts the display will show 3 options: 'To Enable Vote', 'To See Vote' and 'Erase Data/Change Password'.

If the operator chooses 'To Enable Vote' he has to give password-1 to continue the voting process. If the password matches, then the voter can give vote to desired candidate. After every successful voting a sound alarm will activate. Every time password-1 has to be entered before voting. If any voter presses two button at a time or within one second, the vote will be considered as invalid vote and the voter has to give his vote again. The process flow is outlined in Figure 2.

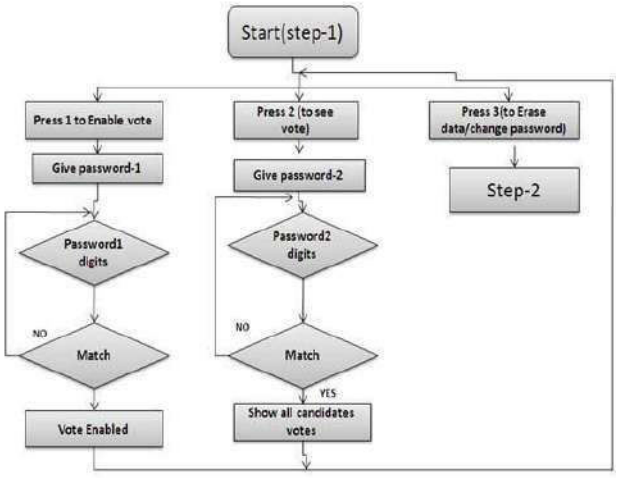

Fig. 2. Flow Chart for Step 1: Enabling Vote

To see the vote, the authority, such as election commission, to enter the 2nd password. If the password matches, then the EVM shall display all the votes cast by the voters through the EVM. If the operator/authority, selects 'Change password or erase all data' then two options will be shown on display. The operator will have to enter password-2 for changing passwords. Then the passwords 1 and 2 can be changed. But password-3 can be changed only after entering password-3. To erase data password-3 has to be entered. If password matches all the data will be cleared and EVM will start from initial step. Figures 3 and 4 illustrate the processes.

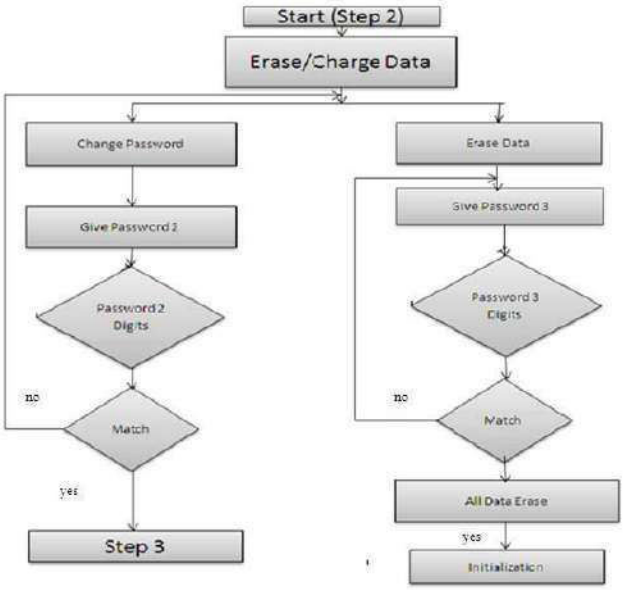

Fig. 3. Flow Chart for Step 2: Viewing Vote

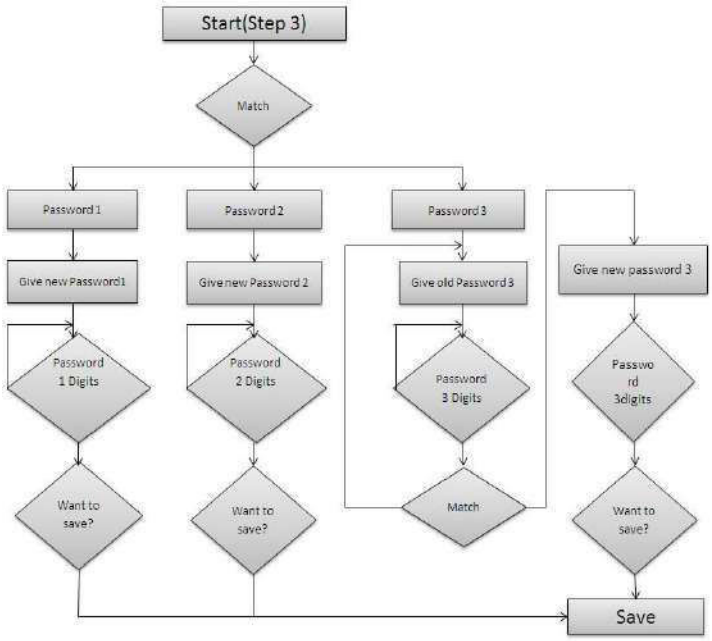

Fig. 4. Flow Chart for Step 3: Erase Data/Change Password

The EVM device, prior to hardware implementation was simulated in Proteus Design Suite, Version 8.0 to check whether it is operational or not. The microcontroller coding was done in C.

The implemented hardware consisted of the ballot unit, control unit and power unit in a single PCB board as shown in figure 5.

Fig. 5. Hardware Implementation

Fig. 6. Four Stages of Implementation

VI. Conclusion

The objective of the project was to introduce a design of an Electronic Voting Machine that uses punch card and password protection. A three level password protection was used in multiple stages. Solar power was used as power source in the circuit to reduce dependency on the grid system. This reduces reduce the manpower requirement for voting purposes. As polling officers are not required for counting votes. This set-up is also very environment friendly as it uses solar power and being digital in nature does not require paper. The vote counting is instant, therefore reducing the delay in publishing the result. As it runs on solar power it can be used in remote locations where there is no access to electricity. Furthermore, due to the voting mechanism being electronic there is a significant reduction in errors. As no human factor is involved in vote collection and counting, there will be almost no scope for fraudulent activity. This will allow and facilitate a peaceful voting environment in the country.

VII. Future Work

There is a vast scope for future work. Further modifications can be introduced to the system. The system could be automated so that every time a paper has been inserted in the ballot, it reads automatically and increases the count to avoid pressing the button every time a paper has been inserted. And also for stringent security purpose, fingerprint system could be implemented so the system avoids multiple counting by the same person. Moreover, by deploying a network based EVM system with the help of internet protocol may avoid people to go to a distance for the purpose of casting vote, rather they could provide vote in the comfort of their home using the internet service.

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A PRACTICAL APPROACH FOR WATER QUALITY MEASUREMENT USING IOT

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ABSTRACT

Nowadays Internet of Things (IoT) and Remote Sensing (RS) structures are used in different locales of research for checking, get-together and examination data from remote zones. In setting of the colossal change in all around present day yield, typical for urban buoy and the over-usage of land and sea resources, the nature of water open to people has disabled gigantically. The high use of excrements in farms what's more heavenly passed on substances in parts, for instance, mining and progression have contributed extraordinarily to the general diminishing of water quality far reaching. Water is a foremost for human survival and along these lines there must be parts set up to vivaciously test water that made open for drinking around the territory city cleared up approaches and what's dynamically the channels, springs and shoreline that join our towns and urban structures. The openness of good quality water is major in butchering scenes of water-borne torments other than redesigning the individual fulfillment. Fiji Islands are worked in the goliath Pacific Ocean which requires a dynamic data gathering framework for the water quality checking and IOT and RS can overhaul the repeating plan estimation. This paper demonstrates an amazing water quality checking structure for Fiji, using IOT and remote unquestionable change.

I. INTRODUCTION

Web of Things is an organized bit of future web and could be portrayed as a dynamic everything considered system structure with self managing cutoff centers in setting of standard and interoperable correspondence traditions where physical and virtual 'things' have characters, physical qualities and virtual identities and utilize sharp interfaces which are immaculately joined into the information facilitate. In the IoT,

'things' are required to wind up incredible individuals in business, data and social structures where they are anchored to take an intrigue and give among themselves and with the earth by exchanging information and data 'saw' about nature, while responding direct to the 'true blue/physical world' occasions and influencing it by running system that trigger activities and make association with or without arrange human intercession. Interfaces as devices strengthen joint undertakings with these 'stunning things' over the Internet, question and change their state and any data related with them, considering security and affirmation issues. The water quality checking is the basic prerequisite for the human life. There are monstrous extents of troubles which cause through the polluted drinking water. The water will be dirtied by the individual, creatures, sad occasions and standard changes. In this way, individuals need to mindful of their own space water bodies conditions. To engage this, a model is proposed to screen water quality in IoT condition.

Remote sensor frameworks (WSNs) have changed into a hot research subject starting late gathering is considered as an achievable procedure to decrease deal with overhead and overhaul flexibility. Remote sensor organize is one of the unavoidable structures which sense our condition through different parameters like warmth, temperature, weight, and so forth. The transmission between the two center centers will keep trade center concentrations to show the refresh throughput and more evident than spatial reuse than remote frameworks to don't have the power controls. Versatile Transmission Power technique to upgrade the Network Life Time in Wireless Sensor Networks utilizing chart hypothesis, we have isolate relationship between's the neighbor center concentrations and furthermore adjacent level related from the closest edges in remote sensor frameworks. A sensor is a contraption that perceives events or changes in aggregates and gives a looking, all things considered as an electrical or optical banner; for instance, a thermocouple changes over temperature to a yield voltage. Regardless, mercury in glass thermometer is in like way a sensor; it changes the consider temperature into expansion and settling of a liquid which can be reviewed on a balanced glass tube. Web of Things (IOT) is the interconnection of abnormally identifiable embedded dealing with contraptions inside the present Internet establishment. Routinely, IOT is depended on to offer moved transparency of devices, systems and affiliations that goes past machine - to-machine trades (M2M) and spreads a collection of traditions, spaces, and applications. The interconnection of these embedded contraptions (checking shrewd articles), is relied upon to exhibit robotization in about all fields,

while in addition empowering moved applications like a Smart Grid.

II. Existing System

Standard strategies for water quality survey intertwine the manual social affair of water test at better places, trailed by examine office clear systems with a particular honest to goodness focus to check the water quality. Those approachs take longer time and never again to be seen as staggering. Notwithstanding the way that the forward and in reverse advancement rationality examinations the physical, compound and steady chiefs, it has a couple of drawbacks: a) poor spatiotemporal inspirations driving concealment, b) it requires work and high intemperate, c) the nonappearance of relentless water quality information to connect with critical decisions for general achievement request. Along these lines, there is a necessity for steady online water quality survey.

III. Proposed System

To crush the above issues our paper plot and build up an immaterial exertion structure for endless checking of the water quality in IoT(Internet of Things) condition. In our arrangement ARM-7 is utilized as an inside controller. The strategy structure utilizes a specific IoT module to get sensor data from ARM7 controller to the beneficial. The sensor data can be seen on the versatile using a remarkable IP address. Moreover, the IoT module besides gives a Wi-Fi to audit the data on versatile.

ARM & ITS ARCHITECTURE

MICROCONTROLLERS

A microcontroller is somewhat, coordinate and frees PC on-a-chip which will be used as an exhibited system. It's a pc on-a-chip moved to direct electrical contraptions. It is prescribed all around for specific errands like a right system. A microcontroller is routinely contracted as μC, or MCU. In like way, a more modest scale controller could be a little extent of a set in structure that is in a general sense a whole card. A settled in system could be a preparing structure predicted that would hold out one or a huge amount of limits over and again with real-time measure limits. It is embedded as fairly a full machine ordinarily check gear and automated parts too.

Points of view of microcontrollers are the 8051, Intel, PIC and Motorola. Microcontrollers that are by and large joined in toys, automobiles, contraptions and workplace machines are gears that amalgamate get-together of constituents of a more humble scale processor structure on an execution chip.

A couple of microcontrollers may utilize four-piece illuminations and work on clock rate frequencies that by and large include:

• A 8 or 16 bit chip

•A minor degree of RAM.

•Programmable PC memory (ROM) and non-capricious cutoff (Flash memory)

• Serial and parallel I/O.

• Timers.

• Analog to Digital and Digital to Analog change

•Programmable PC memory and non-capricious cutoff.

Forms of Microprocessors

Complex Instruction Set Microprocessors:

This kind of chip is furthermore suggested as CISM. CISM depict a little scale processor inside which each and every intrigue will be dead along the edge of an expansive arrangement of low-level cutoff focuses. These cutoff focuses square measure anticipated that would hold out exercises, for instance, moving learning into memory card, re-calling or downloading data from memory card or a rich number juggling figuring an exceedingly single way.

Reduce Instruction Set Microprocessors**:**

Also hinted as diminished course set dealing with, this guessed pace up pc microchips. These chips square measure organized up underneath the strong run draws in the chip to endeavor to a humbler extent of things at between times each interest and this may engage it to complete a basic degree of heading sooner.

Superscalar processors:

These sorts of processors compose the gear on the cut back scale processor so it will perform varying presentation at a practically identical time. These duplicate resources will be submitted number juggling legitimization units or multipliers. Super scalars join distinctive operational units. Superscalar microchips perform in excess of one interest all through one time cycle by then transmittal specific headings to pointless operational units inside the processor.

- **The Application Specific Integrated Circuit (ASIC):**

In like path recommended as ASIC chip is proposed for to a mind blowing degree cure obliges that clearly can fuse auto outpourings affiliation or Personal Digital Assistants PCs. ASICs in some cases is made to specific, in any case may make plant made by making usage of coordinated to-wear gears.

Digital Signal Multiprocessors (DSPs):

DSPs are certain smaller scale processors used to translate and scramble video, or change relationship to automated and the a substitute way. These exercises may require a little scale processor astoundingly mind exploding at completion smart figurings. DSP chips square measure by and large used in resonate sounder, PDAs, RADAR, home execution center sound riggings and affiliation set-top boxes.

How are Microcontrollers absolutely bewildering from microchips?

The closeness between the 2 is that a cut back scale controller merges the options of a chip (ALU, CPU, Registers) along the edge of the nearness of additional characteristics like vicinity of PC memory, RAM, counter, Input/Output ports, et cetera. In spite of what may be ordinary, a microcontroller controls made by a device by using anchored experiences gathered in PC memory that will no change with period.

From an extra purpose for read, the central comparability amidst a standard little processor and a humbler scale controller limiting their space terms is that the locale of their application. Standard microchips like the Intel Core processors or Pentium processors are in PCs as a for the most part working programmable machine. In its age it's to control specific incredibly confusing assignments and errands to such a degree, to the show that that. In capacity a microcontroller of PIC family or 8051 family or the other have seen their applications in unimportant introduced structures, for instance, strategy of action signs or some game-plan of modernized system. Besides these gadgets organize close errand or similar program all through for as long as they can recollect cycle. Another refinement is that the microcontroller generally speaking must regulate minute assignments at any rate paying little respect to what may be common the cut back scale processors in an exceedingly structure possibly won't manage an instantly attempted in the scarcest degree times.

The microcontrollers are depicted per transport width, course set, and memory structure. For a misty family, there are in like route plots with different sources. The classes of microcontroller is showed up in figure, they're depicted by their bits, memory plan, memory/contraptions and bearing set. We should discuss in short concerning it.

Classification in light of Bits

The bits in microcontroller are dealt with into 8-bits, 16-bits and 32-bits microcontroller.

8-Bit Microcontroller-In 8-bit microcontroller inside transport is 8-bit. Right when in-house transport MCU is 8-bit transport then the ALU does the technique for considering and number juggling tries on a PC memory unit at an intrigue. It is 8-bit humbler scale controller. The points of view of 8-bit microcontrollers are 8051, PIC and Motorola families.

16 bit Microcontroller:

A sixteen piece Microcontroller joins a sixteen piece transport and along these lines the ALU performs math and preface hones on the sixteen piece total. It gives more obvious exactness and execution when risen up out of eight piece MCU.

For example eight piece microcontrollers will only use eight bits, activating a last refinement in 0×00 – 0xFF (0-255) for each cycle. In limit, 16 bit microcontrollers with its 16 bit data develop encompasses a move of 0×0000 – 0xFFFF (0-65535) for each cycle. A widened clock most astounding admiration will probably impact be critical in bound applications and circuits. It will mechanically consider 2 sixteen piece numbers. A few perspectives of 16-bit microcontroller square measure 16-bit MCUs square measure widened 8051XA, PIC2x, Intel 8096 and Motorola MC68HC12 families.

32-bit microcontroller:

It uses the 32-bit prologue to do the science and essential organization constrain works out. Right when in-living course of action transport for the bits of learning transmittal works in MCU is 32 transport then the ALU joins out good judgment and math incorporates on total verbalizations of 32 bits on the deals. The MCU is 32-bit humbler scale controller. These give better exactness and execution rose up out of the 16-bit MCUs. those rectangular measure utilized in thusly controlled contraptions and what's more implantable sound devices, engine control structures, workplace machines, devices and exceptional styles of embedded systems. A few models are Atmel 251/Intel family, PIC3x.

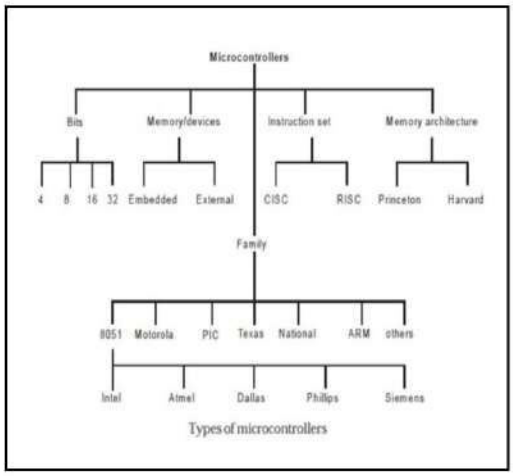

Fig 1 Overview of different types of microcontroller

Classification based on Memory Devices

The memory contraptions are classes into 2 sorts, they are Embedded memory microcontroller: Its includes a microcontroller unit that has all the consider squares open on a chip is named a presented microcontroller. Its mechanical gathering and bundle brought into one unit. Not a ton of or no further fringe unit or structure exists for process all through the association or making utilization of the edges and for example, 8051 having I/O ports, serial correspondence, counters , timekeepers and destructions on the chip is a presented microcontroller.

Outer Memory Microcontroller: Its wraps a microcontroller unit that has not all the consider squares available on a chip, it's proposed as an outside memory microcontroller.Its memory remotely associatedwiththehardware.8031 microcontroller joins of a program memory that is interfaced remotely to that.

ARM Microcontroller:

History

ARM remains for cutting edge reduced heading set managing. ARM began as a dash of Acorn makers of the BCC PC, and beginning at now styles chip for Macintosh iPad. The essential ARM was conveyed in Cambridge University in 1978. The Acorn set PCs share built up the genuine ARM advantageous RISC processor in 1985. ARM was based and have wound up being incredibly distorted up clearly refreshing in 1990.

3. ARM use

The ARM maltreatment over 1980's of the telephones in 2007 and ten billion processors are passed on in 2008. ARM is that the most recent advancement that supplanted by microcontroller and microchips. On an amazingly fundamental level ARM could be a 16 bit/32 bit Processors or Controllers. ARM is heart of the progressed mechanized thing like telephones auto structures moved cameras and private systems connection and remote improvements.

ARM totally startling structures and key choices

V1 (variety):

• Package upsets

• 26-bit address transport

• regulating is fast

V2 (change):
• 26-Bit address transport

• Automatic course to string synchronization

• Co-processor upkeep
V3 (shape):
• 32-Bit tending to

• Multiple information bolster (like thirty two bit=32*32=64).

• Faster than ARM version1 and version2

V4 (arrangement):
• 32-bit address house

• Its help T assortment: sixteen piece THUMB course set

• It maintain M mix: long duplicate recommends that gives a sixty four piece result

V5 (change):
• Improved ARM THUMB interworking

• Its structures for upkeeps CCL heading

• It structures for upkeeps 'E' Type accumulation: enlarged DSP Instruction set

• It structures for upkeeps 'S' Type accumulation: Acceleration of Java PC memory unit code execution

V6 (change):
• Improved memory structure

• Its sponsorships one bearing different learning

Client mode**:** The client mode could be a standard mode; that has scarcest course of action of registers. It doesn't have SPSR and held access to the CPSR. The FIQ and IRQ square measure the 2 square caused systems for the processor. The FIQ is process past miracle and IRQ is defamed intrude. The FIQ mode has additional 5 kept money registers to supply a broad extent of flexibility and common once basic intrudes with square measure managing.
Supervisor mode:

The Supervisor mode is that the bundle interfere with procedure for the processor to fire up or reset. Not well characterized mode. The not well

Version	Family
ARMv1	ARM1
ARMv2	ARM2, ARM3
ARMv3	ARM6, ARM7
ARMv4	Strong ARM, ARM7TDMI, ARM9TDMI
ARMv5	ARM7EJ, ARM9E, ARM10XE
ARMv6	ARM11
ARMv7	Cortex

Fig 2 Different version of ARM Family

AR M architecture

ARM is predicated on decreasing bearing set pc layout; it proposes that the center can't obviously work with the memory. All activities ought to be finished by registers with the finding that is found inside the memory. The endeavor of data and anchoring the motivation back to the memory. ARM includes 37 select sets, 31 broadly profitable registers and 6 are standing registers. The ARM utilizes 7 going out modes that are utilized to track the client assignment

• USER mode
• FIQ mode
• IRQ mode
• SVC mode
• UNDEFINED mode
• ABORT mode
• THUMB mode

Client mode**:** The client mode could be a standard mode; that has scarcest course of action of registers. It doesn't have SPSR and held access to the CPSR. The FIQ and IRQ square measure the 2 square caused systems for the processor. The FIQ is process past miracle and IRQ is defamed intrude. The FIQ mode has additional 5 kept money registers to supply a broad extent of flexibility and common once basic intrudes with square measure managing.
Supervisor mode:

The Supervisor mode is that the bundle interfere with procedure for the processor to fire up or reset. Not well characterized mode. The not well

characterized mode traps silly heading is dead. The ARM center contain 32-bit information transport and speedier learning stream.

THUMB mode:

In THUMB mode the 32-bit of data withdrew into 16-bits and will expand the strategy speed.

A touch of the registers are saved in each mode for particular use by the center. The saved registers are

• SP (stack pointer). • LR (interface enroll).

• Computer (program counter).

• CPSR (current program standing register).

• SPSR (spared program standing register).

INTRODUCTION ABOUT EMBEDDED SYSTEMS

Introduced contraption can be a mix of gear and programming program system won't to pass on the things one specific undertaking. design degree introduced gadget may be a microcontroller-generally based, programming contraption driven, demonstrated, period gadget, self-keeping up, or human or framework standard, in errand on a few essential variables and in a few conditions and offered into an intense and charge really seeing business region.

An introduced contraption isn't a figuring structure that is used in many cases to process, now not a code on workstation or UNIX working device, not an in vogue undertaking or clinical utility. Over the top end introduced and cleave down end embedded structures. High-stop displayed contraption - for the most part thirty two, sixty four Bit Controllers used with OS. Points of view non-open modernized Assistant and PDAs and so forth .lessen finish embedded systems - everything thought about eight, 16 Bit Controllers used with pal degree most reduced being developed structures and device form prepared for the uncommon reason. Models little controllers and contraptions in our strategy for nearness like washer, Microwave Ovens, wherever they're embedded here we should need to discuss the purpose of constrainment of reenactment code, term structures and records getting in interesting examination applications. Out of date exploring particular streets seeing is remarked as "static" testing wherever reliability of portions is investigated by using surrendering apparent data sources and degree yields. These days there's additional stress to request that thing plug speedier and cut back style process lengths.

This has caused a need for "dynamic" testing wherever parts are attempted in any case being utilized with the whole system – either good 'ol fashioned or reenacted. In context of cost and achievement issues, reenacting whatever is left of the contraption with term gear is most absurd all around got the opportunity to testing parts inside the bona fide machine.

The blueprint showed in this slide is that the "V Diagram" it is generally adjusted outline the event cycle. At first advanced to exemplify the appearance approach of code applications, totally sublime diverse separating distinctive decisions modifications of this outline may be found to give a lighting up to excellent thing style cycles. here we have were given demonstrated one event of any such blueprint keeping an eye on the look cycle of embedded control programs standard to auto, part and confinement programs.

For the extent of this chart the last advancement in time of the event ranges is showed up from left to right. Note in any case this can't go without being this is typically this could be constantly A reiterative structure what's progressively the honest to goodness change won't continue unmistakably by systems for these procedures. The aching for snappy advancement is to make this cycle as sensibly viewed as farthest point by system for convincing the emphasess yearned for a game plan. If the deal with rotate of the diagram is perceived of as time, the purpose for existing is basically unbelievably tight the "V" the most totals as potential and along these lines decrease advance time.

The stimulate center motivation behind this outline will be thought of in light of reality the level at that the structure sections are thought of. Favored inside the change, the necessities of the machine must be

thought of. Due to reality the gadget is cut up into sub-structures and segments, the framework changes into horrendously low-degree the detachment obviously down to the illumination behind stacking code onto man or woman processors. After segments are merged and isolated along till such time that the aggregate structure will solidify last collecting looking. As necessities be the unmistakable best of the diagram watches out for the absurd limit structure think about besides the base of the format keeps an eye on a totally low-degree take a gander at. Notes:

- V outline portrays a few uses—got from code change.
- Reason for graph, each bit of style needs a complimentary research standard. Exceptional state to low-level read of use.
- This could be a loosened up adjustment.Loop back/unvaried reasoning, empower center point is time (entire up).

IV. APPLICATIONS:

1. Military and part embedded programming structure applications

2. Correspondence Applications

3. Mechanical robotization and technique affiliation programming structure

Request:

•Real Time Systems.

•RTS is one that must answer events inside with a complete focus on that point.

•A right answers once the dead line may be a wrong answer

RTS Classification:

•Hard Real Time Systems

•Soft Real Time System

Hard Real Time System:

•"Hard" time structures have disagreeably thin sluggishness.

•Example: atomic centrality structure, heart muscle.

Sensitive Real Time System:

•"Soft" time systems have diminished powers on "delay" in any case still should work horrendously quickly and repeatable.

•Example: Railway reservation structure – takes some further seconds the data stays true blue.

Vernaculars Used:

• C

• C++

• Java

• Linux

• Ada

• Assembly

KEIL FEATURES:

•Complete brace for Cortex-R, Cortex-M, ARM7, and ARM9 devices

•µVision4 IDE, debugger, and energy condition

•C/C++ compiler from ARM

•Event and data Trace contraptions for Cortex-M processor-based devices

•Complete Code Coverage data concerning your program's execution

•Execution Profiler and Performance instrument alter program change

•Detailed start-up code abuse the Device information

MICRO CONTROLLER UNIT (LPC 2148)

A PC on-a-chip is in like way a gathering of a little chip which joins the processor focus (CPU), some memory, and I/O (enter/yield) lines, all on one chip. The workstation on-a-chip is known as the pc that is correct that prescribes can be a PC using (one of a kind) microprocessor(s) as its CPUs, in any case the likelihood of the pc is acknowledged to be a microcontroller. A microcontroller is a huge piece of the time saw as a collection of front line method for deduction circuits interweaved on one microchip. This chip is tied down for not as much as particular undertakings. most microcontrollers needn't sit around idly with an enormous extent of a while to be told the as a result of properly programming them,

paying little respect to the way that many, in spite of the way that few of them, that have characteristics, that you may found the opportunity to see before you, consider to expand your first utility.

Along the edge of microcontrollers extending speedier, more moment and unmistakable power in your respect develop they are likewise getting different and assorted choices. Generally, the key model of microcontroller can truly have memory and virtual I/O, at any rate on account of reality the contraption float of relatives creates, stores of and a course of action of pat numbers with variable decisions will be open. On this undertaking we will be inclined to use LPC2148 microcontroller. for abundance social events, we're going while in development to understand a contraption at ranges the family that meets our specs with at any rate outside gadgets, or AN outside yet that can make affixing external devices less bewildering, each to the degree wiring and programming. For different microcontrollers, Programmers will plan exceptionally financially or conceivably in-tried to whatever is left of the application circuit disposing of the need for a substitute circuit. Other than enhancing this intrigue is that the upside of more minor scale controllers mind SRAM and EEPROM for control shop that could allow programming change even as now not taking out the little controller from the mechanical gathering circuit.
BLOCK DIAGRAM & HARDWARE DESCRIPTION

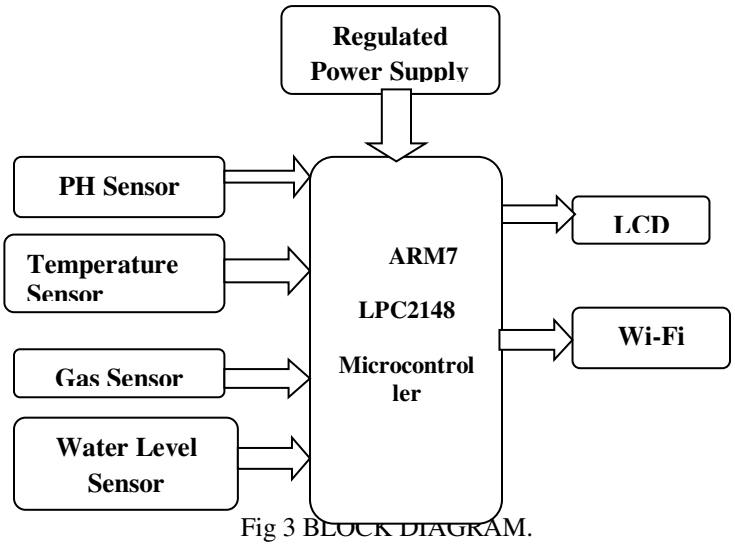

Fig 3 BLOCK DIAGRAM.

V. APPLICATIONS:

1.Used for Dam Gate controlling.

2.Water level recognizable proof reason.

3.Used in Industrial applications and Home applications.

4.For wellbeing division to distinguish the reason of water malady.

5.Aqua culture focuses.

VI. ADVANTAGES:

1.Due to computerization it requires less investment to check the parameters.

2.This is monetarily shoddy for ordinary citizens.

3.Low support.

4.Prevention of water illnesses.

5.Low expense

RESULT, CONCLUSION & FUTURE SCOPE

WORKING DESCRIPTION:

The Water Quality Monitoring System is utilized to assess water. It includes four sensors. Those are Temperature, Ph, Gas, Water level sensors and are connected with the center controller. Here ARM7 controller goes about as an inside controller. The water temperature is seen by utilizing LM35 temperature sensor. Ph sensor is utilized to assess the sharpness of water. Gas sensor is utilized to quantify the gathering of CO2 in parts per million (ppm).Water level sensors measures water level by conveying high recurrent waves at standard time between times. At the information side, the fundamental aggregated information by the sensors is digitized by in-made ADC of ARM7 controller. The gathered information is dealt with and showed up on the LCD screen. Likewise, it transmits the information to the versatile or PC utilizing Wi-Fi, which has momentous IP address. The upside of proposed framework over existing structure is, it is appropriate for more noteworthy allotments. On the off chance that the transmitted information from the sensors beats the required attributes, then it

typically sends message to the minimized in this manner utilizing Wi-Fi.

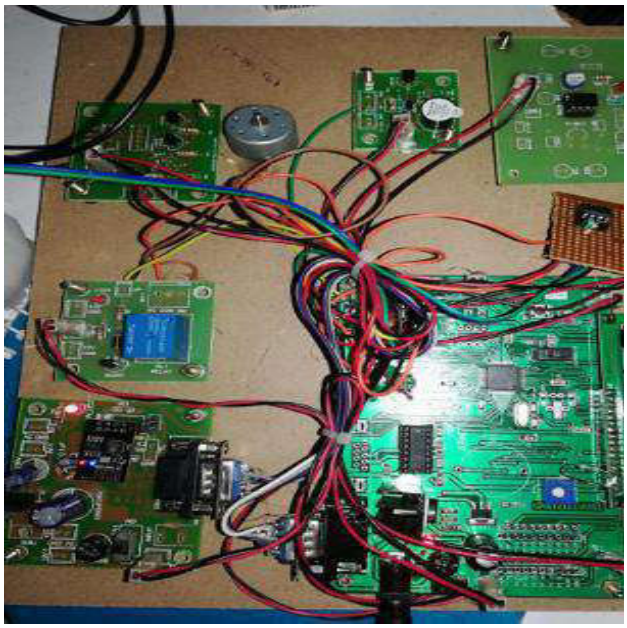

Fig.4. Working model.

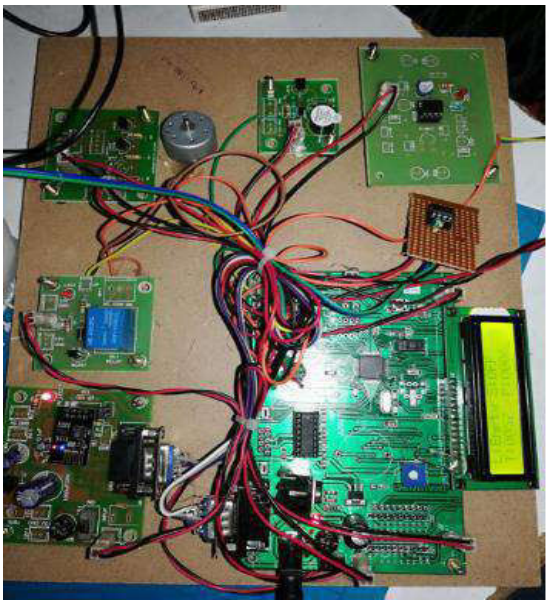

Fig.5 Temperature or gas sensor activated.

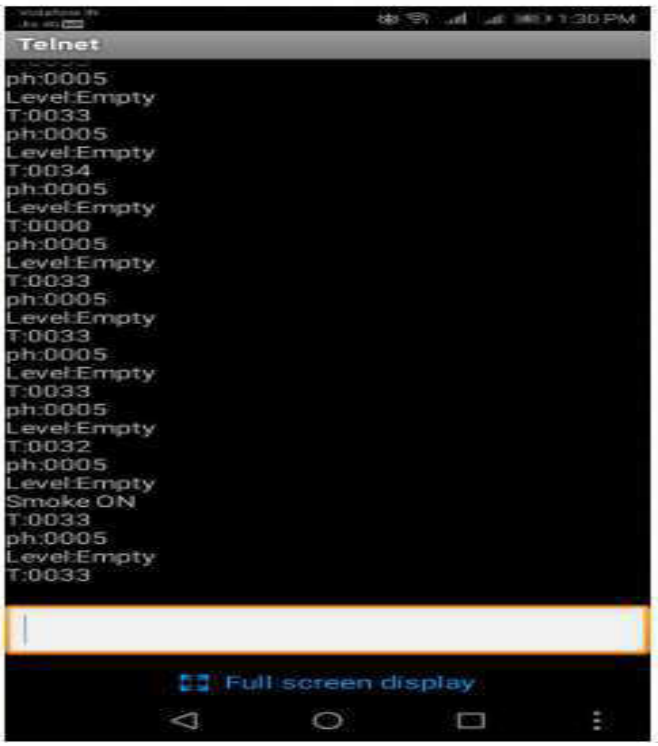

Fig.6. Output results.

VII. CONCLUSION:

Checking of water level, carbon di-oxide(CO2), PH and Temperature of Water makes utilization of water affirmation with novel great position and existing Wi-Fi plan. The structure can screen water quality thusly, and it is low in cost and does not require aces on responsibility. So the water quality testing is most likely going to be more sensible, profitable and speedy. The structure has great adaptability. Just by supplanting the relating sensors and changing the appropriate programming programs, this structure can be utilized to screen other water quality parameters. The development is clear. The structure can be extended to screen hydrologic, air contamination, mechanical and agrarian age and so on. It has wide application and increment respect. By keeping the installed contraptions in the earth for watching attracts self security (i.e., astonishing condition) to nature. To understand, this need to put the sensor contraptions in the earth for social event the information and examination. By putting sensor gadgets in the earth, we can bring the earth into bona fide i.e. it can chat with different difficulties through the system. By then the gathered information and examination results by the sensors will be accessible to the end client through the Wi-Fi.

VIII. FUTURE SCOPE:

In future we use IOT with video preparing for perceiving affirmation thickness of water. Seeing the more parameters for most secure reason. Development the parameters by enlargement of various sensors, by interfacing hand-off we controls the supply of water. This framework could in like way be executed in different present day strategies. The structure can be adjusted by the necessities of the client and can be executed close-by lab view to screen information on PCs.

ACKNOWLEDGMENT

It is with great pressure that we submit this project entitled “A Pratical approach for water quality measurement using IOT .” We take this opportunity to thank those involved directly or indirectly with this project. Without their active co-operation, it would have not been possible to complete this project on time. At the outset, we keep on giving our deep sense of gratitude towards our project guide Mrs.Anitha.P and to Mr. Shiva kumar, Head of Dept. and also Dr. john paul, Principal at Mallareddy College of Engineering. Mrs.Anitha.p, who gave us the guidance right from the initial stage of project and offered us valuable suggestions for developing the project in a systematic and presentable manner.

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THE FinFET TECHNOLOGY

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Abstract: The Integrated Circuit(IC) is become an integral part in all aspects of Industrial growth and modifying Its Characteristics as per updated technology. The semiconductor industries are emerging with new ideas which goes beyond the Moore's law predictions which predicted that "The number of transistor per chip would quadruple for every three years". But this "Physical law" does not hold forever and gave a final conclusion that "another metric will be needed to chosen to allow the future trend to be mapped and predicted". Even the Moore's law was very old Prediction, Most of the industries comparing the its standards with it .Now a days ,Transistor Technology is going towards the low technology node the reason is there is shrinking the transistor size, automatically its driving performance will be improved. So, this paper is discussing on the new proposed technology architectures of Dual gate and tri gate MOSFET.

Keywords*: *Transistors, Bulk MOSFET,FD- Silicon On Insulator(SOI),3DLithiography, High dielectric spacer material/Metal Gate

I.INTRODUCTION

1. History of Transistor

In view of difficulty in Planar CMOS Technology scaling to preserve an acceptable Gate to Channel control Fin FET Multi gate Devices have been proposed as a Technology option For replacing existing Technology. As devices shrink further, the problems with conventional (planar) MOSFETs are on rise. The electronic industries are designing the chip with a perfect logic and finishing up with fabrication verification tests. But , the major concerns lies in the patterning the wafer(Substrate) as per the requirement that The research in technology of Field Effect Transistor has began several centuries ago[1],[2]. Even the name is given as Transistor, several war time efforts was made for the device to show its originality at the times of "developing age" of Technology. Transistor was named as Surface states Triode, Semiconductor Triode, Crystal Triode, Solid Triode and Iotatron prior to the name given as Transistor by John r Pierce. At present , the designing the circuit was made easy by utilizing the resources available to us. So one couldimagine ,how old the roots of transistor Technology is and how many inventions and efforts made by the scientists at those times had still stood behind the Ancient Techniques.

1. Prior to the invention of Transistors, there are
2. Devices existed which are 30-40 years ago before the Transistor was invented.
3. The research in technology of Field Effect Transistor has began several centuries ago.

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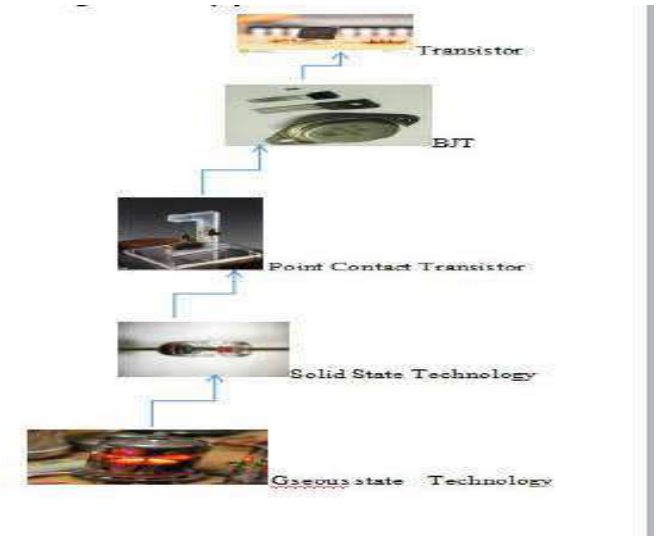

Fig.1. Evolution of Transistor Technologies

At present ,the designing the circuit was made easy by utilizing the resources available to us. So one could imagine how old the roots of transistor Technology is and how many inventions and efforts made by the scientists at those times.

Methods of designing a chip:

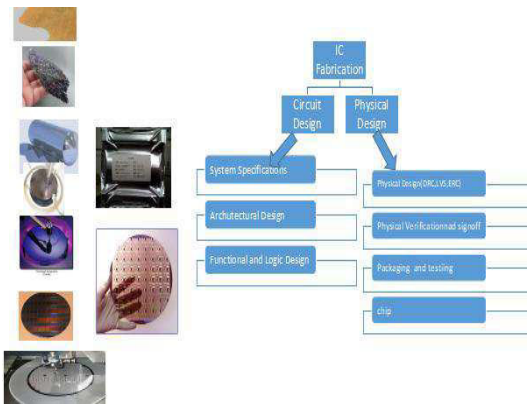

Fig.2. IC Chip Fabrication

A circuit/design which is used in any domain pertained to some common strategies like low cost, high speed ,low power consumption, less heat discippiation, small area. In the scence, what are scaling issues in Bulk MOSFETS and how they are minimized by using accessed technology like Fin FET[3].

They are given by:

1.Short Channel Effect
2.Input Thresh hold voltage
3Leakage current.
4.DIBL & GIBL
5.Hot Carrier Injection(HCI).
6.Thermal stability and
7.Floating Body Effect

II.PROPOSED TECHNOLOGY

In this paper, we are discussing novel device architectures like SOI Tri gate MOSFET with

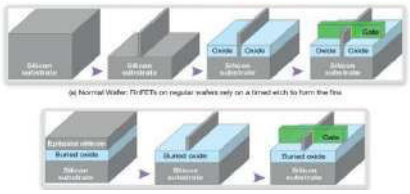

Fig.3. (a).Bulk SOI and Fig(b) Tri gate Fin FETSOI

Electron Beam Lithography:

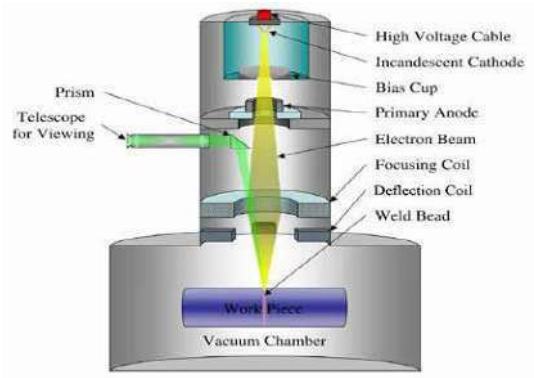

Fig.4.Electron Beam Lithographer

Power Consumption: 50 to 200 kV, 10^4 kW/mm

1.The next generation Extreme Ultraviolet Ray lambda=13nm,but this is not going to intersect with 7nm or 10 nm.But the nodes like 45nm, 32nm, 22nm are convenient for the Industries lithography cost is favourable to them.
2 .But they can't ready to go beyond 22nm.
3 .Now the Question is how the industries print the node that is possible with the given lithography.
4. So that technique is called "double patterning technique" which enables future technology node[4].

Silicon On Insulator(SOI):

Fabrication Method: SIMOX (Separation by implantation ofOxygen).

Process:

FD-SOI, is a planar process technology that delivers the benefits of reduced silicon geometries while actually simplifying the manufacturing process.

1. **Initial Silicon:** Wafer A, Wafer B

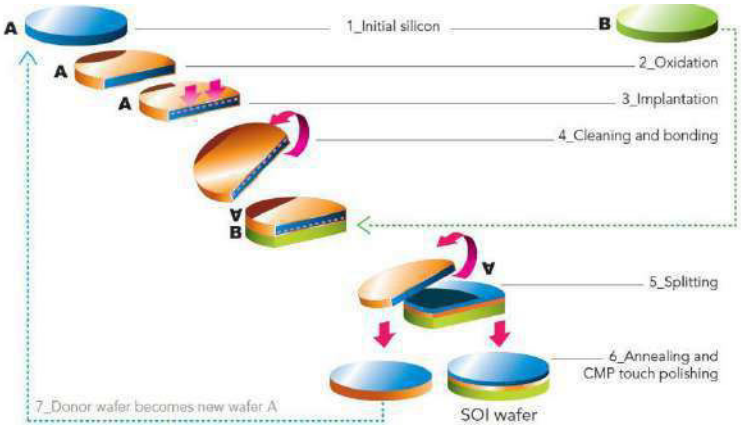

Fig.5.SIMOX method

2. **Oxidation**: Adding molecules, the opposite process to reduction

Substractive Fin Method:

(Etching Silicon into the Fin)

1. Photo Resist material:Silicon Nitride
2. Hard mask: Amorphous Silicon.
3. If we use SiN ,then we don't use top surface of fin for current conduction act as a Bulk Fin FET
4. If we decide to remove Hard Mask, it is commonly forms a Trigate SOI Fin fet

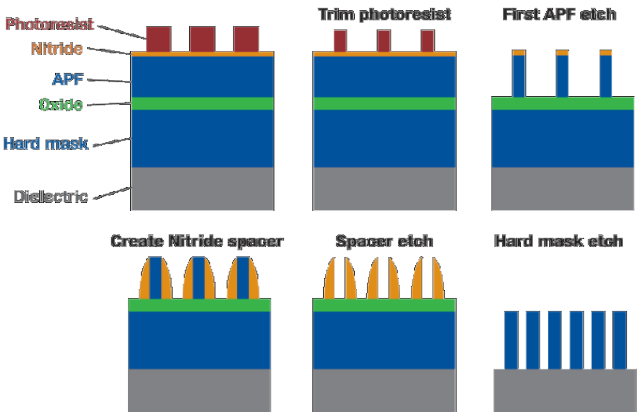

Fig.6. Substractive Fin Method (Etching fin into silicon)

High k, Low k Gate materials/Dual k spacers:

1.Dielectric Constant(k):"It is defined as physical measure of how easily a material can be affected by external electric field"
2.One of the key issues concerning new gate dielectrics is the low crystallization temperature.
3.In planar MOSFETS, we use Sio2 as insulating dielectric.
4.So, we are chosen for other high k dielectric materials to avoid problems like "Thermal Runaway"[5].

Dielectric Classification:

- Dielectric constant of Sio2 is K=3.9.
- High k Materials:"The materials with k>3.9 are called High k materials
- Examples: N(Nickel), Si(silicon), Al(aluminium), Ti(Titanium), Ta and La have been incorporated into the high-k gate dielectrics, especially Hfo2-based oxides
- Low K materials:"The materials with K<3.9 are called Low k materials

Dual K Spacers:

In This paper ,using HFO2/Al2o3 can as dielectric spacer. The reason is given in the

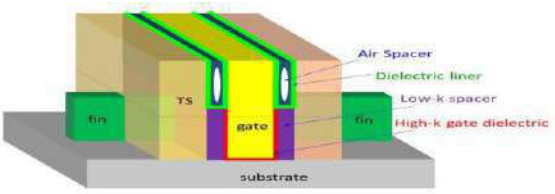

Fig.7. Dielectric and high k gate in Fin FET

The best characteristics of High k material dielectric should have

1. High dielectric constant,
2. large band gap with a favorable band alignment,
3. low interface state density and
4. A good thermal stability.

High k material is of two types:

1.Inner High k Spacer(L sp, h k)=HFO2
2 .Lower High Spacer(L sp, l k)=SiO2

High k spacer HFO2 is introduced for minimizing Tunnelling and for good electric field production then why we introduced l dielectric spacer

Reason:

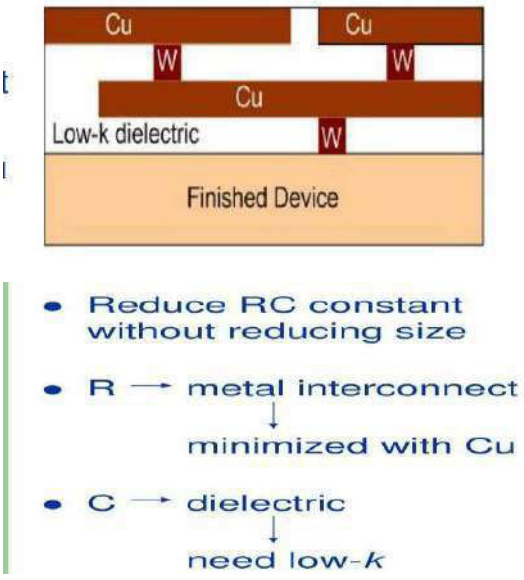

Fig.8.Dual K Spacer

1.Symmetric Dual K Spacer

The devices in which the same apply voltage is applied to Entire device

2. Asymmetric Dual K Spacer:

1. The Devices in which Different Voltage levels can be applied to on a single device

2. Improve the cutoff frequency (f_T)and maximum oscillation frequency (f_{max}) ,given the significant reduction of inner fringe capacitance towards drain side.

3. It is due to the shifting of the drain extension's doping concentration away from The gate edge.

4. Therefore, the asymmetric drain extension Dual-k tri gate Fin FET (AssymmetricDual -k) is a new structure that combines different Dual-k spacers on the source and drain and asymmetric drain extension on a single silicon on insulator (SOI) platform to enhance the almost all analog/RF FOM[6].

Example: FPGA board

The Dual k spacer is an attempt to control lateral spread of the electric electric field at gate sidewalls.

Too high or too low high k dielectric is not a correct choice for alternate gate dielectrics.

Different FinFET Structures:

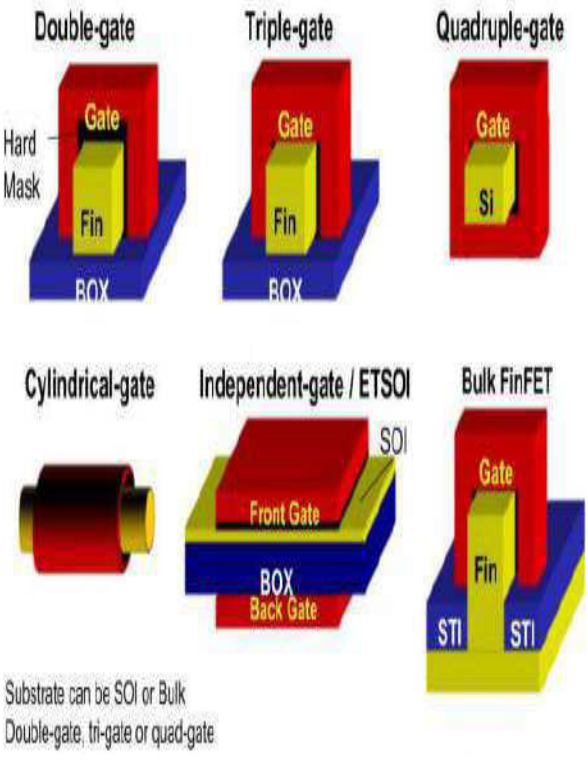

Fig.9. Different FinFET STRUCTURES

TABLE 1. SPECIFICATIONS OF DIELECTRIC SPACERS FOR FinFET:

Zirconium Silicate	12
Hafnium silicate	15
Lanthunum Oxide(La2o3)	20-30
Halfnium Oxide	40
Zirconium Oxide(Zr02)	25
Cesium Oxide (Ce02)	26
Bismuth Silicon Oxide (Bi4Si2o12)	35-75
Titanium Oxide(Tio2)	30

III.GENERAL AND V-I CHARACTERISTICS SOI

Tri gate FinFET:

(a)Sub Threshhold Slope: Sub threshold slope or swing is an important parameter reveals how better the device functions as a switch. The lower the value of SS, the more efficie**nt** and rapid the switching speed of the device from[6] the off state to the on state.

$$S = \frac{dVGS}{d(logIDS)}$$

Sub thresh hold slope=63.7591 m v/Decade

(b)Drain to Source Current (Id sat):

There is an increase in Id sat for SOI TRI-GATE Fin FET

when we use High-k dielectric"

(c)Aspect Ratio (AR) Of Fin:

AR=H fin / w fin

Narrow Fins ensures better SCE immunity.

Reduced Paracitic capacitance.

(d)Fin Width:

LER, Interface roughness varies with W fin, T ox Variation can be larger if Transistor size less than an atom.

(Effects wavelength and pattern Lithiography . Gm decreases with increase in fin width).

(e)Effective Oxide Thickness (EOT):

If Gate thickness is smaller than the dielectric thickness **t**here could be no chance for high leakage current.

$$EOT = TM1\frac{\varepsilon Sio2}{\varepsilon M1} + TM2\frac{\varepsilon Sio2}{\varepsilon M2}$$

TM1 and TM2 are physical Thickness of Metal Oxides M1 and M2.

(f)Drain Source off Current (I off):

One of the biggest challenges faced by MOSFET scaling is high value of off state current or high leakage current resulting in high power consumption. As we use dielectric which can hold sufficient charge which reduces leakage current there by reducing I off current[1].

SOI Tri Gate FinFET(Input Threshhold Voltage)

1.TiN / 1nm
Al2O3/0.8nm Sio2Stack
Vth =0.304175

1. TiN/2nm
HFO2/0.8nm Sio2 Stack
V th =0.309925V
2. Tin/3nm
La2O3/0.8nm Sio2 Stack
Vth = 0.312169V

IV. COMPARISION BETWEEN FDSOI AND FinFET

Characteristics	FD SOI	FinFET on Bulk
Performance Matrics	Better	10 % lower performance
Power Metrics	Betterr	100 mv Higher supply Increased variability
Low Power Features	Ultra Powerful Body Biasing Efficient Multiple Vt	Nobody biasing Low efficiency multiple Vt
Design Compatibility	Easy SOC migration from Bulk	New Technology Implementation
Process Integration	Process Integration is simple	Complex process

V. ADVANTAGES OF FinFET

1. Thresh Hold voltage is controlled without use of heavy doping.
2. Raised Source and Drain on SOI to reduce parasitic capacitance.
3. Good Electro Static Control.
4. The main advantage is Gate burden
5. Over Source and Drain Channels Reduced
6. An ultra thin silicon fin for suppression of ShortChannel Effect.

VI. APPLICATIONS OF ASSYMMETRIC 8T SRAM FinFET

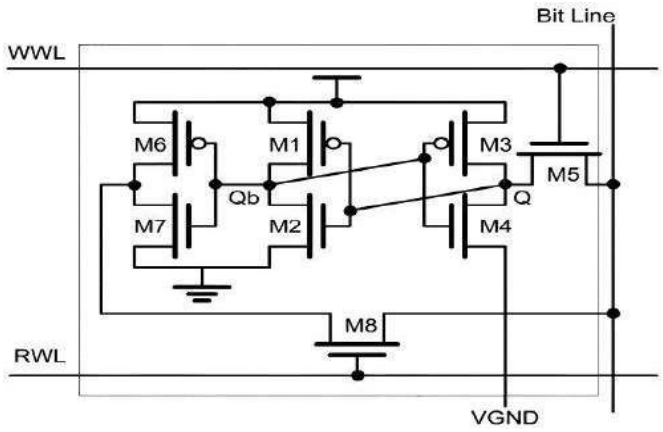

Fig.10. Schematic of a single-ended 8T SRAM cell with asymmetrical cell VGND biasing

SRAM Asymmetric dual structures helps in
1. Maintaining SNM (Static Noise Margin)
2. Adjusting Pull up Ratio Cells Ratio

TABLE2. CONVENTIONAL 6T SRAM AND FinFET SRAM

Parameters	Conventional6 T SRAM		FinFET based 6T SRAM	
	Write	Read	Write	Read
Technology	45n m	45 nm	45 nm	45nm
Supply	700 mv	700 mv	700 mv	700 mv
Leakage Current	69 Amps	55Am ps	69Am ps	53Am ps
Leakage Power	7.3 nW	1.7 W	7.5 nW	1.7 W
Delay	20.57 ns	21.7n s	20.55	21.44 ns

VII. CONCLUSION

The Transistor Technology has efficient even though the devices shape and parameters are changed by different fabrication steps[9]. The Shrinking technology nodes makes Transistor Technologies more beneficial to future generations.

VIII. FUTURE SCOPE

Extending FinFETS

Fin FET are on way to modify its characteristics in form of Carbon Nano Tubes. That means we have Silicon channel in form of Tiny Nano wires.

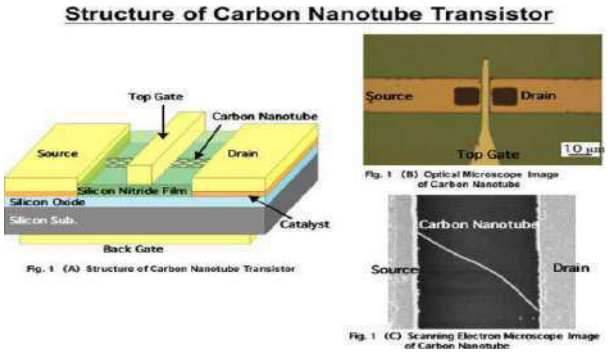

Fig.11. Carbon Nano tube FinFETS

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SUPER ACTIVE MATRIX OLED

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Abstract: **In modern technology, typically use active matrix which contain thin film transistor (TFT's) display. In this TFT's transistor include capacitors that enable individual pixel to active. By using TFT's the active matrix is more efficient then OLED. These active matrices mainly used in mobiles phones i.e., in touch screen for high resolution. But newly Samsung introduced super AMOLED with better brighter screen, low power consumption less sunlight reflection, high resolution and very high-speed refresh rate i.e., speed up the response time. Super AMOLED also called as SAM AMOLED. Samsung adopted diamond PenTile technology for high resolution in mobiles.**

Keywords**: electro luminescence, pixel, pixel per inch, self-emission, thin film transistor.**

I.INTRODUCTION

ACTIVE Matrix Light Emitting diode is a display technology used in mobile as screen. AMOLED describes a specific type of display i.e., thin-film display technology in which organic compounds form the electroluminescent material, and active matrix refers to the technology behind the addressing of pixels. The basic principle behind the working of AMOLED is Electroluminescence. Electroluminescence (EL) is an optical phenomenon and electrical phenomenon in which a material emits light in response to the passage the electric current or by a strong electric field [1]. Electroluminescence is the result of excitation of electrons which releases their energy as photons which produce light [2]. For recombination, electrons and holes may be separated by doping the material to form a p-n junction (in semiconductor electroluminescent devices such as light-emitting diodes) or through excitation by impact of high-energy electrons accelerated by a strong electric field (as with the phosphors in electroluminescent displays) [3]. AMOLED has expresses pure colours when electric current stimulates the relevant pixels. The primary colour matrix is arranged in red, green and blue pixels which are mounted directly to print on board. By using specific colours can improves overall colour contrast. Active-matrix OLEDs (AMOLED) require a thin-film transistor as backplane to switch each and every individual pixel on or off. This layer of organic semiconductor material is situated between two electrodes. Generally, at least one of these electrodes is transparent. AMOLED used in mobiles phones, media players and digital cameras [5]. OLEDs are light weight, durable, power efficient and ideal for portable applications. According to Samsung, Super AMOLED reflects one-fifth as much sunlight as the first-generation AMOLED. Super AMOLED is part of the Pen tile matrix family, sometimes abbreviated as SAMOLED [6][7].

II.EXISTING METHOD

Super-AMOLED (Active-Matrix Organic Light-Emitting Diode) displays are AMOLED displays for mobile devices (such as smartphones, wearables) with an integrated touch function. Samsung's latest Super AMOLED displays adopt a new sub pixel arrangement called Diamond shaped Pixel by replacing the previous PenTile scheme. Modern PenTile OLED displays reach very high pixel densities Samsung are using PenTile for high-resolution (over 230 pixels per inch) OLED. In 2012, AMOLED technology used in mobiles, tv screen display and digital display cameras with low power. AMOLED display contains OLED pixel to generate light by integrated on a thin film transistor (TFT)array which controls electric flowing to each individual pixel. These TFT black plane technologies are polycrystalline silicon and andamorphase silicon are used in AMOLED's. The first EL introduced by pope and coworker in 1963 from an organic molecule, anthracene and its thickness 10μm -5mm when a bias of several hundred volts was applied across it. P. S. Vincent achieved bright blue EL from vacuum which was deposited by 0.6μm thickness and its anthracene crystal films applied with bias of less than 100V. The breakthrough was achieved by Tang and VanSlykein 1987, he made a bilayer structure by using thermally evaporating with the small molecular weight organic materials. In 1989, Tang developed a laser-dye doped Alq3multilayer structure, in which the fluorescent efficiency was increased and the emission color varied from the original green to the dopant emission color. As of 2008, AMOLED technology was used as screen in mobile phones, media players and digital cameras and they continued to make progress for low-power, low-cost. Super-AMOLED displays are AMOLED displays for mobile devices (such as smartphones, wearables) with an integrated touch function. Samsung's latest Super AMOLED displays adopt a new sub pixel arrangement called Diamond shaped Pixel by replacing the previous PenTile scheme. Modern PenTile OLED displays reach very high pixel densities Samsung are using PenTile for high-resolution (over 230 pixels per inch) OLED. In January, it was reported that Samsung will adopt a new sub pixel scheme that uses diamond sub-pixels.

III.PROPOSED METHOD

Super AMOLED is Samsung's own version of AMOLED display which is enhanced for a better output [9]. With Super AMOLED display, a phone can be thinner, consume less battery and offer higher contrast and better touch sensitivity among other benefits. Super-AMOLED is identical to AMOLED. Thus, these two technologies are same but there is only one difference in the layer that detects touch called the digitizer or also known capacitive touchscreen layer. SAM AMOLED is embedded directly

into the screen, whereas the entirely separate layer in AMOLED display i.e., on top of the screen [3].

Super-AMOLED displays carry many benefits over AMOLED displays because of the way these layers are designed:

- The device is thinner because the technologies for display and touch are on the same layer.
- Higher contrast, plus the lack of an air gap between the digitizer and the actual screen, yield a crisper with more high vivid display.
- Less power supply is needed for Super-AMOLED screen because it doesn't generate heat as much older screen technologies. This is due to because the pixels are turned on and off directly therefore not emitting light using power when displaying black.
- The screen is more sensitive to touch.
- Because of many layers light reflection is reduced it makes reading outdoors in bright light easier.
- A higher refresh rate helps to speed up the response time.

PenTile Technology

PenTile (pen means five) matrix is a family of patented sub-pixel matrix schemes used in electronic device displays and also PenTile is a trademark of Samsung. These subpixel are embedded in the display driver, allowing plug and play compatibility with conventional RGB (Red-Green-Blue) stripe panels. The blue sub-pixel is lower luminous efficiency than the red and green sub-pixels. so, the blue sub-pixels need high current which results faster degradation compared to the red and green sub-pixels. By using PenTile layout can reduces the number of sub-pixels which are needed to create a specified resolution. Most PenTile displays uses rectangular grids of alternating green and blue/red pixels. But now Samsung using Diamond Pixel which will give high resolution. In a Diamond Pixel display, there are twice as many green sub-pixels as there are blue and red ones, and the green sub-pixels are oval and small while the red and blue ones are diamond-shaped and larger (the blue sub-pixel is slightly larger than the red one). The diamond shapes were chosen because the sub-pixel packed maximum to achieve the highest possible PPI. The greens are oval shaped because they are squeezed between the larger red and blue ones because green is most efficient OLED emitter when compared to blue which has shortest lifetime.

TFT and SUPER AMOLED:

TFT (Thin Film Transistor) is used in displays in AMOLED. Super AMOLED technology is more expensive and is used only in high-end flagships, offering a number of benefits. This display technology is more bright and vivid colours and also great battery efficiency with wide viewing angles when lighter displays. Each pixel in the display brighter with less power because it doesn't generate as much heat as older screen technologies. The screen is more sensitive to touch and light reflection is reduced because there aren't as many layers, which makes reading outdoors in bright light easier and also addresses the formers' sunlight reflection downside by lowering it to 80%. In effect, it produces brighter and more vivid display regardless of external light intensity[1].

TABLE 1. COMPARISON OF PARAMETERS

Display technique	OLED	AMOLE	SAM AMOLED
Technological type	Self-emission of light	Self-emission of light	Self-emission of light
Resolution	4,800 x 3,840	720 x 1280 pixels	1080*2220
Viewing angle	Good	V good	Super good
PPI	1,443PPI	16:9 ratio	18.5:9 ratio (441 PPI)
refresh rate	120Hz	Medium	Higher than AMOLED

IV.ADVANTAGES AND DISADVANTAGES

- Faster: SAM AMOLED has much better response time than other displays. So, these screens provide us better user experience. By this advantage SAM AMOLED screens in mobile phones
- **High contrast ratio:** High contrast ratio is another advantage of SAM AMOLED
- Overall display quality: With deep blacks combined with high contrast then the images displayed on panel are brighter and more vivid than other display techniques.
- Large Viewing Angle: Viewing angle is always problem in flat screens but by using SAM AMOLED displays, viewing angle is large than 170 degree because they produce their own light to increases their viewing angle.
- Flexible: Today we are getting displays which can bend. This is possible only through SAM AMOLED screens.
- Durability: Another advantage of SAM AMOLED is that it is more durable than traditional screens. Their chance of getting broken is comparatively less to LCD screens and other displays.
- Good for Eyes: SAM AMOLEDs are eye smoothening. These screens provide better viewing experience because they have high contrast, brightness and color aspects.

DISADVANTAGES

- Cost is more

V.APPLICATIONS

- The SAM AMOLED are basically used in the touch screens of mobile phones and also used in computers, netbooks, tablet pc.
- AMOLED technology is already made near to eye display like "virtual images" When projected on a head mounted or helmet mounted display, such image appears like an image in a movie theatre or on a computer monitor, but these are very small display near to the eye. Such an image displayed with very high resolution and contract.
- These are used as flat screens in television[2].

VI.CONCLUSION

Super Active matrix organic light-emitting diode displays have been considered as potential for the next generation. The flat panel displays of SAM AMOLED in providing wider viewing angle, larger colour gamut by using PenTile technology. These efficiently used in mobile displays. SAM AMOLED continues to make progress towards low power. The screen is more sensitive to touch and higher refresh rate helps speed up the response time.

VII. FUTURE SCOPE

Samsung is doing best and developing several next generation display technologies based on OLEDs for display in mobiles, television screen and tab etc. Now Samsung has been developing a foldable OLED device for a long time which may dramatically change in market. The display screen is more sensitive to touch with high resolution. Samsung currently putting a fingerprint sensor, speaker (Sound on Display) and also Haptic capabilities. That increased speed makes ideal for larger, with higher definition display.

Fig.1. Future display of foldable OLED device

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DESIGN OF POWER AND AREA EFFICIENT APPROXIMATE MULTIPLIERS

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Abstract- **Inferred preparing can decrease the arrangement multifaceted nature with an extension in execution and power profitability for screw up adaptable applications The proposed gauge is utilized in two varieties of 16-bit multipliers. Mix results reveal that two proposed multipliers achieve control save assets of 72% and 38%, separately, appeared differently in relation to a right multiplier. They have better precision when diverged from existing estimated multipliers. Mean relative botch figures are as low as 7.6% and 0.02% for the proposed assessed multipliers, which are better than the past works. Execution of the proposed multipliers is surveyed with a photo planning application, where one of the proposed models achieves the most astonishing zenith banner to clatter extent.**

Keywords**: Approximate computing, error analysis, low error, low power, multipliers.**

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I.INTRODUCTION

In applications like multimedia signal processing and data mining which can tolerate error, exact computing units are not always necessary. Research on approximate computing for error tolerant applications is on the rise. Adders and multipliers form the key components in these applications. In [1], approximate full adders are proposed at transistor level and they are utilized in digital signal processing applications. Their proposed full adders are used in accumulation of partial products in multipliers .To reduce hardware complexity of multipliers, truncation is widely employed in fixed-width multiplier designs. Then a constant or variable correction term is added to compensate for the quantization error introduced by the truncated part [2], [3]. Approximation techniques in multipliers focus on accumulation of partial products, which is crucial in terms of power consumption. Broken array multiplier is implemented in [4], where the least significant bits of inputs are truncated, while forming partial products to reduce hardware complexity. The proposed multiplier in [4] saves few adder circuits in partial product accumulation. In [5], two designs of approximate 4-2 compressors are presented and used in partial product reduction tree of four variants of 8 × 8 added multiplier. The major drawback of the proposed compressors in [5] is that they give nonzero output for zero valued inputs, which largely affects the mean relative error (MRE) as discussed later. f overcomes the existing drawback. This leads to better precision. In , inaccurate counter design has been proposed for use in power efficient Wallace tree multiplier. A new approximate adder is presented in [10] which is utilized for partial product accumulation of the multiplier. For 16-bit approximate multiplier in [10], 26% of reduction in power is accomplished compared to exact multiplier. Approximation of 8-bit Wallace tree multiplier voltage over-scaling (VOS) is discussed in [11]. Lowering Bleading to error. Previous works on logic complexity reduction focus on straightforward application of approximate adders and compressors to the partial products. In this brief, the partial products are altered to introduce terms with different probabilities. Probability statistics of the altered partial products are analyzed, which is followed systematic approximation. Simplified arithmetic units (half-adder, full-adder, and 4-2 compressor) are proposed for approximation. The arithmetic units are not only reduced in complexity, but care is also taken that error value is maintained low. While systemic approximation helps in achieving better accuracy, reduced logic complexity of approximate arithmetic units consumes less power and area. The proposed multipliers outperforms the existing multiplier designs in terms of area, power, and error, and achieves better peak signal to noise ratio (PSNR) values in image processing application. Error distance (ED) can be defined as the arithmetic distance between a correct output and approximate output for a given input. In [12], approximate adders are evaluated and normalized ED (NED) is proposed as nearly invariant metric independent of the size of the approximate circuit. Also, traditional error analysis, MRE is found for existing and proposed multiplier designs. The rest of this brief is organized as follows. Section II details the proposed architecture. Section III provides extensive result analysis of design and error metrics of the proposed and existing approximate multipliers. The proposed multipliers are utilized in image processing application.

II.EXISTING METHOD

In applications like sight and sound banner getting ready and data mining which can persevere through error, remedy figuring units are not continually major. They can be supplanted with their construed accomplices. Research on deduced enlisting for screw up tolerant applications is on the rising. Adders and multipliers outline the key fragments in these applications. In [1], inaccurate full adders are proposed at transistor level and they are utilized in cutting edge signal taking care of utilizations. Their proposed full adders are used in social affair of deficient things in multipliers. To diminish hardware multifaceted design of multipliers, truncation is comprehensively used in settled width multiplier designs.

Disdvantages of existing system are given underneath

- More Logic multifaceted nature
- More power and more deferral

III. PROPOSED ARCHITECTURE

Implementation of multiplier comprises three steps: generation of partial products, partial products reduction tree, and finally, a vector merge addition to produce final product from the sum and carry rows generated from the reduction tree. Second step consumes more power. In this brief, approximation is applied in reduction tree stage. A 8-bit unsigned1 multiplier is used for illustration to describe the proposed method in approximation of multipliers. Consider two 8-bit unsigned input operands α = _7 m=0 $\alpha m2m$ and β = _7n =0 $\beta n2n$. The partial product $am,n = \alpha m \cdot \beta n$ in Fig. 1 is the result of AND operation between the bits of αm and βn.1The proposed approximate technique can be applied to signed multiplication including Booth multipliers as well, except it is not applied to sign extension bits.

.

Fig. 1. Transformation of generated partial products into altered partial products

TABLE 1. PROBABILITY STATISTICS OF GENERATE SIGNALS

M	Probability Of The Generate Elements Being				Perr
	All Zero	One 1	Two 1's	Three 1's And More	
2	0.8789	0.1172	0.0039	-	0.00390
3	0.8240	0.1648	0.0110	0.00024	0.01124
4	0.7725	0.2060	0.0206	0.00093	0.02153

From statistical point of view, the partial product *am, n* has a probability of 1/4 of being 1. In the columns containing more than three partial products, the partial products *am ,n* and *an, m* are combined to form *propogate* and *generate* signals as given in (1). The resulting *propogate* and *generate* signals form altered partial products *pm ,n* and *gm, n*. From column 3 with weight 23 to column 11 with weight 211, the partial products *am ,n* and *an, m* are replaced by altered partial products *pm ,n* and *gm ,n*. The original and transformed partial product matrices are shown in Fig. 1

$$pm,n = am,n + an,m$$
$$gm,n = am,n \cdot an,m.$$

The probability of the altered partial product *gm,n* being one is 1/16, which is significantly lower than 1/4 of *am,n*. The probability of altered partial product *pm,n* being one is 1/16 + 3/16 + 3/16 = 7/16, which is higher than *gm,n*. These factors are considered, while applying approximation to the altered partial product matrix

A. Approximation of Altered Partial Products gm,n

The accumulation of *generate* signals is done column wise. As each element has a probability of 1/16 of being one, two elements being 1 in the same column even decreases. For example, in a column with 4 *generate* signals, probability of all numbers being 0 is $(1 - pr)4$, only one element being one is $4pr(1 - pr)3$, the probability of two elements being one in the column is $6pr2(1 - pr)2$, three ones is $4pr3(1-pr)$ and probability of all elements being 1 is $pr4$, where *pr* is 1/16. The probability statistics for a number of *generate* elements *m* in each column are given in Table I. Based on Table I, elements in the altered partial product matrix provides exact result in most of the cases. The probability of error (*Perr*) while using OR gate for reduction of *generate* signals in each column is also listed in Table I. As can be seen, the probability of misprediction is very low. As the number of *generate* signals increases, the error probability increases linearly. However, the value of error also rises. To prevent this, the maximum number of using OR gate in the accumulation of column wise *generate* signals to be grouped by OR gate is kept at 4. For a column having *m generate* signals, $\_m/4\_$ OR gates are used.

TABLE 2. TRUTH TABLE OF APPROXIMATE HALF ADDER

Inputs		Exact Outputs		Approximate Outputs		Absolute Difference
X1	X2	CARRY	SUM	CARRY	SUM	
0	O	0	0	0	0	0
0	1	0	1	0	1	0
1	0	0	1	0	1	0
1	1	1	0	1	1	1

TABLE 3. TRUTH TABLE OF APPROXIMATE FULL ADDER

Inputs			Exact Outputs		Approximate Outputs		Absolute Difference
X1	X2	X3	Carry	Sum	Carry	Sum	
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	1	1	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	1	1	1	0	1

B. Approximation of Other Partial Products

The storing up of other midway things with probability ¼ for am,n and 7/16 for pm,n uses deduced circuits. Assessed half-snake, full-snake, and 4-2 blower are proposed for their social event. Carr y and Sum are two yields of these assessed circuits. Since Carr y has higher weight of matched piece, bungle in Carry bit will contribute more by making botch qualification of two in the yield. Figure is managed with the goal that the aggregate difference between real yield and induced yield is always kept up as one. In this way Carr y yields are approximated

only for the cases, where Sum is approximated. In adders and blowers, XOR entryways tend to add to high district and delay. For approximating half-wind, XOR passage of Sum is supplanted with OR entryway as given in (2). This results in a solitary bumble in the Sum figuring as found as a general rule table of estimated half-snake in Table II. A tick check implies that inferred yield matches with reconsider yield and cross stamp implies jumble

Entire = x1 + x2
Carr y = x1 · x2. (2)

In t he gauge of full-snake, one of the two XOR gateways is supplanted with OR entryway in Sum calculation. This results in botch in last two cases out of eight cases. Carr y is balanced as in (3) displaying one goof. This gives more revisions, while keeping up the qualification among exceptional and evaluated a motivator as one. Reality table of harsh full-wind is given in Table III
W = (x1 + x2)
Total = W ⊕ x3
Carr y = W · x3. (3)

To keep up irrelevant screw up differentiate as one, the yield "100" (the estimation of 4) for four data sources being one needs to b supplanted with yields "11" (the estimation of 3). For Sum figuring, one out of three XOR entryways is supplanted with OR door. In like manner, to make the Sum identifying with the circumstance where all information sources are ones as one, an additional circuit x1 · x2 · x3 · x4 is added to the Sum verbalization. This results in goof in five out of 16 cases. Carr y is unraveled as in (4). The looking at truth table is given in Table 4.

W1 = x1 · x2
W2 = x3 · x4 Sum = (x1 ⊕ x2) + (x3 ⊕ x4) + W1 · W2
Carr y = W1 + W2 (4)

TABLE 4. TRUTH TABLE OF4:2 COMPRESSORS

Inputs				Approximate Outputs		Absolute Difference
X1	X2	X3	X4	Carry	Sum	
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	1	0	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	1	1
0	1	1	1	1	1	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	0	1	1
1	0	1	1	1	1	0
1	1	0	0	1	0	0
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	1

,

.

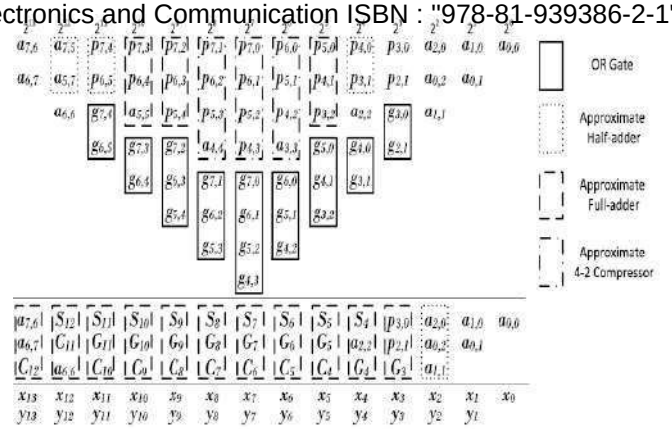

Fig. 2. Reduction of altered partial products

Fig. 2 shows the reduction of altered partial product matrix of 8 × 8 approximate multiplier. It requires two stages to produce sum and arry outputs for vector merge addition step. Four 2-input OR gates, four 3-input OR gates, and one 4-input OR gates are required for the reduction of *generate* signals from columns 3 to 11. The resultant signals of OR gates are labeled as *Gi* corresponding to the column *i* with weight 2*i* . For reducing other partial products, 3 approximate half-adders, 3 approximate full-adders, and 3 approximate compressors are required in the first stage to produce *Sum* and *Carr y* signals, *Si* and *Ci* corresponding to column *i* . The elements in the second stage are reduced using 1 approximate half-adder and 11 approximate full-adders producing final two operands *xi* and *yi* to be fed to ripple carry adder for the final computation of the result.

C. Two Variants of Multipliers

Two varieties of multipliers are proposed. In the essential case (Multiplier1), estimation is associated in all fragments of partial after effects of n-bit multiplier, however in Multiplier2, vague circuits are used in n − 1 smallest enormous segments

IV. SIMULATION RESULT

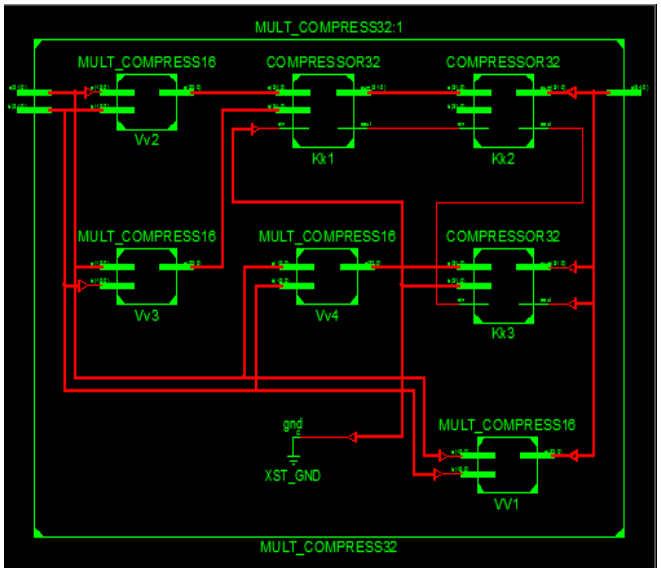

Fig.3. RTL Schematic diagram of Approximate Multiplier

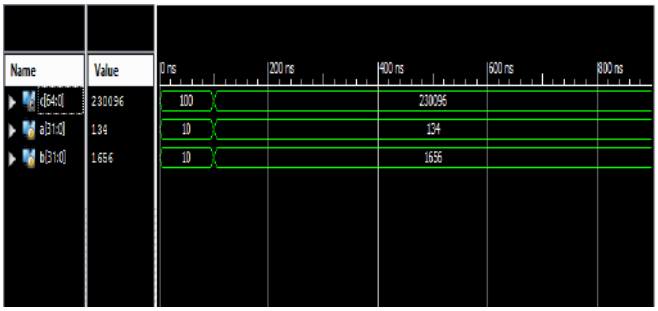

Fig.4.Simulation result of Approximate Multiplier

TABLE 5. DEVICE UTILIZATION SUMMARY

Logic Utilization	Used	Available	Utilization
No.Of Slice LUTs	2692	63400	4%
No.Of fully used LUT-FF pairs	0	2692	0%
No.Of bonded IOBs	129	210	61%

```
LUT5:I4->O          5   0.097   0.314  Kk2/K2/GC3/G1 (Kk2/K2/s<3>)
LUT5:I4->O          2   0.097   0.299  Kk2/K2/GC7/G1 (Kk2/K2/v<7>)
LUT5:I4->O          3   0.097   0.389  Kk2/K2/GC16/G1 (cout2)
LUT6:I4->O          5   0.097   0.712  Kk3/K1/GC1/G1 (Kk3/K1/q<1>)
LUT6:I0->O          2   0.097   0.688  Kk3/K1/GC3/G (Kk3/K1/s<3>)
LUT6:I1->O          2   0.097   0.299  Kk3/K1/GC7/G3_SW0 (N195)
LUT5:I4->O          1   0.097   0.295  Kk3/K1/GC7/G3 (Kk3/K1/GC7/G2)
LUT6:I5->O          1   0.097   0.379  Kk3/K1/GC16/G4_SW0 (N177)
LUT6:I4->O          4   0.097   0.707  Kk3/K1/GC16/G4 (Kk3/cout1)
LUT6:I0->O          4   0.097   0.570  Kk3/K2/GC1/G1 (Kk3/K2/q<1>)
LUT6:I2->O          2   0.097   0.688  Kk3/K2/GC6/G11 (Kk3/K2/GC6/G1)
LUT5:I0->O          4   0.097   0.570  Kk3/K2/GC8/G11 (Kk3/K2/GC8/G1)
LUT4:I0->O          1   0.097   0.295  Kk3/K2/GC8/G1 (Kk3/K2/v<8>)
LUT6:I5->O          1   0.097   0.279  Kk3/K2/Mxor_sum<15:1>_12_xo<0>1 (c_61_OBUF)
OBUF:I->O               0.000          c_61_OBUF (c<61>)
----------------------------------------
Total                     26.335ns (4.075ns logic, 22.260ns route)
                                   (15.5% logic, 84.5% route)
```

Fig.5. Time Summery of Approximate Multiplier

V. RESULTS AND DISCUSSION

All approximate multipliers are designed for n = 16. The multipliers are implemented in verilog and synthesized using Synopsys Design Compiler and a TSMC 65 nm standard cell library at the typical process corner, with temperature 25 °C and supply voltage 1 V. From the Synopsys dc reports, we get area, delay, dynamic power and leakage power. Multiplier1 applies approximation in all columns, whereas in Multiplier2, approximation is applied in 15 least significant columns during partial product reduction.

For the proposed multipliers, the altered partial products are generated and compressed using half-adder, full-adder, and 4-2 compressor structures to form final two rows of partial products. The efficiency of the proposed multipliers is compared with existing approximate multipliers inexact compressor design 2 of [5] is used to design compressor based multipliers ACM1, where all columns are approximated and ACM2, where only 15 least significant columns are approximated.

SSM [6] for m = 12 and n = 16 is designed for implementation. PPP design discussed in [7] for j = 2, k = 2 is designed and implemented under Dadda tree structure. In [8], the partial product matrix of 16-bit under designed multiplier (UDM) comprises approximate 2 × 2 partial products accumulated together with exact carry save adders.

Exhaustive error analysis of the approximate multipliers is done using MATLAB. Exact 16-bit multiplier is designed using Dadda tree structure. Table compares all designs in terms of area, delay, power, power delay product (PDP), and area power product (APP). NED and MRE of the approximate multipliers are listed in Table If high approximation can be tolerated for saving more power, Multiplier1 and ACM1 are the candidates to be considered.

It can be seen that Multiplier1 has better APP, whereas ACM1 has better PDP. However, Multiplier1 has 64% lower NED and three orders of magnitude lower MRE, compared to ACM1. It should be noted that high values of MRE for ACMs are due to nonzero output for inputs with all zeros

VI. APPLICATION—IMAGE PROCESSING

Geometric mean filter is widely used in image processing to reduce Gaussian noise [13]. The geometric mean filter is better at preserving edge features than the arithmetic mean filter. Two 16- bits per pixel gray scale images with Gaussian noise are considered.

3 × 3 mean filter is used, where each pixel of noisy image is replaced with geometric mean of 3 × 3 block of neighboring pixels centered around it. The algorithms are coded and implemented in MATLAB. Exact and approximate 16-bit multipliers are used to perform multiplication between 16-bit pixels. PSNR is used as figure.

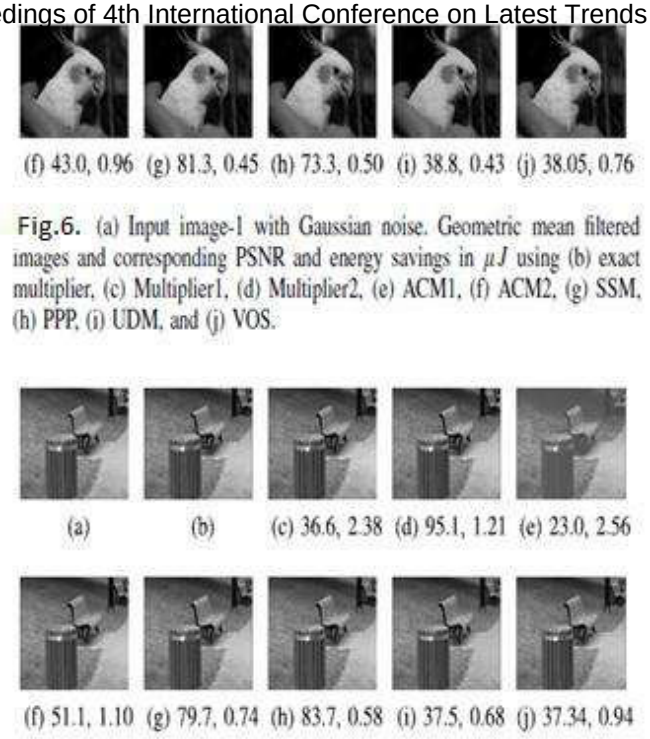

Fig.6. (a) Input image-1 with Gaussian noise. Geometric mean filtered images and corresponding PSNR and energy savings in μJ using (b) exact multiplier, (c) Multiplier1, (d) Multiplier2, (e) ACM1, (f) ACM2, (g) SSM, (h) PPP, (i) UDM, and (j) VOS.

Fig. 6. (a) Input image-2 with Gaussian noise. Geometric mean filtered images and corresponding PSNR and energy savings in μJ using (b) exact multiplier, (c) Multiplier1, (d) Multiplier2, (e) ACM1, (f) ACM2, (g) SSM, (h) PPP, (i) UDM, and (j) VOS. The noisy input image and resultant image after denoising using exact and approximate multipliers, with their respective PSNRs and energy savings in μJ are shown in Figs. 4 and 5, respectively. Energyrequired for exact multiplication process for image-1 and image-2 is savings compared to Multiplier1, Multiplier1 has significantly higher PSNR than ACM1. Multiplier2 shows the best PSNR among all the approximate designs. Multiplier2 has better energy savings, compared to ACM2, PPP, SSM, UDM, and VOS. The intensity of image-1 being mostly on the lower end of the histogram causes poor performance of ACM multipliers. As the switching activity impacts most significant part of the design in
VOS, PSNR values are affected.

VI.CONCLUSION

In this brief, to propose efficient approximate multipliers, partial products of the multiplier are modified using *generate* and *propagate* signals. Approximation is applied using simple OR gate for altered *generate* partial products. Approximate half-adder, full-adder, and 4-2 compressor are proposed to reduce remaining partial products. Two variants of approximate multipliers are proposed, where approximation is applied in all n bits in Multiplier1 and only in $n-1$ least significant part in Multiplier2. Multiplier1 and Multiplier2 achieve significant reduction in area and power consumption compared with exact designs. With APP savings being 87% and 58% for Multiplier1 and Multiplier2 with respect to exact multipliers, they also outperform in APP in comparison with existing approximate designs. They are also found to have better precision when compared to existing approximate multiplier designs. The proposed multiplier designs can be used in applications with minimal loss in output quality while saving significant power and area

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DESIGN AND IMPLEMENTATION OF COMBINATIONAL AND SEQUENTIAL CIRCUITS USING REVERSIBLE LOGIC

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Abstract: **Reversible logic is the emerging Field now a days in research area. The aim of this Paper is to realize the different types of combinational And sequential circuits like 1- bit full adder/fullsubtractor , 2-bit comparator and d=Latch , D-Flipflop 4-bit Johnson counter using reversible logic gates with minimum Quantum cost.there are many reversible logical gates like Feynman , fredkin , peares , TR , BJN , Toffoli gates etc. Reversible logic is nothing but If the number of inputs are equal to the number of outputs i.e., if there is B-number of inputs and M-number of outputs are present than B=M and there is must be a unique mapping. Between the inputs and outputs.**

Keywords: ***Reversible logic Full adder/full subtractor, quantum cost, D-flip flop, Johnson counter.***

I.INTRODUCTION

This research paper focuses on implementation of reversible logic circuits in which main aim is to optimize speed of the design. A Reversible adder is designed using basic reversible gates. Using this adder, an N-bit reversible adder is devised and then compared with the conventional N-bit adder in terms of speed, critical paths, hardware used. And also a 2- bit comparator is developed in Reversible logic is widely used in low power VLSI. Reversible circuits are capable of back-computation and reduction in dissipated power, as there is no loss of information. Basic reversible gates are employed to achieve the required functionality of a reversible circuit[1]. The uniqueness of reversible logic is that, there is no loss of information since there is one-to-one correspondence between inputs and outputs. This enables the system to run backwards and while doing so, any intermediate design stage can be thoroughly examined. The fan-out combinational circuits. With the known fact that sequential circuits are the heart of digital designing, so here two sequential circuits are developed by using master slave combination of D-latch we developed a D-flip flop. And a Johnson counter is developed by using the D-flip flop[2].

II.REVERSIBLE LOGIC

Boolean logic is said to be reversible if the set of inputs are equal to the set of outputs.There is unique correspondence between the inputs and outputs.

THEME OF REVERSIBLE LOGIC:

A.QUANTUM COST: The implementation cost of a quantum circuits is more precise, Quantum cost is defined as the number of elementary quantum operations needed to realize a gate.

B.SPEED OF COMPUTATION: While designing any system the computation speed is very important and it must be high speed that is achieved by the reversible logic.

C.GARBAGE OUTPUTS: Garbage outputs are not useful for further block designing in a circuit hence for better efficiency it is necessary to minimize the number of garbage outputs[3].

III. REVERSIBLE LOGICAL GATES

There are many reversible logic gates are present such as Feynman , peares , fredkin, TR,BJN gate etc. In Boolean logic the universal gates are NAND,NOR gates coming to reversible logic Feynman and toffoli are the universal gates

A.FEYNMAN GATE: Feynman gate is 2x2 universal reversible logic gate[4]. the Quantum cost of FG gate is given by 1.

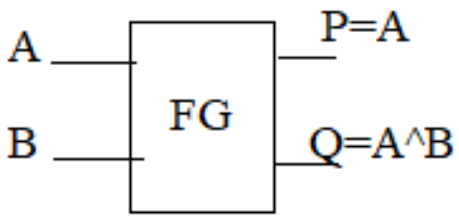

Fig. 1. Feynman gate

B.PERES GATE: Peres gate is a 3x3 reversible gate. The Quantum cost of PG gate is given by 4.

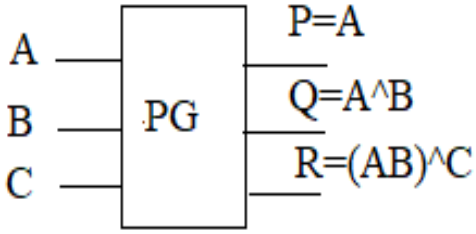

Fig. 2. Peres gate

C.FREDKIN GATE: Fredkin gate also a 3x3 reversible gate with minimum Quantum cost is given by 5.

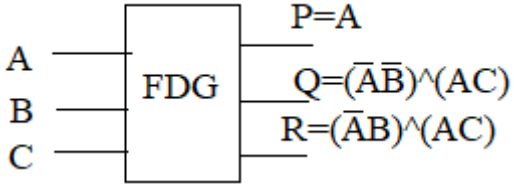

Fig .3. Fredkin gate

D.TOFFOLI GATE: Toffoli gate is a 3x3 reversible gate with minimum quantum cost 4.

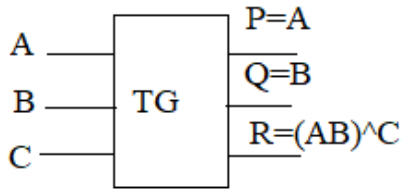

Fig. 4. Toffoli gate

E.TR GATE: TR gate is also 3x3 reversible logic as shown below with minimum Quantum cost is 4.

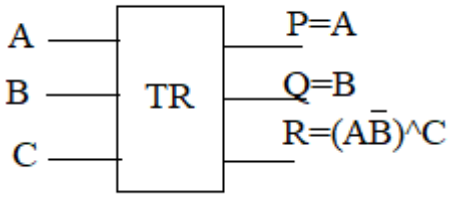

Fig. 5. Tr gate

IV.EXISTING METHOD

In present VLSI technology, power consumption is a very important factor[6]. In present method the designing of a combinational and sequential circuits are done by logical gates it requires more power for overcoming that we are using a reversible logic[7].

V.PROPOSED METHOD

1.COMBINATIONAL CIRCUITS:

A.Reversible 1-bit Full Adder/Full Subtractor: For designing the reversible full adder we need 2-Feynman(2x2) and 2-peres gate(3x3). Here we are using a ctrl as one of the input to the Feynman gate. If the ctrl is one the circuit act as subtractor and if ctrl is zero than it act as adder .the circuit design is as shown in below figure[8].

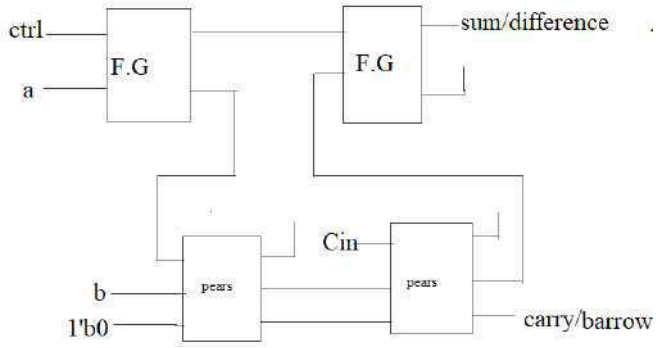

Fig. 6. 1-bit full adder and subtractor

B. Reversible N-bit full adder/full Subtractor: The design of reversible N-bit full adder/full subtractor is by using the cascading of 1-bit full adder/full subtractor by N- times. Here a 4-bit full adder and full subtractor is designed. Here for designing 4-bit full adder we require 4 full adder and full subtractor circuits so the number of full adders and full subtractor required is equal to the no of bits to be add/subtract[5].

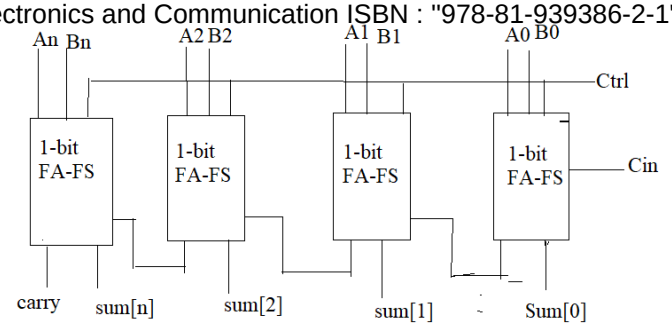

Fig .7 . N-bit full adder/full subtractor

C.2-bit comparator: The design of 2-bit comparator uses 4-TR gates(3x3),3-feynman gates (2x2),1-peres gate(3x3),1-bjn gate(3x3). The output of 2-bit comparator output is obtained at bjn gate[1].

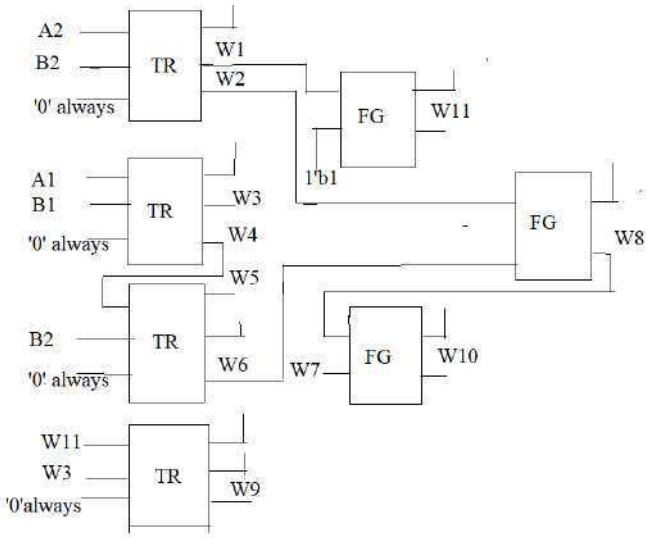

Fig .8. 2-bit comparator

2.SEQUENTIAL CIRCUITS:

A. Design of D-latch: The design of D-latch is done by using 1-fredkin gate(3x3) And 2-feynman gate(2x2).as show in below figure.

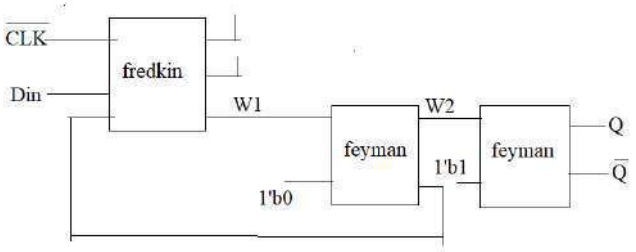

Fig. 9. D-latch

B. Design of D-flip flop: The design of d-flip flop is by using two d-latch in master slave combination. The main aim of master slave combination of d-flip flop is two eliminate the race around condition[2].

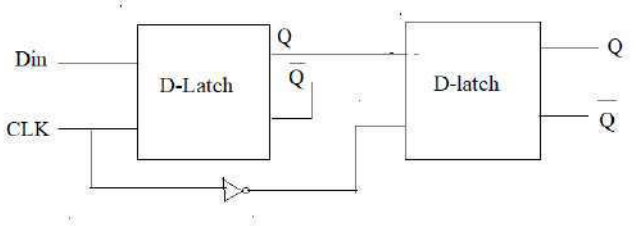

Fig. 10 .D-flip flop

C. Design of 4- Johnson counter: The design of Johnson counter is developed by using D –flip flop combination .

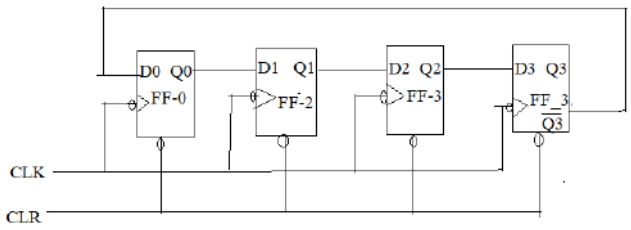

Fig. 11. Johnson counter

VI. SCHEMATIC OF THE CIRCUITS

1. COMBINATIONAL CIRCUITS:

A.Reversible 1-Bit full adder/full subtractor: The schematic of the 1-bit full adder and full subtractor circuit as shown below[2].

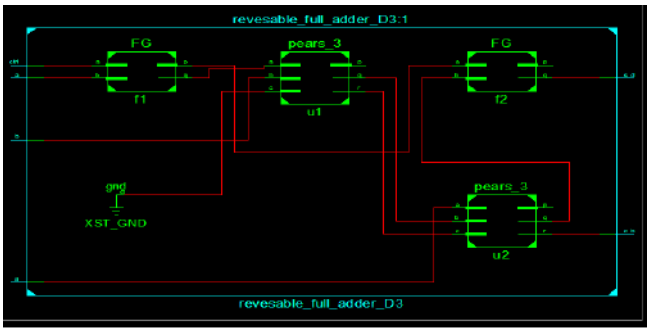

Fig. 12. Schematic of 1-bit full adder/full subtractor

B. Reversible 2-Bit comparator: The reversible 2-bit comparator is designed schematic.

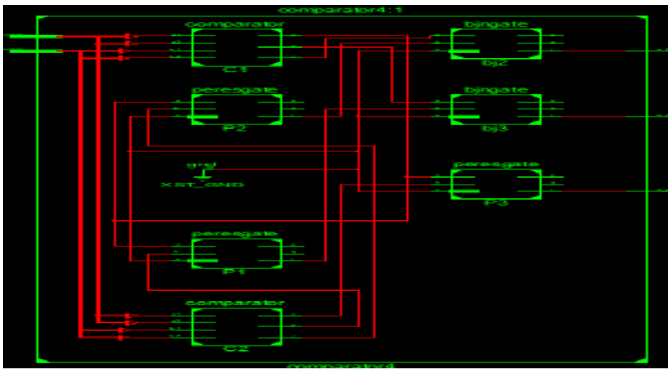

Fig .13. Schematic 2-bit comparator

2. SEQUENTIAL CIRCUITS:

A. Reversible D-Latch:

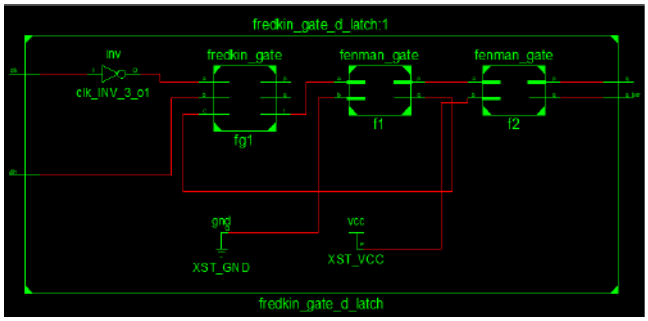

Fig .14. Schematic of D-latch

B. Reversible Johnson counter:

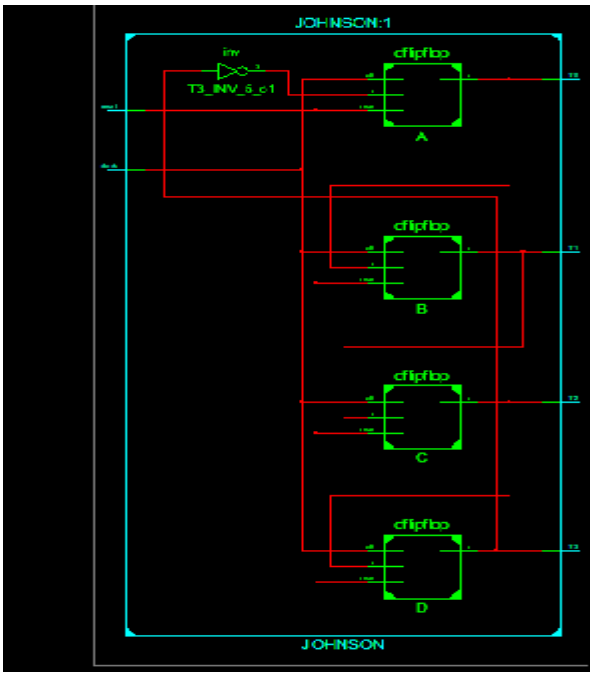

Fig. 15. Schematic of Johnson counter

VII. SIMULATION RESULTS

A. REVERSIBLE 1- BIT FULL ADDER/FULL SUBTRACTOR:

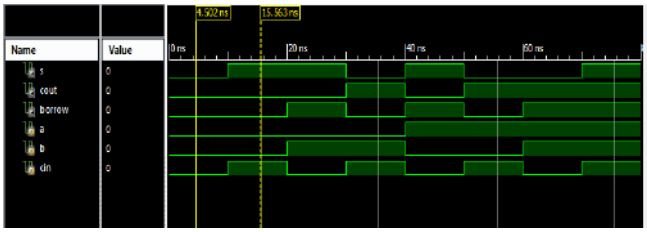

Fig .16. Out put of 1-bit full adder/full subtractor

B.4-BIT FULL ADDER/FULL SUBTRACTOR:

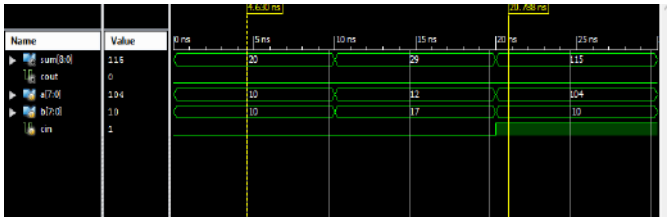

Fig .17. Out put of 4-bit full adder/full subtractor

C.2-BIT COMPARATOR:

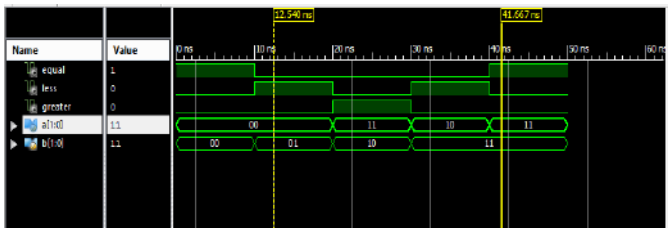

Fig .18. output of 2-bit comparator

D. D-FLIP FLOP:

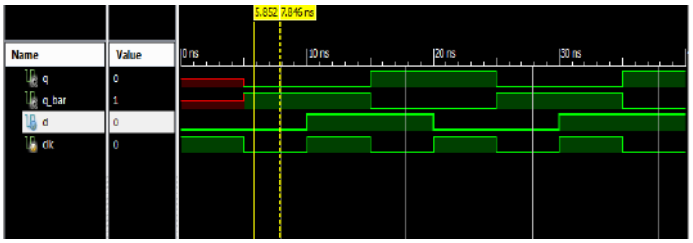

Fig. 19.output of D-Flip flop

E.4- BIT JOHNSON COUNTER:

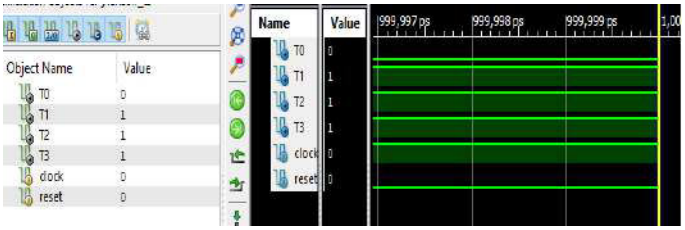

Fig. 20. output of 4-bit Johnson counter

VIII.DESIGN SYNTHESIS OF THE CIRCIUTS

The synthesis of the circuits are done by using Xilinx software 14.2. In this synthesis we are comparing the time delay and power consumption of both reversible and irreversible logic. The comparison table of both reversible and irreversible logic as show in below table.

TABLE I.COMPARISON OF COMBINATIONAL AND SEQUENTIAL CIRCUITS

S.No	Device	Time delay	power	improvement
1	4-bit irreversible adder	5.547ns	290 mW	7.87%
2	4-bit reversible adder	5.547ns	267.1 mW	8.74%
3	2-bit irreversible comparator	11.16ns	380.8 mW	29.94%
4	2-bit reversible comparator	9.54ns	266.8 mW	14.46%
5	Irreversible D-flip flop	8.209ns	364.7 mW	30.43%
6	Reversible D-flip flop	7.906ns	267.8 mW	10.34%
7	Irreversible Johnson counter	14.73ns	830.5 mW	29.53%
8	Reversible Johnson counter	13.07ns	740.9 mW	11.33%

VIII.APPLICATIONS AND FUTURE SCOPE:

Reversible logic design finds applications in various fields including quantum computing, Nano computing , Optical computing,Digital signal processing. The future of computer chips limited by Moore"s law; hence alrtenative is to build a quantum chips. Our future research topic is designing a new reversible gates and implementing a different types of combinational and sequential circuits capable of ultra high speed and infinitesimally low power computing.

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VLSI DESIGN OF N x N BIT HIGH PERFORMANCE MULTIPLIER WITH REDUNDANT BINARY ENCODING

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***Abstract*- Due to its high modularity and carry-free addition, a redundant binary (RB) representation can be used when designing high performance multipliers. The conventional RB multiplier requires an additional RB partial product (RBPP) row, because an error-correcting word (ECW) is generated by both the radix-4 Modified Booth encoding (MBE) and the RB encoding. This incurs in an additional RBPP accumulation stage for the MBE multiplier. In this paper, a new RB modified partial product generator (RBMPPG) is proposed; it removes the extra ECW and hence, it saves one RBPP accumulation stage. Therefore, the proposed RBMPPG generates fewer partial product rows than a conventional RB MBE multiplier. Simulation results show that the proposed RBMPPG based designs significantly improve the area and power consumption when the word length of each operand in the multiplier is at least 32 bits; these reductions over previous NB multiplier designs incur in a modest delay increase (approximately 5%). The power-delay product can be reduced by up to 59% using the proposed RB multipliers when compared with existing RB multipliers.**

Keywords: ***Redundant binary, Modified Booth encoding, Redundant binary encoding, Redundant binary Modified partial product generator (RBMPPG), Redundant binary to normal binary converter***

I.INTRODUCTION

DIGITAL multipliers are widely used in arithmetic units of microprocessors, digital signal processors and multimedia. Many algorithms and architectures have been proposed to design high-speed and low-power multipliers [1], [2]. A normal binary (NB) multiplication by digital circuits includes three steps. In the first step, partial products are generated; in the second step, all partial products are added by a partial product reduction tree until two partial product rows remain. In the third step, the two partial product rows are added by a fast carry propagation adder. Two methods have been used to perform the second step for the partial product reduction. A first method uses four-two compressors, while a second method uses redundant binary (RB) numbers [5], [6]. Both methods allow the partial product reduction tree to be reduced at a rate of 2:1.

This paper focuses on the RBPP generator for designing a 2n-bit RB multiplier with fewer partial product rows by eliminating the extra ECW. A new RB modified partial product generator based on MBE (RBMPPG-2) is proposed. In the proposed RBMPPG-2, the ECW of each row is moved to its next neighbour row. Furthermore, the extra ECW generated by the last partial product row is combined with both the two most significant bits (MSBs) of the first partial product row and the two least significant bits (LSBs) of the last partial product row by logic simplification. Therefore, the proposed method reduces the number of RBPP rows from N=4 þ 1 to N=4, i.e., a RBPP accumulation stage is saved. The proposed method is applied to 8x8-, 16x16-, 32x32-, and 64x64-bit RB multiplier designs; the designs are synthesized using the Nan- Gate 45 nm Open Cell Library. The proposed designs achieve significant reductions in area and power consumption compared with existing multipliers when the word length of each of the operands is at least 32 bits. While a modest increase in delay is encountered (approximately 5 percent), the power-delay product (PDP) at word lengths of at least 32 bits confirms that the proposed designs are the best also by this figure of merit.

This paper is organized as follows. Section 2 introduces radix-4 Booth encoding. The design of the conventional RBPP generator is also reviewed. Section 3 presents the proposed RBMPPG. This section also demonstrates the adoption of the proposed RBMPPG into various word-length RB multipliers. Section 4 provides the evaluation results of the new RB multipliers using the proposed RBMPPG for different word lengths and compares them to previous best designs found in the technical literature.

TABLE:1 MODIFIED BOOTH ENCODING SCHEME

b_{2i+1}	b_{2i+1}	b_{2i-1}	Operation
0	0	0	0
0	0	1	+A
0	1	0	+A
0	1	1	+2A
1	0	0	-2A
1	0	1	-A
1	1	0	-A
1	1	1	0

II. REVIEW OF BOOTH ENCODING AND RB PARTIAL PRODUCT GENERATOR

Radix-4 Booth Encoding

Booth encoding has been proposed to facilitate the multiplication of two's complement binary numbers [17]. It was revised as modified Booth encoding or radix-4 Booth encoding [18]. The MBE scheme is summarized in Table 1. The multiplier bits are grouped in sets of three adjacent bits. The two side bits are overlapped with neighbouring groups except the first multiplier bits group in which it is {b1, b0, 0}. Each group is decoded by selecting the partial product shown in Table 1, where 2A indicates twice the multiplicand, which can be obtained by left shifting. Negation operation is achieved by inverting each bit of A and adding '1' (defined as correction bit) to the LSB [10], [11]. Methods have been proposed to solve the problem of correction bits for NB radix-4 Booth encoding (NBBE-2)

multipliers. However, this problem has not been solved for RB MBE multipliers.

III. RB PARTIAL PRODUCT GENERATOR

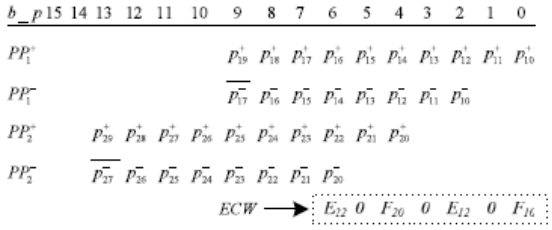
As two bits are used to represent one RB digit, then a RBPP is generated from two NB partial products [1], [2], [3], [4], [5], [6]. The addition of two N-bit NB partial products X and Y using two's complement representation can be expressed as follows [6]:

$$\begin{aligned} X+Y &= X-\overline{Y}-1 \\ &= \left(-x_N 2^N+\sum_{i=0}^{N-1} x_i 2^i\right)-\left(-\overline{y_N}2^N+\sum_{i=0}^{N-1}\overline{y_i}2^i\right)-1 \\ &= -(x_N-\overline{y_N})2^N+\sum_{i=0}^{N-1}(x_i-\overline{y_i})2^i-1 \\ &= (X,\overline{Y})-1, \end{aligned} \quad (2)$$

where Y' is the inverse of Y, and the same convention is used in the rest of the paper. The composite number can be interpreted as a RB number. The RBPP is generated by inverting one of the two NB partial products and adding -1 to the LSB. Each RB digit Xi belongs to the set {1; 0; 1}; this is coded by two bits as the pair.

TABLE 2. RB ENCODING USED IN THIS WORK

X_i^+	X_i^-	RB digit (X_i)
0	0	0
0	1	$\bar{1}$
1	0	1
1	1	0



Conventional RBPP architecture for an 8-bit MBE multiplier (X_i^- , X_i^+). RB numbers can be coded in several ways. Table 2 shows one specific RB encoding [6], where the RB digit is obtained by performing $X_i^+ - X_i^-$ Both MBE and RB coding schemes introduce errors and two correction terms are required: 1) when the NB number is converted to a RB format, -1 must be added to the LSB of the RB number; 2) when the multiplicand is multiplied by -1 or -2 during the Booth encoding, the number is inverted and þ1 must be added to the LSB of the partial product. A single ECW can compensate errors from both the RB encoding and the radix-4 Booth recoding. The conventional partial product architecture of an 8-bit MBE multiplier [5], [6] is shown in Fig. 1, where b_p represents the bit position generated by using an encoder and decoder (Fig. 2) [10]. An N-bit CRBBE-2 multiplier includes N=4 RBPP rows and one ECW; the ECW takes the form as follows:

$$ECW = E_{(N/4)2}0\ F_{(N/4)0}\ldots 0E_{i2}0\ F_{i0}\ldots 0\ E_{12}0\ F_{10}, \quad (3)$$

where i represents the i[th] row of the RBPPs, E_{i2} €{0; 1} and F_{i0} €{0;1}. In F_{i0}, a-1 correction term is always required by RB coding. If F_{i0} also corrects the errors from the MBE recoding, then the correction term cancels out to 0. That is to say that if the multiplicand digit is inverted and added to 1, then F_{i0} is 0, otherwise F_{i0} is -1. The error-correcting digit E_{i2} is determined only by the Booth encoding:

$$E_{i2} = \begin{cases} 0, & \text{no negative encoding} \\ 1, & \text{negative encoding.} \end{cases} \quad (4)$$

As shown in Fig. 1 the first RBPP row, i.e. PP1, consists of the first partial product row PP^+_1 and the second partial product row PP^-_1 .

$$p^+_{19} = \overline{p^+_{18}},$$

$$\begin{aligned} p^+_{18} &= \overline{b_1}\ \overline{b_0}\cdot 0 + \overline{b_1}b_0\cdot a_7 + b_1\overline{b_0}\cdot\overline{a_7} + b_1b_0\cdot\overline{a_7} \\ &= \overline{b_1}b_0\cdot a_7 + b_1\overline{a_7}. \end{aligned} \quad (5,6)$$

According to Eq. (2), the sign extension bit p^+_{29} is also the inverse of p^+_{28}. The p^-_{17} in PP^-_1 and the p^-_{27} in PP^-_2 are also negated as p^-_{17} and p^-_{27}. Eq. (5) and Eq. (6) are further used in the next section when presenting the proposed modified RBPP generator.

IV. PROPOSED RB PARTIAL PRODUCT GENERATOR

A new RB modified partial product generator based on MBE (RBMPPG-2) is presented in this section; in this design, ECW is eliminated by incorporating it into both the two MSBs of the first partial product row (PP^+_1) and the two LSBs of the last partial product row ($PP^-_{(N/4)}$).

Proposed RBMPPG-2

Fig. 3 illustrates the proposed RBMPPG-2 scheme for an 8x8-bit multiplier. It is different from the scheme in Fig. 1, where all the error-correcting terms are in the last row. ECW_1 is generated by PP_1 and expressed as

$$ECW_1 = 0\ E_{12}0\ F_{10}. \quad (7)$$

The ECW2 generated by PP2 (also defined as an extra ECW) is left as the last row and it is expressed as:

$$ECW_2 = 0\,E_{22}\,0\,F_{20}. \quad (8)$$

To eliminate a RBPP accumulation stage, ECW2 needs to be incorporated into PP1 and PP2. As discussed in Section 2.2 forFi0 and as per Table 1, F 20 is determined by b5; b4; b3 as follows:

$$F_{20} = \begin{cases} -1, & b_5b_4b_3 = 000, 001, 010, 011, \text{ or } 111 \\ 0, & b_5b_4b_3 = 100, 101, \text{or} 110. \end{cases} \quad (9)$$

TABLE 3. TRUTH TABLE OF $E_2q^-_{2(-2)}q^-_{2(-1)}$ and p^-_{21},p^-_{20}

$b_7\,b_6b_5$	$E_{22}F_{20}$	$E_2q^-_{2(-2)}q^-_{2(-1)}$	p^-_{21}	p^-_{20}
000	0 $\bar{1}$	$\bar{1}$ 1 1	0	0
001	0 0	0 0 0	a_1	a_0
010	0 $\bar{1}$	$\bar{1}$ 1 1	a_1	a_0
011	0 0	0 0 0	a_0	0
100	1 $\bar{1}$	0 1 1	$\bar{a}_0$	1
101	1 0	1 0 0	$\bar{a}_1$	$\bar{a}$
110	1 $\bar{1}$	0 1 1	$\bar{a}_1$	$\bar{a}_0$
111	0 0	0 0 0	0	0

As per Table 1, when b5b4b3 = 111, -0 = 0 can be used. Therefore, F20 can be expressed as follows:

$$F_{20} = \begin{cases} -1, & b_5b_4b_3 = 000, 001, 010, \text{or } 011 \\ 0, & b_5b_4b_3 = 100, 101, 110, \text{or } 111. \end{cases} \quad (10)$$

By setting PP $^{+}_{2}$ to all ones and adding þ1 to the LSB of the partial product, F20 can then be determined only by b5 as follows:

$$F_{20} = \begin{cases} -1, & b_5 = 0 \\ 0, & b_5 = 1 \end{cases} \quad (11)$$

A modified radix-4 Booth encoding and a decoding circuit for the partial product PP$^{+}_{2}$ are proposed here (Fig. 4); an extra three input OR gate is then added to the design of [10] (Fig. 2). The three inputs of the additional OR gate are b5, b4, and b3. When b5b4b3 = 111, it is clear that b5 b4 b3= 000, p^{+}_{2i} =1, and PP$^{+}_{2}$ is set to all ones. So, E_{22} and F_{20} in ECW_2 are now determined by b7b6b5 without b4; b3. Although the complexity is slightly increased compared with the previous design (Fig. 2), the delay stage remains the same. In this work, Q^{+}_{19}, Q^{+}_{18}, Q^{-}_{21}, and Q^{-}_{20} are used to represent the modified partial products. $q^{-}_{2(-2)}$, and $q^{-}_{2(-1)}$ are used to represent the additional partial products that are determined by F20. As -1 can be coded as 111 in RB format, E_{22} and F_{20} can be represented by E_2, $q^{-}_{2(-2)}$, $q^{-}_{2(-1)}$, (Fig. 3b) as follows:

$$E_2 = \begin{cases} E_{22}, & F_{20} = 0 \\ E_{22} - 1, & F_{20} = -1, \end{cases}$$

$$q^{-}_{2(-2)} = q^{-}_{2(-1)} = \begin{cases} 0, & F_{20} = 0 \\ 1, & F_{20} = -1. \end{cases} \quad (12,13)$$

As per Eq. (11) and Eq. (13), $q^{-}_{2(-2)}$, and $q^{-}_{2(-1)}$ can also be expressed as follows:

$$q^{-}_{2(-2)} = q^{-}_{2(-1)} = \overline{b_5}. \quad (14)$$

This is further explained by the truth table of E_{22}, F_{20} and E_2, $q^{-}_{2(-2)}$, and $q^{-}_{2(-1)}$ (Table 3). Now ECW_2 only includes E_2 and $E_2 \in \{0; 1; -1\}$; E_2 can be incorporated into the modified partial products Q^{+}_{19}, Q^{+}_{18}, Q^{-}_{21} and Q^{-}_{20} by replacing p^{+}_{19}, p^{+}_{18} and p^{-}_{21}, p^{-}_{20} in multiplier.

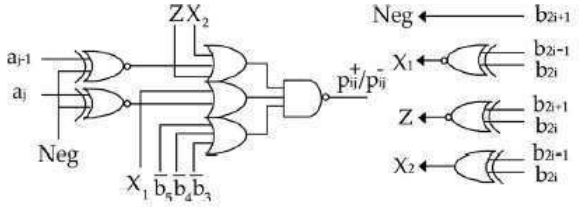


Fig.1. The modified radix-4 booth encoding and decoding scheme for PP$^{+}_{2}$

TABLE 4. TRUTH TABLE OF $Q^{+}_{19}, Q^{+}_{18}, Q^{-}_{21} Q^{-}_{20}$

$p^{+}_{19}p^{+}_{18}p^{-}_{21}p_2$	$Q^{+}_{19}Q^{+}_{18}Q^{-}_{21}Q_2$	$Q^{+}_{19}Q^{+}_{18}Q^{-}_{21}Q_2$	$Q^{+}_{19}Q^{+}_{18}Q^{-}_{21}Q_2$ (E_2=-1)
0100	0100	0101	0011
0101	0101	0110	0100
0110	0110	0111	0101
0111	0111	1000	0110
1000	1000	1001	0111
1001	1001	1010	1000
1010	1010	1011	1001
1011	1011	1100	1010

the shortest path Fig. 3c. From the truth table, E_2 can be determined by $b_7b_6b_5$ as follows:

$$E_2 = \begin{cases} -1, & b_7b_6b_5 = 000, \text{or } 010 \\ 1, & b_7b_6b_5 = 101 \\ 0, & b_7b_6b_5 = 001, 011, 100, 110, \text{or } 111. \end{cases} \quad (15)$$

So the following three cases can be distinguished: 1) When E_2 = 0, Q^{+}_{19}, Q^{+}_{18}, Q^{-}_{21} and Q^{-}_{20} remain unchanged as: $Q^{+}_{19} = p^{+}_{19}$, $Q^{+}_{18} = p^{+}_{18}$, $Q^{-}_{21} = p^{-}_{21}$ and $Q^{-}_{20} = p^{-}_{20}$. 2) When E_2 = 1, a 1 is added to $p^{+}_{19}p^{+}_{18}p^{-}_{21}p^{-}_{20}$. 3) When E_2 = -1, a 1 is subtracted from $p^{+}_{19}p^{+}_{18}p^{-}_{21}p^{-}_{20}$. The relationships between Q^{+}_{19}, Q^{+}_{18}, Q^{-}_{21}, Q^{-}_{20} and $p^{+}_{19}, p^{+}_{18}, p^{-}_{21}, p^{-}_{20}$ are summarized in Table 4. As the two MSBs of PP$^{+}_{1}$ i.e., p^{+}_{19}, p^{+}_{18} take complementary values as shown in Eq. (5), the operations of adding or subtracting a 1 will never incur in an overflow. Therefore, as per Eq. (15) and Table 4, the logic functions of Q^{+}_{19}, Q^{+}_{18}, Q^{-}_{21}, Q^{-}_{20} can be expressed as follows:

$$Q^{+}_{19} = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p^{+}_{19} + \overline{b_7}\,\overline{b_5} \cdot \overline{(p^{+}_{18} + p^{-}_{21} + p^{-}_{20}} \oplus p^{+}_{19}) + b_7\overline{b_6}b_5 \cdot (p^{+}_{18}p^{-}_{21}p^{-}_{20} \oplus p^{+}_{19}),$$

$$Q^{+}_{18} = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p^{+}_{18} + \overline{b_7}\,\overline{b_5} \cdot (\overline{p^{-}_{21} + p^{-}_{20}} \oplus p^{+}_{18}) + b_7\overline{b_6}b_5 \cdot (p^{-}_{21}p^{-}_{20} \oplus p^{+}_{18}),$$

$$Q^{-}_{21} = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p^{-}_{21} + \overline{b_7}\,\overline{b_5} \cdot \overline{p^{-}_{21} \oplus p^{-}_{20}} + b_7\overline{b_6}b_5 \cdot p^{-}_{21} \oplus p^{-}_{20},$$

$$Q^{-}_{20} = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p^{-}_{20} + \overline{b_7}\,\overline{b_5} \cdot \overline{p^{-}_{20}} + b_7\overline{b_6}b_5 \cdot \overline{p^{-}_{20}}. \quad (16, 17, 18, 19)$$

The delay of the RBMPPG-2 can be further reduced by generating Q^{+}_{19}, Q^{+}_{18}, Q^{-}_{21}, Q^{-}_{20} directly from the multiplicand A and the multiplier B. The relationships between p^{+}_{19}, p^{+}_{18} and A, B have been discussed in Section 2.2 as Eq. (5) and Eq. (6). The relationships between p^{-}_{21}, p^{-}_{20} and A, B are also shown in Table 3 according to the MBE scheme. Therefore, Q^{+}_{19}, Q^{+}_{18}, Q^{-}_{21}, Q^{-}_{20} can be expressed as follows by replacing p^{+}_{19}, p^{+}_{18}, p^{-}_{21}, p^{-}_{20} with the multiplicand bits (ai) and the multiplier bits (bi) after simplification:

$$Q^{+}_{19} = \overline{\overline{b_1}b_0a_7 + b_1\overline{a_7}}\left(\overline{\overline{b_5} \cdot \overline{b_7 + b_6a_0 + b_6a_1}}\right) + \left(\overline{b_1}b_0a_7 + b_1\overline{a_7}\right) \cdot b_5 \cdot b_7\overline{b_6}\,\overline{a_1}\,\overline{a_0},$$

$$Q^{+}_{18} = \overline{\overline{b_1}b_0a_7 + b_1\overline{a_7}} \cdot \left(\overline{b_5} \cdot \overline{b_7 + b_6a_0 + b_6a_1} + b_5b_7\overline{b_6}\,\overline{a_1}\,\overline{a_0}\right) + \left(\overline{b_1}b_0a_7 + b_1\overline{a_7}\right) \cdot \left[\overline{b_5} \cdot (b_7 + b_6a_0 + b_6a_1) + b_5 \cdot b_7\overline{b_6}\,\overline{a_1}\,\overline{a_0}\right], \quad (20,21)$$

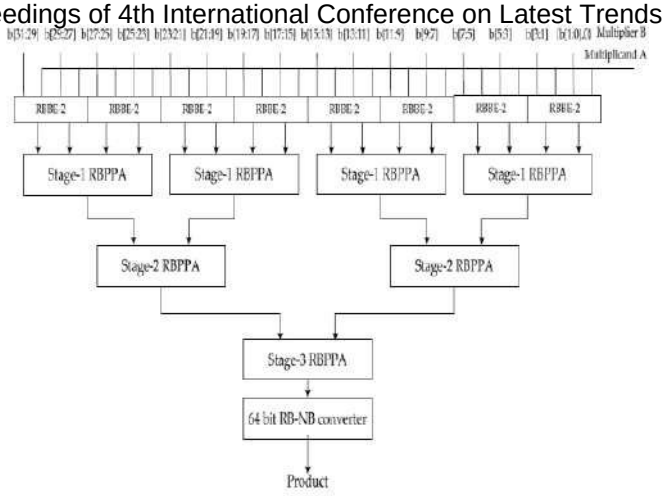


Fig 6. The block diagram of a 64-bit RB multiplier using the proposed RBMPPG-2

The above figure performs multiplication for 64 bit,128 bit and up to N-bits

V. DESIGN OF RBMPPG-2-BASED HIGH-SPEED RB MULTIPLIERS

The proposed RBMPPG-2 can be applied to any 2n-bit RB multipliers with a reduction of a RBPP accumulation stage compared with conventional designs. Although the delay of RMPPG-2 increases by one-stage of TG delay, the delay of one RBPP accumulation stage is significantly larger than a one-stage TG delay. Therefore, the delay of the entire multiplier is reduced. The improved complexity, delay and power consumption are very attractive for the proposed design.

A 32-bit RB MBE multiplier using the proposed RBPP generator is shown in Fig. 6. The multiplier consists of the proposed RBMPPG-2, three RBPP accumulation stages, and one RB-NB converter. Eight RBBE-2 blocks generate the RBPP; they are summed up by the RBPP reduction tree that has three RBPP accumulation stages. Each RBPP accumulation block contains RB full adders (RBFAs) and half adders (RBHAs). The 64-bit RB-NB converter converts the final accumulation results into the NB representation, which uses a hybrid parallel-prefix/carry select adder (as one of the most efficient fast parallel adder designs).

There are four stages in a conventional 32-bit RB MBE architecture; however, by using the proposed RBMPPG-2, the number of RBPP accumulation stages is reduced from 4 to 3 (i.e., a 25 percent reduction). These are significant savings in delay, area as well as power consumption. The improvements in delay, area and power consumption are further demonstrated in the next section by simulation. Table 5 compares the number of RBPP accumulation stages in different 2n-bit RB multipliers, i.e., 8x8-bit, 16x16-bit, 32x32-bit, 64x64-bit multipliers.

TABLE 5. COMPARISON OF RBPP ACCUMULATION STAGES IN RBPP REDUCTION TREE

Methods	64X4X	32X32	16X16	8X8
CRBBE-2	5	4	3	2
RBBE-4[4]	4	3	2	1
Proposed	4	3	2	1

For a 64-bit multiplier, the proposed design has four RBPP accumulation stages; it reduces the partial product accumulation stages; it reduces the partial product accumulation delay time by 20 percent compared with CRBBE-2 multipliers. Although both the proposed design and RBBE-4 have the same number of RBPP accumulation stages, RBBE-4 is more complex, because it uses radix-16 Booth encoding.

VI. PERFORMANCE EVALUATION

The performance of various 2n-bit RB multipliers using the proposed RBMPPG-2 is assessed; the results are compared with NBBE-2, CRBBE-2 and RBBE-4 [14] multipliers that are the latest and best designs found in the technical literature. All designs of RB multipliers use the RBFA and RBHA of [7]. An RB-NB converter is required in the final stage of the RB multiplier to convert the summation result in RB form to a two's complement number. It has been shown that the constant-time converter in [7] does not exist [19], [20], [21]. However, there is a carry-free multiplier that uses redundant adders in the reduction of partial products by applying on-the-fly conversion [22] in parallel with the reduction and generates the product without a carry-propagate adder.

A hybrid parallel-prefix/carry-select adder is used for the final RB-NB converter. The NBBE-2 multiplier design uses the same encoder and decoder as shown in Fig. 2. Four-two compressors are used in the partial product reduction tree. The extra ECW in the NB multiplier designs is also modified as proposed in [11].

The multiplier designs are described at gate level in Verilog HDL and verified by Synopsys VCS using randomly generated input patterns; the designs are synthesized by the Synopsys Design Compiler using the Nan Gate 45 nm Open Cell Library. In the simulation of each design, a supply voltage of 1.25 V and room temperature are assumed. Standard buffers of a 2X strength are used for both the input drive and the output load. The option for logic structuring is turned off to prevent the tool from changing the structure of the unit cells. The average power consumption is found using the Synopsys Power Compiler with back annotated switching activity files generated from 2,500 random input vectors. Table 6 summarizes the delay, area, power and power-delay product of the NB and RB multiplier designs; the delay, area, power and PDP metrics are compared separately. Consider the delay first; compared with CRBBE-2, the proposed designs can reduce the delay.

TABLE 6. DESIGN PULSE OF RB MULTIPLIER (USING NAN GATE 45NM OPEN CELL LIBRARY)

N-bit	NB and RB Multiplier	Delay(ns)	Area(μm^2)	Power(μW)	PDP(pj)
8	NBBE-2	0.95	1,210	301	0.285
	CRBBE-2	1.20	1,322	485	0.582
	RBEE-4[14]	1.32	1,071	546	0.721
	Proposed	1.00	1,258	496	0.496
16	NBBE-2	1.20	4,055	1,128	1.353
	CRBBE-2	1.48	4,165	1,549	2.293
	RBEE-4[14]	1.62	3,897	2,498	4.047
	Proposed	1.26	4,004	1,500	1.890
32	NBBE-2	1.51	14,420	4,215	6.364
	CRBBE-2	1.79	13,925	3,227	5.776
	RBEE-4[14]	2.09	14,454	5,745	12.007
	Proposed	1.57	13,589	3,090	4.851
64	NBBE-2	1.92	54,120	16,047	30.81
	CRBBE-2	2.29	48,264	11,852	27.141
	RBEE-4[14]	2.47	55,119	20,517	50.677
	Proposed	2.05	47,903	11,199	20.958

VII. SIMULATION AND RESULT

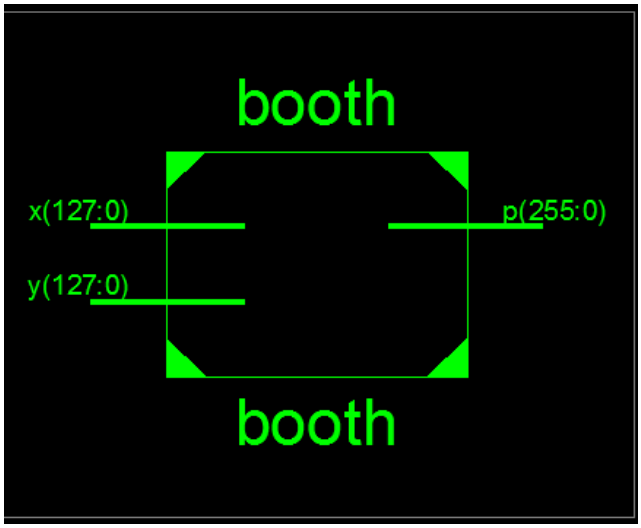


Fig .3. RTL of the multiplier

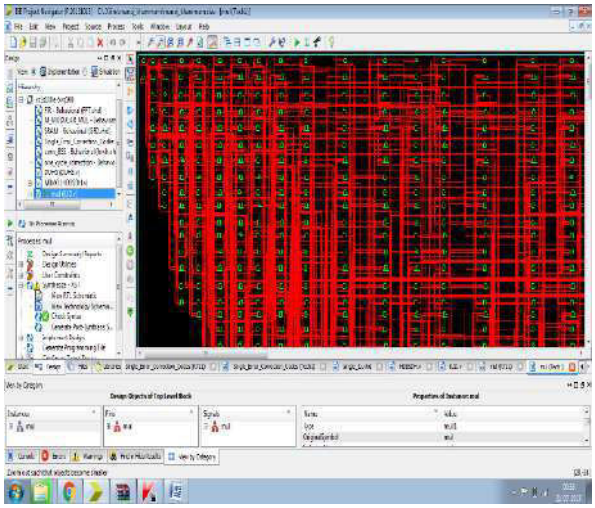


Fig. 4. Internal architecture for Multiplier RTL

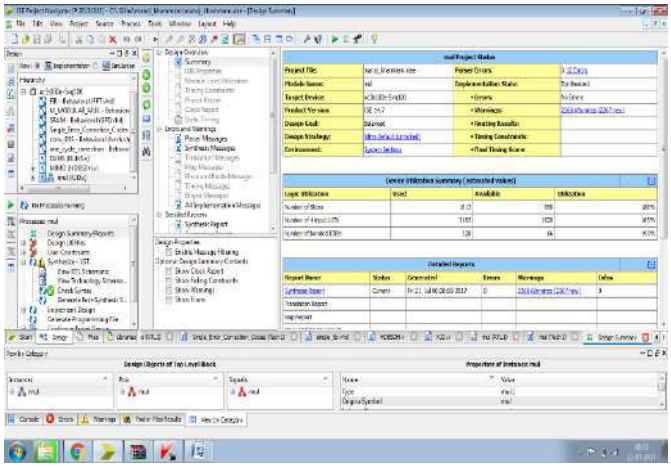


Fig. 5. Multiplier Synthesis report

Fig .6. Simulation result of NxN bit multiplier

TABLE 7. DEVICE UTILIZATION SUMMARY

Logic Utilization	Used	Available	Utilization
No.Of Slice LUTs	30432	63400	48%
No.Of fully used LUT-FF pairs	0	30432	0%
No.Of bonded IOBs	512	210	243%

VIII. CONCLUSION

We have proposed a novel recursive decomposition algorithm for RB multiplication to derive high-throughput digit-serial multipliers. By suitable projection of SFG of proposed algorithm and identifying suitable cut-sets for feed-forward cut-set retiming, three novel high-throughput digit-serial RB multipliers are derived to achieve significantly less area-time-power complexities than the existing ones. Moreover, efficient structures with low register-count have been derived for area-constrained implementation; and particularly for implementation in FPGA platform where registers are not abundant. The results of synthesis show that proposed structures can achieve saving of up to 94% and 60%, respectively, of ADPP for FPGA and ASIC implementation, respectively, over the best of the existing designs. The proposed structures have different area-time-power trade-off behaviour. Therefore, one out of the three proposed structures can be chosen depending on the requirement of the application environments. Compare existing method the proposed method is less power consumption, high speed, less time requirement and performance is high.

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Optimization Techniques in Power System: A Review

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***Abstract*—Power systems are very large and complex, it can be influenced by many unexpected events this makes Power system optimization problems difficult to solve, hence methods for solving these problems ought to be, an active research topic. This review presents an overview of important mathematical optimization methods those are Unconstrained optimization approaches Nonlinear programming (NLP), Linear programming (LP), Quadratic programming (QP), Generalized reduced gradient method, Newton method, Network flow programming (NFP), Mixed-integer programming (MIP), Interior point (IP) methods and Artificial intelligence (AI) techniques such as Artificial Neural Network (ANN), fuzzy logic, Genetic Algorithm (GA), Particle Swarm Optimization (PSO), Tabu Search (TS) algorithm, etc. and Hybrid artificial intelligent techniques are discussed. And also applications of optimization techniques have been discussed. Finally classification, application area, observation, conclusion, and recommendation for future research work will be forwarded.**

Keywords— Genetic Algorithm, Particle Swarm Optimization, Tabu Search (TS) algorithm, Nonlinear Programming, Artificial Neural Network, etc.,

I. INTRODUCTION

It's known that Power systems are very large, complex and geographically distributed. Therefore, to take the advantages in simplifying the problem and its implementation it is necessary to utilize most efficient optimization methods. Related to the power system operation numerous activities require optimum searching techniques [1]. Many researchers working with optimization techniques to solve economic issue, reliability, quality, optimal load flow, protection, cost and soon. D. Hore. et al [2] presented about Artificial Intelligence methods such as GA, PSO, BFO, ANN that used for Optimal Power Flow and economic load dispatch problem.

K. Liu. et al [3] combined adaptive genetic algorithm with Simulated annealing was presented to solve active power loss minimization. J. Lu. et al [4] presented the techniques of GA and PSO are combined to obtain good particles from genetic algorithm for the initial population input of PSO. A. Badar. et al [5] Improved or hybrid artificial intelligence methods have been discussed after Genetic algorithm, Particle Swarm Optimization, Ant Colony Optimization, Tabu Search, Simulated Annealing and Differential Evolution presented. Binitha S. et al [6] presents an overview of biologically inspired optimization algorithms which grouped by the biological and application areas. O.P. Malik [7] the possibility of implementing an adapting controller using different approach has been presented. G. Hwang. et al [8] to determine the optimal PID gain Craziness based Particle Swarm Optimization (CRPSO) and binary coded GA methods has been proposed. V. Mukherjee. et al [9] propose the hierarchical fuzzy PSS to enhance stability.

M. Caner. et al [10] was used Bacteria Foraging Optimization (BFO) technique. S.P. Ghoshal. et al [11] to design PSS A robust adaptive fuzzy controller proposed. A. Badar. et al [12] has been presented an overview of different artificial intelligence (AI) optimization techniques used in power optimization problems and a Hybrid or improved AI techniques. Yuvaraja T. et al [13] was presented the performance of the implemented PSO algorithm for solving an optimization problem that is related to improving the quality of the power supply in a Microgrid scenario. S. Khajeh. et al [14] was presented Genetic algorithm for Optimal Reconfiguration of Power Distribution Systems in radial 33 buses distribution network. S. H. Kiran.et al [15] has been presented Particle Swarm Optimization (PSO) and Artificial Bee Colony (ABC) with Hybrid-Genetic Algorithm (H-GA) for determination of sizing of FACTS.

A. K. Khamees. et al [16] proposed shuffled frog leaping algorithm and grey wolf optimizer, to solve the optimal power flow problem in electrical power system. C. M. K. Sivalingam. et al [17] Interactive artificial bee colony (IABC) was proposed to obtain reactive power optimization after comparing the results obtained from IPSO, QPSO, ABCO, and IABCO. Ö.P. Akkaş. et al [18] propose genetic algorithm to minimize fuel cost tested on 6-generator test system by ignoring line losses. S. Dean. et al [19] proposed a multi-stage procedure, called Coarse-ID control, that estimates a model from a few experimental trials, estimates the error in that model with respect to the truth, and then designs a controller using both the model. C.T.M. Clack .et al [20] shows that linear programming techniques can represent an electrical power system from a high-level without undue complication brought on by moving to mixed integer or nonlinear programming. A year wise invention of different optimization techniques is shown in Fig. 1.

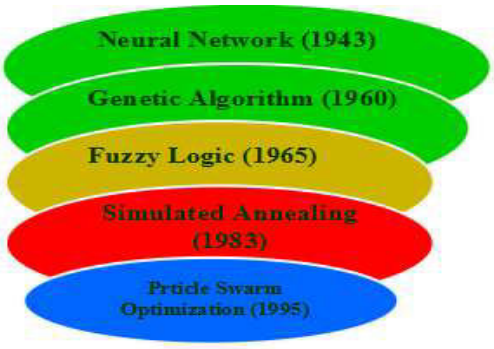

Fig. 1: Some optimization methods with its invention year

II. OVERVIEW OF OPTIMIZATION TECHINIQUES

The main objective of optimization is to minimize undesirable things (e.g. cost, energy loss, errors, etc.) or maximize desirable things (e.g. profit, quality, efficiency, etc.) since its mathematical model, subject to some

constraints. Optimization is a commonly encountered mathematical problem in all engineering disciplines. It literally means finding the best possible/desirable solution. Optimization problems are wide ranging and numerous, hence methods for solving these problems. From the view of optimization, the various techniques including traditional and modern optimization methods, which have been developed to solve power system operation, control and planning problems.

III. CLASSIFICATION OF OPTIMIZATION TECHNIQUES

After Basically optimization techniques are classified into three groups. Which are traditional method, Artificial intelligent method and hybrid artificial intelligent techniques.

A. Traditional Method

Traditional methods are optimality mathematical rigorous in some algorithms and problems can be formulated to take advantage of the existing sparsity techniques applicable to large-scale power systems. Those methods are Unconstrained optimization approaches Nonlinear programming (NLP), Linear programming (LP), Quadratic programming (QP), Generalized reduced gradient method, Newton method, Network flow programming (NFP), Mixed-integer programming (MIP), Interior point (IP) methods and soon[50-56].

B. Artificial Intelligent Techniques

Artificial Intelligence (AI) techniques proved to be effective tools to resolve many power system problems and that they could be more effective when properly joined together with conventional mathematical approaches [43-46]. These techniques are Artificial Neural Network (ANN), Fuzzy logic, intelligent optimization, genetic algorithm, particle swarm optimization and soon. Different PSSs were proposed based on these AI techniques [2,5,7,12,16,29,61,64,67,95,98].

C. Hybrid AI Techniques

Power system problems may effectively solved by the strengths and capabilities or fit the assumptions of a single AI technique. One approach to deal with these complex real world problems is to integrate the two or more techniques in order to combine their strengths and overcome each other's weaknesses to generate hybrid solutions [29]. Those techniques are Fuzzy neural network systems Fuzzy/ neural/expert/genetic systems, simulated annealing with, fuzzy/genetic/expert systems and soon [21-28].

IV. CLASSIFICATION OF OPTIMIZATION TECHNIQUES AND RELATED WORKS

A. Classification

Optimization techniques are applicable on different power system stages such as generation, transmission, distribution and customers side for minimizing different problems, and its percentage applicability as shown Fig. 3. The application areas are shown in Table I and its classification with optimization problem is shown in Fig. 4.

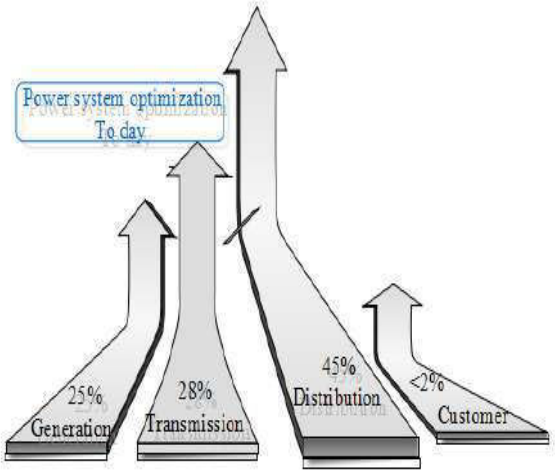

Fig. 3: Optimization techniques percentage applicability on power systems today

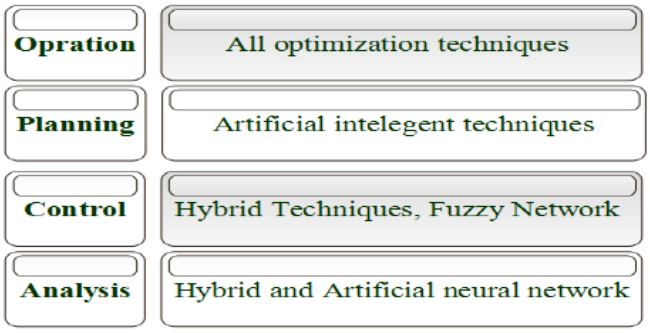

Fig. 4: Classification of optimization methods with its application depends on Table I.

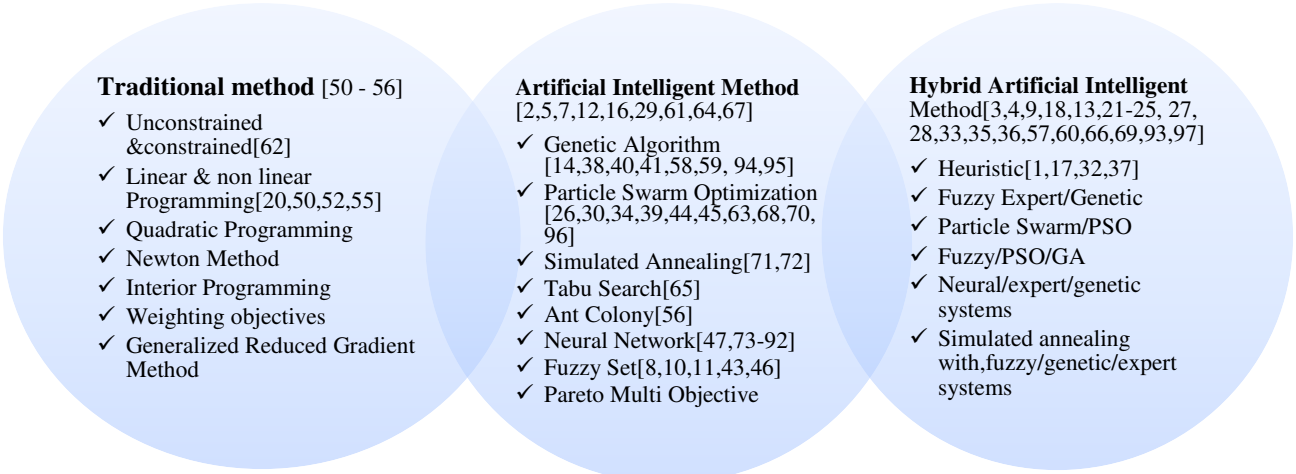

Fig. 2: Classification of optimization techniques and related works

TABLE I: Application of optimization techniques and related works.

Operation [2,5,12-19,26,27,31-34,38-42,45,46,50-66,68-71,81-90,96,97]	Control [3,4,6,7,9,10,36, 43,44,79, 92]	Planning [20-23,25,28,35,67, 72 - 78,80, 91,94,95]	Analysis [8,11,24,47,93]
✓ Constrained load flow ✓ Unit commitment / economic dispatch ✓ Optimal power flow ✓ Voltage/Var and loss reduction ✓ Dynamic load modeling ✓ Short-Term load forecast ✓ Network reconfiguration and load reduction ✓ Market operations, etc. ✓ Fault diagnosis ✓ Stability/Transient stability ✓ Static and dynamic security assessment	✓ Prioritizing investments in distribution network ✓ Optimal protection and switching device placement ✓ Reactive power control ✓ Power system control ✓ Relaying ✓ FACTS (Flexible AC Transmission System) control	✓ Reactive power planning ✓ Generation expansion planning ✓ Generation and distribution ✓ Generation scheduling ✓ Maintenance scheduling ✓ Power mix planning ✓ Capacitor placement/ voltage control ✓ Hydro scheduling ✓ Long term load foretasting	✓ Power system stabilizer ✓ Power plant operation optimizer

B. Advantages and disadvantages of some artificial intelligent techniques over traditional methods

Advantages:

- Artificial intelligent methods applicable for smart grid because of its modernity.
- Genetic algorithm needs only rough information of the objective function and places no restriction such as differentiability and convexity on the objective function.
- Genetic algorithm works with a set of solutions from one generation to the next, and not a single solution, thus making it less likely to converge on local minima.
- Genetic algorithm the solutions of developed are randomly based on the probability rate of the genetic operators such as mutation and crossover; the initial solutions thus would not dictate the search direction of GA.
- Fuzzy logic is more accurately represents the operational constraints of power systems and fuzzified constraints are softer than traditional constraints
- Ant Colony Search technique has been mainly used in finding the shortest route for transmission network
- The advantages of simulated annealing are, general applicability to deal with arbitrary systems and cost functions its ability to refine optimal solution, and its simplicity of implementation even for complex problems.

Disadvantages:

- Poor computational of the Ant Colony Search is the main drawback of this technique.
- The major drawback of simulated annealing is repeated annealing.
- Genetic algorithm method is requires tremendously high time.

V. OBSERVATIONS

- Some authors work with hybrid artificial intelligent technique's for better performance of all optimization problems.
- Others indicating Swarm intelligence has more potential in power system analysis and they are also the most recent in the field of computational intelligence technique.
- Many researchers indicates that simulated annealing are selected for arbitrary system, cost functions, refine optimal solution and simplicity of implementation complex problem.
- Artificial intelligence problems require use of knowledge bases to store human knowledge, operator judgment particularly in practical solutions, experience gained over a period of time, characterization by network uncertainty, load variations, etc.
- Power system optimization is aimed at improvements in more areas than cost: reliability, efficiency, economics, environmental friendliness, security.

VI. CONCLUSIONS AND RECOMMENDATIONS

A. Conclusions

Power system planning and operation raises many important decision making problems, which are generally stated as large scale, nonlinear, mixed integer continuous, and non-convex stochastic and or robust optimization problems. Many researcher works with different optimization techniques but still the issue is not solved. Using artificial intelligent techniques is the better choice compared with traditional methods but for any power system optimization problem hybrid artificial intelligent optimization techniques are still not comparable. Generally this review indicates which optimization techniques appropriate for power system problem such as profit, quality, efficiency and soon.

B. Recommendation

- ❖ It is recommended that using PSO and BFO based techniques are faster and more advance method for finding optimum load flow solutions.
- ❖ Using Improved or hybrid artificial intelligence methods are recommended to combine the better performance characteristics of various search methods .
- ❖ GWO is the most useful technique for solving the complicated OPF problem.
- ❖ IABCO was one among various optimization methods that produces better results. Maintenance of voltage profile, reduction of power loss, and optimization of reactive power has been facilitated by the algorithm.
- ❖ Usage of meta-heuristic genetic algorithms is recommended to find the optimal location for placing the FACTS device.

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A Privacy-Preserving Pay-by-Phone Parking System

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ABSTRACT—Most cities around the world require drivers to pay for the time they occupy a parking spot. In this way, drivers are encouraged to shorten parking time so that other drivers are given a reasonable chance of finding parking. The traditional way, based on moving to a pay station and placing the issued parking ticket on the dashboard of the car, presents several drawbacks like having to predict in advance the duration of parking or the need to move to the car in case the parking time has to be extended. Over the last few years, several applications permitting to pay through the mobile phone have appeared. Such applications manage detailed information about parking operations so that accurate profiles of parking habits of car owners can be created. In this paper we propose a system to pay for parking by phone which preserves the privacy of drivers in the sense that the information managed by the system is proven not to help an attacker with full access to it to do better that she would do by patrolling the city for collecting information about parked cars.

I. INTRODUCTION

THE amount of vehicles in cities is growing every day while it is hardly impossible to increase the amount of on-street parking bays. Restricting the maximum time a vehicle can occupy a parking spot is required to encourage a regular turnover of parking bays and give drivers a reasonable chance of finding parking. An accurate monitoring can only be carried out by installing in-ground sensors that send a notification to a parking officer when a car exceeds the parking time limit. In-ground sensors have been installed in several cities like Melbourne, Westminster or San Francisco. These systems are expensive to install and maintain. In San Francisco, maintenance of a single parking space is beyond $20 per month [5].

A cheaper solution is implemented by requiring drivers to pay for the time they occupy a parking bay. After parking her car, a driver moves to the closest pay station and makes a payment. Some parking machines provide credit card facilities as an additional option to coins. After that, the machine issues a parking ticket that has to be placed on the dashboard of the car. Parking enforcement officers patrol parking zones and monitor for violations which will be punished. Time restrictions are included by limiting the parking duration in a parking ticket. This way of limiting parking time is not accurate since a ticket which is about to expire can simply be replaced with a new one. Nevertheless, paying for parking time encourages most drivers to move their cars as soon as possible.

These systems present several drawbacks:

- Drivers must ensure to have sufficient coins prior to parking (if credit cards are not supported).
- Drivers have to predict (and pay for) the duration of parking in advance. If parking takes less time than predicted, the money corresponding to unused time is lost. If parking time has to be extended, the driver is required to move to the car.
- Moving to the pay station and coming back to the car to place the parking ticket takes time.

Many towns and cities provide the possibility to pay for parking by phone [8], [12]–[16], [19], [21]. A driver installs an app in her mobile phone and creates an account in which she indicates a source for funding such as a credit card number. Upon parking, the driver logs in her account, indicates her car license plate number, the area of the city she has parked in, and the expected duration. After that, a payment for the corresponding amount is performed. Some of these applications permit to interrupt a parking session so that the money corresponding to unused time is refunded. Also, a driver can extend parking time without the need to move to her car.

Parking officers are provided with a mobile device where they can type a car license plate number and check whether a payment for that car is in effect. In such a system, a system server that collects information of all the parking operations is required so that parking officers can query it. Data provided to pay-for-parking applications give rise to privacy concerns since all the parking operations performed by the same car can be linked through the car license plate number. Hence, the information collected by these applications permits to infer the parking habits of car owners.

A. Privacy in car technology

The European Union directive 2010/40/EU (7 July 2010) defines Intelligent Transportation Systems (ITS) as advanced applications which, without embodying intelligence as such, aim to provide innovative services relating to different modes of transport and traffic management and enable various users to be better informed and make safer, more coordinated, and 'smarter' use of transport networks.

The inclusion of intelligent devices and radio interfaces on vehicles opens the door to automatic data collection for tracking and monitoring of drivers' behaviour. Security and privacy has been widely addressed in the design of vehicular technology solutions by making use of advanced cryptography.

Privacy-preserving solutions have been proposed for Vehic-ular Ad-Hoc Networks (VANETs). In [7] the authors present a privacy-preserving system for vehicle-generated announce-ments based on the use of threshold digital signatures which

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is secure against external and internal attackers. The pro-posal [18] employs identity-based group signatures to divide a large-scale VANET into easy-to-manage groups and es-tablish liability while preserving privacy. In [6] anonymous credentials are used to protect the privacy of the drivers in a navigation scheme that utilizes the on-line road information collected by a vehicular ad hoc network to guide the drivers to desired destinations in a real-time manner. The authors in [10] propose an authentication framework which makes use of pseudonyms for privacy preservation in which legitimate third parties achieve non-repudiation of vehicles in certain situations like investigations for accidents or liabilities.

Privacy is also an issue in parking space management systems. The system described in [23] gathers information from sensors in parking spaces which is transmitted to drivers' mobile devices so that empty spots are viewed and can be reserved. The application considers privacy by encrypting the wireless communications. Nevertheless, since a parking reservation includes the Electronic License Plate (ELP), sys-tem servers are aware of the exact time a car checks in and leaves the parking lot. A similar proposal is presented in [11]. Bilinear pairing cryptography is employed for securing wireless communications. Transactions are performed by an on-board unit (OBU) which is assigned a pseudo-identifier employed to authenticate itself against parking lot road side units (RSU). Since the same pseudo-identifier is employed in all the transactions, profiles can be created.

Transportation systems in which vehicles collect data for services are vulnerable to fake data injection attacks. These attacks are partially avoided by preventing vehicles from send-ing data about places where they have not been. The authors in [24] present a system in which vehicles construct location proofs from the information received from roadside units. The system provides privacy by not including information about user's identifiers in location proofs.

B. Contribution and plan of this paper

In this paper we present a privacy-preserving pay-by-phone parking system. Privacy is provided by implementing an anonymous e-coin based payment system in which payments are performed for short time intervals. A spent e-coin remains anonymous unless a parking officer located close to a vehicle checks its parking status. In such a case, the spent e-coin can be linked to the car to prove that its driver has actually paid for parking her car. As a result of this query, the available information allows to determine that a payment for the present time has been performed, but it does not permit to get the start and end times of the parking operation. The system also permits a driver who has been fined unfairly to provide cryptographic evidences that a payment had really been made. Last but not least, our system does not require the driver to predict the duration of a parking operation in advance. The driver simply indicates the start and the end times upon parking and removing her car, respectively.

Section I introduces the paper by providing an overview about regulated parking zones together with a review of some papers that describe solutions providing privacy in car technology. After that, Section II surveys current pay-by-phone parking systems. Next, Section III describes the cryptographic tools used by our proposal while Section IV introduces the system and adversary models together with the privacy requirements to be provided by a privacy-preserving pay-by-phone parking system. The novel proposal is detailed in Section V. Its privacy and security properties are analyzed in Section VI. Section VII shows the performance of an An-droid implementation run over different mobile phones while Section VIII discusses some implementation and deployment challenges. Finally, Section IX concludes the paper.

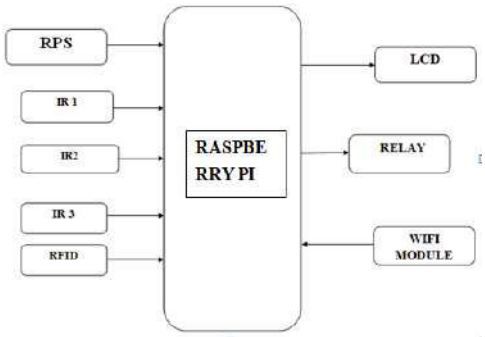
2. LITERATURE SURVEY

Internet of Things (IOT) plays a vital role in connecting the surrounding environmental things to the network and made easy to access those un-internet things from any remote location. It's inevitable for the people to update with the growing technology. And generally people are facing problems on parking vehicles in parking slots in a city. In this study we design a Smart Parking System which enables the user to find the nearest parking area and gives availability of parking slots in that respective parking area. And it mainly focus on reducing the time in finding the parking lots and also it avoids the unnecessary travelling through filled parking lots in a parking area. Thus it reduces the fuel consumption which in turn reduces carbon footprints in an atmosphere.

EXISTING SYSTEM:

In existing system Current parking systems are all manually operated systems with personnel deployed to handle the parking process. Here we propose a fully automated parking management system. Here we use a combination of IR and RF technology in order to provide an advanced fully automated parking management system. The system keeps track of vehicles entering and exiting the system. Also keeps track of the balance amount of the vehicle, deducts a particular amount when vehicle enters the parking premises. Our system first takes user id through his rf notification. It then tallies the rf code to check for user balance in account. If user has sufficient balance then the system waits for him to arrive at the parking gate. The gate uses IR sensors to detect a car arrival. Once the IR sensor pair detects it gives intimation to the system that the vehicle has arrived. The system then deducts balance from that particular account and increments the number of vehicles entered in the facility. It does not open the gate if user has insufficient balance. The system also continuously scans for number of vehicle exiting the gate through exit gate. An IR sensor pair at the exit gate is used for this purpose. When the sensor detects a car at exit gate it signals the system to decrease the count of parked vehicles by one. Thus we provide a fully automated parking management system that successfully parking space along with account balance management with ease.

3. BLOCK DAIGRAM

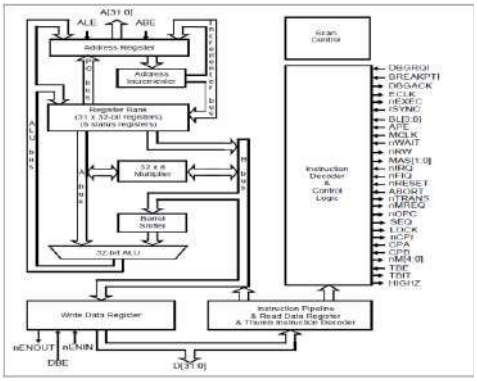


INTRODUCTION TO ARM ARM7 TDMI

The ARM7TDMI Core Diagram. The ARM7TDMI middle is based totally at the Von- Neumann architecture with a 32-bit information bus that consists of every instructions and records. Load, store, and swap instructions can get entry to statistics from reminiscence. Data can be eight-bit, sixteen-bit, and 32-bit.

Instruction pipeline

The ARM7TDMI center uses a three-degree pipeline to growth the glide of commands to the processor. This permits more than one simultaneous operations to take location and continuous operation of the processing and reminiscence structures. The instructions are done in 3 levels: fetch, decode and execute.



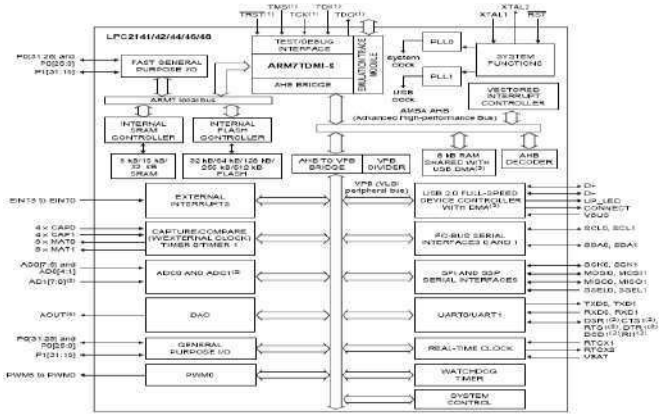
Memory interface

The ARM7TDMI memory interface is designed to permit most useful normal overall performance capability and minimize reminiscence utilization. Speed crucial control signals are pipelined to permit machine manage talents to make the most the short-burst access modes supported with the resource of many memory technology. The ARM7TDMI has four number one forms of memory cycle: Internal, Non sequential, Sequential, Coprocessor registers transfer. There is likewise the choice to apply each a unmarried bidirectional data bus or separate unidirectional data input and output buses.

4.LPC2148 MICROCONTROLLER

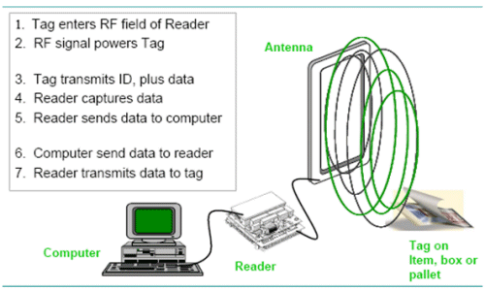
LPC2148 microcontroller board primarily based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace aid, that combine microcontrollers with embedded high-pace flash reminiscence beginning from 32 KB to 512 KB. A 128-bit massive reminiscence interface and precise accelerator structure enable 32-bit code execution on the maximum clock price. For vital code period applications, the possibility sixteen-bit Thumb mode reduces code through extra than 30% with minimum performance penalty. The that means of LPC is Low Power Low Cost microcontroller. This is 32 bit microcontroller synthetic through Philips semiconductors (NXP). Due to their tiny length and occasional power consumption, LPC2148 is right for packages wherein miniaturization is a key requirement, inclusive of get right of entry to control and factor-of-sale.

LPC2148 MICROCONTROLLER ARCHITECTURE



Working of RFID:

In a typical RFID system, tags are attached to objects. Each tag has a certain amount of internal memory (EEPROM) in which it stores information about the object, such as unique ID (serial) number, or in some cases more details including manufacture date and product composition. When these tags pass through a field generated by a reader, they transmit this information back to the reader, thereby identifying the object.



4 . EXPERIMENTAL RESULTS

The designed system has been implemented as an An-droid app. We have then measured the time required for e-coin generation and time slot payment. These are the two procedures that will be run frequently on drivers' mobile phone. The performance of the remaining procedures is not so relevant. For instance, the setup procedure is run just once after installing the application, while fine complaint will rarely be required. In any case, their complexities are similar to those of the measured procedures so that times with similar magnitude would be obtained.

TABLE II
MOBILE APPLICATION RUNNING TIMES (IN MILLISECONDS).

Mobile phone	Request 12 e-coins		Pay 12 time slots	
	Parallel	Serial	Parallel	Serial
HTC EVO 3D	3009	4958	2961	4874
S. Galaxy S III mini	2250	2835	2218	3043
LG Nexus 4	2977	4160	2932	4057
LG Nexus 5	559	1762	470	1428
LG Nexus 5X	326	553	264	539
Huawei Nexus 6P	300	520	218	479

Our implementation employs 2048–bit RSA and 224–bit elliptic curve keys which, as of 2016, are considered secure. We have measured the time required to request 12 e-coins and the time to pay for 12 time slots, both in serial and in a threaded parallel version of each procedure on a collection of Android phones with different capabilities. The following list summarizes their processors and Android versions. The RAM memory sizes are not included since the app requires very little memory.

HTC EVO 3D: Qualcomm MSM8660 Snapdragon S3 (Dual-core 1.2 GHz Scorpion), with Android 4.0.3.
Samsung Galaxy S III mini: NovaThor U8420 (1.0 GHz dual-core Cortex-A9), with Android 4.2.2.
LG Nexus 4: Qualcomm APQ8064 Snapdragon S4 Pro (Quad-core 1.5 GHz Krait), with Android 5.1.1.
LG Nexus 5: Qualcomm MSM8974 Snapdragon 800 (Quad-core 2.3 GHz Krait 400), with Android 6.0.1.
LG Nexus 5X: Qualcomm MSM8992 Snapdragon 808 (Quad-core 1.44 GHz Cortex-A53 & dual-core 1.82 GHz Cortex-A57), with Android 6.0.1.
Huawei Nexus 6P: Qualcomm MSM8994 Snapdragon 810 (Quad-core 1.55 GHz Cortex-A53 & Quad-core 2.0 GHz Cortex-A57), with Android 6.0.1.

Table II shows the measured times for requesting 12 e-coins (serial and parallel) and paying for 12 time slots (also serial and parallel) for each device. It has to be taken into account that the Nexus devices used in our experiments manage an encrypted filesystem which negativelly affects their performances, specially in the Nexus 4 model. Our experiments do not include the time due to delay in network communications since this is an aspect depending exclusively on the communication network. With the adventure of 4G networks, network delay will surely become negligible in the near future.

We have observed that the running time strongly depends on the device computation power. The slowest speed is obtained for the HTC EVO 3D mobile phone which was released on July, 2011. More up-to-date devices, like LG Nexus 5X and Huawei Nexus 6P, both released in 2015, provide ten times faster times. In all the cases, the measured computation times prove that the proposed system is feasible to be implemented for current mobile devices.

Regarding the complexity at the server side, the system has been tested on a computer with an Intel i5-4460 3.2 GHz processor. In our experiments, a single core was able to compute more than 50,000 RSA blind signatures per second, which is the cryptographic operation performed by the server when generating an e-coin. Regarding the reception of e-coin payments, a single core could validate up to 170 e-coins per second. In a quad-core parallel implementation, we achieved over 200,000 RSA signature computations and 680 e-coin validations per second.

VIII. IMPLEMENTATION AND DEPLOYMENT CHALLENGES

The system server should be deployed on a computer with a reliable Internet connection placed in a secure en-vironment protecting it against eventual attacks aiming to disrupt it. Hence, placing it in a data center with intrusion detection and protection mechanisms is recommended. We also recommend to contract the services provided by an online payment provider to deal with the payments received from the drivers when acquiring e-coins. The timestamp server could be deployed on the same computer but it would be better to place it on a separate machine accessible only from the system server.

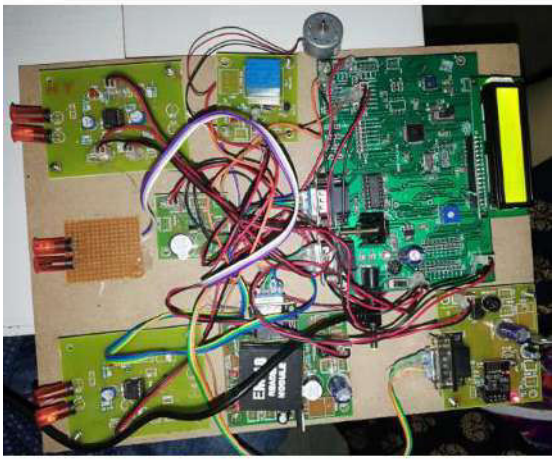
Regarding the mobile app (run by drivers), it must be run on a mobile phone with an Internet connection. The system makes use of direct client-server communications against the server during the e-coin request and fine complaint procedures, and a client-server anonymous communication during time slot payment procedure. Software implementing anonymous communications for mobile phones is currently available. The mobile device should be NFC enabled, which is a common feature in nowadays mobile phones, for communicating with the on-board device during setup.

Parking officers carry a mobile device with an Internet connection and an HF RFID reader capable of querying the on-board device. Such devices are already available.

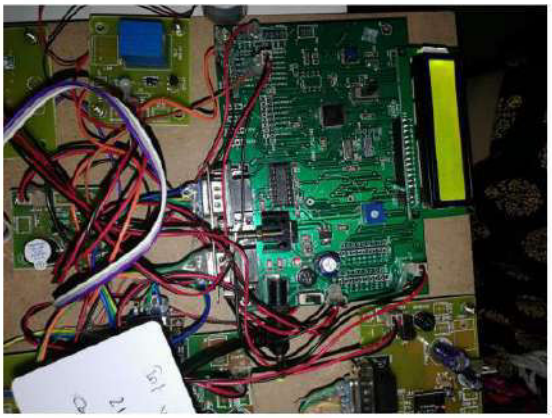
The most challenging part is the on-board device to be placed in cars. That device should be composed of a smartcard–type tamper–resistant processor able to compute HMAC digests and AES decryption operations. It also carries an internal clock which requires the device to be fed through its own batteries. Regarding communications, the device has to be able to act as a receiver for NFC communications (run during the setup procedure) and respond to RFID queries coming from parking officers.

As for the cryptographic operations, there already exist smartcard processors implementing the required operations. Some of them support 128-bit AES encryption/decryption and SHA-1 among others. NFC operates at the 13.56 MHz frequency, also used by High-Frequency (HF) RFID tags.

Working model:



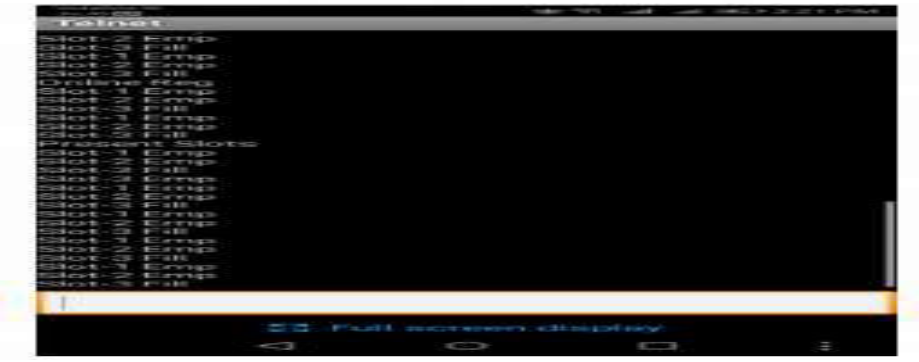
RFID activated time



With power supply

WIFI MODULE:

OUTPUT RESULTS:



4

5 . CONCLUSION

A privacy-preserving pay-by-phone parking system has been presented. From the driver's point of view, the system is composed of two components: an RFID and NFC enabled on-board device which is placed in the car, and an app which is installed in the mobile phone.

The app manages an electronic wallet which is loaded with e-coins. When the driver parks her car in a regulated area, the mobile app starts making periodic e-coin payments for short time intervals until the car is removed from the parking spot.

The system has been proven to provide privacy by not allowing the creation of profiles about drivers' parking habits. The system is also secure against e-coin forgery and double-spending and permits a driver who has been fined unfairly to prove, by providing cryptographic evidences, that a payment had really been made.

In the future we plan to investigate the design of the app focusing on its usability. Together with the design of the graphical interface, we will also investigate solutions permitting to use the application even when the driver expects to be out of coverage during part of the time her car is parked.

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PAPR REDUCTION OF FBMC/OQAM SYSTEMS AND BER ANALYSIS

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Abstract: Filter bank multi carrier (FBMC) is a modulation technique with enhanced spectral properties and also finds an alternate solution for cyclic prefix based OFDM system in coordination with offset quadrature amplitude modulation (OQAM). Peak to average power ratio (PAPR) is still a defined problem in this system; in this paper a modified selective mapping (SLM) approach is proposed for the reduction of PAPR and selection of optimal candidate signal. The proposed approach experimental results reveal that this approach is performing better than tradition FBMC-SLM approaches under different channeling environments.

Keywords: OFDM, FBMC, OQAM, PAPR, OBI

I. INTRODUCTION

Since three decades OFDM is widely adopted in many of the broadband wired and wireless communication systems because of its high range of advantages over other technologies like carrier and symbol synchronization, low ICI, maximum collection of narrow bands over a limited available bandwidth and many. However, the time frequency resources cannot be assigned flexibly leading to poor performance and spectral behavior for high data rates [1]. Filter bank multi carrier (FBMC) with OQAM provides a solution for poor spectral efficiency by employing the pulses that are localized in both time and frequency. Many properties of FBMC is similar to OFDM and one of the critical issue is implementing of this is its high PAPR value [2].

FBMC with OQAM provides several advantages over traditional OFDM systems like (i) the cyclic prefix is no longer required (ii) the side lobe of its power spectrum density is very low [3]. However this system also suffers from few disadvantages like heavier computation cost due to extra filtering operation, complex channel equalization and channel estimation due to the presence of imaginary interference components. This work is concentrated on reducing PAPR value and to provide good spectral efficiency by reducing the side lobes.

Several works were proposed in past few years on reduction of PAPR for FBMC systems; in [4] Rahim et. al introduced clipping based reduction scheme for OFDM/OQAM systems. However, the bit error rate is increased and also the side lobe. In [5] Kollar et.al, proposed a iterative noise cancellation technique by employing Bus-gang noise cancellation at the receiver but it increased the decoder complexity at the receiver. In [6] Javaudin et.al proposed SLM (selective mapping) approach for reducing PAPR in which the OFDM/OQAM symbol is divided into two parts 2K parts (K:length of the prototype filter). Due to the selection of random phase rotation vectors the performance was poor when K is too long. In [7] Yuen et.al, inserted a precoded matrix in between the multiplexer and OFDM/OQAM modulator to reduce PAPR. In [26] and [27], a sliding window tone reservation (SW-TR) technique has been proposed. The SW-TR method utilizes the peak reduction tones of several consecutive data blocks to cancel the peak power of the FBMC/OQAM signals inside a window. In this paper a progressive SLM approach is proposed to reduce the PAPR while attaining good BER performance and side lobe efficiency. This paper is organized as follows, the first part presents introduction to OFDM/OQAM systems, its importance and the research done so far by different authors. In the second part the topology of OFDM/OQAM system, its architecture and mathematical analysis is presented. Third part presents the proposed approach for minimizing the PAPR. Fourth part presents the experimental results obtained with the proposed approach under different constraints and conditions ending with conclusions.

Procedure for Paper Submission

OFDM/OQAM system

This has drawn much interest in research due to its high spectrum efficiency where the signal is obtained by summing M time shifted OFDM/OQAM symbols each of which is obtained by passing QAM symbols through a prototype filter [2].

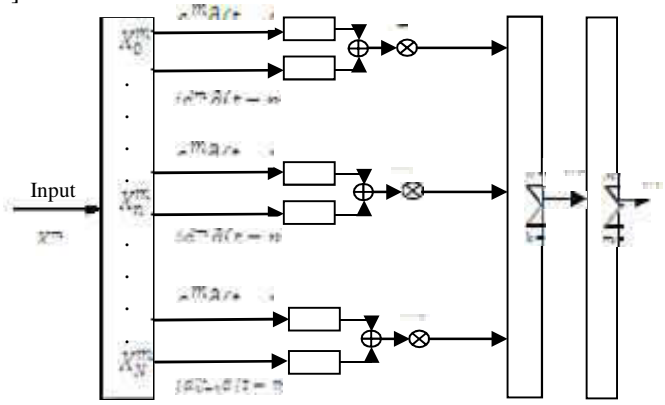

Figure 1: Block diagram of OFDM/OQAM system

The OFDM/OQAM transmitter structure is depicted in figure 1 which consists of „N" number of sub carriers, after the QAM modulation the input symbols are first converted into parallel form by serial to parallel converter which can be represented as

$$X = [X^0, X^1, \ldots\ldots\ldots, X^{M-1}] \quad (1)$$

Where „M" is the number of data blocks and X^m is the m^{th} data block which is defined as $X^m = [X_0^m, X_1^m \ldots\ldots\ldots X_{N-1}^m]^T$, Where „N" represents the number of subcarriers then

$$X_n^m = c_n^m + jd_n^m \quad (2)$$

Where „c" and„d" represents the real and imaginary parts of X_n^m . The real and imaginary parts of X_n^m are staggered by T/2 and passed through the prototype filter to obtain

$$x_n^m(t) = c_n^m h(t - mT) + jd_n^m(t - \frac{T}{2} - mT) \quad (3)$$

Where h(t) is the response of the prototype filter. Here in this paper the prototype filter coefficients is represented below

$$h(t) = \alpha(c(0) + 2\sum_{i=1}^{K-1}(-1)^i c(i)\cos(\frac{2i\pi}{KN}t)) \quad (4)$$

Where α is the normalization factor and c(i),i=0,1……K-1 are given as c(0)=1 ,c(1)=0.97195 c(2)=0.7071 c(3)=0.23514

The modulated symbols in N orthogonal sub carriers is represented as

$$S_n^m(t) = \{c_n^m h(t - mT) + jd_n^m(t - \frac{T}{2} - mT)\}e^{jn(\frac{2\pi}{T}t + \frac{\pi}{2})} \quad (5)$$

For K=0, 1, 2….N-1. Then $S_n^m(t)$ on all the N sub carriers are added up together to obtain

$$S^m(t) = \sum_{n=0}^{N-1} s_n^m(t) \quad (6)$$

The desired OFDM/OQAM signal is represented as

$$s(t) = \sum_{m=0}^{M-1} S^m(t) \quad (7)$$

For $0 \le t \le \left(M + N - \frac{1}{2}\right)T$. Finally the PAPR for the system is represented as

$$PAPR = 10log10(\frac{\max_{pT \le t \le (p+\frac{1}{2})T}|s(t)|^2}{Pave}) \quad (8)$$

Where Pave: is the average power of S(t)

3. Proposed Approach

The main intension of the proposed approach is to optimize the phase sequences in a sequential manner. By considering previous block symbols may reduce the peak power of the current block that is $S^0(t), S^1(t), \ldots\ldots S^{m-1}(t)$ may reduce the peak power of $S^m(t)$. Initially at the zeroth block $S^0(t)$ by different phase sequences and chose the one with minimum peak power which is then forwarded to the first block which is represented as below

$$\min_{b^{1,u}} \max_{2T \le t \le 4T} |\hat{S}^0(t) + \sum_{n=0}^{N-1} S_n^1(t) b_n^{1,u}|^2 \quad (9)$$

The optimal phase rotation vector is denoted as $b^{1,u*}$ and the new symbols generated are represented as

$$\hat{S}^1(t) = \sum_{n=}^{N-1} S_n^1(t) b_n^{1,u^*} \quad (10)$$

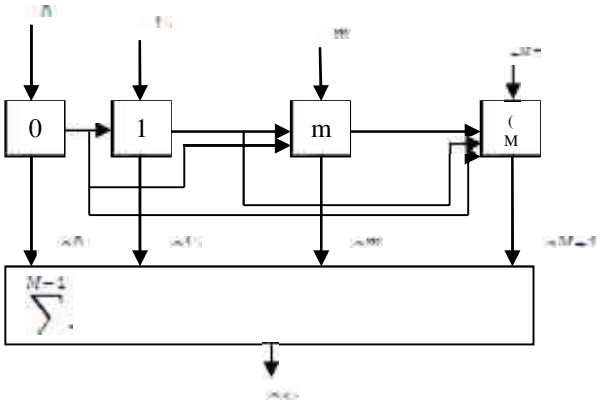

Figure 2: Block diagram for the proposed approach

Both these symbols are sent to the second block for the calculation of new symbols and this process is repeated till M-1 blocks, all merge together to for the OFDM/OQAM signal.

4. Experimental Results

Simulations were carried with N=256 sub carriers under 4, 16-QAM modulation schemes. The proposed approach is compared against tradition SLM OFDM [10], PTS OFDM [11] and FBMC SLM [6] approaches. Parameters like CCDF (complementary cumulative distribution function), BER (bit Error Rate) and PSD (power spectral density were considered to evaluate the performance of the proposed approach.The BER performance is evaluated under AWGN (additive white Gaussian noise) environment and Rayleigh fading channel environment.

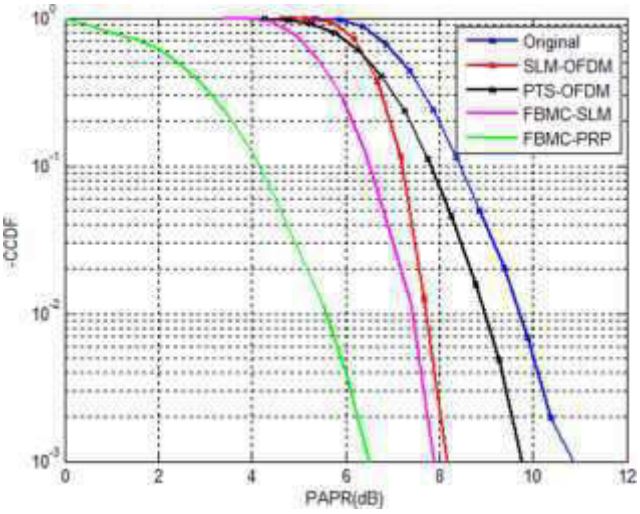

Figure 3: CCDF Vs PAPR with N=256 and 16-QAM modulation

From figure 3 graph it can be observed that the proposed approach is obtaining 0.8dB less PAPR than conventional FBMC based SLM approach at CCDF of 10^{-3}

The above figure depicts the PAPR analysis of the proposed approach at different values of „U" it is clearly observed that at U=32 it obtaining a CCDF of 10^{-3} at 6.2dB which is less than 0.7 db when compared with other methods.

From all the experimental results it is evident that the proposed approach of sequential adding of blocks yielding

better results in terms of BER, PAPR. It can also be observed that it can provide a high spectral efficiency as shown in figure 7 & 8.

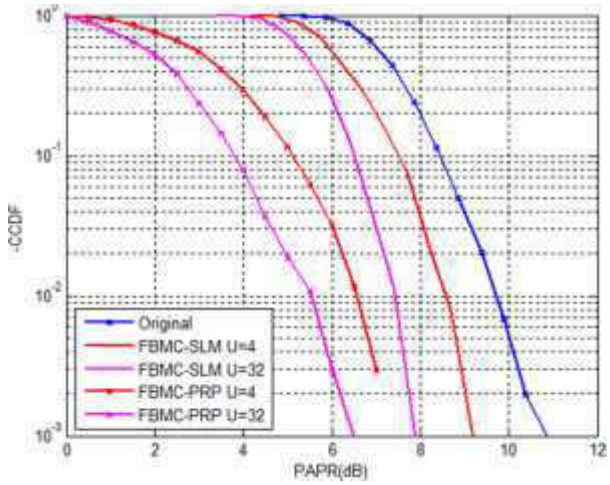

Figure 4: CCDF Vs PAPR with N=256,sub-carrier and at U=4 & 32 for 16-QAM

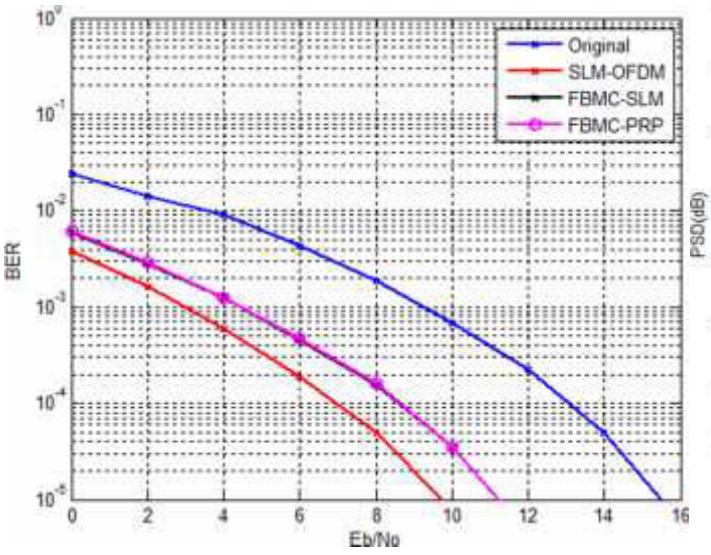

Figure 5: BER performance under AWGN channel with N=256, 16-QAM

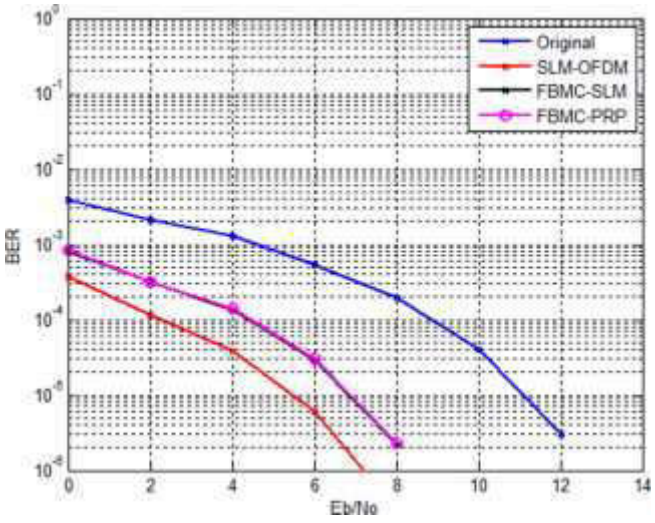

Figure 6: BER performance under Rayleigh channel with N=256 & 16-QAM

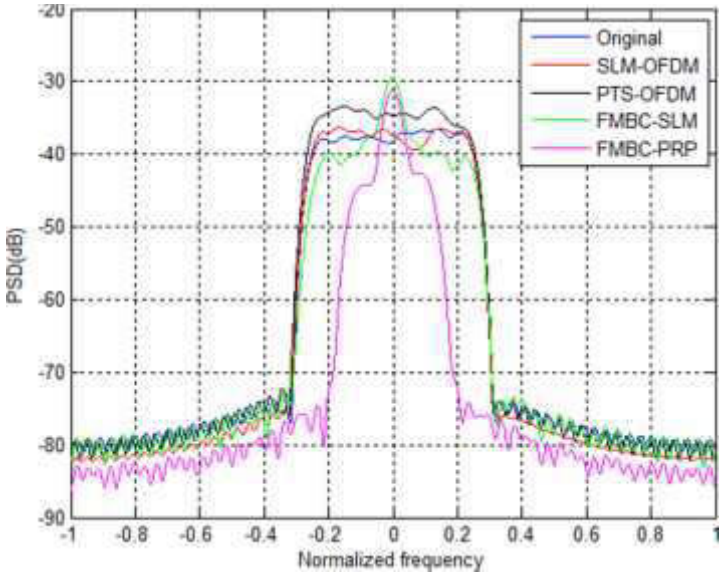

Figure 7: OBI performance with N=256 subcarriers

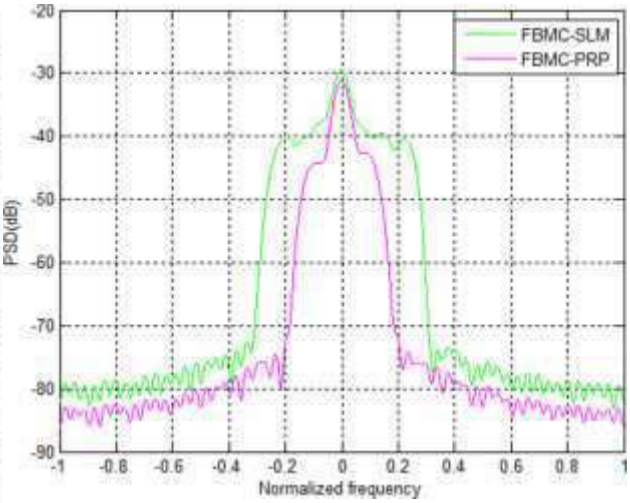

Figure 8: OBI performance and comparison with FBMC-SLM

Conclusion

A PAPR reduction approach for FBMC OFDM/OQAM system is proposed in this paper, the method is simpler in implementation as it involves the summation of the previous blocks ith the current blocks of the symbol. Experimental show that the proposed approach could attain a considerable better performance when compared against the traditional OFDM approaches like SLM, PTS and FBMC based SLM approach. The method can be further improved by introducing the new phase sequences and testing under different channeling environments.

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A SURVEY ON LOW POWER WIRELESS BODY MOUNTED SENSORS FOR HEALTH MONITORING

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Abstract—This paper describes the design of a custom LSI which operated at less power nearly 0.5 μW for wireless sensor nodes used in animal health monitoring systems. A wireless sensor network system is composed of sensors, signal processing units, receiver and other components. There is a huge requirement to monitor body temperature and activity of animal or human with low power consumption, low power sensors and ultra-low power signal processing are essential. This presentation depicts low power technologies of wireless sensor network system developed for chicken health monitoring system. The average power consumption calculated of the wireless sensor node is less than 1**μW.** Here the Measurement method with bimetal type and piezoelectric type MEMS sensors which need almost no electrical power and on chip circuits of multistep selectable voltage reference generator for comparators to detect the output signal of the sensors. The piezoelectric sensor which generates even 1 mV of output voltage can be utilized by this method. The LSI consists of CMOS combination logic circuits and works at low frequency and RC oscillator to decrease the power Utilization.

Index Terms— LSI, MEMS, ultra low power, sensor network, health monitoring, chicken.

I. INTRODUCTION

Wireless sensor networks which consist of a lot of wireless sensor nodes distributed in our surrounding and linked together are expected to be used for health and medical monitoring applications as well as environmental monitoring[1], control and security .In general a wireless sensor node, consisting of sensors, a transceiver (or transmitter), a battery. In addition to this the sensor node functions, miniaturized and performance improved by using Micro electro mechanical systems (MEMS) technology. The MEMS technology is contribute to realization of autonomous sensor nodes without batteries by providing a small high-efficient energy harvesting device. Recent research has focused on hen productivity, feed consumption, health, or the quality and investigating the dynamic behavior and activity of hens housed in indoor non-cage environments. In this paper we report the results of a lightweight wireless body mounted wireless sensor system used monitor the activity of laying hens within non-cage housing systems. As an application of wireless sensor network, our group has been developing a global avian influenza surveillance system by monitoring the health of chickens with wireless sensor nodes in poultry farms[3]. The highly pathogenic avian influenza (HPAI) virus (H5N1) infection in birds has continued, and has acquired pathogenicity not only in birds but also in

mammals. The more cases of migratory birds and domestic fowls increase, the more human cases increase and the variation of the virus progresses. Consequently, risks of occurrence of a pandemic flu with transmissibility among humans increase. Therefore a global avian influenza surveillance system for the early-stage detection of birds cases must be effective to defend human beings from an influenza pandemic.The concept of our avian influenza surveillance system[5] is initial diagnosis with body temperature and activity of a chicken. In previous research, we carried out the infection experiments and found that the both sensors are useful tool for early detection. Several percentages of chickens in poultry farms are attached with wireless sensor nodes with thermistor and accelerometer. When the surveillance system detects an anomaly state of the chickens, the system automatically alerts administrators through the internet. The system can also report a history of health conditions (fever and weakness) obtained by sensors. Finally, using these data, the administrators decide whether this incident is caused by avian influenza or not. Basically, chickens have vaccinations against diseases caused by viruses except for influenza. Thus if many chickens shows abnormal states, the cause is likely to be due to influenza viruses. Although chickens can become abnormal states by physical stresses, e.g. summer heat, we can find if the cause is influenza or not by finding that how the chickens showing abnormal state spread out in a chicken house. In the case that the cause is influenza, these chickens could increase in a concentric fashion. Thus, we have to attach a wireless sensor node to some quantity of chickens in a chicken house. This paper describes avian influenza outbreaks would be detected 2 days earlier if 5 % of chickens in a chicken[6] house are attached a wireless sensor node than the current patrol system by farm workers Radio frequency identification (RF-ID) system is used for identification in livestock industry or pets. The advantage of the RF-ID system is low cost and long life time, however, the communication length is less than 1 m and the measurement of the body temperature or movements of an animal can be done only when a reader is brought close to the tag. Thus, RF-ID system is not suitable for continuous monitoring. On the other hand, in the case that we use wireless sensor nodes with transmission function using the own battery the power consumption has to be decreased[7]. For the avian influenza surveillance system, the nodes should work continuously for periods of longer than 2 years without battery replacement. Because the period when chickens produce eggs well is about 500 days. In addition, since the weight of the wireless sensor node including a battery should be less than 1 g, small button battery has to be used. Thus, an upper limit of the average power consumption could be 1 μW level.

Previously, earliar a development of an ultra low power custom LSI which has signal processing and wireless transmission functions and wing band type wireless sensor node.This paper, describes a wireless sensor node using a **"S"** shaped piezoelectric micro-cantilever with more sensitive to tiny movements of a chicken than ordinary type micro-cantilever. And thermistor is used as not only body temperature measurement but also mode change event generator to reduce the power consumption. In addition, a demonstration experiment using more than

100 wireless sensor nodes in a chicken house are reported.

II. TECHNICAL CHALLENGES

The major challenge involved in the behavior detection of chickens is two-fold, both of which stems from the size of the subject. First, the size and weight of the sensor should be such that when it is mounted on a chicken, it does not cause any significant change in its natural behavior. This limitation does not exist in larger animals like cattle and hence sensors equipped with better processing capabilities and larger batteries, which might be bigger in size, can be used without any considerable concerns. Second, due to their smaller size and general movement patterns, the magnitude of acceleration produced by their movement is not significant when compared to that of larger animals, and hence the state space of accelerometer values obtained from chickens is very small compared to that of larger animals. The brief and jittery movements produced by chickens result in a weak correlation between the accelerometer data and the activity of the individual, which makes the behavior detection non-trivial. Furthermore, while all the accelerometer data mentioned above has provided valuable information about the behavior of the individual animal, most sensors were designed to store the accelerometer data on the sensor itself. Therefore, at some point, the accelerometer needed to be physically retrieved for data recovery and subsequent analysis, and hence, the animal must be re-caught for the data to be accessible. Thus, the current systems do not provide remote sensing and real-time instantaneous information about events of interest. Instantaneous access to data can be very useful for researchers and animal managers who could use this information about individual hen behavior to make adjustments to the system or catch problems at early stages.

Fig: Photograph of a laying hen wearing a wireless sensor

III. LITERATURE REVIEW

In order to decrease the power consumption, the design that the LSI consists of CMOS combination logic circuits and works with 1.55V VDD (button battery). In addition, since the signal processing do not need high speed, this LSI operates using 1 kHz RC oscillator. The estimated consumption current of RC oscillator is 134 nA.

A. Input circuit for accelerometer

The enough data about activity of chickens for this surveillance system is the number of movement with 1 axis acceleration over a threshold exceeds a setting value. In this case, a 1 bit A/D converter, e.g. CMOS inverter and a comparator, is enough for this sensor. Although a CMOS inverter is the least power consumption circuit, the threshold voltage is high (about 0.7 V at 1.55 V of VDD). In addition, the threshold voltage of a CMOS inverter cannot be adjusted. There could be individual specificity of the output voltage of a piezoelectric accelerometer. And the output voltage is very low (several mV) at slow chicken's movement. Thus, the designed one

is a comparator of which threshold voltage can be changed as the input circuit of the accelerometer.

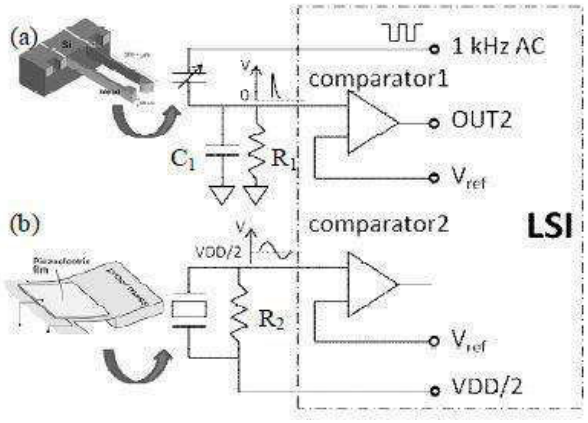

Figure 2. Input circuit for (a) MEMS bimetalthermometer (b) MEMS piezoelectric accelerometer

Fig. 2 shows a circuit by which an output voltage of a piezoelectric accelerometer can be detected even if the output voltage is 1 mV at slow chicken's movement. Generally, a comparator most sensitively detects a voltage difference if the voltage reference (Vref) is the half of a supplied voltage (VDD).Thus ,to raise the output voltage of the accelerometer, one electrical pad of the accelerometer was connected to VDD/2. The comparator input is stabilized by R2 resister in fig. 1 connected to VDD/2 output. In the case that Vref is VDD/2 + 1 mV, the output of the comparator changes if the output voltage of the accelerometer is over 1 mV. In order to reduce the power consumption of the comparator, the bias current of the comparator was decreased down to 10 nA using an external 50 MΩ resister. The calculated total current of the comparator is 20 nA.

B. Input circuit for body temperature sensor

When a chicken is infected with the influenza, although the change of the body temperature depends on the viruses, the body temperature basically increases. For example, when a chicken is infected with a certain highly pathogenic avian influenza virus, the chicken died with slight (0.6 ^{0}C) fever. In this case, it is difficult to detect the infection with a body temperature sensor. However, since the activity of a chicken infected with any viruses decreases, we can find the infection earlier with the accelerometer. Because there are viruses which induce high fever (2.4 ^{0}C) and the infection can be found with a temperature sensor. From these results, we decided that a chicken of which body temperature is more than 42 ^{0}C (fever) or less than 38 ^{0}C (just before death) could be anomaly state. Fig. 2 shows the input circuit for the variable capacitor type MEMS bimetal thermometer. This sensor is composed of 2 bimetal cantilevers like fig. 2. One cantilever connects with an output of 1 kHz AC signal and the other cantilever connects with capacitor C1, resistor R1 and input of a comparator. First, one tip of the cantilever is away from another tip and the capacitance between 2 cantilevers is almost zero. In this case, the 1 kHz AC signal cannot go through the bimetal sensor. When the surrounding temperature change, the 2 tip of cantilevers approach each other. And then the capacitance between the 2 cantilevers increase and the AC signal starts to flow through the bimetal sensor. Thus, the sensor works like a switch. The capacitance of C1 is for accumulation of the signal. The resistor R1 is for stabilize the voltage of input of the comparator. The temperature at which the AC signal starts to flow through the sensor can be

changed by changing the length of the cantilever. We have been fabricating 2 bimetal sensors which are electrically on-state at more than 42 ^{0}C or less

than 38 ^{0}C. Since the basal body temperature of a chicken is 41 ^{0}C, these sensors are off-state when the chicken is in good physical health. Thus, in this health state the power consumption of the circuit is zero because the AC signal cannot be flow. On the other hand, when the health state of the chicken becomes bad, the AC signal flows to the input of the comparator and to the R1. In this case leak current of input of the comparator and the current flowing through R1 are consumed. If the R1 has high resistance, the power consumption of R1 can be neglected.

C. Multi-step voltage refecence(Vref) generator

Fig. 3 shows the on-chip circuit of Vref generator which gives 32 voltages from VDD/2 + 16 mV to VDD/2 -16 mV with 1 mV increment. Because Vref has to be optimized for each accelerometer, we need to be able to select the Vref by one-time programmable ROM. Generally, divided electrical potentials can be obtained by cascade connected transistors. However, if the voltage between the gate and the souse (V gs) is too small by large number of connected transistors, little current flows in the transistor. In the case of 1.55 V of VDD, the potential can be unstable. We connected transistors like fig. 3 to supply enough current. The calculated consumed current of this circuit was about 13 nA.

D. Work flow

Fig. 5 shows the work flow of the designed LSI. The MEMS bimetal thermometer changes the operation mode depending on the body temperature of a chicken. When the body temperature is from 42^{0}C to 38^0 C, the

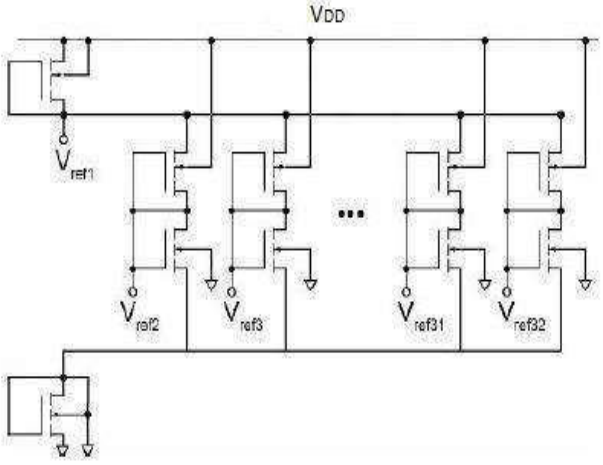

Figure 3. On-chip circuit of Vref generator for the comparators.

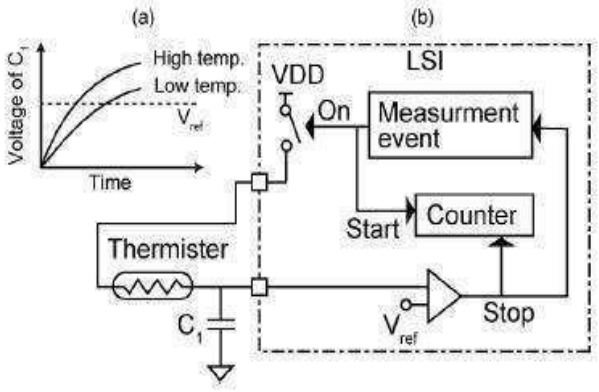

Figure 4. (a) Voltage change of the capacitance C1 (b)Measurement circuit for the thermister.

transmission event is occurred by the accelerometer. The LSI count the number of movement with acceleration over a threshold exceeds a setting value. If the count is over the setting value, the LSI transmits only the body temperature data measured by thermister. The activity of a chicken is shown in the receiving frequency. Therefore, if the frequency of the receiving become low, we can find that the health state of the chicken is not good. On the

other hand, the body temperature is more than 42^0C or less than 38^0C, the transmission event occurred by timer in the LSI. Because when the body temperature of a chicken is in that range, the chicken become low spiritedness then the transmission event almost does not occur by the accelerometer.

E. Measurement method for thermister:

fig.4 shows a circuit for a thermister. The thermister and capacitance C1 compose a integrating circuit. When the thermister measurement event occur, one electrode of the thermister is connected to the VDD and the counter in the LSI starts to work at the same time. When the voltage of the C1 increases up to a voltage reference, the counter stops. The value of the temperature is the count value.

IV. SYSTEM MODEL

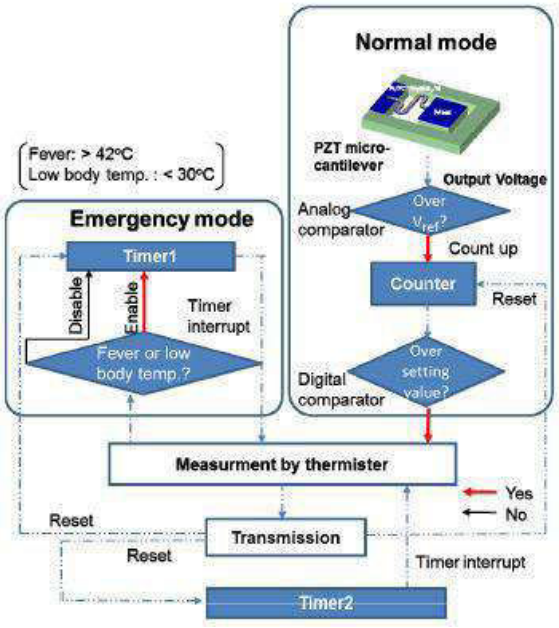

Figure 5:the work flow of the wireless sensor node

Fig. 5 shows a work flow of the developed custom LSI. There are two operation modes and the LSI changes the modes depending on the body temperature. In the normal state, the transmission event is occurred only when the activity, accumulated the number of acceleration which is over a threshold acceleration, exceeds a threshold number. If the chicken is infected and becomes weak, the transmission event may not be generated. In this case, we cannot know whether the wireless sensor node was broken or the chicken became weak for a long time. To avoid this situation, we designed that the transmission event can occur by a timer (Timer1) when the chicken's body temperature becomes abnormal state. In this system, the interval time is set to 10 minutes. In this system, the thermistor checks the body temperature per the transmissions and changes the mode if the body temperature is over 42^0C (fever) or below 30^0C (low body temperature caused by the death). In the previous research, a switch type MEMS temperature sensor which composed of two bimetal cantilever always monitors the body temperature and changes the mode if the body temperature becomes abnormal state [8,9]. The power consumption of this MEMS sensor is almost zero. However the current consumption of the input circuit is need and it is better to reduce the number of components on this wireless sensor node to decrease the cost. In this system, we use another timer (Timer2) to alternate the MEMS temperature sensor. In this case without the MEMS sensor, the event to measure the body temperature by the thermistor is never occurred unless the chicken's activity is over the threshold. This timer generates the event of thermistor measurement. In order not to increase the power consumption, the interval time of this timer is set to relatively longer time, such as 30 minutes. To realize this work with ultra low power, we must decrease the power consumption of the components which always work. In this system, the clock source and activity sensor and the circuits for signal processing of the sensor input are mainly power consumed devices. In this system, we

introduced a piezoelectric micro-cantilever as a zero power activity sensor and a comparator. The piezoelectric micro cantilever can generate charges by chicken's movements, then the necessary power to activate this sensor itself is zero. In the previous research, piezoelectric micro- cantilever with ordinary shape was used [8,9]. The cantilever generated charges, however, the output voltage is small not enough to detect at tiny movement of a chicken. In this research, "S" shaped piezoelectric micro-cantilever [10] like fig. 6 is used. The output voltage of the "S " shaped micro-cantilever is about several mV at 0.05G and 6 Hz of input acceleration.

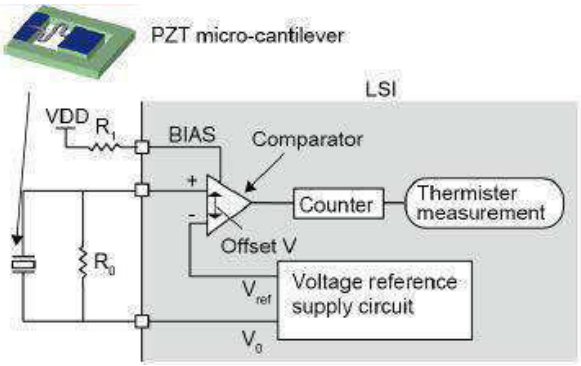

Figure 6: Schematic diagram of the work flow of the developed wireless sensor node.

The required data to detect an abnormal state of chickens at an early stage were already decided by the simulation using data obtained by influenza infection experiments [5]. The results indicated that the infection can be detected before more than about 40 hours of the death with detecting the fever. Although a chicken infected with HPAI viruses basically has a fever, there are HPAI viruses, such as A/chicken/Yamaguchi/7/2004(H5N1)/CkYM7 , which cause the death without a fever [11]. However, the activity of chickens infected with all viruses is decreased. We developed a detection method using the number of 1-axis acceleration which exceeds a threshold. In this case, the average detection time was about 6 hours with detecting the lower activity than before 24 hours [5]. Using this method, we can use 1 bit A/D converter. Fig. 6 shows the circuits to realize the above method at ultra low power. A comparator is used as 1 bit A/D converter. The output signal of the comparator is entered into a counter. If the count value exceeds a threshold value, the thermistor measurement event occurred based on the work flow. The calculated current consumption of the comparator including bias current is 20 nA. In this system, a voltage generator for the reference voltage of the comparator was integrated. The calculated current consumption of this voltage generator is 16 nA.

Table 1: Power consumption of the developed wireless sensor node.

	current (nA)
1kHz RC clock	134
BIAS for comparator	10
comparator	10
Voltage reference	30
Logic off leak	22
Total standby current	206
Total standby power	320 nW

Table 1 shows the calculated current consumption at standby state. The total power consumption is 320 nW using 1.55V button battery. Assuming that the transmission current, time and transmission interval are 10 mA, 2 ms and 5 minutes, the average current consumption is about 70 nA. Therefore the total average power consumption including thermister measurement is about 460 nW. If a small button battery with 30mAh is used, the estimated life time is more than 10 years.

V.RESULTS

Fig. 7 shows the developed wing band type wireless sensor nodes with "S" shaped piezoelectric micro cantilever and thermistor. This wireless sensor node consists of two parts connected by a flexible cable. One part is the

main substrate including custom LSI, ceramic packaged piezoelectric micro cantilever, passive components and patterned loop antenna for 315MHz. The custom LSI was bonded to a printed circuit board directly and then covered by a resin. The other part is battery substrate with thermistor. A SR726W with battery capacity of 30 mAh and size of 7.9 mm and 2.6 mm height was used. The battery fixture has two holes at both sides to support the fixing pin. The main substrate also has two holes to pass the fixing pin. How to fix the wing band type wireless node to a chicken is to pass the fixing pin through chicken's arm and the holes in the main substrate, then the end of the fixing pin was bent like a stapler. The demonstration experiment was carried out in a chicken house. We attached 120 wireless sensor nodes to chickens and monitored the chicken's health for 1 week. Fig. 8 shows a result. It was found that the necessary data for the system could be measured during this period.

VI.CONCLUTION

We developed the ultra low power wireless sensor node with continuously monitoring of activity for chicken health monitoring system. The calculated power consumption of the wireless sensor node with piezoelectric micro-cantilever and thermistor is 320 nW. If SR726W with 30mAh of battery capacitance is used, the estimated life time is morethan 10years.

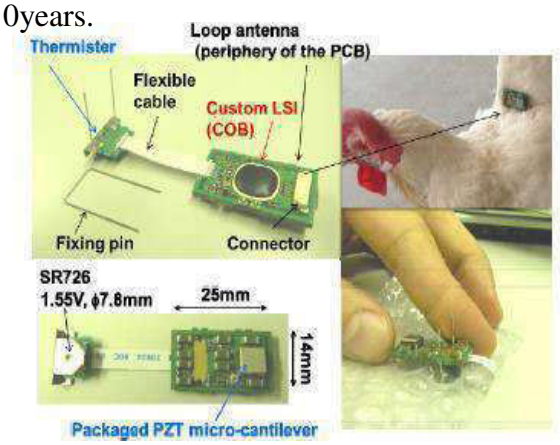

Figure 7: Photograph of the developed wing band type wireless sensor node.

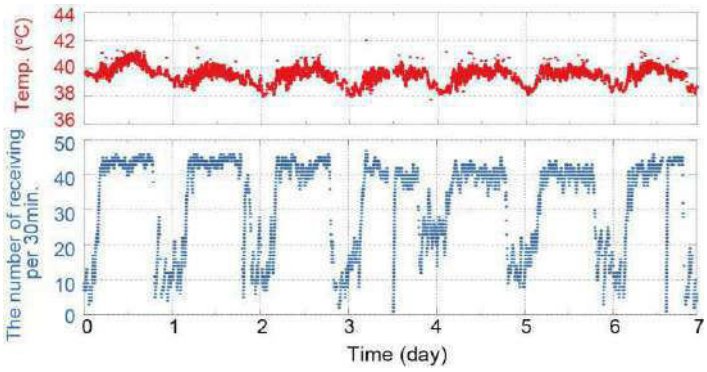

Figure 8: Results of the body temperature change and activity change

We also carried out the demonstration experiment with the developed wireless sensor node. 120 wireless sensor nodes were attached to chickens and monitored the body temperature and activity of the chickens. The results indicated that the obtained data is enough to detect the abnormal state of chickens at an early stage.

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Design, Implementation and Analysis of different 32-bit multipliers on aspects of Power, Speed and Area

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***Abstract*—** VLSI is a domain that is constantly pushing the boundaries in the field of logical devices by striving to get greater compute power from reduced device area by composition of high number of logical devices onto ever decreasing areas. It is well known that multipliers consume most of the power in DSP computations. It is of utmost importance for modern DSP systems to come up with multipliers that consume low power to reduce the power dissipation without needing to compromise on speed and area. This paper talks about the implementation of four different 32-bit multiplier architectures and the comparison of the speed, area and power of the multipliers and their applications. The four multipliers being considered are Booth multiplier, Wallace Tree Multiplier, Vedic Multiplier and Dadda multiplier. The Multipliers are designed and implemented using Verilog and synthesised using Xilinx ISE tool. A Wallace tree multiplier is the improved version of tree-based multiplier architecture. It uses the Carry -Save addition algorithm to reduce the latency. Many modifications and new techniques are being worked upon to enhance speed of the standard Booth Multiplier. Vedic multiplier is built on the foundation of Vedic mathematics. It is an area that's drawing wide interest and focus due to its capabilities of being a low power multiplier combined with faster compute speed. There are sixteen sutras in Vedic multiplication in which "Urdhva Tiryakbhyam" has been noticed to be the most efficient one in terms of speed. Dadda multiplier does the minimum reduction necessary at each level to perform the reduction in the same number of levels as required by a Wallace tree multiplier it exhibit similar delay.

***Keywords*—** Vedic Mathematics, Ripple Carry Adder, VLSI, Low power, High speed, Low area.

I. INTRODUCTION

Multiplier is an important building block in the design of digital circuits. Multiplier is widely used in Digital signal processing and in communication applications. A modern high performant digital signal processing system needs multipliers with high speed and throughput for real-time signal processing. High compute speed has been the focus of MAC design in the last few years. High Speed Multipliers form the backbone of a high-speed MAC. Designing multipliers for the high speed integrated circuit with low power consumption is an area of major focus and research for the VLSI field. In this paper, the multipliers architectures are compared in terms of speed, power dissipation and area.

The Booth multiplier is the highest speed multiplier when compared to the Dadda, Wallace and Vedic multipliers. The Vedic multiplier consists of low power and low area when compared to other multipliers. The Wallace tree adders are obtained by a reduction phase on the Dadda multiplier.

II. BOOTH MULTIPLIER

In the Booth Multiplier Encoding scheme the number of stages involved to achieve multiplication are reduced. It performs 2-bit multiplication at once [6], so it requires half the stage. In this scheme, the complexity of all stages involved are slightly more than a simple multiplier. However, the complexity of the adder/subtractor is almost on par with the complexity of a simple adder. Booth Multiplier Multiplication consists of three steps:

- The first step to generate the partial products.
- The second step involves generation of partial products to the exclusion of the last two rows.
- The third step does the job of arriving at the final multiplication results by adding the last two rows

A. *Booth Multiplier Architecture*

Booths algorithm involves encoding of multiplier bits and partial product generation as shown in Fig 1. Different modified booths algorithms have been proposed according to how many number of bits are used to encode multiplier as shown in Fig 1. Modified booth algorithm reduces the number of partial products [7]. The NxN bit multiplication involves N partial products but modified produces N partial. Each group of 3 bits has been considered according to modified Booth Algorithm for generation of partial products 0, ±1A, and ±2A. In first group, first bit is taken zero and other bits are least significant two bit of multiplier operand. In second group, first bit is most significant bit of first group and other bits are next two bit of multiplier operand. In third group, first bit is most significant bit of second group and other bits are next two bit of multiplier operand [6]. This process is carried on Partial product is generated using multiplicand operand A. For n bit multiplier there is n/2 or [n/2 + 1] groups and partial products, for 16X16 bit multiplication 8 partial products are generated. So it reduces the number of partial products in comparison to Booth algorithm improves the computational efficiency of multiplier, reduce the calculation delay. The Bits generated from Modified Booth Encoder fed to the partial product generator.

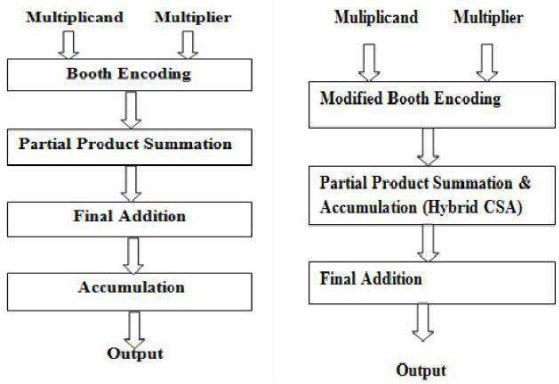

Fig. 1. Booth multiplier and Modified booth multiplier

B. IMPLEMENTATION

Fig 2 and Fig 3 shows the RTL schematic and simulation of 32-bit booth multiplier.

Fig. 2. RTL schematic of booth multiplier

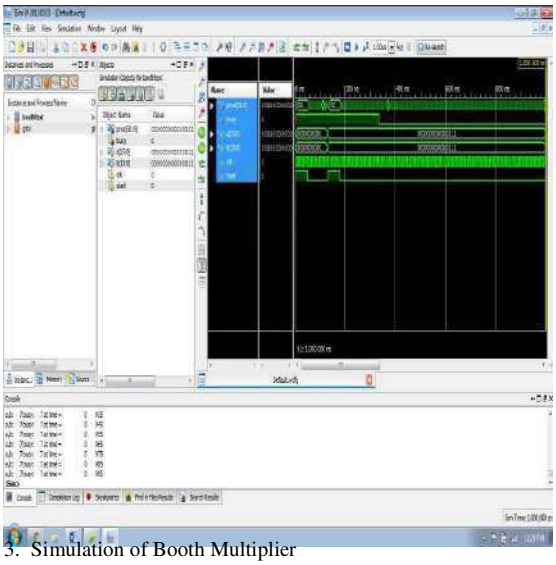

Fig. 3. Simulation of Booth Multiplier

III. VEDIC MULTIPLIER

Vedic multiplier built on the foundation of Vedic mathematics and is currently the focus of intense research as it exhibits the characteristics of being one of the fastest and low power multiplier. There are sixteen sutras in Vedic multiplication in which "UrdhvaTiryakbhyam" has been noticed to be the most efficient one in terms of speed [10].

A. Vedic Multiplier Architecture

The architecture of 16x16 Vedic multiplier by means of "UrdhvaTiryakbhyam" Sutra is shown in Fig.4. The 16x16 Vedic multiplier architecture is implemented using four 8x8. In Vedic multiplier modules, there is one 16-bit carry save adder and two binary adder stages. Multiplication Output = (p31-p16) & (p15-p8) & (p7-p0). Where & is the concatenate operation. The proposed architecture employs a 16 -bit carry save adder and 16-bits adder modules to come up with the final 32-bits product (p31-p16) & (p15-p8) & (p7-p0).The p7 - p0 (8-bits) of the product represents least significant 8-bits of the 16-bit output of the right hand most 8x8, each 16-bit output of second and third 8x8 multiplier modules multiplier module. The 16 -bit carry save adder adds three input 16-bit operands [13]. The 16-bit carry save adder provides output in two 16-bit operands namely sum vector and carry vector. The outputs of the carry save adder are then provided to the first 16 -bit adder to generate 16-bit sum. The central part (p15- p8) characterizes the least important eight bits of 16-bit sum. The 16-bit output of the left most 8x8 multiplier module and concatenated 16-bits 00000"& the most significant nine bits of 16-bits sum) are fed into second 16-bit adder. The p31 -p16 represents sixteen bit sum [15] [16]. The 32rd carry bit is ignored when coming up with the final product.

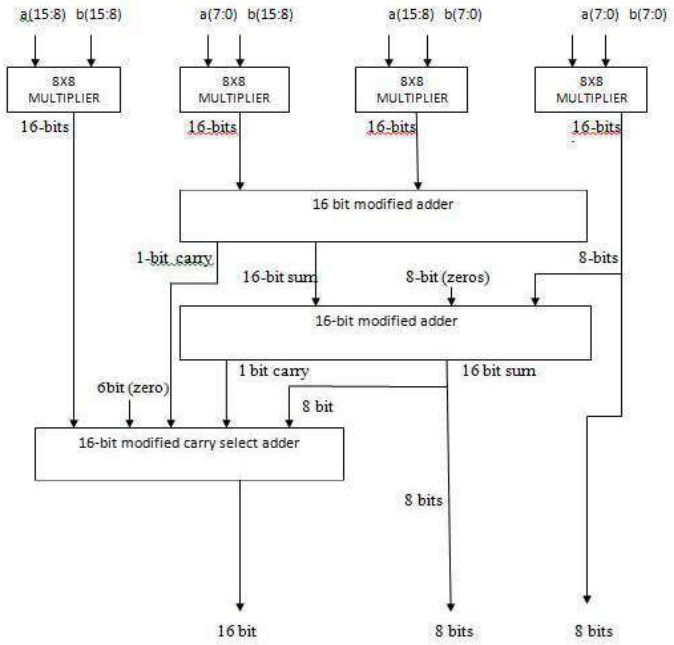

Fig. 4. Architecture of Vedic Multiplier

B. IMPLEMENTATION

Fig 5 and Fig 6 shows the RTL schematic and simulation of 32-bit booth multiplier.

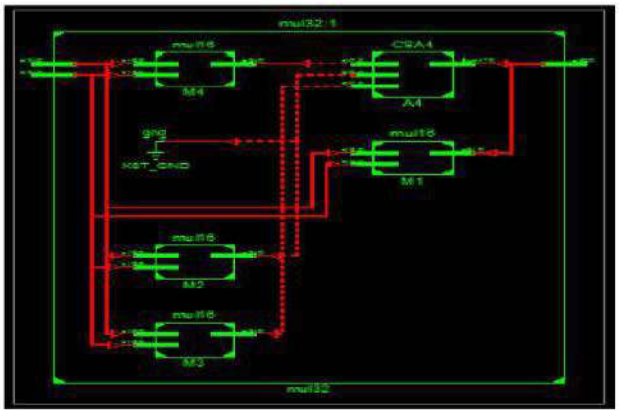

Fig. 5. RTL schematic of Vedic multiplier

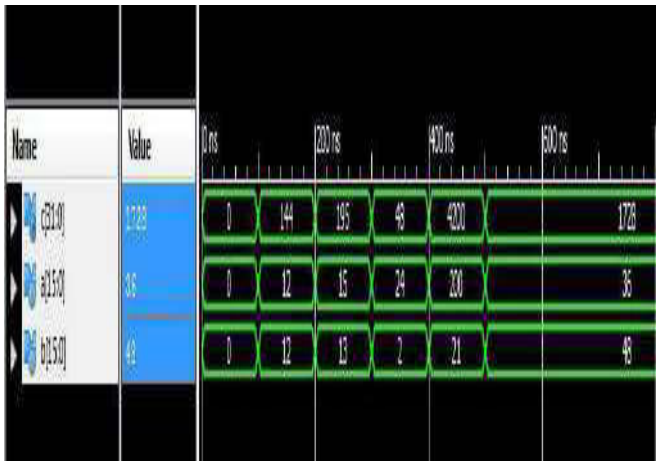

Fig. 6. Simulation of Vedic Multiplier

IV. WALLACE TREE MULTIPLIER

Wallace multiplier is characterized by low power consumption. It also has a switching speed that is faster when pitted against other multiplier architectures. Due to these factors, there has been deep interest shown on Wallace multiplier which has helped in the creation of different architectures to come up with a better Wallace multiplier architecture [2]. A conventional Wallace multiplier and a reduced complexity Wallace multiplier are two architectures among them.

A. Wallace Tree Multiplier Architecture

The 2's Complement Generator adjusts the unsigned multiplicand to signed multiplicand by doing 1's Complement and then 2's Complement of the input multiplicand binary0110, to convert it to a signed number we have to do its

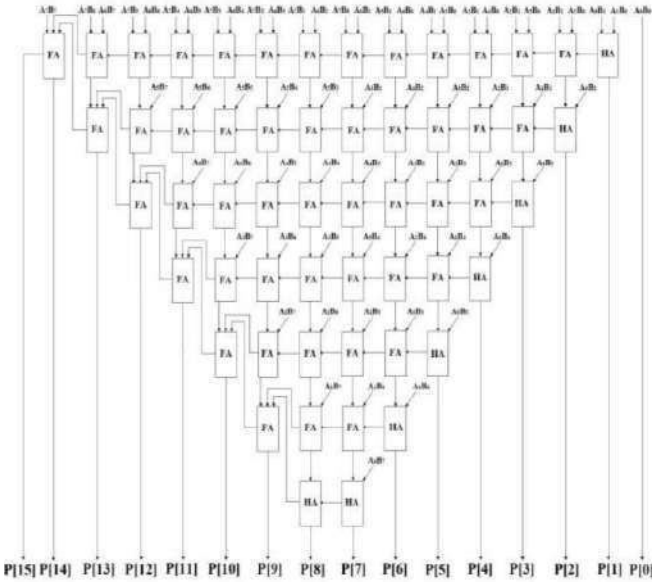

Fig. 7. Architecture of Wallace Tree Multiplier

2's complement. number. The unsigned number is directly given to the partial product generator [5]. The 32-bit Wallace structure is composed of 30 carry-save adders and one 54-bit recursive doubling based CLA [3]. The Block 1 has 14 Carry Save adders (CSA), 2 Carry Save adders. Cell III has in its composition six Carry Save adders. So in total the 32-bit Wallace structure has a cumulative count of (4∗14) +(2∗2)+(1∗6) = 66 Carry Save adders, four 25-bit recursive doubling based CLAs, two 40 -bit recursive doubling based CLAs and one 54-bit recursive doubling based CLA [1] [3]. And hence, this enormous difference causes increase in total cell area, total number of cells and net power than conventional structure

B. IMPLEMENTATION

Fig 8 and Fig 9 shows the RTL schematic and simulation of 32 bit Wallace Tree multiplier

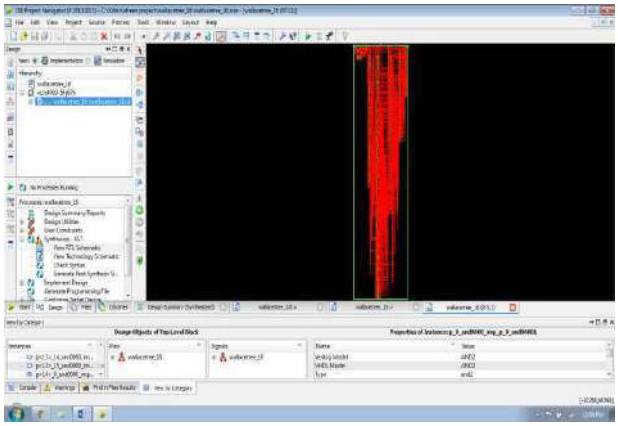

Fig. 8. RTL schematic of Wallace Tree Multiplier

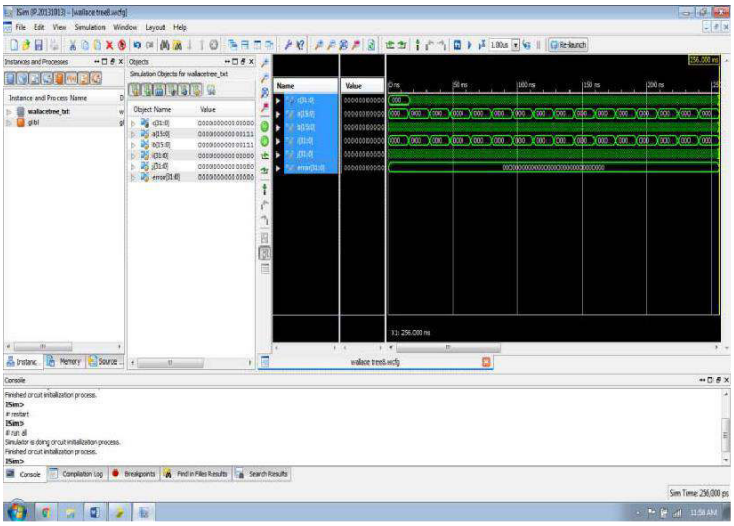

Fig. 9. Simulation of Wallace Tree Multiplier

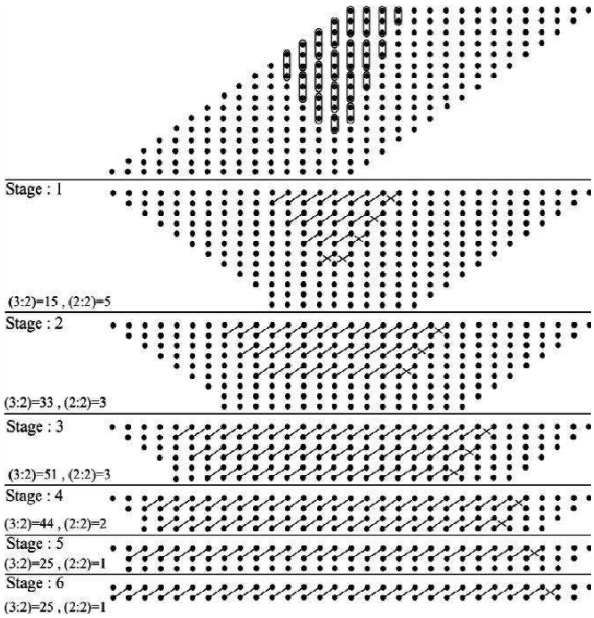

Fig. 10. Architecture of Wallace Tree Multiplier

V. DADDA MULTIPLIER MULTIPLIER

The Dadda multiplier is an invention by computer scientist Luigi Dadda in 1965 in the field of hardware multiplier design. It has similarity to the Wallace multiplier, but also exhibits faster compute capability for all operand sizes and at the same time requires lesser number of gates for all but few smaller operand sizes [17].

A. Dadda Multiplier Architecture

Dadda multiplier has less expensive reduction phase, but the numbers may be a few bits longer, hence requires a few bigger adders. In order to have this behavior, the structure of the second step is governed by slightly more complex rules when compared to the Wallace multipliers. Both the Dadda and Wallace multipliers have similar steps (3 in number) for two bit strings and lengths respectively.

- Multiply (logical AND) each bit of , by each bit of , yielding results, grouped by weight in columns
- Reduce the number of partial products by stages of full and half adders until we are left with at most two bits of each weight.
- Add the result with a conventional adder as with the Wallace multiplier, the multiplication products of the first step carry different weights reflecting the magnitude of the original bit values in the multiplication. For example, the product of bits has weight unlike Wallace multipliers that reduce as much as possible on each layer, Dadda multipliers attempt to minimize the number of gates used, as well as input/output delay [18]. Due to the above reasons, Dadda multipliers have a much lower expensive reduction phase. However, the final numbers may be a few bits longer necessitating somewhat bigger adders.

The reduction rules for Dadda Multiplier are as follows:
If there are 2 outputs of the similar weight left, and the current number of output wires with that weight is equal to 2 (modulo 3) , input them into a half adder. However, when a layer carries at most 3 input wires for any weight, that layer will be the last one. Implementation the multiplication of an M-bit multiplicand by an N-bit multiplier [20] yields an N by M matrix of partial products. The reduction of this partial product matrix through the parallel application of (3, 2) and (2, 2) counters results in a matrix with a height of two. The implemented 32 × 32 Dadda multiplier with the help of dot diagram is shown in Fig 10..

B.Dadda Multiplier Implementation

Fig 11 and Fig 12 shows the RTL schematic and simulation of 32 bit Dadda Multiplier.

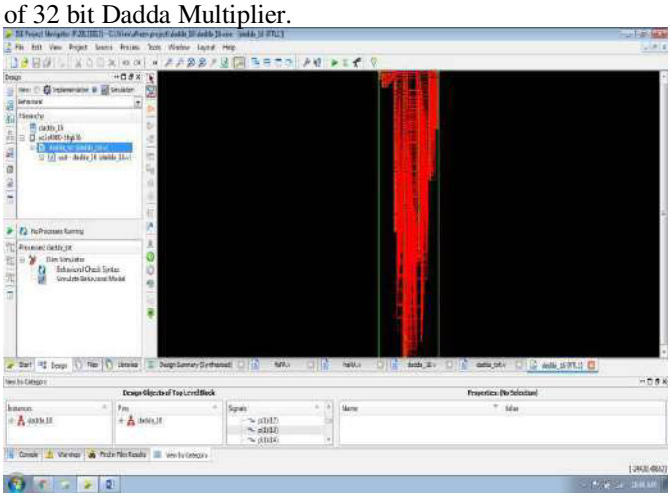

Fig. 11. RTL schematic of Dadda Multiplier

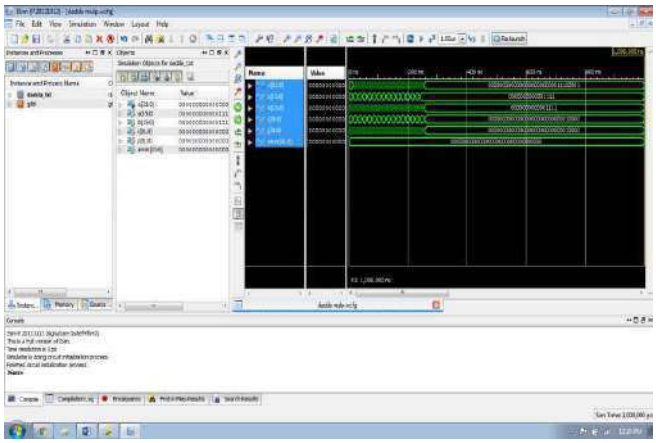

Fig. 12. Simulation of Dadda Multiplier

RESULT

TABLE I. COMPARISON OF SPEED

Multipliers	Speed
Booth	6.152ns
Dadda	48.235ns
Wallace tree	48.235ns
Vedic	31.526ns

TABLE II. COMPARISON OF POWER

Multiplier	Static(mw)	Dynamic(mw)	Total(mw)
Booth	0.277	0.095	0.372
Dadda	0.275	0.027	0.302
Wallace	0,274	0.004	0.278
Vedic	0.274	0.003	0.274

TABLE III. COMPARISON OF AREA IN VEDIC MULTIPLIER

Names	Used	Total	Percentage
Number of Slice	1188	4656	25%
Number of 4 inputs LUTS	2054	9312	22%
Number of bounded IOS	128	232	55%

TABLE IV. COMPARISON OF AREA IN DADDA MULTIPLIER

Names	Used	Total	Percentage
Number of Slice	350	27548	1%
Number of 4 inputs LUTS	610	55296	1%
Number of bounded IOS	64	489	13%

TABLE V. COMPARISON OF AREA IN BOOTH MULTIPLIER

Names	Used	Total	Percentage
Number of Slice	110	27648	0%
Number of 4 inputs LUTS	89	55296	0%
Number of bounded IOS	67	489	13%

TABLE VI.COMPARISON OF AREA IN WALLACE TREE

Names	Used	Total	Percentage
Number of Slice	350	27648	1%
Number of 4 inputs LUTS	610	55296	1%
Number of bounded IOS	64	489	13%

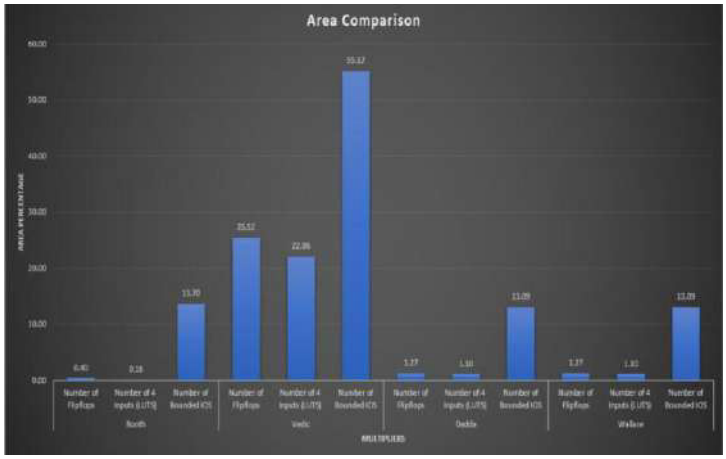

Fig. 13. Bar Graph for Area Comparison

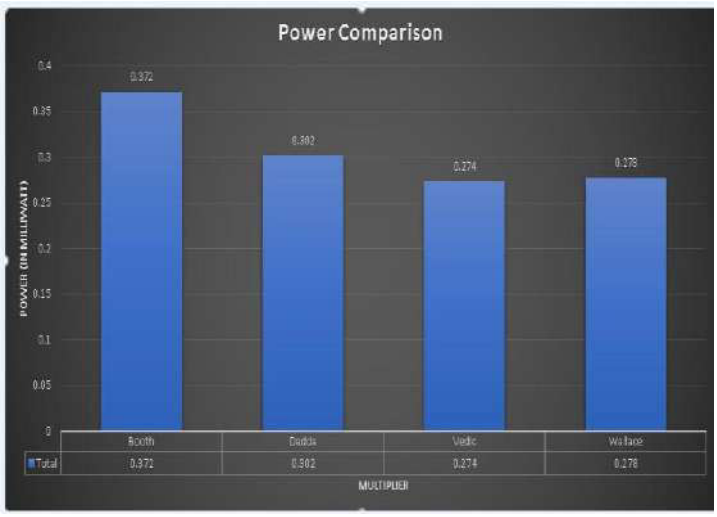

Fig. 14. Bar Graph for Power Comparison

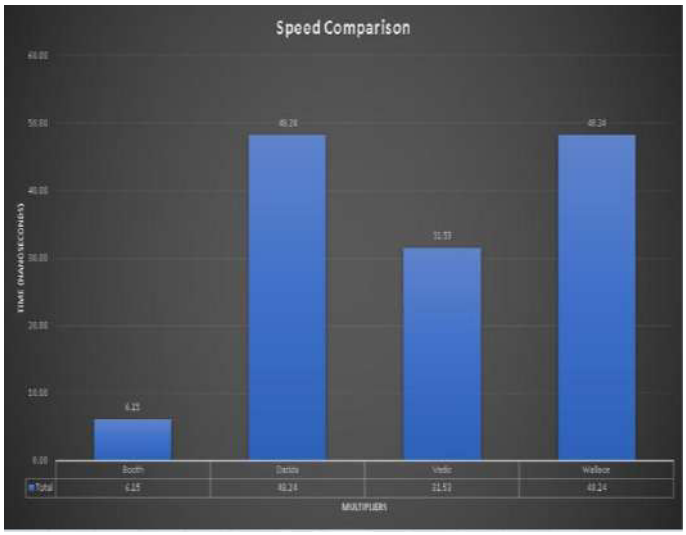

Fig. 15. Bar Graph for Speed Comparison

CONCLUSION

In this section, the four multipliers discussed above are compared based on speed, area and power consumed. The basic Booth multiplier is the simplest of all multipliers for high speed and therefore occupies small area. Based on the above study, it can be concluded that of all the multipliers, Modified Booth and Wallace tree multiplier are the fastest multiplier because the modified Booth Multiplier reduces the number of partial products by half or one third of the multiplier bits based on the algorithm it uses and the Wallace tree multiplier increases the speed of accumulation because of the use of carry-save adders. However, it has the drawback of complexity thus occupying the largest area. Whereas, Dadda multiplier and Vedic multiplier both have high power requirements. Thus, a multiplier should be selected depending of the performance requirements and the nature of the applications.

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LUT OPTIMIZATION TECHNIQUES FOR DIGITAL FILTERS

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ABSTRACT-As technology improves day by day wide and vast, we were expecting to get the things in the reduced size. Multiplication is major arithmetic operation in signal processing. In ALU's the multiplier uses lookup-table (LUT) as memory for their computations and it consume much hardware area, to reduce the size of the LUT, we present the antisymmetric product coding (APC) and odd-multiple-storage (OMS) techniques for lookup-table (LUT) design for memory-based multipliers to be used in digital signal processing applications. This LUT–memory based multiplication implements in Finite Impulse Response (FIR) filter where the filter outputs are computed as inner-product of input-sample vectors and filter-coefficient vector. It is found that the proposed LUT-based multiplier involves comparable area and time complexity for a word size of 8 bits, 16- and 32-bits, respectively, it offers more than 16% and 20% of saving in area–delay product.

Keywords: Digital Signal Processing, FIR, Look-Up-Table (LUT)-Based Computing, Memory-Based Computing, Digital Filters, Digital Signal Processing, FIR, VLSI.

I.INTRODUCTION

In most of the DSP processors the memory based computing structures are of primary concern than the multiply accumulate structures. Computational or functional operations performed in the DSP blocks of an FPGA for implementing a particular task are time consuming and require more components like adders, multipliers. In the processors like DSP core in FPGAs multiply and accumulate structures are replaced with Look Up Tables. Instead of using conventional multipliers for complex multiplication, operations are simplified with the usage of LUTs that are used for the direct storage of the complex computational values. Further optimization of Look-up-tables provides better performance in terms of speed and effective area utilization. In this paper, LUT optimization using the APC coding and OMS methodology are the primary concern.

In this paper, APC-OMS LUT based FIR filter is designed for DSP applications. A combined approach of the two methods is defined (i.e, Antisymmetric product coding and Odd Multiple Storage that are used previously to optimize LUTs with in a DSP cores for their related operations). The input address and LUT output could always be transformed into odd integers. Previously it is observed that, when an Antisymmetric product coding approach is combined with the

Odd multiple storage technique, the two's complement operations could be very much simplified since the input address and LUT output could always be transformed into odd integers, and both cannot be combined since the words generated are odd numbers.

II. PROPOSED APC FOR LUT OPTIMIZATION

For simplicity of presentation, we assume both X and A to be positive integers. The product words for different values of X for L = 5 are shown in Table 1. It may be observed in this table that the input word X on the first column of each row is the two's complement of that on the third column of the same row. In addition, the sum of product values corresponding to these two input values on the same row is 32A. Let the product values on the second and fourth columns of a row be u and v, respectively.

Input, x	Product values	Input, x	Product values	Address $\bar{x}_3 x_2 \bar{x}_1 x_0$	Apc words
00001	A	11111	31A	1111	15A
00010	2A	11110	30A	1110	14A
00011	3A	11101	29A	1101	13A
00100	4A	11100	28A	1100	12A
00101	5A	11011	27A	1011	11A
00110	6A	11010	26A	1010	10A
00111	7A	11001	25A	1001	9A
01000	8A	11000	24A	1000	8A
01001	9A	10111	23A	0111	7A
01010	10A	10110	22A	0110	6A
01011	11A	10101	21A	0101	5A
01100	12A	10100	20A	0100	4A
01101	13A	10011	19A	0011	3A
01110	14A	10010	18A	0010	2A
01111	15A	10001	17A	0001	1A
10000	16A	10000	16A	0000	0A

Table.1. APC words for different input values for L = 5

Since one can write,

$$u - \left[\frac{u+v}{2} - \frac{v-u}{2}\right] \quad \text{and}$$

$$v - \left[\frac{u+v}{2} + \frac{v-u}{2}\right], \quad \text{for } (u+v)=32A,$$

$$u = 16A \quad \left[\frac{v-u}{2}\right], \quad v = 16A + \left[\frac{v-u}{2}\right]$$

The product values on the second and fourth columns of Table.1 therefore have a negative mirror symmetry. This behavior of the product words can be used to reduce the LUT size, where, instead of storing u and v, only [(v − u)/2] is stored for a pair of input on a given row. The 4-bit LUT addresses and corresponding coded words are listed on the fifth and sixth columns of the table, respectively. Since the representation of the product is derived from the antisymmetric behavior of the products, we can name it as antisymmetric product code. The 4-bit address X^1 = ($x_3^1 x_2^1 x_1^1 x_0^1$) of the APC word is given by

$$X_1 = \begin{cases} X_L & \text{if } X_4 = 1 \\ X_L{}^1 & \text{if } X_4 = 0 \end{cases}$$

where XL = (x3x2x1x0) is the four less significant bits of X, and X_L^1 is the two's complement of XL. The desired product could, however, be easily extended for signed values of A and X in sign magnitude form or two's complement form.

table.2 oms-based design of the lut of apc words for l = 5

product could be obtained by adding or subtracting the stored value (v − u) to or from the fixed value 16A when x4 is 1 or 0, respectively, i.e,

Product word = 16A + (sign value) × (APC word)

where sign value = 1 for x4 = 1 and sign value = −1 for x4 = 0. The product value for X = (10000) corresponds to APC value

"zero," which could be derived by resetting the LUT output, instead of storing that in the LUT.

II. IMPLEMENTATION OF THE LUT MULTIPLIER USING APC FOR L= 5

The structure and function of the LUT-based multiplier for L

5 using the APC technique is shown in Fig. 2. It consists of a four-input LUT of 16 words to store the APC values of product words as given in the sixth column of Table. 1, except on the last row, where 2A is stored for input X=(00000) instead of storing a "0" for input X = (10000). Besides, it consists of an address-mapping circuit and an add/subtract

circuit. The address-mapping circuit generates the desired address ($x_3^1 x_2^1 x_1^1 x_0^1$).

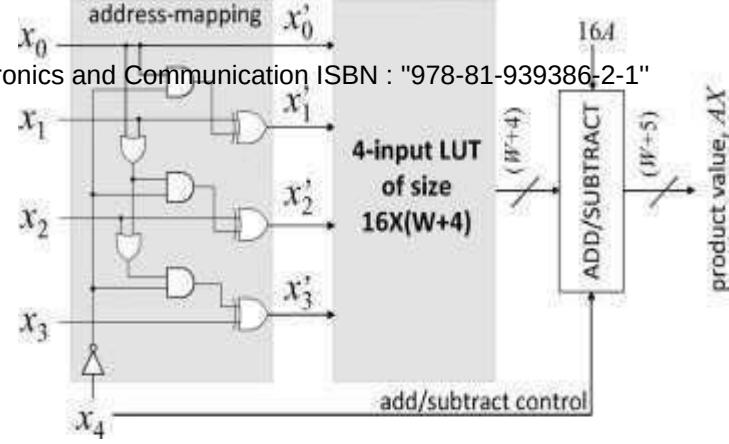

Fig. 2. LUT-based multiplier for L=5 using the APC technique.

A straightforward implementation of address mapping can be done by multiplexing X_L and X_L^1 using x4 as the control bit. The address-mapping circuit, however, can be optimized to be realized by three XOR gates, three AND gates, two OR gates, and a NOT gate, as shown in Fig. 2. The output of the LUT is added with or subtracted from 16A, for x_4 = 1 or 0, respectively, by the add/subtract cell. Hence, x_4 is used as the control for the add/subtract cell.

III. PROPOSED OMS FOR LUT OPTIMIZATION

In Table.2, we have shown that, at eight memory locations, the eight odd multiples, A × (2i + 1) are stored as Pi, for i = 0, 1, 2, . . . , 7. The even multiples 2A, 4A, and 8A are derived by left-shift operations of A. Similarly, 6A and 12A are derived by left shifting 3A, while 10A and 14A are derived by left shifting 5A and 7A, respectively. A barrel shifter for producing a maximum of three left shifts could be used to derive all the even multiples of A.

It may be seen from Table.2. that the 5-bit input word X can be mapped into a 4-bit LUT address (d3d2d1d0), by a simple set of mapping relations,

$$d_i - x^{11}{}_{i+1} \quad \text{for i–0,1,2 and } d_3 – x_0{}^{11}$$

where X^{11}= ($x_3^1 x_2^1 x_1^1 x_0^1$) is generated by shifting-out all the leading zeros of X^1 by an arithmetic right shift followed by address mapping, i.e.,

$$X_1 = \begin{cases} Y_i. & \text{if } X_4 = 1 \\ Y_L{}^1 & \text{if } X_4 = 0 \end{cases}$$

where Y_L and Y_L^1 are derived by circularly shifting-out all the leading zeros of X_L and X_L^1, respectively.

Input x_1 x_3 x_2 x_1 x_0	Product value	No of shifts	Shifted input, x_{11}	Stored APC word	Address $d_3d_2d_1d_0$
0001	A	0	0001	P0=A	0000
0010	2×A	1			
0100	4×A	2			
1000	8×A	3			
0011	3A	0	0011	P1=3A	0001
0110	2×5A	1			
1100	4×3A	2			
0101	5A	0	0101	P2=5A	0010
1010	2×5A	1			
0111	7A	0	0111	P3=7A	0011
1110	2×7A	1			
1001	9A	0	1001	P4=9A	0100
1011	11A	0	1011	P5=11A	0101
1101	13A	0	1101	P6=13A	0110
1111	15A	0	1111	P7=15A	0111

Table.2. OMS-based design of the LUT of APC words for L=5

IV. IMPLEMENTATION OF THE LUT MULTIPLIER USING OMS

The proposed APC–OMS combined design of the LUT for L = 5 and for any coefficient width W is shown in Fig.3.

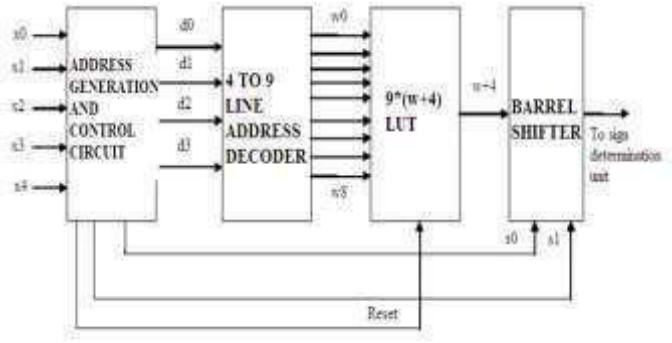

Fig.3. Proposed APC–OMS combined LUT design for the multiplication

It consists of an LUT of nine words of (W + 4)-bit width, a four-to-nine-line address decoder, a barrel shifter, an address generation circuit, and a control circuit for generating the RESET signal and control word (s1s0) for the barrel shifter.The decoder takes the 4-bit address from the address

generator and generates nine word-select signals, i.e., $\{w_i$, for $0 \le i \le 8\}$, to select the referenced word from the LUT.

The 4-to-9-line decoder is a simple modification of 3-to- 8-line decoder, as shown in Fig. 4(a). The control bits s0 and s1 to be used by the barrel shifter to produce the desired number of shifts of the LUT output are generated by the control circuit, according to the relations

$$s_0 = \overline{x_0 + \overline{(x_1 + \overline{x_2})}}$$

$$s_1 = \overline{(x_0 + x_1)}$$

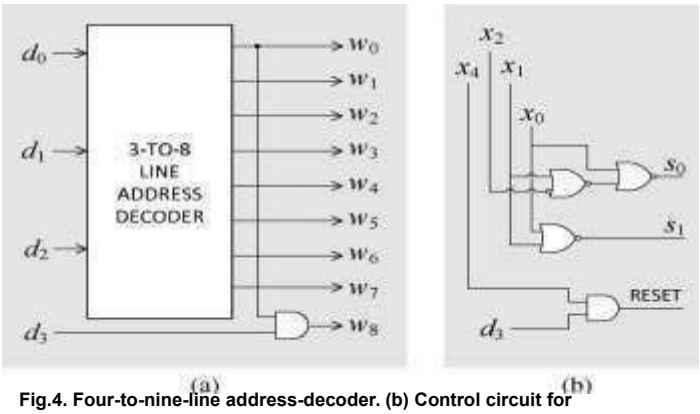

Fig.4. Four-to-nine-line address-decoder. (b) Control circuit for generation of s_0, s_1, and RESET.

Note that ($S1S0$) is a 2-bit binary equivalent of the required number of shifts specified in Tables.2 and Table.3. The RESET signal can alternatively be generated as ($D3$ AND $X4$). The control circuit to generate the control word and RESET is shown in Fig. 4(b). The address-generator circuit receives the 5-bit input operand X and maps that onto the 4-bit address word ($D3D2D1D0$).

Input X $x_4x_3x_2x_1x_0$	Prouduct value	Encoded word	Stored value	No of shifts	Address $d_3d_2d_1d_0$
10000	16A	0	---	---	---
00000	0	16A	2A	3	1000

Table.3. Products and encoded words for X = (00000) and (10000)

The product values and encoded words for input words X = (00000) and (10000) are separately shown in Table.4.3. For X = (00000), the desired encoded word 16A is derived by 3-bit left shifts of 2A [stored at address (1000)]. For X = (10000), the APC word "0" is derived by resetting the LUT output, by an active-high RESET signal given by

$$\text{RESET} = \overline{(x_0 + x_1 + x_2 + x_3) \cdot x_4}.$$

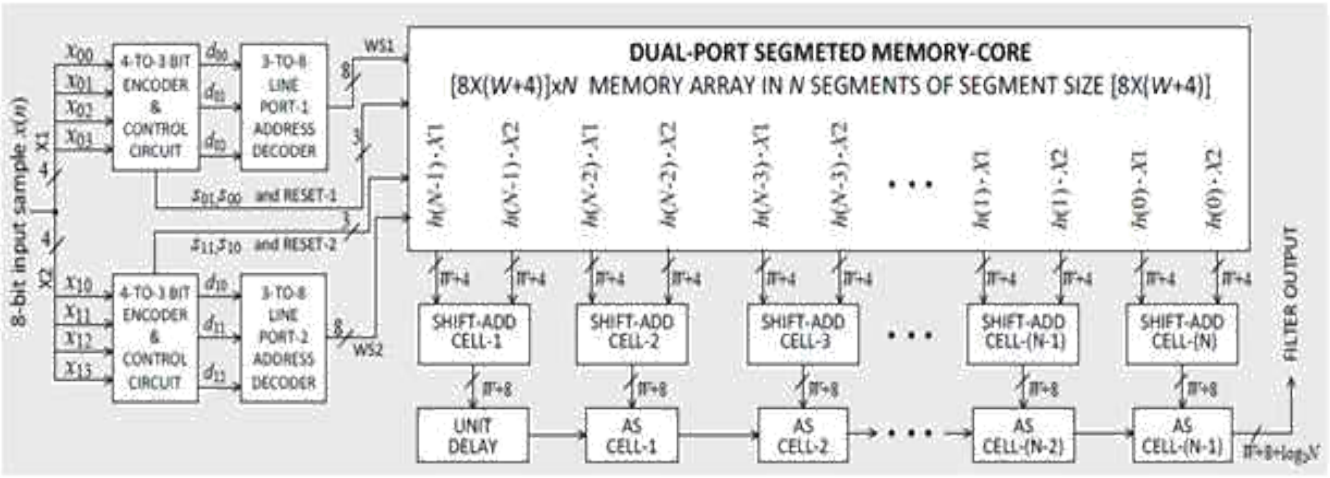

Fig. 5. Structure of N-th Order FIR filter using proposed LUT-Multiplier

V. MEMORY-BASED FIR FILTER USING PROPOSED LUT DESIGN

APC-OMS method is a different approach for implementing digital filters. The basic idea is to replace all multiplications and additions by a table & shifter-accumulator. An optimized FIR filter is designed, and the basic block diagram of the matched filter resembles the basic architecture of FIR filter The memory-based structure of FIR filter (for 8-bit inputs) using the proposed LUT design is shown in Fig.5.

i)The convention.al LUT-multiplier is replaced by proposed odd-multiple-storage LUT, so that the multiplication by an L-bit word could be implemented by (2L/2)/2 words in the LUT in a dual-port memory.

ii)Since the same pair of address words X1 and X2 are used by all the N LUT-multipliers, only one memory module with N segments could be used instead of N modules.

If all the multiplications are implemented by a single memory module, the hardware complexity of 2(N − 1) decoder circuits could be eliminated as shown in Fig.5, the proposed structure of FIR filter consists of a single memory-module, and an array of N shiftadd (SA) cells, (N − 1) AS cells and a delay register., it consists of a pair of 4- to-3 bit encoders and control circuits and a pair of 3-to-8 line decoders to generate the necessary control signals and word select signals for the dual-port memory core.

VI. RESULTS AND DISCUSSION

FIR filter design using the High – Speed LUT structure thus implemented and simulated through CADENCE 180nm Technology. The simulated results are as shown in the Fig.6 and Fig.7. The overall design process enhances the system performance in terms of speed and area that doubles the transmission rate, increasing the overall throughput. The result shows that more than 20% of saving in area-delay product.

Word Size	Existing method		Proposed method		Area saving
	LUT Area	LUT Time	LUT Area	LUT Time	
8bits	624	08.001	127	09.031	20.35%
16bits	1632	09.013	275	11.001	16.85%
32bits	3168	11.001	411	13.235	13.08%

Table.4. Area complexity comparisons using different bits

Area complexity comparisons using different bits, ie., 8bits,16bits and 32bits are shown in the table.4. The simulation results of APC-OMS filter architecture using the cadence tool for L=16 and L=32 are shown in Fig.6 and Fig.7.

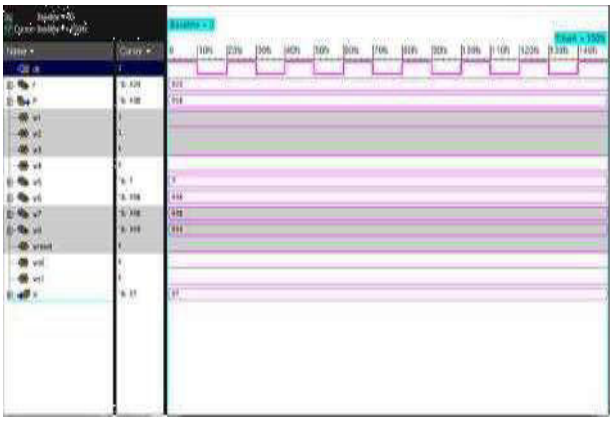

Fig.6. Simulation result for APC-OMS filter Architecture for L=16

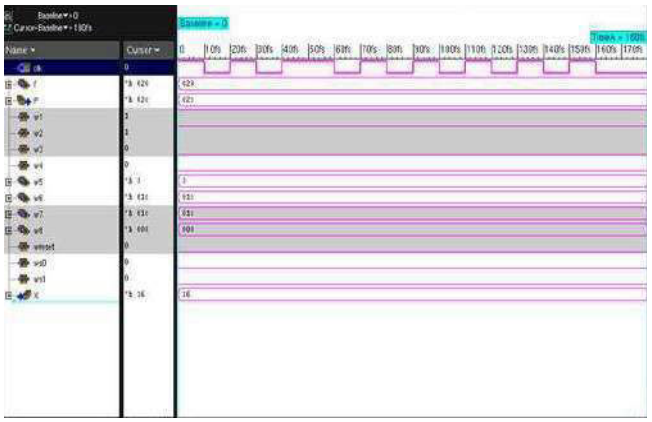

Fig.7. Simulation result for APC-OMS filter Architecture for L=32

CONCLUSION

An efficient approach is thus specified for optimizing the LUTs and is implemented through APC-OMS method FIR filter that results in improving performance. FIR filter, resembling the Matched filter structure is thus implemented through the design that is applicable for many DSP applications. The specified method and the design process thus provide 16% and 20% savings of area-delay product, 16bit and 32bit respectively. The overall implementation process is thus simulated using CADENCE 180nm Technology and the simulated result are shown.

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Coupling Faults Detection in Memories using with Finite State Machine and Microcode based and Microcode based Memory Built In Self Test(MBIST)

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***Abstract*— Built-in Self-Test, or BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, testing of their own operation using their own circuits, thereby reducing dependence on external automated test equipment (ATE). BIST is also the solution to the testing of critical circuits that have no direct connections to external pins, such as embedded memories used internally by the devices. In the near future, even the most advanced tester may no longer be adequate for the fastest chip, a situation wherein self-testing may be the best solution. Microcode-based and FSM-based controllers are two widely known architectures used for programmable memory built-in self-test. These techniques are popular because of their flexibility of programming new test algorithms. In this paper, the architectures for both controllers are designed to implement a new test algorithm MARCH SAM that gives a better fault coverage in detecting single-cell fault and all intra-word coupling fault (CF).The components of each controllers are studied and designed. The both of the controller are written using Verilog HDL and implemented FPGA. The simulation and synthesis results of both architectures are presented.**

Keywords—Built in self test , FSM, Coupling faults, march Sam, fault, FPGA.

I. INTRODUCTION

Now a days techniques are improved to detecting the errors towards to Static Random Access Memory. many effective algorithms are integrated in Memory Built In Self-Test Architecture[1]. The MBIST is technique played a major role as embedded memories for System On Chip[2]. The constellation of this component is tremendous and crowded due to the large number of data to be stored [3]. However the complexity because of the embedded memories are making challenge among the problems are encountered while testing the memories. Memory BIST has been used successfully for years to solve the test issues of embedded memories. In addition to testing embedded memories using expensive external memory tester, BIST is considered a good alternative solution[4]. MBIST Architecture has is proposed for memory testing in itself. But the thing is limited data patterns are generated and memory accessing schemes also. Large number of programmable architectures has been proposed to solve the problems[5].

II. LITERATURE SURVEY

Facing achieve optimal System on Chip (SOC),the mechanism must be implemented to test the embedded memories[3]. To achieve optimal SOC yield, an at-speed testing mechanism must be implemented to test these embedded memories[6]. Consequently the only practical solution is derivable from Built In Self-Test. BIST is having two patterns those are 1. Pseudorandom Pattern 2. Deterministic pattern Pseudorandom pattern usually preowned to test with logical test sequences and the other one deterministic pattern is used to test memories with MARCH Algorithm. Hence the only practical solution available is by employing built-in-self-test (BIST). BISTs have either two patterns; pseudorandom pattern or deterministic pattern. Pseudorandom pattern is usually used to test logic circuits while the deterministic pattern is applied to test memories. MARCH. The below table 01. Is showing binary code corresponding with algorithms and March Elements.

TABLE 01: TEST PATTERNS OF BUILT IN SELF TEST

Code	Algorithm	March Elements
000	MATS+ (3n)	↕ (w0);↑ (r0,w1);↓ (r1,w0)
001	MARCH X (4n)	↕ (w0);↑ (r0,w1);↓ (r1,w0);↕ (r0)
010	MARCH C- (6n)	↕ (w0);↑ (r0,w1);↑ (r1,w0); ↓ (r0,w1);↓ (r1,w0);↕ (r0)
011	MARCH A (5n)	↕ (w0);↑ (r0,w1,w0,w1); ↑ (r1,w0,w1);↓ (r1,w0,w1,w0); ↓ (r0,w1,w0)
100	MARCH B (5n)	↕ (w0);↑ (r0,w1,r1,w0,r0,w1); ↑ (r1,w0,w1);↓ (r1,w0,w1,w0); ↓ (r0;w1,w0)
101	MARCH U (5n)	↕ (w0);↑ (r0,w1,r1,w0);↑ (r0,w1); ↓ (r1,w0,r0,w1);↕ (r0)
110	MARCH LR (6n)	↕ (w0); (r0,w1);↑ (r1,w0,r0,w1); ↑ (r1,w0);↑ (r0,w1,r1,w0);↕ (r0)
111	MARCH SS (6n)	↕ (w0);↑ (r0,r0,w0,r0,w1); ↑ (r1,r1,w1,r1,w0); ↓ (r0,r0,w0,r0,w1); ↓ (r1,r1,w1,r1,w0);↕ (r0)

The familiar technique is Pseudorandom Built In Self-Test (PBIST) are generated the test sequences widely for integrated circuits and systems[7]. The Test Pattern Generators The Pseudorandom generators includes, linear feedback shift registers (LFSRs) [2], cellular automata [5], and accumulators driven by constant value [3].

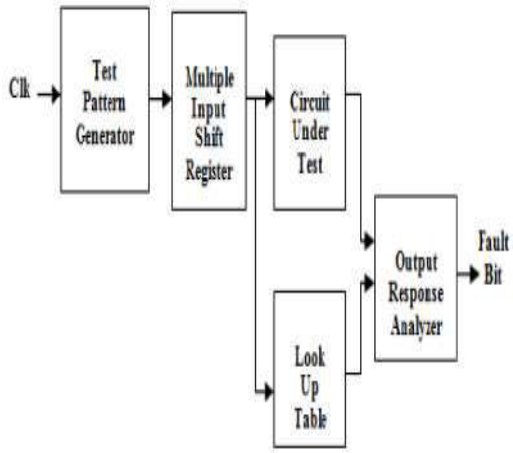

Fig.01 Block Diagram of Test Pattern Generator (TPG)

In lineup to recognize the faults in any circuits or devices, the large number of random patterns are to be generate before high fault coverage is rack up[8]. Therefore, weighted pseudorandom techniques have been suggested. Weighted random pattern generation methods relying upon an individual weight assigning generally fail to achieve complete fault coverage applying a reasonable number of test patterns since, although the weights are computed to comprise for most faults, several faults can require long test sequences to be perceived on this weight assignment whenever they do not match their activation and extension demands[9]. Multiple weight assignments have been suggested for the case that a different fault involve various biases of the input combinations applied to the circuit, to assure that a comparatively smaller number of patterns can detect all faults[10][11] [4].

Although, get bigger in the circuit complexity was in the view of the embedded memories verification more challenging. Among the obstacle encountered while testing the memories are 1. Controllability of the logic elements problem. The controllability is involved in the desired values on the internal signal of the circuit by exploiting an suitable test vector input combination to the inputs of the primary. 2. The Observability of the logic element is facing problem. Observability is an internal signal can be propagated through primary output for comparison with expected the value of the application of an appropriate primary input combination. 3. Insufficiency fault coverage in the testing of embedded memory.4. Sprouting the testing data to be stored and resolved. 5. The state of the art jet set and expensive testers are needed to test the embedded memory.

III. MOTIVATION OF THE BIST VERSES ATE

There are two main approaches for testing embedded memories: external test by direct access using Automatic Test Equipment, (ATE) and internal testing using Built-In-Self Test (BIST). When external testing is employed, the input test vectors and correct response data are stored in the ATE memory. For external testing, the comparison is carried out on the tester.

ATE limitations make BIST technology an attractive alternative to external test for complex chips. BIST is a Design for Test method where part of the circuit is used to test the circuit itself where the test vectors are generated and test responses are analyzed on-chip.

ATE, as well as very long testing time since tester channels are timeshared by different memories under test. On the other hand, BIST provides at-speed and high bandwidth access to the embedded memory cores and it only needs a low cost to initialize the test sessions and to inspect the final results either status bits pass or fail. However, although BIST is may induce excessive power, in addition to performance and area overhead.

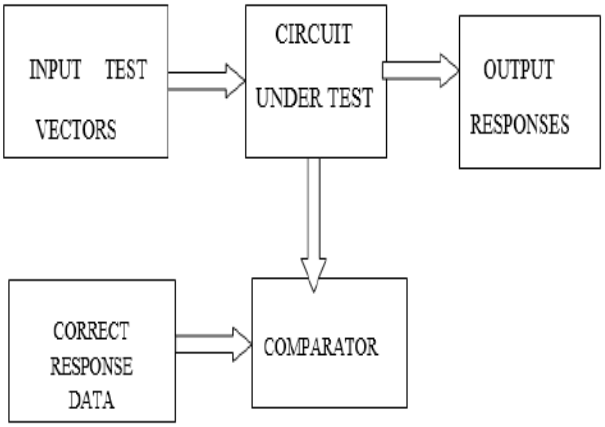

Fig. 2 Test pattern Application for BIST

IV. PROPOSED ARCHITECTURE

Both Microcode-based and FSM-based controllers are two widely known architectures for programmable memory built-in self test process. These two widely techniques are much popular because of their flexibility of programming new test algorithms. In this proposed paper, the architectures for both controllers are designed to implement a new better test algorithm MARCH SAM, which gives a better fault coverage in both detecting single-cell fault and all intra-word coupling fault (CF).

Memory built-in self test (MBIST) system mainly consists of three main components such as controller, comparator and fail/pass register. The MBIST controllers are either microcode-based or FSM-based controllers. Both of the controllers made of address generator, read/write sequence generator and data generator. The address generator produces memory address to be tested in ascending order, descending order and hold order.

Read/write sequence generator controls the assertion of test data to memory and retrieval of test data from the memory. The test data sequences are applied to the memory under test (MUT) and also wait at the comparator

for comparison with tested data from the memory. The results (pass/fail) from the comparator is stored in the register. Some of the latest MBIST design are combined with micro code and Finite state machine based architectures are used to compensate the are versus speed issues

Developing and MBIST engine for a memory or a group of memories and its verification can become a challenge when Time-To-Market (TTM) factor is considered. EDA Companies in the recent years had developed various tools for automating MBIST hardware generation it can be argued that adapting such MBIST engine generator could be a good alternative to develop an "in-house" MBIST architecture.

While most ASIC companies employ memory compilers to generate their required memories and microprocessors companies heavily concentrate on custom memory designs to meet their requirements in terms of speeds of GHz range, wide data buses ranging on addresses of notes, error detection and correction capabilities for reliability , and huge memory capacity. An efficient memory testing solution in terms of parameters such as test quality, test time and failure bit mapping capabilities would need to accommodate all these requirements, which may not be achievable with a generic commercial solutions. Furthermore, the MBIST based solutions should provide a bridge to the post – silicon activities. Availability of a high number of features, such as various operating modes and addressing modes, necessitates the existence of an efficient test program generation methodology. The MBIST engine should enable quick access to these operating modes to generate failure bit map for yield improvement and memory repair. To meet the challenges imposed by the state of the art memory designs and their requirements, we have decided to develop our code by MBIST RTL code generator as well as all the infrastructure to perform verification and post – silicon activities.

A. MICRO CODE BIST

Micro code or predefined instructions are used to wire the selected test algorithms. The written tests are loaded into the Memory BIST controller. The Micro code-based type of BIST allows changes in the chosen test algorithm with no impact on the hardware of the controller. However the flexibility is there but cost of the higher logic is over head for the controller. A recent Micro-code based type of Memory BIST allows changes in the selected test algorithm with no impact of hardware of the controller. A recent Micro code based MBIST implementing modified proposed MBIST can be widely used for the embedded memory testing, especially under SOC design environment because of superior flexibility and expendability. .

B. HARD WIRE –BASED BIST:

A hardwired-based controller is a hardware realization of a selected memory test algorithm, usually in the form of a Finite State Machine (FSM). This type of memory BIST architecture has optimum logic overhead, however, lacks the flexibility to accommodate any changes in the selected memory test algorithm. This results in re-design and reimplementation of the hardwired-based memory BIST for any minor changes in the selected memory test algorithm. Although it is the oldest memory BIST scheme amongst the three, hardwired-based BIST is still much in use and techniques have been kept developing. Table 2: Trade-offs between Different Memory BIST Schemes Table 1 gives the summary of this comparison of the three implementations. The four evaluation metrics used are: test time, area overhead, routing overhead, and flexibility. The routing overhead is directly translated into design efforts and time to market. The flexibility is

.

C. MARCH SAM Test ALGORITHM:

The test patterns used in the designs are MARCH SAM This algorithm is applied for all intra-word coupling fault detection. Table 2 shows types of test algorithms i.e. stored in the ROM and their read /write sequnces . Upward and downward arrows represents the ascending and descending order respectively. The d and d' indicates the true and inverted of the choosen data backgrounds(DBs). The notations of d 0-d9 are the specific DBs to test intraword coupling faults (CF). Design efforts and possesses the least flexibility. On the opposite end of spectrum, the Processor-based BIST is the most flexible, zero area or routing overhead, but incur long test time. The Microcode-based designs is somewhere in between these two extreme prototypes.

TABLE 2: MARCH SAM TEST ALGORITHM

Test Pattern	Description
MARCH SAM level 1	↕wd0a, rd0a, wd0a, rd0a, rd0a ↕wd1, rd1, wd1, rd1, rd1 ↕wd2a, rd2a, wd2a, rd2a, rd2a ↕wd3, rd3, wd3, rd3, rd3 ↕wd2a, rd2a; ↕wd1, rd1 ↕wd0a, rd0a; ↕wd3, rd3
MARCH SAM level 2	↕wd0b, rd0b, wd0b, rd0b, rd0b ↕wd1, rd1, wd1, rd1, rd1 ↕wd2b, rd2b, wd2b, rd2b, rd2b ↕wd3, rd3, wd3, rd3, rd3 ↕wd2b, rd2b; ↕wd1, rd1 ↕wd0b, rd0b; ↕wd3, rd3
MARCH SAM level 3	↕wd0c, rd0c, wd0c, rd0c, rd0c ↕wd1, rd1, wd1, rd1, rd1 ↕wd2c, rd2c, wd2c, rd2c, rd2c ↕wd3, rd3, wd3, rd3, rd3 ↕wd2c, rd2c; ↕wd1, rd1 ↕wd0c, rd0c; ↕wd3, rd3
MARCH SAM level 4	↕wd0d, rd0d, wd0d, rd0d, rd0d ↕wd1, rd1, wd1, rd1, rd1 ↕wd2d, rd2d, wd2d, rd2d, rd2d ↕wd3, rd3, wd3, rd3, rd3 ↕wd2d, rd2d; ↕wd1, rd1 ↕wd0d, rd0d; ↕wd3, rd3

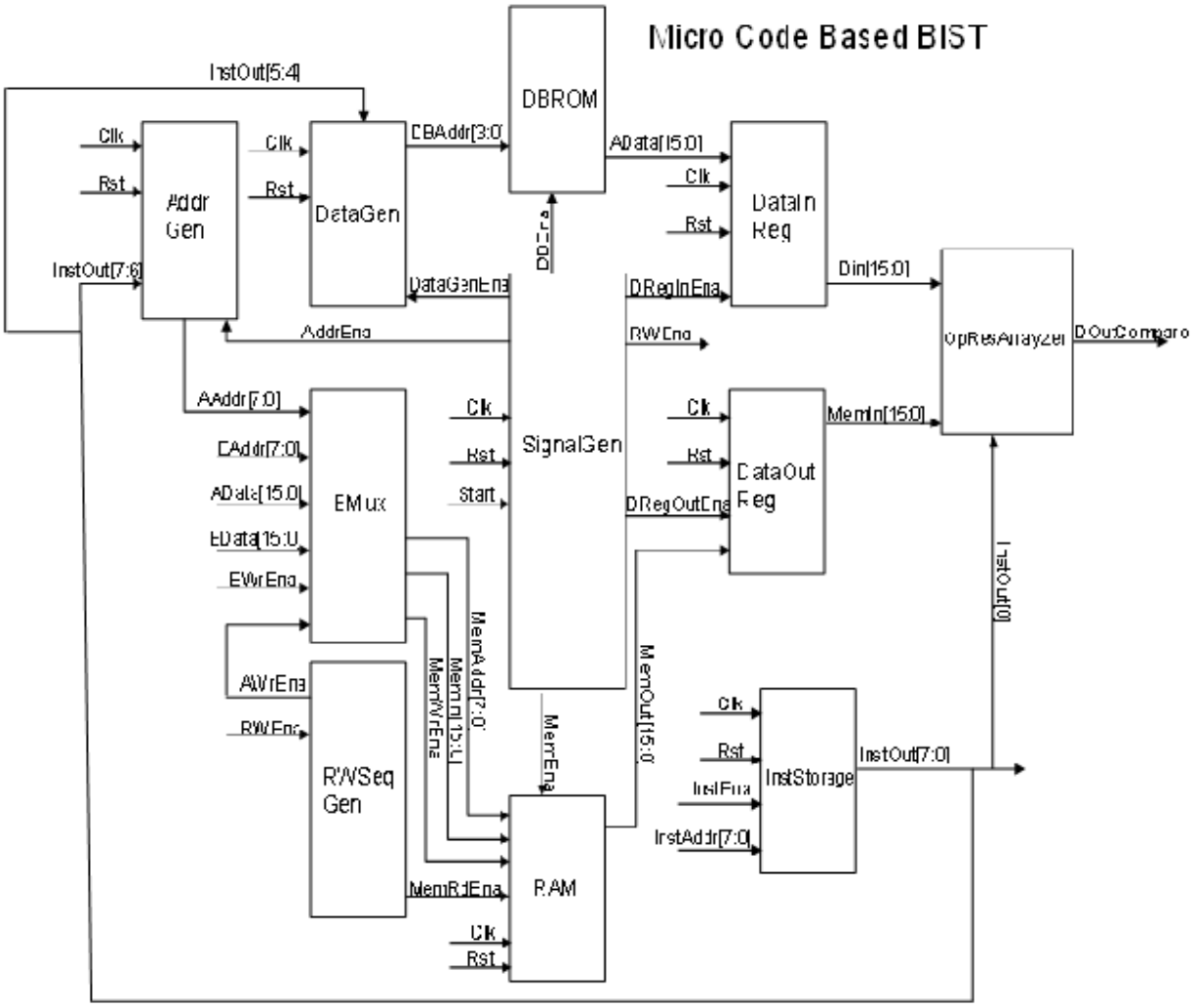

Fig. 3 Block Diagram of Micro Code Based Architecture

The controller comprises of instruction storage, address generator, data generator, read/write sequence generator, data input/output registers and output response analyzer. It uses counters to determine the instruction cycles and the selected data background

The instruction storage stored all the MARCH SAM's microcode instructions. Each microcode instruction is 8 bit wide. Bit 7 and 6 represents the memory address status (increment, decrement or hold).Bit 5 selects the desired data background while bit 4 represents the true or inverted data background. Read/write sequences are controlled by bit 3. Looping feature is represented by bit 2 and bit 1 but this feature is temporary halted since it is not used in this design. The last bit is set to compare the expected data and the tested data. The last two bits i.e 7 & 6 are given to address generator which indicates whether to increment or decrement or hold the memory location in the RAM. the 5and 4 bits are to data generator and the output of data generator is of 4 bits which indicates which data back ground to be selected is given to DBROM. The DBROM selects the desired data background whether to take the true value or inverted value of the background. Its output is given to the MUX which is used to take the address given by the DBROM or the externally given address and the output of EMUX is given to RAM.

Depending on whether to read or write bit the data from the RAM is read or data is written into the RAM. Another EMUX is used which takes the address given by address generator or an external address and the output of EMUX is given to RAM. The RAM gives the output data to the data output register. The output response analyzer compares both values present in data output and data input registers and gives the response to the pass/fail register

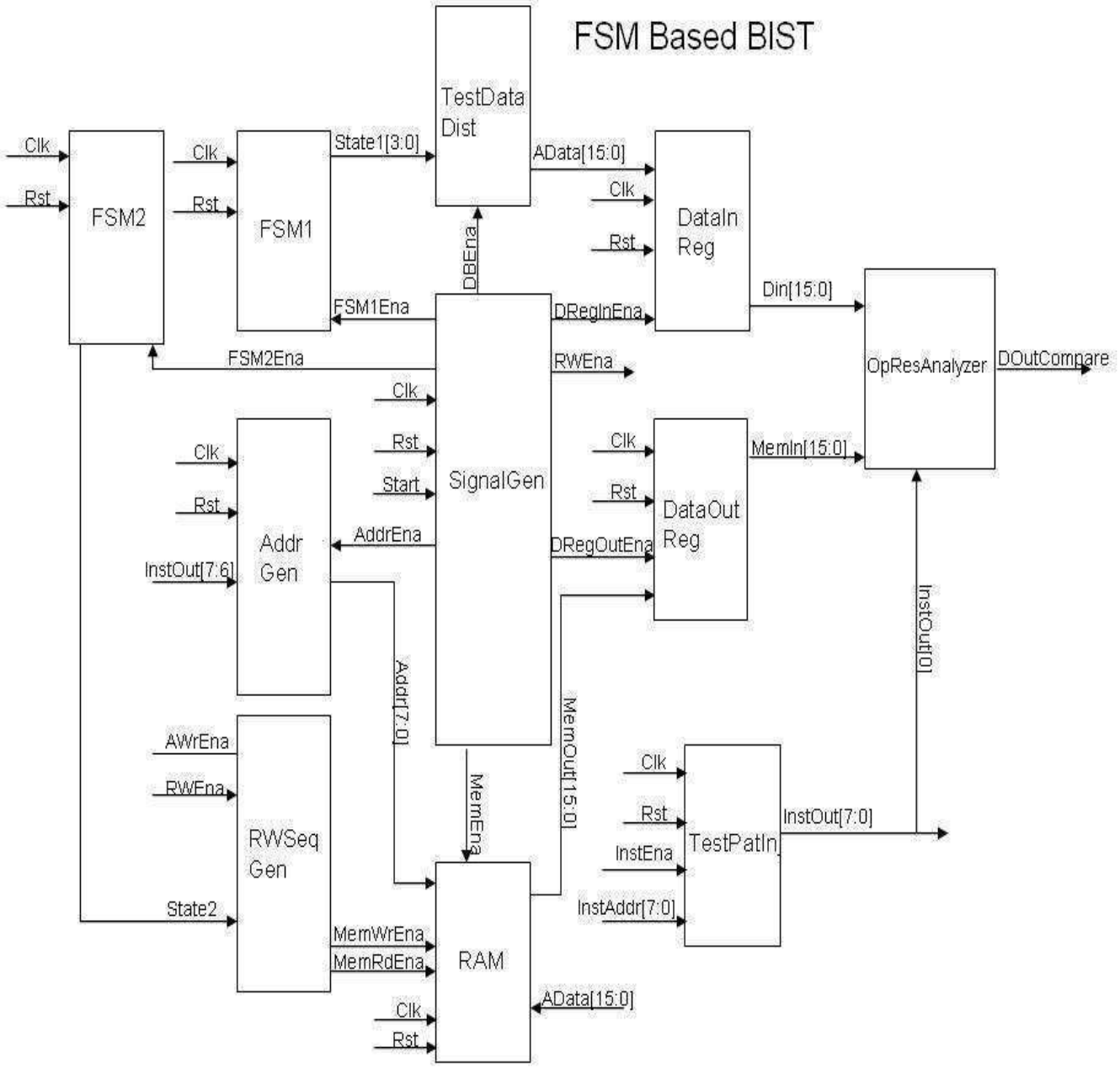

Fig. 4. Block Diagram of Finite State Machine Architecture

The design of FSM based MBIST using MARCH SAM for WOM is developed. The controller comprises of 2 FSMs; state1 to inject each DB's sequences to be tested and state2 to control the read/write sequences. The test patterns can directly inputted in the FSM but to allow flexibility of inserting different kind of test patterns, ROM is chosen for storage. The controller embodies the test pattern injector block, test data distributor block, r/w sequences generator and address generator.

State1 FSM has 11 states Sdb_init, Sdb0, Sdb1, Sdb2, Sdb3, Sdb4, Sdb5, Sdb6, Sdb7,Sdb8,sdb9,sdb10).Each states (Sdb0-Sdb10) will loop back to the state Sdb_init after their operation is finished. Counter at Sdb_init will determine which states will be treated next. Clk_db is the clock that controls the states' operation.

State2 FM has 4 states namely Sx , Sr , Sw. Sx is the initialization state which are vital to be included in the design to ensure read/write sequences on each DBs follows any desired test algorithms. The pass and flag is controlled mainly by the memory clock and the active low of read/write sequences clock. If the state2 is Sr and the output equals the injected data, the pass flag will be up. But if the

output is different from the injected area, then the fail flag will be on

V. SIMULATION RESUTLS AND FLOOR PLAN DESIGN

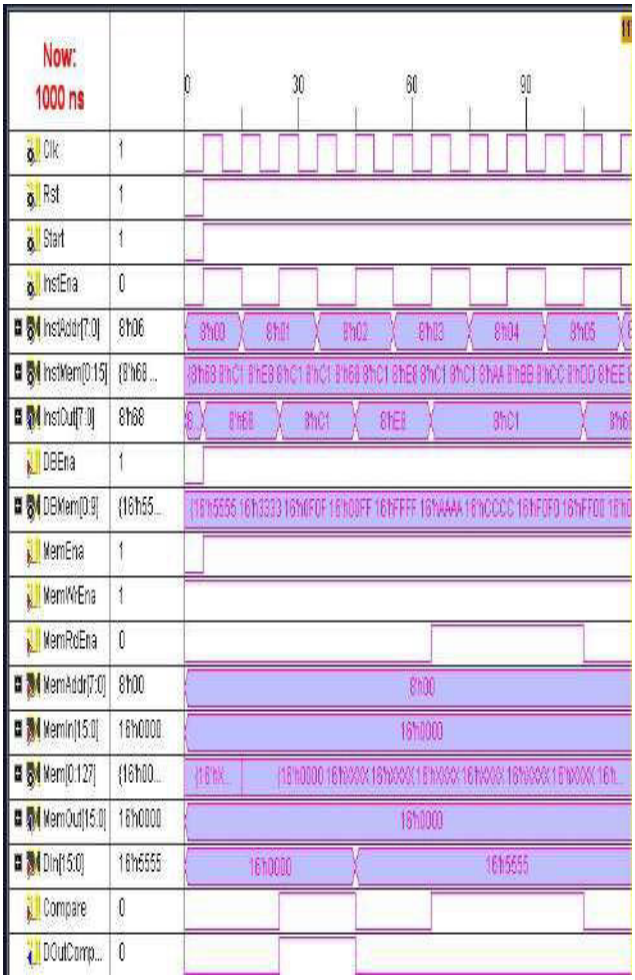

Fig.4 Top Module of Top Module for FSM Output

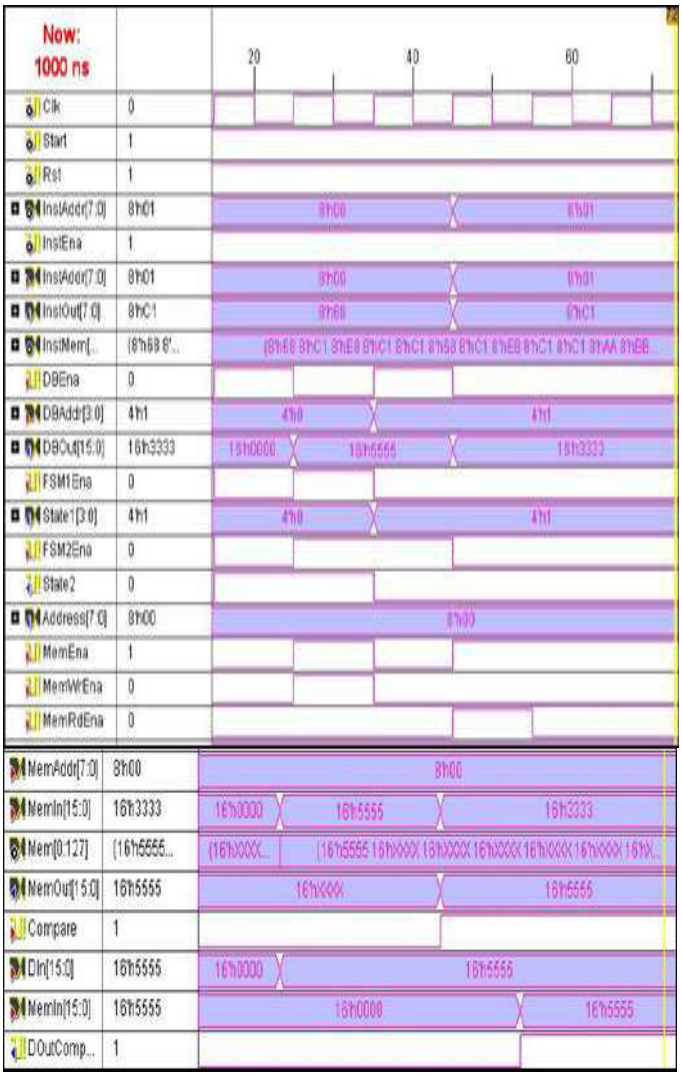

Fig.6 Top Module of Micro Code Based Output

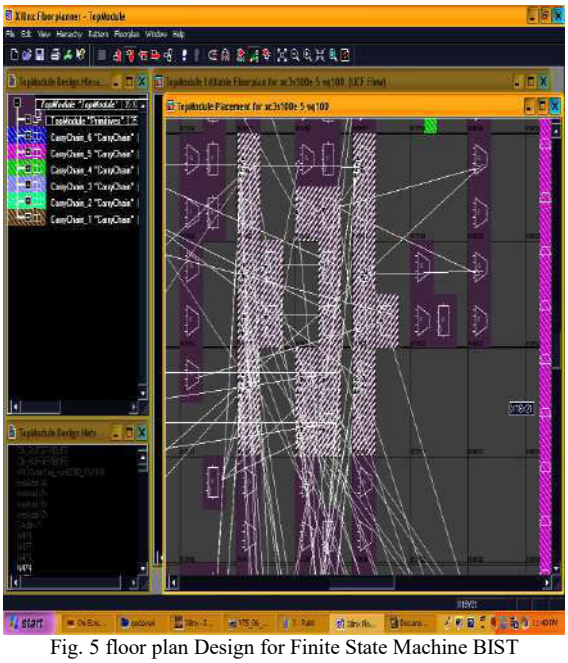

Fig. 5 floor plan Design for Finite State Machine BIST

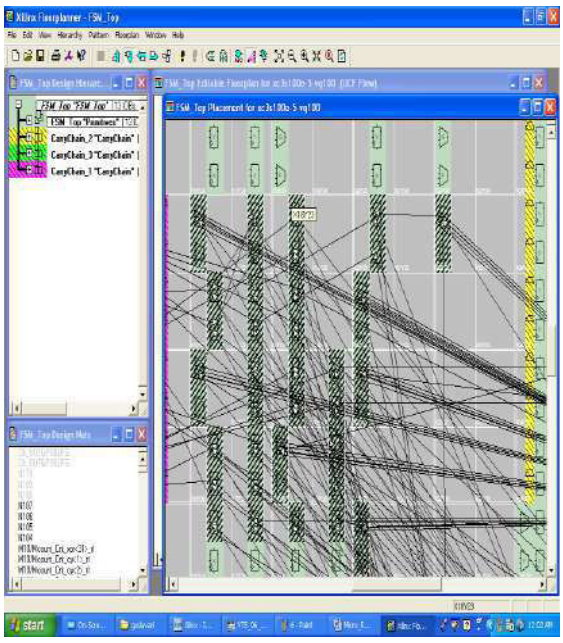

Fig. 7 Floor plan design for Micro code based BIST

VI. CONCLUSION:

Micro Code based and FSM based MBIST controllers are designed to detect coupling faults. The architectures for both controllers are designed to implement a new test algorithm MARCH SAM that gives a better fault coverage in detecting single-cell fault and all intra-word coupling fault (CF).The components of each controllers are studied and designed. Both of the controllers are written using Verilog HDL.

Architecture for Micro Code based and FSM based controllers is designed. Individual modules are designed and integrated. Simulation results for individual and integrated modules are verified. Synthesis results are obtained. Synthesis is done using Spartan3E device. Total equivalent gate count for Micro Code based MBIST Controller top module is **19,519** and for FSM based MBIST Controller top module is **5,647.** So Micro Code based controller has higher area consumption compared to FSM based controller.

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Look Up Table Optimization for Memory Based Computation Techniques

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***Abstract*— Recently, we have proposed the antisymmetric item coding (APC) and odd-multiple storage (OMS) methods for query table (LUT) outline for memory-based multipliers to be utilized as a part of advanced flag preparing applications. Each of these systems brings about the decrease of the LUT measure by a factor of two. In this short, we show an alternate type of APC and a changed OMS conspire, keeping in mind the end goal to join them for proficient memory-based augmentation. The proposed joined approach gives a lessening in LUT size to one-fourth of the customary LUT. We have likewise recommended a basic system for particular sign inversion to be utilized as a part of the proposed plan. It is demonstrated that the proposed LUT outline for little information sizes can be utilized for productive execution of high-exactness augmentation by input operand decay. It is discovered that the proposed LUT-based multiplier includes practically identical range and time many-sided quality for a word size of 8 bits, however for higher word sizes, it includes altogether less territory and less augmentation time than the sanctioned marked digit (CSD)- based multipliers. For 16-and 32-bit word sizes, individually, it offers over 30% and half of sparing in area– defer item finished the comparing CSD multipliers.**

Index Terms*—Digital signal processing (DSP) chip, lookuptable (LUT)-based computing, memory-based computing.*

I. INTRODUCTION

Digital signal processing algorithms typically require a large number of mathematical operations[1,2,3] to be performed quickly and repetitively on a set of data. Signals are constantly converted from analog to digital, manipulated digitally, and then converted again to analog form, as diagrammed below. Many DSP applications have constraints on latency; that is, for the system to work, the DSP operation must be completed within some fixed time, and deferred processing is not viable. Digital signal processing[5-7}:

Fig. 1 Basic Block diagram of digital signal processing

In-order to reach a certain criteria memory based computation plays a vital role in dsp (digital signal processing) application.

A. FILTER DESIGNING :

Finite impulse response (FIR) digital filter is widely used as a basic tool in various signal processing and image processing applications[7,8,9]. The order of an FIR filter primarily determines the width of the transition-band, such that the higher the filter order, the sharper is the transition between a pass-band and adjacent stop-band. Many applications in digital Communication (channel equalization, frequency channelization), speech processing (adaptive noise cancelation), seismic signal processing (noise elimination), and several other areas of signal processing require largeorder FIR filters. Since the number of multiply-accumulate[12,13,14] (MAC) operations required per filter output increases linearly with the filter order, real-time implementation of these filters of large orders is a challenging task. Several attempts have, therefore, been made and continued to develop low-complexity dedicated VLSI systems for these filters.As the scaling in silicon devices has progressed over the last four decades,[11]semiconductor memory has become cheaper, faster and more power-efficient. According to the projections of the international technology roadmap for semiconductors (ITRS) , embedded memories will continue to have dominating presence in the system-on-chip (SoC), which may exceed 90% of total SoC content. It has also been found thatthe transistor packing density of SRAM is not only high, but also increasing much faster than the transistor density of logic devices[15] .

B. BINARY MULTIPLICATION:

Multiplication in binary is similar to its decimal counterpart. Two numbers A and B can be multiplied by partial products: for each digit in B, the product of that digit in A is calculated and written on a new line, shifted leftward so that its rightmost digit lines up with the digit in B that was used. The sum of all these partial products gives the final result.

C. MEMORY BASED MULTIPLICATION :

The input-output relationship of an N-tap FIR filter in time-domain is given by

$$Y(n)= h(0).x(n) + h(1).x(n-1)-------h(N-1).x(n-N+1) \quad \ldots(1)$$

where h(n), for n = 0,1,2,--------N-1, represent the filter coefficients x(n-i), while for i== 0,1,2,--------N-1, for x(n) , represent recent input samples y(n), and represents the current output sample. Memory-based multipliers can be implemented for signed as well as unsigned operands

The objectives of this work are:

- Multiplying two binary numbers one number is fixed X[4:0] and another variable _A‘
- Using APC–OMS combined LUT design for the multiplication of W-bit fixed coefficient A with 5-bit input X.
- Number of calculations reduced and memory required is less to perform multiplication.

For 16- and 32-bit word sizes, respectively, it offers more than 30% and 50% of saving in area–delay product over the corresponding CSD multipliers.

II. PROPOSED WORK:

A. ANTI -SYMMETRIC PRODUCT CODING:

Anti symmetric product coding is the technique used to process the multiplication based on LUT multiplication which reduces the size of conventional lut by 50 % .

The anti symmetric product coding is based on the antisymmetric coding i.e the 2‘s complement phenomenon which is used to reduce the LUT size by half.

For simplicity of presentation, we assume both X and A to be positive integers.2 The product words for different values of X for L = 5 are shown in Table I. It may be observed in this table that the input word X on the first column of each row is the two‘s complement of that on the third column of the same row. In addition, the sum of product values corresponding to these two input values on the same row is 32A. Let the product values on the second and fourth columns of a row be u and v, respectively.

Since one can write
u = [(u + v)/2 − (v − u)/2] and
v = [(u + v)/2 + (v − u)/2], for (u + v) = 32A, we can have

TABLE I
APC WORDS FOR DIFFERENT INPUT VALUES FOR $L = 5$

Input, X	product values	Input, X	product values	address $x_3'x_2'x_1'x_0'$	APC words
0 0 0 0 1	A	1 1 1 1 1	$31A$	1 1 1 1	$15A$
0 0 0 1 0	$2A$	1 1 1 1 0	$30A$	1 1 1 0	$14A$
0 0 0 1 1	$3A$	1 1 1 0 1	$29A$	1 1 0 1	$13A$
0 0 1 0 0	$4A$	1 1 1 0 0	$28A$	1 1 0 0	$12A$
0 0 1 0 1	$5A$	1 1 0 1 1	$27A$	1 0 1 1	$11A$
0 0 1 1 0	$6A$	1 1 0 1 0	$26A$	1 0 1 0	$10A$
0 0 1 1 1	$7A$	1 1 0 0 1	$25A$	1 0 0 1	$9A$
0 1 0 0 0	$8A$	1 1 0 0 0	$24A$	1 0 0 0	$8A$
0 1 0 0 1	$9A$	1 0 1 1 1	$23A$	0 1 1 1	$7A$
0 1 0 1 0	$10A$	1 0 1 1 0	$22A$	0 1 1 0	$6A$
0 1 0 1 1	$11A$	1 0 1 0 1	$21A$	0 1 0 1	$5A$
0 1 1 0 0	$12A$	1 0 1 0 0	$20A$	0 1 0 0	$4A$
0 1 1 0 1	$13A$	1 0 0 1 1	$19A$	0 0 1 1	$3A$
0 1 1 1 0	$14A$	1 0 0 1 0	$18A$	0 0 1 0	$2A$
0 1 1 1 1	$15A$	1 0 0 0 1	$17A$	0 0 0 1	A
1 0 0 0 0	$16A$	1 0 0 0 0	$16A$	0 0 0 0	0

For $X = (0\ 0\ 0\ 0\ 0)$, the encoded word to be stored is $16A$.

The product values on the second and fourth columns of Table I therefore have a negative mirror symmetry. This behavior of the product words can be used to reduce the LUT size,where, instead of storing u and v, only [(v − u)/2] is stored for a pair of input on a given row. The 4-bit LUT addresses and corresponding coded words are listed on the fifth and sixth columns of the table, respectively. Since the representation of the product is derived from the anti-symmetric behavior of the products, we can name it as anti-symmetric product code.Decoding is necessary in applications such as data multiplexing, 7 segment display and memory address decoding.

A simple CPU with 8 registers may use 3-to-8 logic decoders inside the instruction decoder to select two source registers of the register file to feed into the ALU as well as the destination register to accept the output of the ALU. A typical CPU instruction decoder also includes several other things.

selector is used to generate PVN (product value number) which is used to calculate the corresponding product value i.e (PVN X A)

The PVN is calculated depending on the W input corresponding bit set in order to generate the stored APC word i.e

The possible PVN values are
When w = 000000001 then PVN = 1
When w = 000000010 then PVN = 3
When w = 000000100 then PVN = 5
When w = 000001000 then PVN = 7
MULTIPLIER RESULT:

Multiplier result module is used to calculate multiplication of individual bits of operand and get the individual multiplication results .

```
Ex:    1 0 1 1  (A)
     × 1 0 1 0  (B)
     ---------
       0 0 0 0 ← ress0        i.e B(0)  X A
   +   1 0 1 1 ← ress1        i.e B(1)  X A
   +   0 0 0 0 ← ress2        i.e B(2)  X A
   +   1 0 1 1 ← ress3        i.e B(3)  X A
```

B. BARREL SHIFTER :

Barrel Shifter is an combinational logic circuit which is used to do any no. of shift‘s for one clock cycle. Depending upon the _s‘ the no of shift‘s is decided and output _outp‘ is given .For example, take a 4-bit barrel shifter, with inputs A, B, C and D. The shifter can cycle the order of the bits ABCD as DABC, CDAB, or BCDA; in this case, no bits are lost. That is, it can shift all of the outputs up to three positions to the right (and thus make any cyclic combination of A, B, C and D). The barrel shifter has a variety of applications, including being a useful component in microprocessors (alongside the ALU).

Implementation:

A barrel shifter is often implemented as a cascade of parallel 2×1 multiplexers. For a 4-bit barrel shifter, an intermediate signal is used which shifts by two bits, or passes the same data, based on the value of S[1]. This signal is then shifted by another multiplexer, which is controlled by S[0]:

```
im = IN, if S[1] == 0
   = IN << 2, if S[1] ==
1 OUT = im, if S[0] == 0
   = im << 1, if S[0] == 1
```

It is used to add the intermediate results to 16A to get the final output .It may make output 0 when _clr‘ is high.

u = [(u + v)/2 − (v − u)/2] and
v = [(u + v)/2 + (v − u)/2], for (u + v) = 32A,

$$u = 16A - \left[\frac{v-u}{2}\right] \quad v = 16A + \left[\frac{v-u}{2}\right].$$

$$\text{Product word} = 16A + (\text{sign value}) \times (\text{APC word})$$

When xin(4) = _1‘ then sign value = 1
When xin(4) = _0‘ then sign value = 0.

4-bit_ripple_carry_adder-subtracter.svg

In digital circuits, an adder-subtractor is a circuit that is capable of adding or subtracting numbers.

This works because when D = 1 the A input to the adder is really $\overline{A}$ and the carry in is 1. Adding Bto $\overline{A}$ and 1 yields the desired subtraction of B − A.

The adder-subtractor above could easily be extended to include more functions. For example, a 2-to-1 multiplexer could be introduced on each Bi that would switch between zero and Bi; this could be used (in conjunction with D = 1) to yield the two's complement of A since $-A = \overline{A} + 1$.

A further step would be to change the 2-to-1 mux on A to a 4-to-1 with the third input being zero, then replicating this on Bi thus yielding the following output functions:

0 (with the both Ai and Bi input set to zero and D = 0)
1 (with the both Ai and Bi input set to zero and D = 1)
A (with the Bi input set to zero)
B (with the Ai input set to zero)
A + 1 (with the Bi input set to zero and D = 1)
B + 1 (with the Ai input set to zero and D = 1)
A + B
A − B
B − A
$\overline{A}$ (with Ai set to invert; Bi set to zero; and D = 0)
− A (with Ai set to invert; Bi set to zero; and D = 1)
$\overline{B}$ (with Bi set to invert; Ai set to zero; and D = 0)
− B (with Bi set to invert; Ai set to zero; and D = 1)

By adding more logic in front of the adder, a single adder can be converted into much more than just an adder — an ALU.

LUT APC – OMS Optimization Top Model

The APC approach, although providing a reduction in LUT size by a factor of two, incorporates substantial overhead of area and time to perform the two‘s complement operation of LUT output for sign modification and that of the input operand for input mapping.

The proposed APC–OMS combined design of the LUT for L = 5 and for any coefficient width W is shown in Fig. 2.4. It consists of an LUT of nine words of (W + 4)-bit width, a four-to-nine-line address decoder, a barrel shifter, an address generation circuit, and a control circuit for generating the RESET signal and control word (s1s0) for the barrel shifter.

The recomputed values of A × (2i + 1) are stored as Pi, for i = 0, 1, 2, . . . , 7, at the eight consecutive locations of the memory array, as specified in Table II, while 2A is stored for input X = (00000) at LUT address ―1000,‖ as specified in Table III. The decoder takes the 4-bit address from the address generator and generates nine word-select signals, i.e., {wi, for 0 ≤ i ≤ 8}, to select the referenced word from the LUT. Here we observe that they will Antisymmetry in the address for the LSB 4 bits. We will get all the address from 0 to 15 for 0 to 31.Thus we reduce the memory locations required to store coefficients by half. Then we will store only odd coefficients in the look up table .

Thus we reduce the number of coefficients by half again. On total we have reduced the number coefficients by quarter.

RESULTS AND CONCLUSION:

The proposed LUT multipliers for word measure L = W = 8, 16, and 32 bits are coded in VHDL and integrated by Synopsys Design Compiler utilizing the TSMC 90-nm library, where the LUTs are actualized as varieties of constants, and increases are executed by the Wallace tree and swell convey exhibit. The CSD-based multipliers having a similar expansion plans are additionally integrated with a similar innovation library. The territory and defer complexities of the multipliers evaluated from the combination comes about are recorded in Table IV. It is discovered that the proposed LUT configuration includes similar region and time complexities for a word size of 8 bits, yet for higher word sizes, it includes fundamentally less region and less augmentation time than the CSD-based multiplier. For L = W = 16, and 32 bits, separately, it offers over 30% and half of sparing in area– postpone item (ADP) over the CSD multiplier.

In this short, we have demonstrated the likelihood of utilizing LUT based multipliers to actualize the steady duplication for DSP applications. The full points of interest of proposed LUT based plan, be that as it may, could be determined if the LUTs are actualized as NAND or NOR read-just recollections and the number juggling shifts are executed by a cluster barrel shifter utilizing metal– oxide–semiconductor transistors [11]. Additionally work should at present be possible to infer OMS– APC-based LUTs for higher info sizes with various types of deteriorations and parallel and pipelined option plans for reasonable area– postpone tradeoffs.

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High Frequency AC Link Dual Active Bridge Isolated Bidirectional Dc–Dc Converter for PV Application

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ABSTRACT: In this paper, high repeat cooling association twofold dynamic platform separated bidirectional dc –dc converter for PV application is proposed. The proposed converter beats most of the issues associated with at present open PV converters. Dual active bridge (DAB) converters have been standard in high voltage, low and medium power DC-DC applications, further more a center high repeat interface in solid state transformers. The proposed DAB has the upside of being used as a piece of high walk up/down converters, which oversee higher voltages, when diverged from normal two -level DABs.

Index Terms: Bidirectional converters, dc–dc conversion, and dual active bridge.

I. INTRODUCTION

For the present, power transformation frameworks (PCSs) essentially utilize line-recurrence (LF) transformers to accomplish galvanic detachment and voltage coordinating [1]–[5]. Apid improvement of appropriated era and vitality stockpiling has prompted the expanding prevalence of PCSs as a continually enduring key interface [6].

Be that as it may, massive, substantial, misfortunes, and boisterous LF transformers impede the effectiveness and influence thickness of PCSs. Lately, the utilization of high- recurrence (HF) transformers set up of conventional LF transformers is thought to be the creating pattern of cutting edge power transformation. Fig. 1 demonstrates a similar photograph of 50-Hz LF and 20-kHz HF transformers. The upsides of HF transformers are low volume, light weight, and ease. Furthermore, high-recurrence join (HFL) PCSs in light of HF transformers can likewise maintain a strategic distance from voltage and current waveform bending brought about by the center immersion of LF transformers. Furthermore, when the exchanging recurrence is over 20 kHz, PCS commotion can be significantly decreased. Particularly, out of sight of fast extend of PCS; HFL-PCSs have wide application prospects.

In the exploration of HFL-PCSs, disengaged bidirectional dc–dc converters (IBDCs) generally serve as the key circuit. By and large, all of IBDCs can be developed from conventional secluded unidirectional dc–dc converters (IUDCs, for example, fly back IUDC can make double fly back IBDC, half-connect or push–pull IUDC can form double half-connect or double push–pull IBDC, and full- connect IUDC can create double dynamic scaffold IBDC. Actually, other than the IBDCs made out of IUDCs with the same sort, the IUDCs with distinctive sorts likewise can create IBDCs, for example, half-connect IUDC and push– pull IUDC can make a half-scaffold push-pull IBDC in light of the fact that the half-extension and push force structures can withstand high- and low-source voltages, separately, so this kind of IBDC can be utilized as a part of the application with a wide voltage extent and a bidirectional force stream.

Fig. 1. Comparative photo of 50-Hz LF and 20-kHz HF transformers

Like the order of conventional dc–dc converters in force gadgets, this paper introduces an arrangement of IBDC topology

in light of the quantity of switches, The easiest IBDC topology is a double switch structure, for example, double fly back IBDC, double Cuk IBDC, and Zeta-Sepic IBDC . The run of the mill model of three-switch topology is forward-fly back IBDC . Four-switch topologies essentially contain double push-pull IBDC, push-draw forward IBDC, push pull-fly back, and double half- span IBDC . The commonplace model of five-switch topology is full-extension forward IBDC. The regular model of six-switch topology is half-full connect IBDC . Eight-switch topology is essentially double dynamic extension IBDC

II. MODELLING OF PV MODULE

A photovoltaic cell is one which changes over approaching daylight into electric current by method for photoelectric impact. It is fundamentally a p-n intersection manufactured in a wafer. The yield of a PV cell is low and thus these cells are associated in arrangement and parallel to expand the voltage and current levels. Since a PV cell displays nonlinear connection in the middle of voltage and current for differing levels of temperature and Irradiance levels. A sun oriented cell can be demonstrated by utilizing an one diode model, which is the most broadly utilized system. We can likewise a two diode model or a three diode model for displaying a PV cell. In this work, a solitary diode mode is considered. In a some diode demonstrate, a PV cell is displayed as a variable current source in hostile to parallel with a diode, additionally an arrangement and shunt resistance (RS & RP) [4].

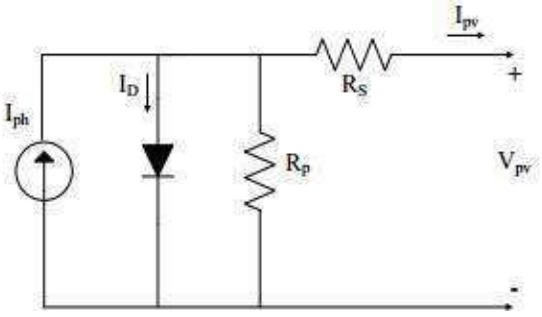


Figure 2. The one diode model

The yield of PV cell is given by

$$I = N_p I_{ph} - N_p I_o \left(exp\left[\frac{q(V/Ns + IRs/Np)}{AkT}\right] - 1 \right) - \frac{V}{R_p}$$

where, I is the present, V is the voltage of the PV module, Iph is the photograph current, I0 is the opposite immersion current, Np is the quantity of cells associated in parallel, Ns is the quantity of cells joined in arrangement, q is the charge of an electron
(1.6*10-19C), k is Boltzmann's consistent (1.38*10-23J/K), An is p-n intersection ideality calculate, (1 < a < 2, a = 1 being the perfect worth), and T is the PV module temperature.
For a sun powered cell, the main produced current is by method for a photograph current which is straightforwardly subject to temperature and also irradiance level given by

$$I_{ph} = [I_{sc} + k_1(T - T_{ref})]G$$

Where I_{sc} is the short out current of the PV cell, K1 is the short out current/temperature coefficient T is the present barometrical temperature and Tref is the temperature at ostensible condition (250oC and 1000W/m2), G is the present irradiance level.
The P-V and I-V attributes of a PV cell are demonstrated in figure 3. The most extreme force is achieved when the cell works at Imp and V_{mp}.

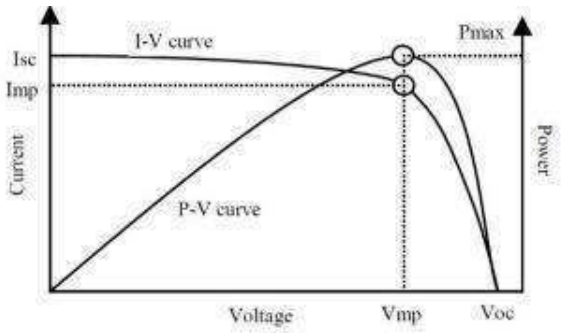


Fig -3: Current-voltage and power-voltage characteristics of a solar cell

The PV module considered for reproduction was Tata TP 250 Series with determinations at Nominal Operating Cell Temperature (NOCT – 20oC & 800 W/m2) was viewed as opposed to Standard Test Condition (STC – 25oC & 1000W/m2).

III. PROPOSED CONVERTER

A. Basic Principle

The far reaching investigations of the operation, outline, and control of DAB-IBDC in consistent state and a limit control plan for DAB-IBDC utilizing the common exchanging

surface is available. Examined the brief while scale transient procedures with stage movement control and proposed an arrangement of methods to build framework strength.

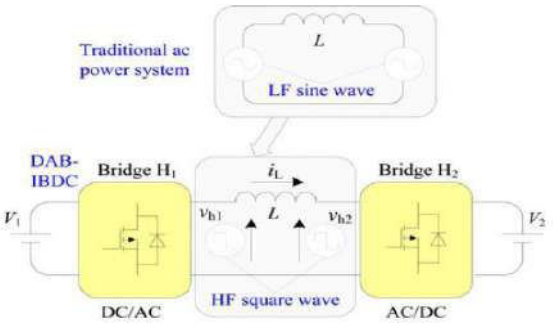


Fig. 4. Basic principles of traditional ac power system and DAB-IBDC.

Fig. 4 demonstrates that like the control of the force transmission in conventional air conditioning force frameworks, the course and extent of the inductor current i_L can be changed by conforming the stage move between air conditioning yield square wave voltages vh_1 and vh_2 of scaffolds H_1 and H_2 , which can control the bearing of force stream and size of DAB-IBDC. The distinction is that the voltages in both sides of the inductor in conventional air conditioning force framework are line-recurrence sinusoidal waves and in DAB-IBDC are high-recurrence square waves. The transmission force models of the customary air conditioning force framework and of DAB-IBDC can be determined as

$$\begin{cases} P_{\text{sine}} = \dfrac{V_{\text{rms1}} V_{\text{rms2}}}{2\pi f_s L} \sin\varphi \\ P_{\text{square}} = \dfrac{nV_1 V_2}{2\pi^2 f_s L} \varphi(\pi - \varphi) \end{cases}$$

Where V_{rms1} and V_{rms2} are the root mean square (RMS) of sinusoidal waves, and ϕ is the stage move between air conditioning voltages. Truth be told, in light of the high-recurrence power transmission, the force thickness and particularity enhance altogether. Subsequently, DAB-IBDC is considered as the center circuit of the HFL-PCSs pulling in a great deal consideration. Beside these essential qualities, the studies on DAB-IBDC likewise concentrate on transmission power portrayal, dead band impact, and element model.

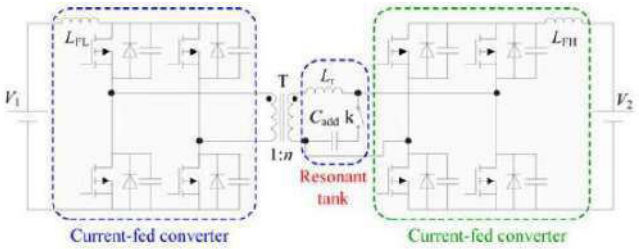
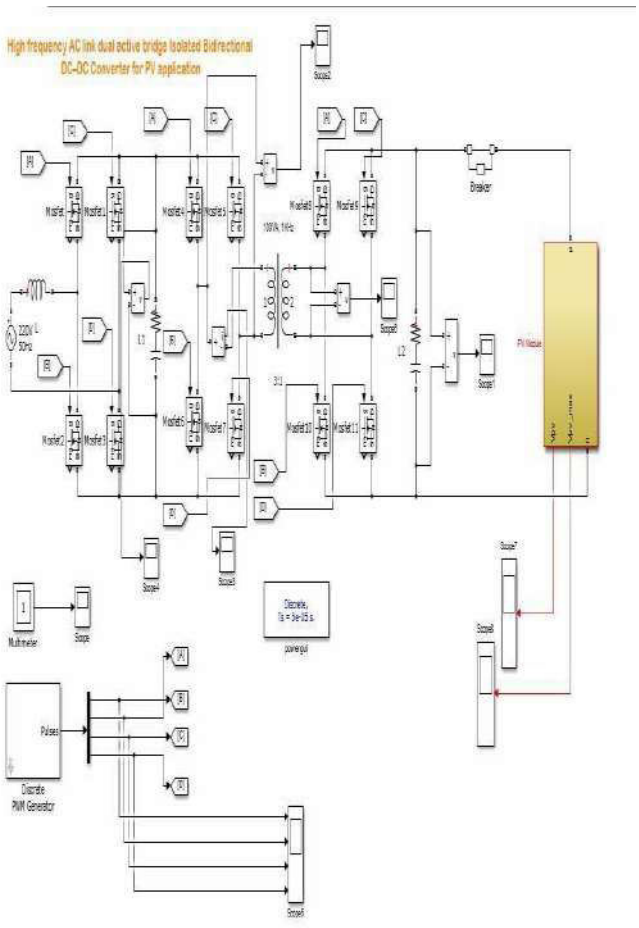


Fig 5.Resonant DAB-IBDC

VI. SIMULATION RESULTS

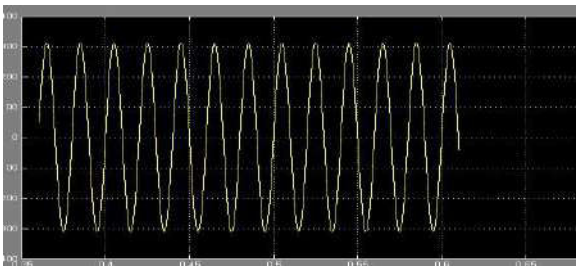
Simulation is performed using MATLAB/SIMULINK software. Simulink library files include inbuilt models of many electrical and electronics components and devices such as diodes, MOSFETS, capacitors, inductors, motors, power supplies and so on. The circuit components are connected as per design without error, parameters of all components are configured as per requirement and simulation is performed.

SIMULATION CIRCUIT

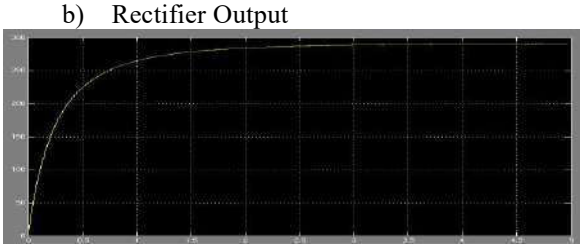


WAVEFORMS

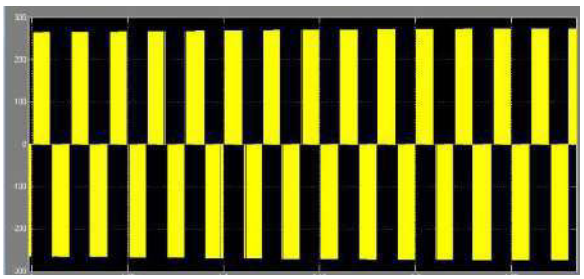
a) Input voltage



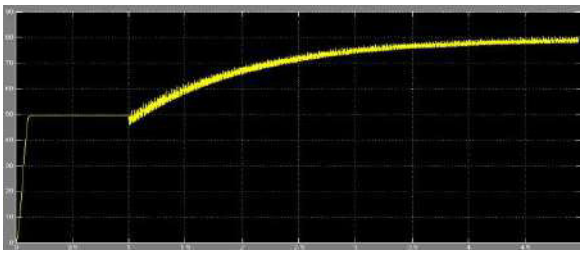
b) Rectifier Output



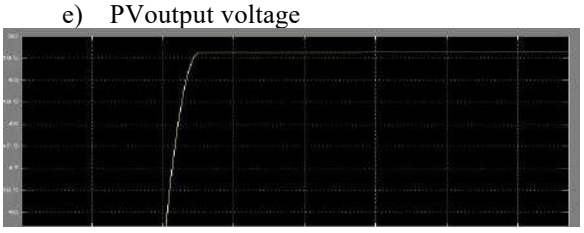
c) Inverter output



d) DC output



e) PVoutput voltage



V.CONCLUSION

In this paper a high frequency ac link converter with dual active bridge isolated is proposed for a bidirectional dc–dc power converter for PV application is proposed . Simulation study is carried out using MATLAB/SIMULINK software.

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INTEND INNOVATIVE TECHNOLOGY FOR RECOGNITION OF SEAT VACANCY IN BUS

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***Abstract*— Contemporary comes close to readily available to locate the bus area do not anticipate the seat accessibility in bus when it gets to the boarding factor. In the active globe, waiting on a public transportation without recognition of either seat schedule. An individual waiting on bus needs to know the present seats accessibility of the following readily available bus as well as the offered ability to take a trip. It is worthless to await a bus without expertise of existing readily available capability of bus. The suggested system will certainly give the offered seats when it gets to the individual's terminal. This system could inspire travelers to take a trip in bus instead of investing for cars or taxis. By making use of WIFI component for information interaction objective. That information, openings information will be upgraded. This android system would certainly aid the guests to have a sufficient traveling by capturing the best bus at the correct time with much less initiative..**

Keywords—Face detection, Haar-like features, Morphological image processing, Contrast limited adaptive histogram equalization

I. INTRODUCTION

By comprehending the future extent of modern technologies offered today we will certainly have a numerous kinds of application and also enhancement of bus stand tracking and also control. Previous deal with bus radar there is an as well substantial. Yet could ‟ To do numerous applications at the very same time in previous job. In bus stand tracking as well as control carries out complete bus stand task on basis of 2 components „ In bus component ‟ as well as „ bus stand component ‟. Supply accessibility to live info pertaining to bus timetables, Expected Time of Arrival (ETA), Estimated Time of Departure (ETD), and so on, with Display at Bus stands, Self-service Short Messaging Service (SMS) along with the Internet. Showing uninhabited seats and also uninhabited systems for buses in bus stops. Counting of the individuals existing in the bus in bus side as well as counting the uninhabited placements of the system on system side.

Nowadays, most people use public vehicle instead of personal car due to the rising of fuel price and traffic jams. Public company has been developing the system for displaying the position of the passenger vehicle for convenience of customers. However, those systems only indicate the position of the vehicle but not show the availability of seats in the vehicle. Customers will waste a time for waiting the next passenger vehicle and cannot manage the time travel or activities correctly. If customers know both of the position of the passenger vehicle and vacancy of seats, customers can use the time to other activities before the passenger vehicle arrives. Customers can plan their travel better.

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In this research, the seat vacancy identification system is designed by using image processing technique. Webcam is connected with Raspberry Pi 2 in the electric vehicle for detecting the object on vehicle and sending the data to the server via 3G communication.This system use Open Source Computer Vision (OpenCV) to analyze and process the data then calculated the vacancy of the electric vehicle by using the maximum face detection data.

II. LITERATURE REVIEW AND RELATED THEORY

“Real-Time Integrated CCTV using Face and Pedestrian Detection Image Processing Algorithm for Automatic Traffic Light Transitions”, this research deals with the traffic light for pedestrian who wants to cross the road. If the pedestrian cross the road they press the button and wait for traffic light. This system use CCTV instead the button and use image processing for detecting the face of pedestrian. If CCTV detects the face of pedestrian, the system will set the red light to show for 45 second. On the other hand if CCTV does not detect the face, the red light will show for only 30 second. [1] “To Analyze the Impact of Image Scaling Algorithms on Viola – Jones Face Detection Framework”, this research deals with the Viola – Jones algorithm about the problem from low quality of the image and find the optimum solution from Viola – Jones algorithm. The system uses two methods to scaled image that are window scaling and image scaling. The image scaling has 5 techniques that is Nearest Neighbor, Bi-Linear, Bi-Cubic, Extended Linear, and Piece-Wise Extended Linear. The system uses 5 difference face database for analyzing the performance of 5 different image scaling techniques. The system was developed by using C++, Visual studio 2010, and Open Source Computer Vision (OpenCV). They used confusion matrix that compose of True Positive, False Positive, and False Negative to compute the performance of each technique. From the result, they found that the analysis in format of the window scaling is better than image scaling. [2] “FACE DETECTION USING COMBINATION OF SKIN COLOR PIXEL DETECTION AND VIOLA-JONES FACE DETECTOR”, this research studies the detection of the human skin. It uses a combination of two techniques that are a novel hybrid color models and Viola – Jones algorithms. Its purpose is to identify the object is human or not. The system is designed in MATLAB and use ECU face and skin database to evaluate the accuracy. From the results, this method has high performance more than the other. When use this method with Viola – Jones face detector, it will be more efficient. [3]

A. Haar-like features

Haar-like features are a popular technique for detecting the face of human in the present. They are a method that has fast processing and more accuracy. The method is proposed by Paul Viola and Michael Jones in 2001. [4] Algorithms of Haar-like features are separating the image from input image to the sub window and scanning for detecting the face. They use integral image technique for finding the summation of the pixel inside the image, and then use the detector that can change the size and the position for finding the difference of white and black areas. When finish from integral image process, the next step is calling Adaptive Boosting or AdaBoost. This process is the data classification by increasing weight to the classification of a face until the best face detected. Determine is classification by i = {0, 1, 2, 3,…, n}, the process starts from . The classification of may be less accuracy. If finish from the process of , AdaBoost will increase accuracy of the classification and create the new classification that is . This process will do continuously until the final classification ——————————— and end the process. The last step is Cascaded Classifier. This step separates the image to sub-window and check the sub-window for finding the face. If a sub-window is not a face, it will reject the sub-window. If the sub-window has a chance of having human face, it will go to the next classifier that increases the weight of classifier. This step will find the face from the sub-window until get the best of face detected.

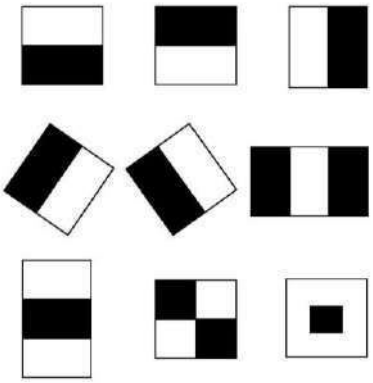


Figure 1: Type of Haar-like features

B. Contrast limited adaptive histogram equalization or CLAHE

Contrast limited adaptive histogram equalization or CLAHE is the process for increasing the image quality. This process is developed from adaptive histogram equalization. This method considers the data of histogram equalization in each of pixel of gray scale format. In the first step, this method finds average histogram value of the image. The method uses the histogram value that has higher than the average value to share to all pixels inside the image for equal histogram value. [5]

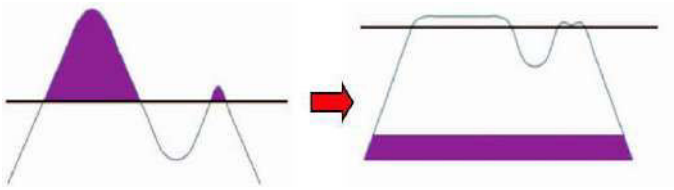


Figure 2: Contrast limited adaptive histogram equalization method

(A) (B)

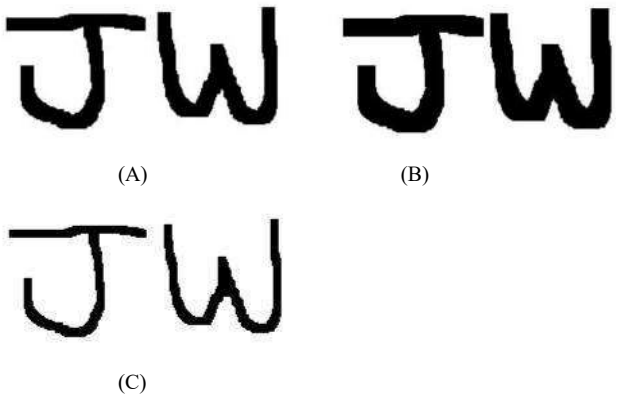
Figure 3: (A) Original image (B) The image from CLAHE process

C. Morphological process

Morphological process is the process for changing shape or structure of the image. The process use matrix data that comprise the binary values 0 and 1 for calculation. It is called structuring element. Morphological process has 2 methods that are dilation and erosion.

Dilation is a technique for adding the edge pixel of object. This technique creates the structuring element (set B), then use structuring element to scan the data of image (set A). When the data of image (set A) has some binary data on the image matching with structuring element (set B), the binary data of the image will change by using $A \oplus B = \{x \mid (B)_x \cap A \neq \emptyset\}$.

Erosion is a technique that is different from dilation technique. It reduces the edge pixel of object by using structuring element (set B) to scan the data of image (set A) same dilation technique. When the data of image (set A) has some binary data on the image matching with structuring element (set B), the binary data of the image will change by using $A \ominus B = \{x \mid (B)_x \subseteq A\}$. [6][7]



(A) (B)

(C)

Figure 4: (A) Original image (B) Dilation method (C) Erosion method

III. METHODOLOGY

The devices that include webcam, Raspberry Pi 2 model B, and 3G module are installed in electric vehicle at the top-front of the electric vehicle. When the electric vehicle leaves from the station, the system will capture the image in the passenger seat area (1 image per 1 second) and send to the server by using 3G communication. The server processes the images that receive from Raspberry Pi in electric vehicle by using Open Source Computer Vision (OpenCV).

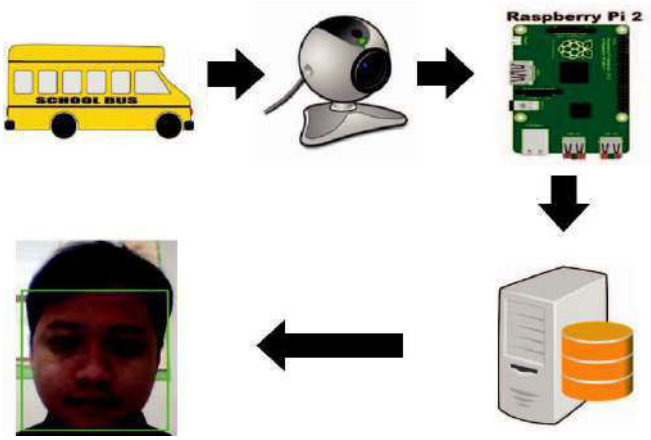


Figure 5: Overview of overall system

The system is divided into two parts. The first part is hardware. It installed and worked on the vehicle. The second part is program on the server. It is used for process the data from hardware. The system work is shown in figure 6.

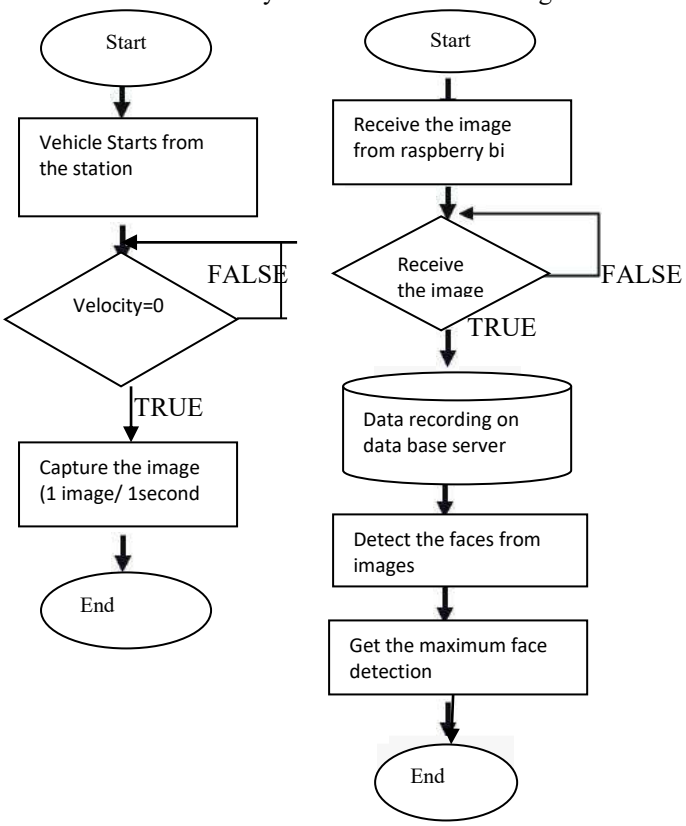


Figure 6: Program flowchart of the system in the vehicle and server

The program has processes to reduce the image noise. It uses method from Open Source Computer Vision (OpenCV). It is shown in figure 7.

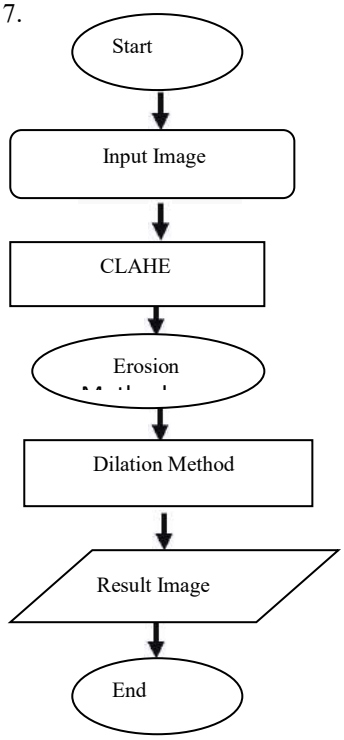


Figure 7: Reducing noise method flowchart

The program use contrast limited adaptive histogram equalization or CLAHE method. This step will adjust the histogram of the image for the appropriate value and change to grayscale format.

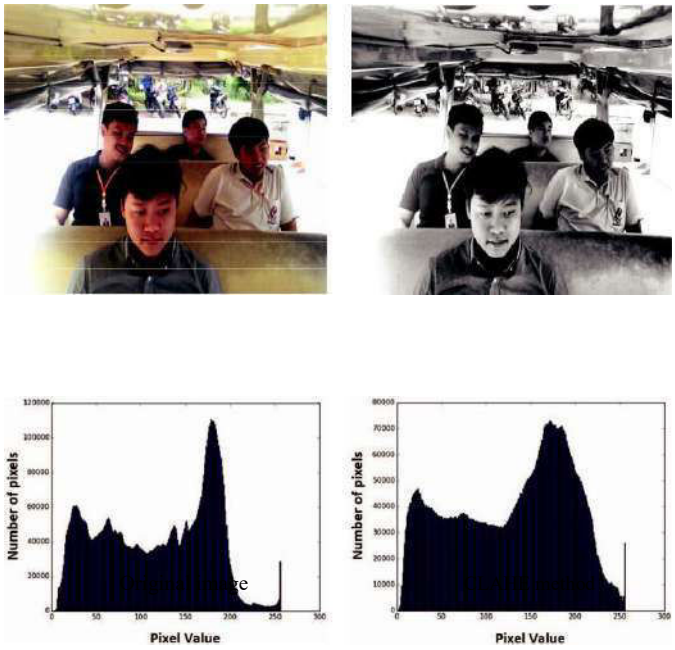


Figure 8: The comparison histogram of original image and the image from CLAHE method

When the system finishes adjusting histogram then the image noise will be reduce by using the morphological process. The image noise is processed by using the erosion method for removing unwanted pixel. Then, the dilation method applies after the erosion method to increase the edge pixel of the image. The result of the face in the image is clearer when compare with the original image (figure 9).

Figure 9: The comparison of original image and the final image result

In the last process, the system will use Haar-like feature algorithm for finding the passengers faces. The system will detect only the face of human by using the face shape. In each image, the result of passengers face detection is not equal. When the process finish, the system will give only the maximum number of the passenger face from all of the images. Finally, the system will use the maximum number of the face detection to subtract with the number of the electric vehicle seat and show the remaining seat of the electric vehicle.

Figure 10: Example of face detection

A. Result

The experiment use different number of passengers and experimental time. Three experiments are conducted. The passengers in electric vehicle are not equal in each round. In each experiment uses different number of images to evaluate the accuracy of face detection in electric vehicle. The result of experiment is shown in table I.

TABLE I.

The number of images	**Round 1**		**Round 2**		**Round 3**		**Accuracy (Percent)**
5	6	4	7	4	8	5	57.33
40	6	5	7	6	8	7	74.00
100	6	5	7	6	8	6	79.19
150	6	5	7	6	8	7	78.96
200	6	5	7	4	8	4	90.65
240	6	5	7	8	8	8	90.66
280	6	5	7	8	8	4	90.69

* : Number of passengers; Number of passengers detected by face detection technique.

From the result, the number of images has an effect for face detection. If we use fewer images, the program will be low performance and accuracy. The program cannot detect the face because the face of passengers is not clear. This problem consists from environment around the vehicle. It makes the images too light or dark. If the number of image is increases (long capturing time), the movement of passenger face is increase as well. The program can detect the face of the passenger better because the program has a more chance to detect the passengers face from many images.

IV. Conclusion

Vehicle Seat Vacancy Identification using Image Processing Technique was designed and tested. Webcam and Raspberry Pi were installed in electric vehicle. When the vehicle starts from the station, webcam captured the images and send to the server by using Raspberry Pi and 3G communications. The images were sent completely. From experimental result (Table I), the number of images have a direct impact to the face detection result. If the number of images increases, the accuracy of face detection is increase as well. Because the system will has more chance to detect the passengers face from many images. The noises in images occur from environment inside and outside the vehicle such as the light and face blur. The system improve quality of images by using contrast limited adaptive histogram equalization and morphological process. The system can work well at 200 – 300 images data. It gives 91.67 % accuracy.

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Reversible Adder/Subtractor Circuits: A Study

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***Abstract*— The Reversible logic is a unconventional form of computing where the computational process is reversible. The study of this technology is to implement reversible computing where they offer what is predicted to be the only potential way to improve the energy efficiency of computers beyond von Neumann- Lindauer limit. This is new and emerging area in the field of computing that taught us to think physically about computation. Quantum Computing will bring a total change in how the computer will operate and function. The reversible arithmetic circuits are efficient in terms of number of reversible gates, garbage output and quantum cost. Study of Reversible Binary Adder Subtractor- Mux, Adder- Subtracter - TR Gate., Adder-Subtractor- Hybrid is studied in this paper. In all the three design approaches, the Adder and Subtractor are realized in a single unit as compared to only full adder/subtractor in the existing design.**

***Index Terms*— Reversible gates, Fredkin gate, Feynman gate, Toffoli Gate, Peres gate**

I. INTRODUCTION

REVERSIBLE logic is generally used in Nanotechnology, quantum computing, Low power CMOS, Optical computing and DNA computing, etc. Quantum computation generally uses reversible logic. Basically, reversible gates are used to perform reversible computations [1-4]. These circuits do not lose information and reversible computation in a system that can be performed only when system comprises of reversible gates. The gates that are used in digital design are not reversible (i.e) AND, OR and EXOR gates does not perform reversible operation.

A reversible gate can generate a unique output from each input vector, and vice versa, hence one to one mapping between the input and output vectors are obtained. Among all the gates only the NOT gate is reversible. Loss of energy is important criteria in digital design. The energy dissipation is related to non ideality of switches and materials. Two reversible gates are generally used to design a reversible circuit. Reversible gates acts as building blocks for reversible circuits [5-7].

The following are the characteristics of Reversible gates.

- A reversible gate has input and output with a one to one correspondence. i.e. the inputs of a reversible gate is uniquely determined from there outputs.
- The number of inputs and outputs should be equal in reversible logic gate.
- The fan out of every signal including primary inputs in a reversible gate must be one.

In design of reversible logic circuit, the Classical logic synthesis methods cannot be applied directly.

II. REVERSIBLE GATES

Reversible logic types:

- The basic reversible gate is NOT gate and is a 1x1 gate, Controlled NOT (CNOT) gate is a 2x2 gate.
- Fredkin gate, Toffoli gate, Peres gate and TR gate are all 3x3 reversible gates.
- Each reversible gate has a cost associated with it called quantum cost. The quantum cost of 1x1 reversible gates is '0', and quantum cost of 2x2 reversible gates is '1'.
- Reversible gates is identified by using 1x1 NOT gates and 2x2 reversible gates, i.e. V and V+ [where V is square root of NOT gate and V+ is its Hermitian] and Feynman gate (CNOT gate).

The property of V and V+ gate is :
V x V = NOT
V x V^+ = V^+ x V = I
V^+ x V^+ = NOT

The quantum cost of a reversible gate is calculated by counting the number V, V+ and CNOT gates used in implementing it except in some cases.

A. *NOT Gate*

Among all the conventional logic gates, **Not gate** is the only reversible gate (1x1 gate). The quantum cost of NOT GATE is zero.

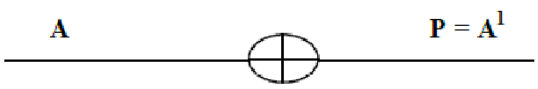

Fig.1 NOT gate

B. *Feynman Gate (CNOT gate):*

This is a 2x2 gate having mapping (A, B) to (P=A, Q=A B) where A, B are inputs and P, Q are outputs respectively. Feynman gate can be used as a copying gate. Since a fan-out is

not allowed in reversible logic, this gate is useful for duplication of the required outputs.

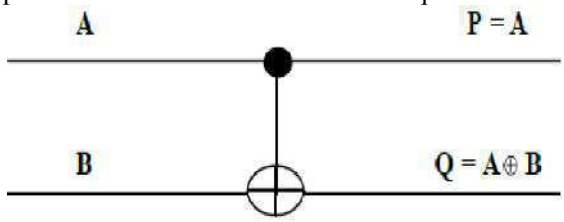

Fig. 2 Feynman or CNOT gate

C. *Toffoli Gate:*

This is a 3x3 reversible gate with two of its outputs are same as inputs with the mapping (A, B, C) to (P=A, Q=B, R= A.B C). Where A, B, C are inputs and P, Q, R outputs respectively. Toffoli gate is most popular reversible gates and has quantum cost of 5. It requires 2V gates, 1 V+ gate and 2 CNOT gates.

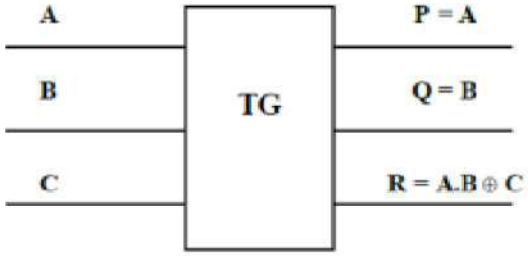

Fig. 3 Toffoli gate

D. *Peres Gate:*

Peres gate is a three input and three output (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q= A B, R= (A.B) C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Peres gate has the quantum cost of 4, since it requires 2 V+ gate, 1 V gate and 1 CNOT gate. Among 3x3 reversible gates, this has the minimum quantnum cost

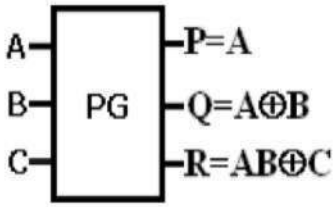

Fig. 4 Peres Gate

E. *Fredkin Gate:*

Fredkin gate is a 3x3 conservative reversible gate. It maps (A, B, C) to (P=A, Q= A' B+AC, R=AB+ A'C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Fredkin gate can be implemented with a quantum cost of 5 and it requires 2 dotted rectangles, 1 V gate and 2 CNOT gates.

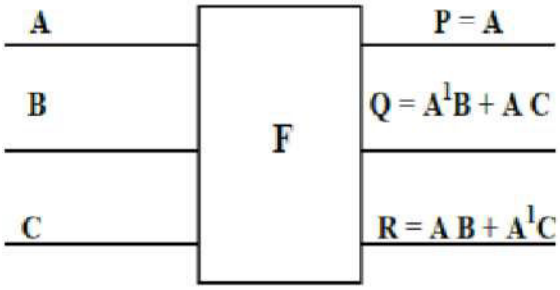

Fig. 5 Fredkin Gate

F. *TR Gate:*

TR gate has 3 inputs and 3 outputs having inputs and outputs mapping as (P = A, Q=A B, R= (A . B') C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. TR gate may also be realized in a different implementation with quantum cost of 6 or lesser than 6. Therefore it is considered that the quantum of TR gate as 6 for the calculation of parallel Subtractor implementing by reversible gate.

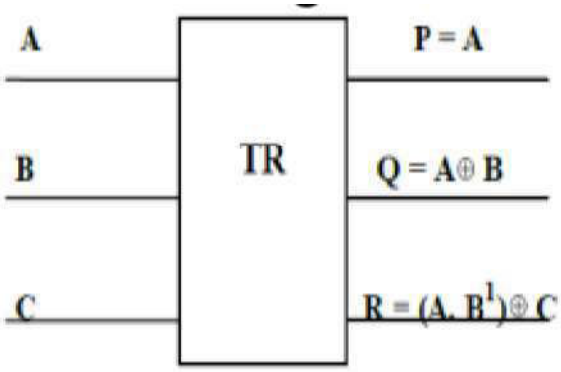

Fig. 6 TR Gate

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Any machine, which can build up arbitrary combinations of logic gates from a universal set is then a universal computer [8-12]. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. Parameters for determining the complexity and performance of circuits.

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic

circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.

- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.
- A 3-input and 3-output reversible logic gate was proposed in. It has inputs a, b, c and outputs x, y and z as shown.
- The truth table of the gate is shown in the Table. It can be verified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined. The gate can be used to invert a signal and also to duplicate a signal.
- The signal duplication function can be obtained by setting input b to 0. The EX-OR function is available at the output x of the gate.
- The AND function is obtained by connecting the input c to 0, the output is obtained at the terminal z. An OR gate is realized by connecting two new reversible gates.
-

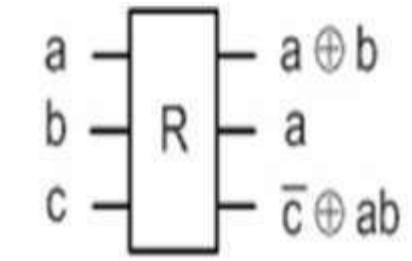

Fig. 7 Reversible gate R

Table: 1 Truth Table for Gate R

a	b	c	x	y	z
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	1	0	1	1

III. REVERSIBLE ADDER/SUBTRACTOR

A. Adder circuits:

Several types of adders are used in computing systems [13]. A ripple carry adder has the simplest structure compared to any another. In a ripple carry adder, full adders connected in series generate the sum and the carry outputs based on the addend bits and the carry input. The disadvantage of a ripple carry adder is that the carry has to propagate through all stages.

B. Ripple carry adders:

Building block of a ripple carry adder is a full adder block [14]. A full adder computes the sum bit Si and the carry output c i+1 based on addend inputs a and b and carry input c.

The output expressions for a ripple carry adder are

(i) Si = a xor b xor c;

(ii) Ci+1 = ab + bc + ca; (i = 0,1, 2,)

A Reversible gate can generate unique output vector from each input vector, and vice versa. Hence the number of outputs in a reversible circuit has the same number of inputs, and commonly use NOT gate as it is the only reversible gate. One of the most important features of a Reversible gate is its garbage output i.e. The input of the gate which is not used with other gate is called garbage output.

A four-bit parallel adder/subtractor is built using the full adder/subtractor and half adder/subtractor units.

Table 2: Truth Table For Full Adder/Subtractor

CTRL	A	B	C	Carry/ Barrow	Sum / Difference
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	1

Half Adder sub:

Subtractor Reversible half adder/subtractor logic is implemented with the four reversible gates i.e. two are Feynman gates and 2 are fredkin gate. Here there are 3 garbage values. Inputs of garbage are '2' and the quantum cost is '12'.. This half adder/subtractor is basically used in implementing four-bit parallel reversible adder/subtractor unit.

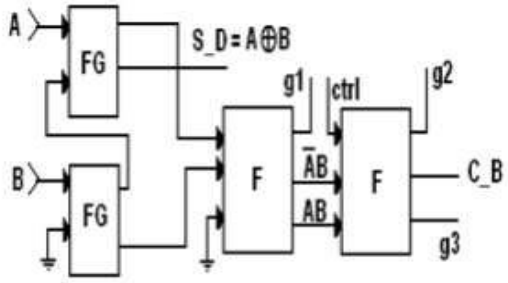

Fig. 8 Implementing reversible Half Adder/ Subtractor.

Table 3: Truth Table For Half Adder/Subtractor

CTRL	A	B	Carry/ Barrow	Sum / Difference
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	0	0
1	0	0	0	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

Full Adder-Subtractor-Mux :

This design is mainly based on the usage of reversible gates for each function i.e. Peres gate for adder function, TR gate for subtractor function and Fredkin gate for multiplexing the Carry and Borrow line into single line output. For creating signal multiplication of each signal 3 Feynman gates are used . For this kind of design 8 reversible gates, 3 Feynman gates, 2 Peres gates, 2 TR gates and one Fredkin gate are used. The table shows that among 7 garbage outputs 5 garbage (constant) inputs and the total quantum cost is 28.

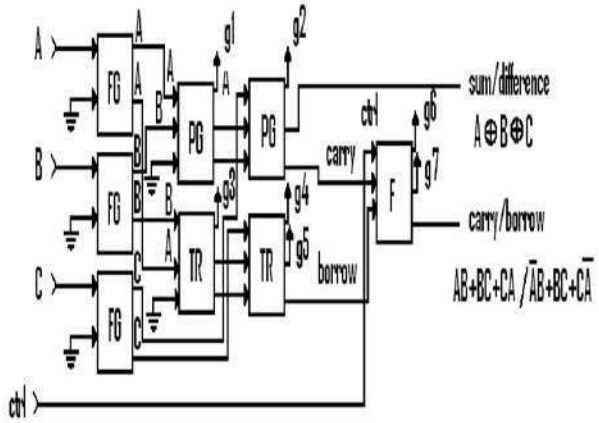

Fig. 9 Implementing reversible full Adder/Subtractor

- This is implemented by using VHDL code and simulated by using Modelism simulator.
- The functionality of individual gates is implemented using Behavioural style of modelling and the overall logic is implemented using structural style of modeling.

Full Adder-Subtractor-TR gate:

The main function of addition and substraction is realized by using TR gates.. The design includes 3 TR gates and 6 Feynman gates. Feynman gates are used for input signal buffering. The garbage output in this design is 7 and the garbage inputs are 5. The quantum cost is 24. If one additional Feynman gate (C-NOT Gate) is used in this design, a quantum cost advantage of 4 is obtained. This quantum cost advantage is mainly due to the realization of arithmetic blocks of adder and subtractor is realized with 3 TR gates as against the 5 numbers of 3x3 reversible gates for Adder-Subtractor- Mux design.

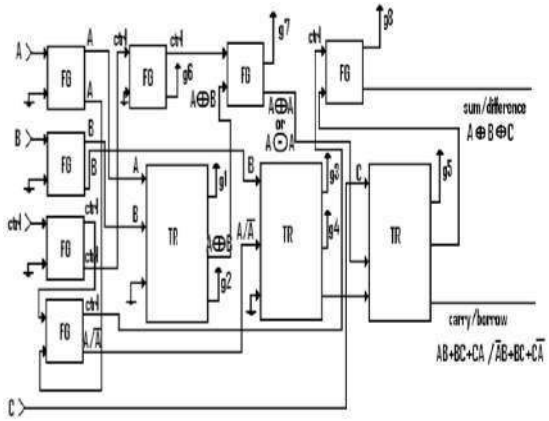

Fig. 10 Implementing reversible Full Adder-Subtractor-TR gate

- This is implemented by VHDL code and simulated using Modelsim simulator.
- The individual gates functions are implemented by using Behavioral style of modeling .

Full Adder-Subtractor- Hybrid:

It is an optimized implementation of adder-substractor function. In this case two Feynman gates are used to realize sum/difference output.. Two Fredkin gates and a TR gate are used to realize carry borrow line. This design utilizes 8 gates including the C-NOT gates for input signal multiplication. The garbage output is 5 and garbage input in this design is 3. The quantum cost is 21. By optimal utilization of gates the optimization of the garbage input, garbage output and quantum cost in this case is obtained. By two CNOT gates, the sum/difference function in this case is realized. Hence it is essential to have a design approach where, the required functionality may be realized with simplest gates as much as possible.

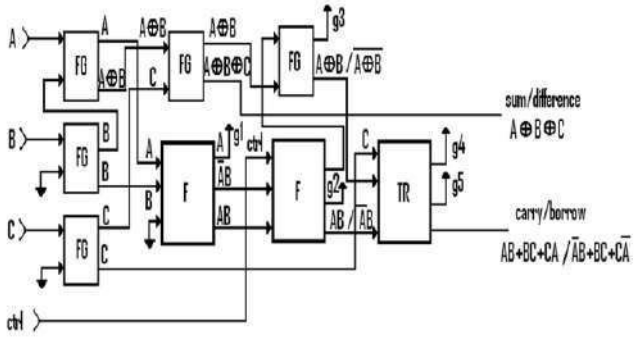

Fig. 11: Implementing reversible Full Adder-Subtractor-Hybrid

IV. CONCLUSION

The Reversible logic is breakthrough for energy efficiency of computers beyond von Neumann- Lindauer limit. The study performed in this paper detailed about Reversible Binary Adder Subtractor- Mux, Adder- Subtracter - TR Gate., Adder-Subtractor- Hybrid. In all the three design approaches, the Adder and Subtractor has been realized in a single unit as compared to only full adder/subtractor in the existing design.

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Secure IoT Platform for Industrial Control Systems

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ABSTRACT:

Calamity preparation as well as reaction calls for facility and also even more clinical evaluation. The stages of the discovery as well as rescue procedure require a very reliable administration system, which could anticipate the calamity, stop, prepare, as well as cause prompt clinical reaction, support, and also recovery. The calamity that triggers extreme losses in human lives and also linked items due to a big quantity of warmth created is called as a thermal calamity. In instance of a melt calamity, a recognized thermal representative acts upon living beings triggering a variety of injuries as well as fatality. The warm dissipation is normally on a huge range. The task concentrates on the manufactured catastrophes like leak of gas or the most awful instance of a fire. Poisonous and also ignitable gases are extensively utilized in market, furnace, residence devices and also Lorries. This consists of flammable gases like gas, ethane, butane, methane, and ethylene and so on. Liquefied Petroleum Gas (LPG), likewise described as gas or butane are typically kept in pressurized cylindrical tubes in fluid kind and also they evaporate at typical temperature levels. A leak could fire up as well as trigger a surge.

Keywords : Internet of things, Industrial control system, Supervisory control and data acquisition, Programmable logical controller, remote terminal units, and Advance encryption standard Introduction

1.INTRODUCTION: Industrial control system (ICS) is an important term, which has been set for monitoring and controlling of industrial infrastructures such as Oil, Gas, Manufacturing, Electricity and Transportation, and others, mainly combined with the most prominent control systems, such as the "supervisory control and data a

aacquisition (SCADA) systems and distributed control systems (DCS), and also used in several inndustrial sectors of current years. ICS mainly deployed in the industries to control the overall structure of production plant, or other employed equipment's, to produce the desired production goals a according to specifications and requirements, through employing of several control components, varies according to industries specifications and performance of model, that combine together for producing of output. The ICS have been designed and networked to providing the controlling functions that are may fully automated in controlling of the overall structure of sectors, such a transportation controlling and other areas like oil industry, or these controlling systems are self-control by individual or human in case of manual operational mode[1-4]. Industrial control system uses several control components and required network (or system) configurations and setting of sensors, actuators and programmable logic controllers (PLCs), also including system controlling loops, diagnostics and maintenance equipment, graphical interfaces or human machine interface (HMI) and proprietary and non-proprietary protocols such as DNP3, TCP/IP , UDP and others. ICS deployed system is usually controlled by one or more controllers (or control loops), however, overall system information is manipulated bases on the system specified set points between various networked equipment or sensors, with the usage of proprietary or/and non-proprietary protocols and functional control algorithm that controls these set points[1, 2].

IoT and SCADA System

Internet of things (IoT), is another advance technology in IT sector, provides internetworking for numerous of devices such as sensors,

actuators, PLCs and other electronic embedded smart devices and controls, and various software's' and provides systems network configuration and connectivity, which enables communication between these numerous devices for information exchanging [5-7]. Nowadays, IoT is one of the most advanced, efficient, and cost less technological solution which encompasses various hardware and software resources; and allows remotely connected sensing devices to sense with more capabilities, provides efficiency and can be monitored and controlled through deployed of existing systems or infrastructures, resulting the physical World integration with computer controllers (or systems).

As IoT provides interconnectivity among various real-time sensing sensors and PLC and other intelligent devices, therefore this technology will be an entity indicated for the more advance cyber-systems encircling the significant developments, "such as smart grid, smart vehicle systems, smart medical systems, smart cities, and others smart systems." In early future, IoT has striven to provide advance or smart connectivity for variety of electronic and intelligent equipment's or devices, IT-based systems and the more advanced services through deploying of various traditional and real-time protocols, networks domains, and system software/hardware applications, which will be an work followed by machine-to-machine technological concept. Through interconnection of various devices and managing ofapplications for remotely monitoring and controller, the IoT becomes a tremendous development in the arena of industrial control systems (ICSs), or for real-time industrial infrastructures, including SCADA systems [7]. Figure 1 shows the typical IoT applications platform for SCADA system.

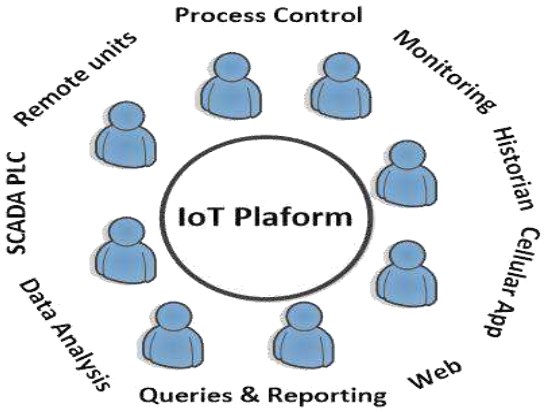


Fig. 1. IoT platform

2. SYSTEM SETUP AND IMPLEMENTATION:

Nowadays, industrial systems and their automation are accessible and control through deploying of the IP-centric network, thus the information will be collected from anywhere, where the remote industrial stations are setup having various electronic devices, such as terminals units, PLCs, and intelligent sensors [14]. To design and model an Internet of thing based generic industrial control system, or IoT-SCADA system, few common parameters have to be considered:

- Efficient and smart network selection,
- Protocol selections for reliable communication,
- Efficient and scaled software's selection for information collection, monitoring, and control,

- Generic security mechanism for information protection,
- Smart network intrusion detection solution,
- Information analytics and performance monitoring,
- and Historian, respectively.

To fulfill the target goals of the study, IoT_SCADA system is setup where numerous of devices are connected with each other through secure channels. In the IoT_SCADA system is modeled and setup, which encompassed six main functional parts, such SCADA main controller or control center with human machine interface, remote station, historian, reporting and maintains, data analytics, and user devices, connected through the internet of things (IoT) platform over the Internet.

As mentioned, SCADA system is also connected to the Internet. As mentioned, the IoT is a critical component for the industrial control systems (ICSs), or smart industrial manufacturing. The industries, such as oil, electric, water/waste water, and gas, have been achieving their productions through deploying of sensors and controlling from the computerized controller [14,15]. As most of industrial based systems, employing sensors, actuator, PLCs, and other controlling and monitoring facilities, were limited and not connected to the Internet. In SCADA system, typically, the hierarchical structure of the system is defined in advance. Therefore the overall system scope is limited as a part of industry uses, and disconnected with the advance and open IP networks that provide extensive connectivity with other network systems, over the Internet access.

3. HARDWARE COMPONENTSOF THE SYSTEM :

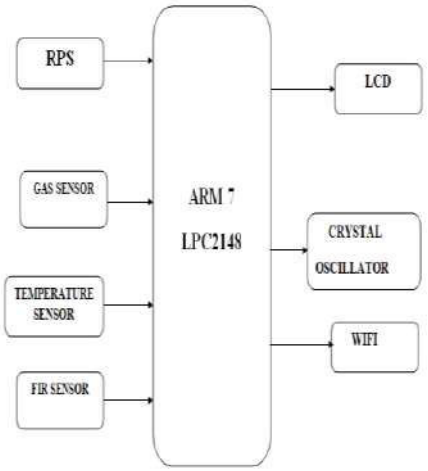


FIG.2: BLOCK DIAGRAM OF HARDWARE SYSTEM

3(A) . GAS SENSOR:

Gas sensors need to be calibrated and periodically checked to ensure sensor accuracy and system integrity. It is important to install stationary sensors in locations where the calibration can be performed easily. The intervals between calibrations can be different from sensor to sensor. Generally, the manufacturer of the sensor will recommend a time interval between calibrations. Calibration here is simply a safety check, unlike laboratory analyzers that require a high degree of accuracy. Calibration of the gas sensor involves two steps. First the “zero” must be set and then the “span” must be calibrated. Sensor resistance will drop very quickly when exposed to gas, and when removed from gas its resistance will recover to its original value after a short time. The speed of

response and reversibility will vary according to the model of sensor and the gas involved.

3(B) . TEMPERATURE SENSOR:

The Temperature Sensor LM35 sensor series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature.

LM35 Sensor Specification:

The LM35 series are precision integrated-circuit LM35 temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 sensor thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 sensor does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full -55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies.

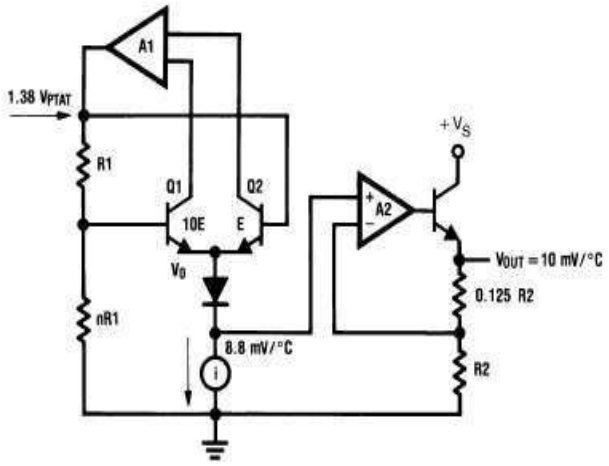


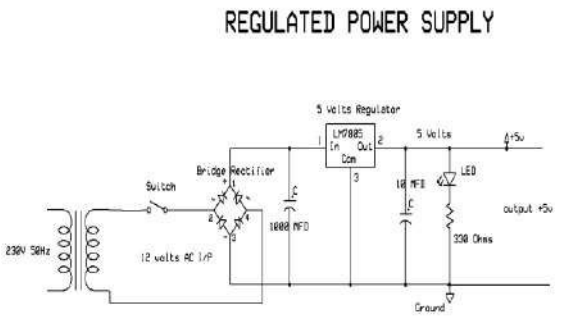
FIG.3:LM35 Sensor Circuit Schematic

3(C) . WIFI MODULE:

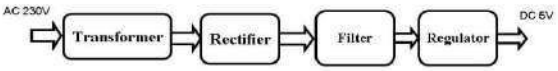
The NETGEAR R6300 WiFi Router delivers next generation WiFi at gigabit speeds. It offers the ultimate mobility for WiFi devices with speeds up to 3x faster than 802.11n. Compatible with next generation WiFi devices, and backward compatible with 802.11 a/b/g and n devices, it enables HD streaming throughout your home. The R6300 with simultaneous dual band WiFi technology offers speeds up to 4501 to 13002 Mbps and avoids interference, ensuring top WiFi speeds and reliable connections. This makes it ideal for larger homes with multiple devices. In addition, four gigabit Ethernet ports offer ultra-fast wired connections. Wirelessly access and share a USB hard drive and USB printer using the two USB 2.0 ports.

3(C).REGULATED POWER SUPPLY:

Power supply is a supply of electrical power. A device or system that supplies electrical or other types of energy to an output load or group of loads is called a power supply unit or PSU.



Regulated Power supply



4.RESULT S:

Protection is main issue for each one. This Project explains a layout of efficient protection security system that could keep an eye on a market with various sensing units. Unapproved gain access to, Temperature increment, IR discovery could be kept track of by the standing of each private sensing unit. Undoubtedly, this alarm system additionally has an input to 'equip' the alarm system, a meddle input as well as a few outcomes to regulate an alarm and also Auto dialing system. The alarm system is likewise fitted with a supposed 'panic switch'. The alarm system is developed around the 8051 mini controller from Atmel. This mini controller gives all the performance of the alarm system. It additionally cares for filtering system of the signals at the inputs. Just after an input has actually stayed the same for 30 nanoseconds, is this brand-new signal degree handed down for handling by the mini controller program. This moment could be differed by embracing little adjustments in the resource code. An optimum of 5 sensing units could be attached to the warning device. These sensing units have to have their get in touches with shut when in the non-active state (i.e. Normally Closed). Additionally, each sensing unit has to have its meddle link wired also. A power supply voltage of +5 VDC is offered for every sensing unit at the matching electrical wiring terminals. The originality of this task is not just signaling the next-door neighbors by alarm, it likewise dials a mobile number which is currently set right into the system. A mobile number or a land line number could be configured right into the system. As this system works with existing telephone line, it could call the number also the customer runs out terminal.

Fig.5 : Output Displayed On The Mobile

5. CONCLUSION :

When it comes to a manufactured calamity, occasionally the discovery is so late that the catastrophe has actually currently spread out commonly. The job prepares to earn a mobile robotic that would certainly have the ability to signal and also respond to emergency situation scenarios. In the current past, there have actually been numerous instances where the traditional protection systems have actually verified to be a failing. Additionally, existing systems are based upon Wi-Fi connection which is unstable in the circumstance of the calamity. The improvement remains in the kind of GSM (Global System for Mobile Communication) for interaction to ensure that the reaction is constructing independent and also calamity could not interfere with the working of the system. Better, the real-time sensing unit information will certainly be moved to the IoT web server by means of GPRS (General Packet Radio Service) connection. The setting of the car will certainly be figured out by a shade sensing unit which will certainly review the shade of the neighboring wall surface skirting.

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FPGA based Auto Correction of Hard Faults

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***Abstract*— Multi-core systems have more functional units fabricated in to a single chip and they are more vulnerable to faults. These faults have to be handled efficiently without substantial loss of overall performance. In this paper a self repairing approach for hard faults using Field Programmable Gate Array (FPGA) is proposed. The proposed multi-core system will have a reconfigurable hardware unit and a fault look-up table included to individual cores of the multi-core system. The faulty unit details are updated in the fault look-up table as a result of fault detection phase. The faulty unit details are given as input to the decoder unit along with the usual inputs. Depending on these, the decoder unit will decide to choose either the Arithmetic and Logic Unit (without fault) or the Reconfigurable hardware unit (Faulty unit reconfiguration).**

***Index Terms*— Self Reparing, Hard faults, Field Programmable Gate Arrays, Reliability, Online Fault Repair**

I. INTRODUCTION

WITH the advancements in the VLSI technology, more and more functional units are fabricated in a single chip. With more number of circuits in the chip, the probability of occurrence of faults in the circuit is also high. The faults can be classified in to a) Transient (or soft) errors, [1] caused by environmental disturbances, b) Permanent (or hard) errors[2], caused by latent manufacturing defects as well as aging (wear out phenomena) and c) Verification inefficiencies that allow important design bugs to escape in the system.

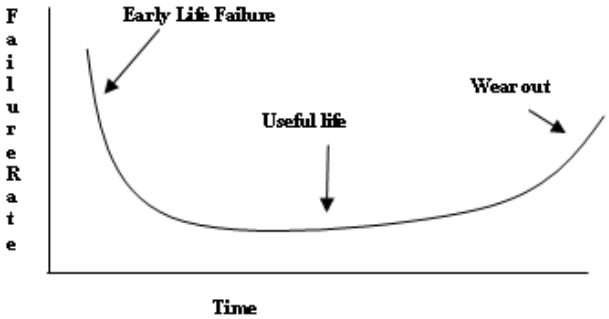

Figure 1. Product reliability [1]

Any type of fault in the system has to be taken care off, for graceful degradation of the system. The hard faults can occur during any stage of the chip's life cycle. The following figure 1 shows the trend in a chip's failure rate [3]. From the above diagram it is clear that the faults can happen at early life of the product or during its useful period or can wear out after a long time. Early life failures are also called as infant mortalities and they are the faults that escape during design verification process. Ideally, the early life failure should have a brief region in the figure 1. Even with today's advanced design verification and testing tools, early aging in multi-core processors is high because of their high transistor density [4]. For handling hardware failure during the early life or useful life, a post silicon fault repairing technique that can be done on the field is essential. Self-repairing of hardware fault is the capability of the processor to handle the hardware fault by itself. This paper proposes the idea of using FPGA for self-repairing of hardware faults in an ASIC design. The following section explains the existing post silicon self-repairing techniques.

II. PROBLEM FORMULATION

Self-repairing is an emerging field that will have a major impact on increasing the reliability of the system. The importance of failure prediction is emphasized in [5]. Circuit failure prediction in [5] predicts the occurrence of hard faults even before it surfaces on the system's state or data. This prediction is made possible by collecting information about various system parameters over time and comparing them with the fault free signatures. Other available self-testing techniques includes Built In Self-Test(BIST) for failure prediction[6], Concurrent self-test[7] for failure prediction and Genetic algorithm based BIST [8].

After a fault has been detected in the system, it has to be repaired effectively. The use of Triple Modular Redundancy (TMR) for self-repair of transient faults is described in [14]. The use of TMR also does not guarantee fault repair on all the three systems involved. For repairing faults in any of the three system involved in the TMR using FPGA is proposed in [11]. FPGA is the most suitable for self-repairing and lots of work has already been proposed to heal a FPGA. The use of an autonomous self-healing architecture proposed in [15] uses FPGA. Fault tolerant FPGA processor architecture proposed in [17] considers a FPGA architecture on which faults are handled efficiently by reconfiguration. Software based self-repair discussed in [10] uses software based micro architecture

self-configuration. Another method of Self repair using FPGA is to include a spare core [9] to the processor architecture and use the spare core for any permanent fault. Using a spare core for fault handling provides dynamic fault recovery in the field. When fault repair is done through a spare FPGA core in a multi-core environment, there is a complication of inter processor communication involved. So it will be better to have a within core mechanism to repair hard faults. This paper proposes the idea of using FPGA as a unit inside each core of the multi-core processor architecture for self-repairing of permanent fault.

III. Problem Solution

Multi-core processor can be shared or distributed. In any type of multi-core architecture, including a FPGA hardware unit inside the core will enable self-repairing of hard faults. The proposed system includes a reconfigurable hardware in every core of a multi-core system. The reconfigurable hardware will be handling the hardware faults occurring in that particular core. A self-detection technique based on software [2] can be incorporated to detect a fault before it surfaces on the system state. After the fault is detected, the FPGA is configured to perform the functionality of the unit on which fault has occurred. The permanent faults can be maintained in a table so that any future reference to that unit may be handled by the reconfigurable hardware. By providing self-repairing like this will enable reduced space and time for fault recovery. For explaining the details about the implementation of the above concepts, OpenSPARC T1 [18] architecture is considered. OpenSPARC T1 is the open source code of SPARC architecture provided by SUN Micro systems. OpenSPARC T1 architecture has 8 CPU cores, with 4 threads per core, for a total of 32 threads. The cores are connected by a cache cross bar. Each core has 132 Gbytes of level 1 instruction cache and 8 Kbytes of level 1 data cache. The execution unit of OpenSPARC T1 has an ALU, a multiplier circuit, a divider circuit and shifter circuit. There is a Execution Control Logic (ECL) that generates the necessary select signals that control the multiplexers, keeps track of the thread, and reads each instruction and implements the bypass logic. The bypass logic does the operand bypass E,M, W stages to the D stage. The ALU consists of an adder and logic operations such as ADD, SUB, AND, NAND, OR, NOR, XNOR, NOT. The ALU is also used for branch address or virtual address calculation. The method proposed in this paper for the self-repairing of hard faults on the ALU can also be extended to other units.

A. Model Proposed

The overall system of the SPARC core along with Reconfigurable Hardware Unit (RHU) and Fault Lookup Table (FLT) is shown in the following figure.1. In the figure 1, the FLT and RHU are represented using dotted boxes as in

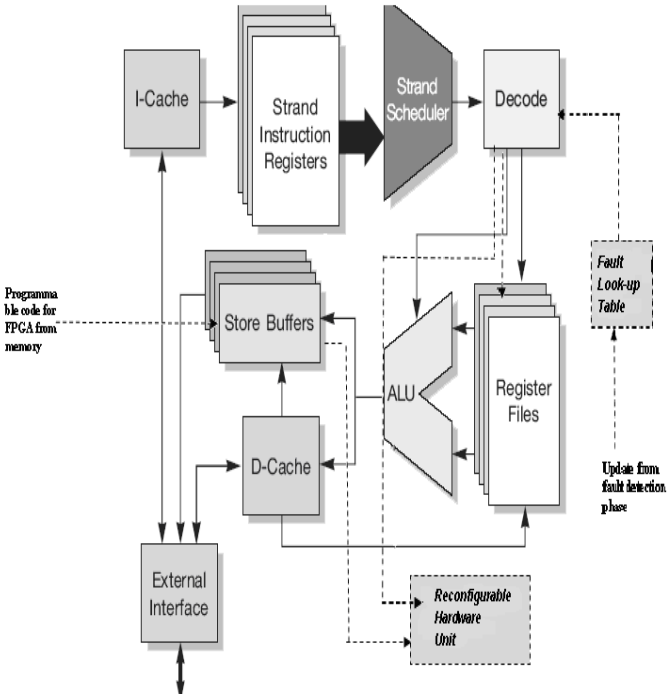

Figure 2. OpenSPARC Core with RHU and FLT

The reconfigurable hardware is a FPGA unit that will reconfigured to work as the faulty unit. The FLT will store the details of the faulty functional unit that has been obtained as a result of fault detection.

If a fault occurs in the system, the fault can be predicted by using one of the methods proposed in [6]-[8]. The faults predicted will be loaded on to the FLT. Every time the system is switched off the details of the (FLT) are updated in a secondary memory file. So when a future reference to the faulty unit occurs, the details of the faulty unit are seen by the decoder and hence the necessary functionality will be initiated on the Reconfigurable hardware. A similar proposed solution in [17] for fault recovery had complex control logic. But in this proposed method, the control logic of this test and recovery units are made much simpler. The faulty unit is captured in a table and it will be given to the decoder unit which will in-turn initiate the necessary reconfiguration.

B. Working Principle of the Proposed System

The detailed communication between the fault lookup table, the instruction decoder and the reconfigurable hardware is explained in the following figure 3. The fault lookup table is an on chip table to store the list of the permanent faults happened in the system and their diagnosis details. This will aid in the repair of the faulty circuit online. The decoder takes input from the thread selection mux which has details about the instruction to be executed and also the fault lookup table. If the instruction requires the usage of the faulty unit listed in the fault lookup table then instead of sending control signals to the faulty unit, they are sent to the reconfigurable hardware.

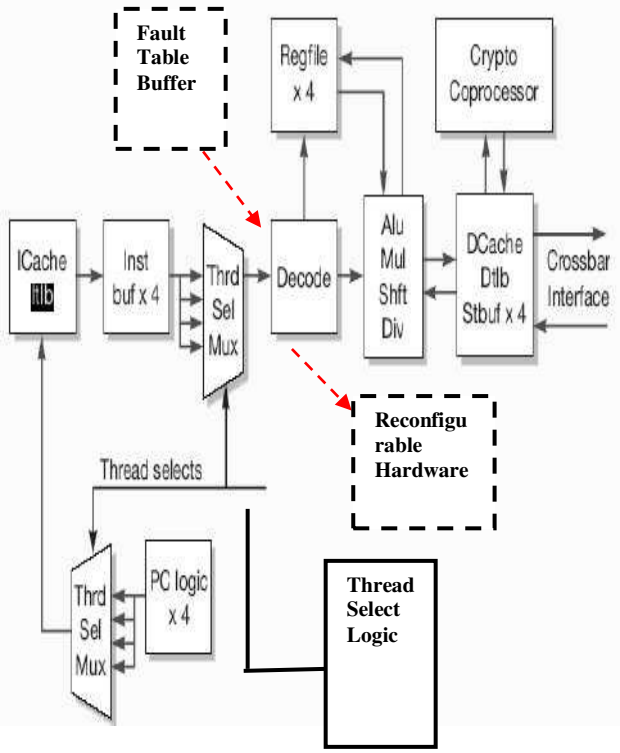

Figure 3. OpenSPARC Pipeline logic with RHU and FLT

The code for configuration of the FPGA stored off the cache is loaded on to the FPGA via the DCache buffer. The architecture proposed is a hybrid that uses FPGA to augment an ASIC design [16]. The main concern in such a design is that, ASIC's are fine-grained whereas FPGA's are medium grained or coarse-grained. However for fault repair considering coarse-grained reconfiguration will not harm the system. Because of the above reason, in the proposed system, we have used library based FPGA mapping.

The FPGA considered here consists of Programmable logic blocks and Programmable interconnects. The structure of the programmable logic block is given in the following figure 4.

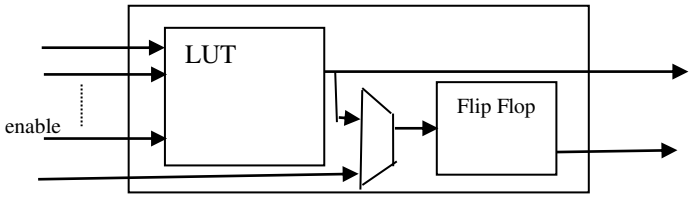

Figure 4. FPGA Cell Structure

The FPGA and the ASIC hybrid architecture can be a parallel one with ASIC processor being the master and the FPGA being the slave. The faults detected by [6][7][8] are keyed in the FLT . The FLT can also be a FPGA so that dynamically the table size can be varied. Unique identification numbers can be given for all the units under test. Look up tables are usually arrays or associative arrays often used for indexing. The indexing here points to the memory space where the program for reconfiguration for that particular unit lies.

C. Analysis

The gate counts for basic circuits are given in the following table.

Table.1 Gate Counts for common functions

Function	**Gates**
2-input NAND	1
2 to 1 mux	4
3 input XOR	6
4 input XOR	9
2 bit carry full adder	9
D flip flop	6
D flip flop with set and reset	8
D flipflop with reset and enable	12

By using hashing function for the look up table, the searching for a particular unit in the table will be O(1). Even with multiple faults searching the lookup table for all the instruction will take O(1) for each instruction. For a program with 'n' instructions there will be 'n' reference to the table.

Reconfiguration time of the FPGA is an important criterion on runtime reconfigurable architectures. For example the full time reconfiguration time of Spartran3. The reconfiguration of FPGA takes milliseconds and hence the fault repair using FPGA will increase the overhead by milliseconds. There some algorithms [17]-[21] already proposed to reduce the reconfiguration time. Using one of them, the reconfiguration time cane is reduced by 40%. The reconfiguration time for the FPGA can be given from the following equation.

TbitLoad=((BitStreamLength)/(ClockFrequency* ConfigurationPortBandwidth))

The OpenSPARC T1 has an ALU unit with a gate count of 1968. For this the bits stream size will be with the above table the reconfigurable hardware proposed can be made from a bit stream size of 48.07KBytes. With an 8 bit parallel port and clock frequency of 5GHZ, the Tbit load time can be calculated as 119.91 microseconds [24]. If the number of faults and the frequency of its reference is increased then we get a curve C1 given in the following figure 4. If number of faults increases but the references remains constant, curve C2 will be obtained. When the number of faults is not increased, then there will be no change in the performance degradation. From the figure it could be seen that if the number of faults and the reference to it is increased to a higher value, the system degrades. But the degradation is graceful. The proposed system is a model which will be implemented with synchronous fault repair using XILINX Virtex FPGA board.

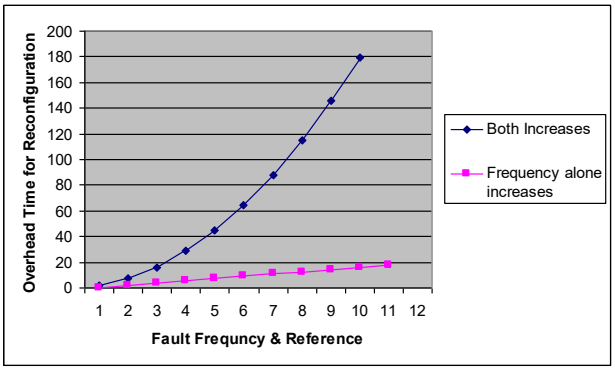

Figure 5. Fault frequency versus overhead time

IV. CONCLUSION

Faults (or) permanent faults occurring during the early or working lifetime of the processor should be avoided. But the probability of early life permanent faults has increased with multi-core processors where the chip density per square area is high. This has made online permanent fault repair on the field a necessity. In this paper such a method is proposed for handling hard faults on the field by using reconfigurable arrays. As discussed in the previous section, there will be some overhead to perform the fault repair. This overhead time is proportional to the fault occurrence. Since the multiple fault occurrences will not be very high during the initial or working lifetime of the processor , the overhead will not affect much of the system's performance. Thus with the aging of the processor, the proposed technique guarantees graceful degradation. In future the proposed technique can be refined to have minimum overhead.

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Picture Scaling utilizing Data Compression with Wavelet Transform Techniques

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Abstract— It presents the comparison of the performance of discrete wavelets and Single-level inverse discrete 1-D wavelet transform for implementation in a still image compression system. Image compression is a method through which we can calculate the storage space of images which will helpful to calculate THR SORH, L2 norm. The performances of these transforms are compared in terms of Mean squared error (MSE) and CR, BPP PSNR etc. The main objective is covert indexed image to gray scale image. These results provide to perform single-level and multilevel image decompositions and reconstructions

Keywords—Image Compression, Discrete Wavelet Transform, inverse Discrete Wavelet Transform

I. INTRODUCTION

The Discrete Wavelet Transform (DWT) of image signals produces a non-redundant image representation, which provides better spatial and compared with other multi scale representations such as Gaussian and Laplacian pyramid. Recently, Discrete Wavelet Transform has attracted more and

more interest in image de-noising. The DWT can be interpreted as signaldecomposition in a set of independent, spatially oriented frequency channels. The components can be assembled back into the original signal without loss of information. The mathematical manipulation, which implies analysis and synthesis, is called discrete wavelet transform and inverse discrete wavelet transform

An image can be decomposed into a sequence of different spatial resolution images using DWT.

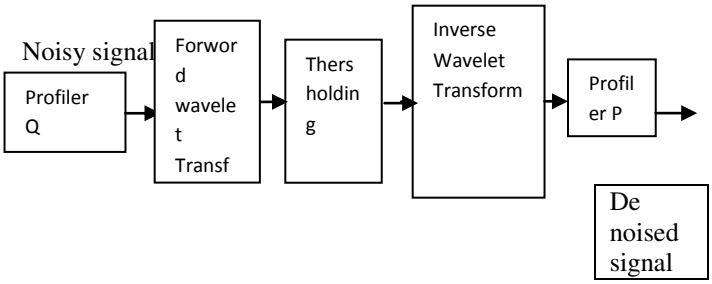

Figure1: Diagram of wavelet based image De-noising

The Discrete Wavelet Transform (DWT), based on time-scale representation, provides efficient multi-resolution sub- band

Decomposition of signals. It has become a powerful tool for signal processing and finds numerous applications in various fields such

s audio compression, pattern recognition, texture discrimination, computer graphics etc. Specifically the 2-D DWT and its

counterpart 2- D Inverse DWT (IDWT) play a significant role in many image/video coding applications.[3]

The wavelet transform describes a multi-resolution decomposition process in terms of expansion of an image onto a set of wavelet basis functions. Discrete Wavelet Transformation has its own excellent space frequency localization property.[4]

II. LITERATURE REVIEW

Image compression is a method through which we can reduce the storage space of images which will helpful to increase storage and transmission process's performance. In this paper, we present the comparison of the performance of discrete wavelets like Haar Wavelet for implementation in a still image compression system. The performances of these transforms are compared in terms of Mean squared error (MSE) and Energy Retained (ER) etc. The main objective is to investigate the still image compression of a gray scale image using wavelet theory. This is implemented in software using MATLAB Wavelet Toolbox and 2DDWT technique.[1]

The image de-noising naturally corrupted by noise is a classical problem in the field of signal or image processing. De-noising of natural images corrupted by Gaussian noise using wavelet techniques is very effective because of its ability to capture the energy of a signal in few energy transform values. The wavelet de-noising scheme thresholds the wavelet coefficients arising from the standard discrete wavelet transform. In this paper, it is proposed

to investigate the suitability of different wavelet bases and the size of different neighborhood on the performance of image de-noising algorithms in terms of PSNR. [2]

In contrast, the algorithms in transform domain, such as DCT, DWT have certain robustness against some multimedia processing. In this work the authors propose a novel stegano graphic method for hiding information in the transform domain of the gray scale image. The proposed approach works by converting the gray level image in transform domain using discrete integer wavelet technique through lifting scheme. This approach performs 2-D lifting wavelet decomposition through Haar lifted wavelet of the cover image and computes the approximation coefficients matrix CA and detail coefficients matrices CH, CV, and CD. [5]

III. DISCRETE WAVELET TRANSFORM

DWT is a transformation technique is used to represent an image in a new time and frequency scale by decomposing the input image into low frequency, middle and high frequency bands. The value of low frequency band is the averaging value of the filter whereas the high frequency coefficients are wavelet coefficients or detail values. The DWT can be used to decompose image as a multistage transform. In the first stage, an image is decomposed into four sub bands LL1, HL1, LH1, and HH1, where HL1, LH1, and HH1 represent the finest scale wavelet coefficients, while LL1 stands for the coarse level coefficients, i.e., the approximation image. Fig.1 shows the one level wavelet decomposition of an [6]

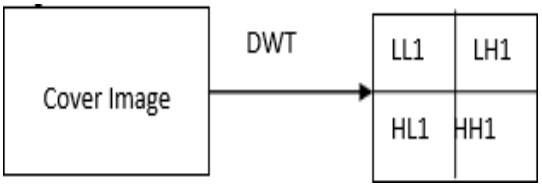

Fig. 2 one level of Wavelet Decomposition

IV. INVERSE DISCRETE WAVELET TRANSFORM

The DWT represents the signal in dynamic sub-band decomposition. Generation of the DWT in a wavelet packet allows sub-band analysis without the constraint of dynamic decomposition. The specific decomposition will be selected according to an optimization criterion. The Discrete Wavelet Transform (DWT), based on time-scale representation, provides efficient multi resolution sub- band decomposition of signals. It has become a powerful tool for signal processing and finds numerous applications in various fields such as audio compression, pattern recognition, texture discrimination, computer graphics etc. Specifically the 2-D DWT and its counterpart 2- D Inverse DWT (IDWT) play a significant role in many image/video coding applications. [3]

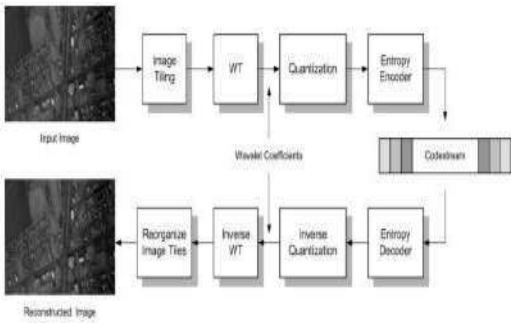

Figure 3 IDWT Decomposition

The DWT architecture, the input image is decomposed into high pass and low pass components using HPF and LPF filters giving rise to the first level of hierarchy. The process is continued until multiple hierarchies are obtained. A1 and D1 are the approximation and detail filters.

V. COMPERISION OF IMAGE COMPRESSION

In the DWT transformation, the image is taking into HL, LH, HH, LL Ratios. Then the image is moved into DWT transforms, and then DWT Quantization is processed. After that the process is move to DPCM encoder. Then the compressed image will come IDWT. The IDWT transformation of the image is taken in to the pixel ratio us nxn matrix formation. Then the image is transforms into the IDWT quantization. Then the compressed image will come us output. The output image has the good compression ratio. The PSNR value of the compressed image is good us expected.

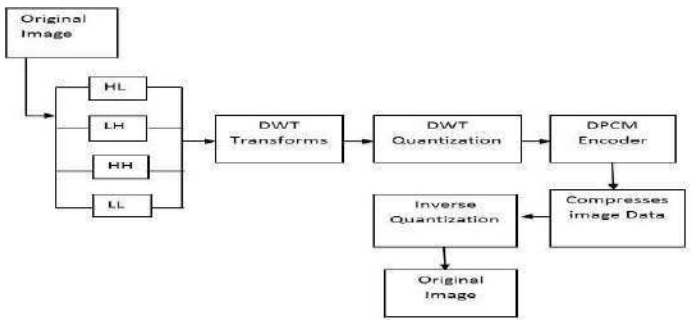

Figure.1.1.Architecture of DCT and DWT

Performance	DWT	IDWT
Multi Resolution	YES	NO
Filter Banks	NO	YES
Fast Computation	YES	NO
Low Memory and Power	YES	NO

Table 1.1 Performances of DCT andDWT Comparison

I. CONCLUSION

In this study, the image de-noising using discrete wavelet transform is analyzed. The experiments were conducted to study the suitability of different wavelet bases and also different image sizes. Among all discrete wavelet bases performs well in image de-noising. The design is simulated using MATLAB software.

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A Literature Survey in light of Flexible Algorithms

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Abstract- Hypothetical this survey paper is investigated in changed concerns. It has been coordinated to consider sketching out of flexible channel and also to know where the adaptable computations are used in the distinctive applications. The essential target of this diagram paper is to study and execution of different adaptable channel estimations for uproar crossing out and resonate revocation.

Keywords-Adaptive algorithms, Adaptive Filter, Adaptive Noise dropping System, Convergence rate, Noise

I. Introduction

A writing survey unmistakably builds up the need of the work. It tends to questions about advancement in these investigations and allow it for some, uncertain issues to emerge and in this way clearly express all limits about the advancement of the exploration work. Advanced flag handling frameworks are ending up increasingly fascinating because of the improvement in computerized circuit outline. There are a few methods which incorporate advanced frameworks for different separating application. Advanced frameworks are utilized to deal with the data of the different information signal. Adaptive channels are made relevant in any sort of new condition. Versatile channel is utilized for advanced flag handling and also maintain various applications in time changing condition of info insights. Debased flag is enhanced by certain and indeterminate commotion which is reduced with the assistance of versatile channels. The uses of versatile channels, for example, ID, opposite demonstrating, obstruction wiping out and expectation are the real fundamentals to tackle the issue of commotion and acoustic reverberate retraction. Different calculations are composed basically LMS, NLMS and RLS calculation for obstruction scratch-off to get appropriate versatile channel. The execution proportions of versatile calculation are misadjustment, rate of union, computational prerequisites, strength and numerical heartiness,. Segment 2 gives an outline of versatile channel. The concise portrayal of commotion crossing out framework is clarified in segment 3. The essential idea of a versatile clamor crossing out framework is to permit the tainted flag from an advanced channel that impact to stifle the commotion ruined flag while leaving the first flag unaltered. Versatile Noise Cancellation (ANC) totally choke the low recurrence

clamor for which uninvolved strategies are ineffectual. Segment 4 gives depiction about versatile calculations, for example, Least Mean Square (LMS), Data Sign LMS, Leaky LMS, and Recursive Least Square (RLS) .Section 5 closes the fundamental research work.

II. Adaptive Filter

It is a versatile channel which can change itself its exchange work relating to the best versatile calculation passed on by a blunder or undermined flag. The majority of the versatile channels are advanced channels on account of the confounded of these versatile calculations. Versatile channels are utilized for different applications since a few parameters of the coveted preparing activity are not known in advance [1] [2]. The versatile channel utilizes input as a mistake flag to channel its exchange capacity to relate the changing parameters. The versatile procedure requires the utilization of a cost work which is a rule for introductory execution of the channel, to convey a calculation, which decides how to alter the channel exchange capacity to limit the cost on the following cycle. Fig.1 demonstrates the square graph of versatile channel [3].

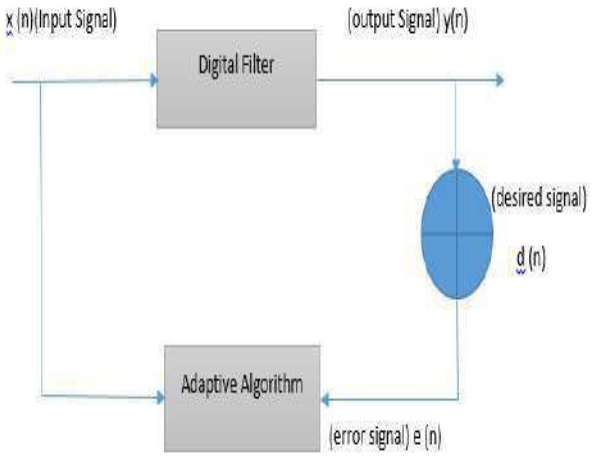

Fig 1 Block diagram of adaptive filter

III. Noise Cancellation System

Clamor is unsettling influence undesirable flag amid flag correspondence. Clamor can happen due to numerous components like deferral, covering and impedance. These issues in the earth are acquired as a result of the intemperate change of innovation that has quickened to loud motors, and other commotion sources. Commotion scratch-off framework working for different applications, for example, to drop the intermittent obstruction in discourse signals, to drop the occasional impedance in electrocardiography. Versatile separating has been to a great extent utilized in numerous down to earth applications. Imperative outcomes have been gotten in clamor and obstruction dropping for biomedical applications [4]. During the time spent flag handling for clamor or time changing signs, Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) settled coefficient channels can't accomplish best separating. Thus, we should plan versatile channels, to give the progressions

of flag and commotion flag. Versatile channel innovation gives better execution when contrasted with customary techniques. The general setup of Noise Cancellation System [5] is appeared in Fig.2. It comprises of two information flags, the flag d(n) which is ruined by an undesired clamor x1(n) , and wanted flag s(n) and the other reference flag x(n), that will be sifted through of the framework. The primary objective of Noise Cancellation framework is to lessen the commotion flag, and to get the de-noised flag. A reference flag x (n) is required for filteration. However, the reference flag is generally not indistinguishable flag from the commotion segment of the essential sufficiency, stage or time. In this way, the reference flag can't be subtract straightforwardly from the information flag to get the coveted outcome at the yield .Noise which effects on the discourse flag can be considered as White clamor or Colored commotion.

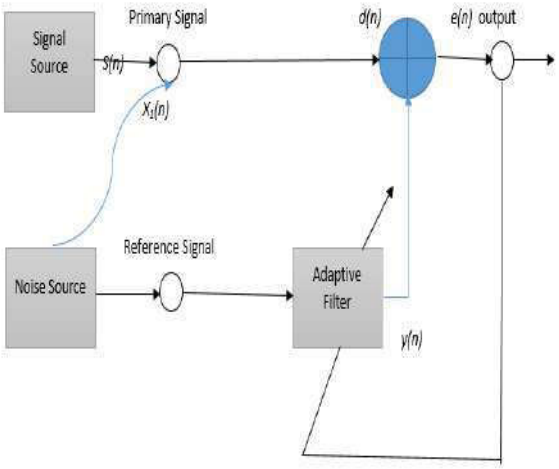

Fig2: Adaptive noise cancellation system

Where s(n) –primary signal, d(n)- corrupted signal, x(n)-noise reference input, x1(n) - noise signal, y(n)-output of adaptive filter, e(n) -system output signal.

Versatile Noise Cancellation framework use two signs, one flag that is utilized to quantify the adulterated flag while the other flag is utilized to gauge the commotion flag alone. This system adaptively alters its channel coefficients in order to expel the commotion from the undermined flag. This system requires high cognizance between the clamor part in the undermined flag and the commotion in the reference flag. Lamentably this is a restricting component, as the mouthpieces should be space separated with a specific end goal to keep the discourse being constituted in the commotion reference flag and along these lines it being evacuated. In synopsis, we utilize two information signals and a versatile channel to understand a versatile commotion crossing out framework. One information flag is the undermined by clamor which can be communicated as:

$$d(n)=s(n)+x_1(n) \qquad 1$$

The other information flag which is commotion reference input flag go through a versatile channel and yield y(n) is delivered as close a copy as conceivable of x1(n).The channel straightens out itself its channel coefficients consistently to limit the mistake between and amid this procedure. At that point the yield is subtracted from the adulterated flag to deliver the framework yield. It is communicated as:

$$e(n)=s(n)+x_1(n)-y(n) \qquad 2$$

This is the de-noised signal.

IV. Adaptive Algorithms

The versatile calculation gives different utilization of impedance end, and after that with the assistance of these calculations we can modify the flag qualities could be speedier. The versatile channels like Least Mean Square, sign Least Mean Square and Normalized Least Mean Square are majorly used in the distinctive flag preparing application, since it is anything but difficult to actualize and broadly utilized for basic calculation. The RLS calculation is "a definitive" algorithm to outline the best meeting conduct [6]. Another changed versatile calculation is given by Chansarkar, M.M.Desai and U.B. in 1997.An assessed recursive usage calculation is known as the Robust Recursive Least Square calculation (RRLS). The RLS calculation is shocking concerning steady limited information intrusion. Reproduction results are described to exhibit the adequacy of the RRLS calculation [7].The new Variable-Step-Size (VSS-LMS) calculation were assessed in 2001.The outcomes insinuate that preferred execution can be accomplished over the past calculation .The settled advance size (FSS) calculation can be connected to sub band versatile resound end. Reproduction result demonstrates that the proposed calculation yields a lower enduring state misadjustment and in addition a lower remaining MSE when contrasted and FSS sub band LMS calculation. The recommended calculation results in a slower merging rate yet in addition a lower relentless state disappointment modification in examination with the NLMS sub band calculation. It iso bserved that the enhanced framework execution is accomplished with an alternate advance size adaption for each and with each individual sub band [8].The versatile calculation is utilized for channel estimation, obstruction undoing, and channel equalization in computerized flag preparing system. The Least Mean Square calculation is the most essential calculation shape different versatile calculations. Its union speed is chosen by the progression square calculation is utilized for getting both the leftover blame level and additionally give most noteworthy speed of combining. A few Variable Step-Least Mean Square calculations have looked into and a changed of this calculation created in 2007 [9]. Totally results assign that meeting strength and following capacity are better than other versatile calculations [10]. P.Radhika, Chunduri.V.M.NarenSimha&MonpurAshwin are utilized different procedurs in 2014 for end of spontaneous substances from different signs. The electrical cable impedance from all delicate checking hardware's can be disposed of by actualizing different strategies with various mistake nonlinearity-in view of versatile channels. The proposed calculation is best for applications, for example, biotelemetry and so forth. These frameworks are using simple expansion and surrender speed over alternate LMS-based acknowledge [11].

The LMS versatile channel family is extremely appealing for usage of ease continuous frameworks because of its low computational multifaceted design and heartiness [6] [12].

A. LMS Algorithm

This is generally utilized for various applications, for example, channel leveling, reverberate wiping out and clamor undoing. The condition beneath is LMS calculation for refreshing the tap weights of the versatile channel for every emphasis.

$$w(n+1)=w(n)+\mu e(n)x(n) \quad -3$$

Where x(n) is the information vector of time deferred input esteems and w(n) is the weight vector at the time n. μis the progression estimate parameter. This calculation is utilized because of its computational straightforwardness. It requires 2N+1 duplications and increases yet it has a settled advance size for every cycle.

B. Data Sign LMS algorithm

In a high speed communication the time is critical, thus faster adaptation processes is needed

$$\text{Sgn(t)}=\begin{cases} a & a>0 \\ 0 & a=0 \\ -1 & a>0 \end{cases} \quad 4$$

For data Sign algorithm [7] weight update coefficients equation is:

$$w(n+1)=w(n)+2\mu e(n)\text{sgn}x(n) \quad 5$$

By presenting the flag capacity and setting an estimation of intensity of two, the equipment execution is exceedingly disentangled. It enhances the combination conduct, requires less computational multifaceted nature and furthermore gives great outcome yet throughput is slower than LMS Algorithm.

C. Leaky LMS Algorithm

It introduces a leakage coefficient into LMS algorithm so it becomes as:

$$w(n+1)=(1-2\mu\gamma)w(n)+2\mu e(n)x(n) \quad -6$$

Where $0<\gamma<<1$ .The effect of introducing the leakage coefficient γ is to force any undamped modes to become zero and also force to the filter coefficients to become zero if either e(n) or x(n) is zero.

D. RLS (Recursive Least Square) Algorithm

This algorithm [13] attempts to minimize the cost function in Equation (7). k= 1is the time at which the RLS algorithm commences and is a small positive constant very close to, but smaller than 1. With values of 1 more recent input samples, this results in a scheme that places more emphasis on recent samples of observed data and tends to forget the past

$$\zeta(n)=\sum_{k=1}^{n}\gamma^{n-k}\ e_k^n\quad(k) \quad -7$$

V. Conclusion

In this paper a review has been carried out about the Adaptive filtering algorithm with respect to the noise cancellation problem. Now-a days we have many adaptive algorithms available each having its various types of properties. The survey of designed adaptive filter was conducted where we get LMS adaptive algorithm is the best for its stability and also for its high speed capability, convergence rate. To achieve minimum mean square error at a high convergencerateis the main task of this

algorithm. When compared to LMS algorithm, RLS algorithm offers a faster convergence and lower error at steady state. But, this RLS algorithm is more computationally complex and if proper design procedures are not followed, RLS algorithm may diverge away resulting in instability.

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